

NOVOSENSE Gate Driver with 2 Level-Slew-rate Control

Datasheet (EN) 1.0

Product Overview

The NSI6601S is a single-channel isolated gate driver to drive IGBTs, MOSFETs and SiC MOSFETs in many applications. It implements 2 level slew rate control by controlling two independent gate resistors. This feature can optimize both EMI and switching losses. It can source and sink 25A peak current. System robustness is supported by 200kV/μs minimum common-mode transient immunity (CMTI). The driver operates with a maximum supply voltage of 32V, while the input-side accepts from 3V to 5.5V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

Because of high driving current ability, excellent robustness, wide supply voltage range and fast signal propagation, NSI6601S is suitable for high reliability, power density and efficient switching power system.

Key Features

- Isolated single-channel driver
- Two level slew rate control through independent resistors
- Enable on the fly & circle by circle gate resistor change to optimize both EMI and efficiency losses
- Input side supply voltage: 3V to 5.5V
- Driver side supply voltage: up to 35V with 12V UVLO
- 25A peak source and sink output current
- Minimum CMTI: $\pm 200\text{kV}/\mu\text{s}$
- Active output clamping
- 40V absolute maximum output supply voltage
- 105ns typical propagation delay
- Operation ambient temperature: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- RoHS & REACH compliant
- Lead-free component, suitable for lead-free soldering profile: 260 °C, MSL3

Safety Regulatory Approvals

- UL recognition: 5700V_{RMS}
- DIN EN IEC 60747-17(VDE 0884-17)
- CSA component notice 5A
- CQC certification per GB4943.1

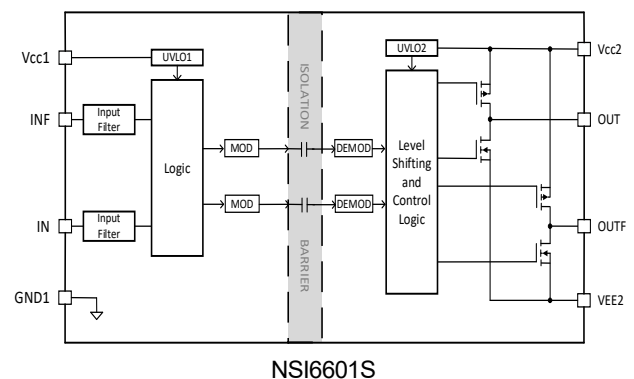
Applications

- Isolated DC/DC and AC/DC Power Supplies
- Solar Inverters
- Motor Drives and EV Charging
- UPS and Battery Chargers

Device Information

Part Number	INF level of fast- Rising	switching Falling	Clamp Feature
NSI6601SRC-DSWVR	Low	High	YES
NSI6601SH3-DSWVR	High	High	YES
NSI6601SHC-DSWVR	Low	Low	NO

Function Block



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Pin Configuration and Function

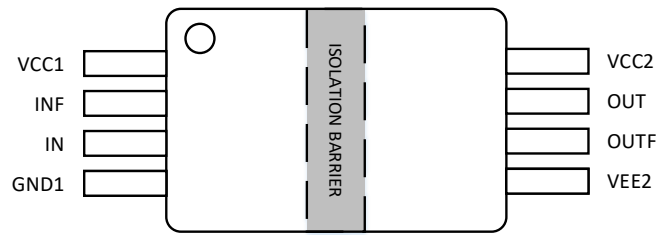


Figure 1.3 NSI6601S
(Top View)

Table 1.1 NSI6601S Pin Configuration and Description

<i>Pin Name</i>	<i>Pin NO.</i>	<i>Function</i>
VCC1	1	Input-side supply rail
INF	2	Driver input for operation OUTF
IN	3	PWM driver input
GND1	4	Input-side ground reference
VEE2	5	Driver-side ground reference
OUTF	6	Additional driver output
OUT	7	Main driver output
VCC2	8	Positive output supply rail

1. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VCC1-GND1	-0.3	6	V
Input Signal Voltage	V _{IN} -GND1, V _{INF} -GND1	-0.3	6	V
Driver Side Supply Voltage	VCC2-VEE2	-0.3	40	V
Output Signal Voltage	V _{OUT} - VEE2, V _{OUTF} - VEE2	-0.3	VCC2+0.3	V
Operating Junction Temperature	T _J	-40	150	°C
Storage Temperature	T _{stg}	-55	150	°C

2. ESD Ratings

		Value	Unit
Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ● All pins	±4000	V
	Charged-device model (CDM), per AEC Q100-011 ● All pins	±2000	V

3. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VCC1-GND1	3	5.5	V
Input Signal Voltage	V _{INF} -GND1, V _{IN} -GND1	-0.3	5.5	V
Driver Side Supply Voltage	VCC2-VEE2	14	35	V
Ambient Temperature	T _A	-40	125	°C

4. Thermal Information

<i>Parameters</i>	<i>Symbol</i>	<i>SOW8</i>	<i>Unit</i>
Junction-to-ambient thermal resistance	θ_{JA}	75	°C/W
Junction-to-case (top)thermal resistance	θ_{JC}	32.5	°C/W
Junction-to-board thermal resistance	θ_{JB}	31	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	29.2	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	9.6	°C/W

- 1) Simulated using High Effective Thermal Conductivity Test Board (2s2p) described in JESD51-7
- 2) Simulated following the environment described in JESD51-7

5. Specifications

5.1. DC Electrical Characteristics

All min and max specifications are at $T_A = -40^{\circ}\text{C}$ to 125°C . Typical values are tested at $V_{CC1} = 3.3\text{V}$ or 5V , $V_{CC2} = 15\text{V}$ or 30V .

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Currents						
Input side Quiescent Current	I_{CC1_ON}		5.5	7	mA	$V_{IN} = V_{CC1}$, $V_{CC1} = 5\text{V}$
	I_{CC1_OFF}		1.4	2.3	mA	$V_{IN} = \text{GND1}$, $V_{CC1} = 5\text{V}$
Driver side Quiescent Current	I_{CC2_ON}		2.3	3.5	mA	$V_{IN} = V_{CC1}$, $V_{CC2} = 15\text{V}$
	I_{CC2_OFF}		2.1	3.3	mA	$V_{IN} = \text{GND1}$, $V_{CC2} = 15\text{V}$
Input Side Supply UVLO Threshold						
VCC1 UVLO Rising Threshold	V_{CC1_ON}	2.7	2.87	3.1	V	
VCC1 UVLO Falling Threshold	V_{CC1_OFF}	2.5	2.67	2.9	V	
VCC1 UVLO Hysteresis	$V_{CC1_HYS}^{(1)}$		0.2		V	
Driver Side Supply UVLO Threshold						
VCC2 UVLO Rising Threshold	V_{CC2_ON}	11	11.8	13	V	
VCC2 UVLO Falling Threshold	V_{CC2_OFF}	10	10.8	12	V	
VCC2 UVLO Hysteresis	$V_{CC2_HYS}^{(1)}$		1		V	
Input Pin Characteristics						
Logic High Input Threshold (IN, INF)	V_{INH}	1.6	2.1	2.8	V	
Logic Low Input Threshold (IN, INF)	V_{INL}	0.7	1.2	1.9	V	
Input Hysteresis Voltage (IN, INF)	$V_{IN_hys}^{(1)}$		0.9		V	
Input Current (IN, INF)	I_{IN}	50		100	μA	
Pull down resistance (IN, INF)	$R_{IN}^{(1)}$		75		$\text{k}\Omega$	
IN minimum pulse width	t_{IN_min}	20		40	ns	
INF minimum pulse width	$t_{INF_min}^{(2)}$	50			ns	
Output Pin Characteristics						
High Level Output Voltage	$V_{OH}^{(1)}$			0.11	V	$V_{OH} = V_{CC2} - V_{OUT}$, $I_{OUT} = -0.1\text{A}$, $V_{IN} = \text{High}$
Low Level Output Voltage	$V_{OL}^{(1)}$			0.08	V	$V_{OL} = V_{OUT} - V_{EE2}$, $I_{OUT} = 0.1\text{A}$, $V_{IN} = \text{Low}$
OUT Pull-up Resistance	R_{OH}		0.59	1.1	Ω	
OUT Pull-down Resistance	R_{OL}		0.45	0.8	Ω	
OUTF Pull-up Resistance	R_{OH}		0.48	0.9	Ω	
OUTF Pull-down Resistance	R_{OL}		0.32	0.6	Ω	
Peak Source Current(OUT)	$I_{OH}^{(1)}$		-10		A	
Peak Sink Current(OUT)	$I_{OL}^{(1)}$		10		A	

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Peak Source Current(OUTF)	$I_{OH}^{(1)}$		-15		A	
Peak Sink Current(OUTF)	$I_{OL}^{(1)}$		15		A	
Clamping Voltage (OUT, OUTF) ($V_{OUT} - V_{CC2}$)	V_{CLP_OUT}		0.55	1.5	V	$I_{OUT}=500mA$ with $t_{pulse}=10\mu s$, $V_{IN}=High$
Active Pull down Voltage	V_{ACTPD}		1.6	2.5	V	$I_{OUT}=10mA$, $V_{CC2}=Open$

⁽¹⁾ Not test covered, guaranteed by characterization.

⁽²⁾ Not test covered, guaranteed by design.

5.2. Specialized Electrical Characteristics

All min and max specifications are at $T_A = -40^{\circ}\text{C}$ to 125°C . Typical values are tested at $V_{CC1} = 3.3\text{V}$ or 5V , $V_{CC2} = 15\text{V}$ or 30V .

Parameter	Symbol	Min	Typ	Max	Unit	Condition
NSI6601SRC						
Clamp ON Threshold Voltage	$V_{\text{CLAMP_ON_TH}}$	0.5	1	1.5	V	$V_{CC2} - V_{OH}$
Clamp OFF Threshold Voltage	$V_{\text{CLAMP_OFF_TH}}$	1.5	2	2.5	V	$V_{OL} - V_{EE2}$
Low Level Clamp Current (Peak)	$I_{LL_CLAMP}^{(1)}$		5		A	$V_{IN} = \text{Low}, V_{\text{clamp}} = 2\text{V}$
Clamp ON Delay	$t_{\text{CD_ON}}^{(2)}$		850		ns	
Clamp OFF Delay	$t_{\text{CD_OFF}}^{(2)}$		80		ns	
NSI6601SH3						
Clamp ON Threshold Voltage	$V_{\text{CLAMP_ON_TH}}$	0.5	1	1.5	V	$V_{CC2} - V_{OH}$
Clamp OFF Threshold Voltage	$V_{\text{CLAMP_OFF_TH}}$	1.5	2	2.5	V	$V_{OL} - V_{EE2}$
Low Level Clamp Current (Peak)	$I_{LL_CLAMP}^{(1)}$		5		A	$V_{IN} = \text{Low}, V_{\text{clamp}} = 2\text{V}$
Clamp ON Delay	$t_{\text{CD_ON}}^{(2)}$		850		ns	
Clamp OFF Delay	$t_{\text{CD_OFF}}^{(2)}$		80		ns	
Active Clamp ON Delay	$t_{\text{clp_ON_delay}}$	1.6	2.4	3.2	μs	
Active Clamp OFF Delay	$t_{\text{clp_OFF_delay}}$	5.5	7	8.5	μs	

⁽¹⁾ Not test covered, guaranteed by characterization.

⁽²⁾ Not test covered, guaranteed by design.

5.3. Switching Characteristics

Typical values are at VCC1=5V, VCC2=15V. All min and max specifications are at T_A=-40°C to 125°C. If not mentioned, C_{LOAD}=0.1nF.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Propagation Delay	t _{PLH}	70	105	130	ns	
Propagation Delay	t _{PHL}	70	105	130	ns	
Pulse Width Distortion t _{PLH} -t _{PHL}	t _{PWD}			30	ns	
Dismatch OUT vs OUTF	t _{dismatch} ⁽¹⁾			5	ns	
Output Rise Time (20% to 80%)	t _R ⁽¹⁾		52		ns	C _{LOAD} =10nF
Output Fall Time (80% to 20%)	t _F ⁽¹⁾		60		ns	C _{LOAD} =10nF
Common Mode Transient Immunity	CMTI ⁽¹⁾	200			kV/μs	

⁽¹⁾ Not test covered, guaranteed by characterization.

⁽²⁾ Not test covered, guaranteed by design.

5.4. Typical Performance Characteristics

Typical characteristics are measured by using VCC1=5V, 1uF capacitor from VCC1 to GND1, and VCC2=15V with 10uF bypass capacitor from VCC2 to VEE2 T_J =-40°C to 125°C (unless otherwise noted).

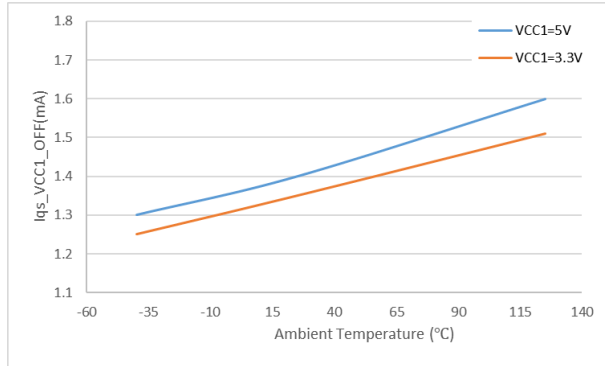


Figure 5.1 VCC1 OFF supply current vs temperature

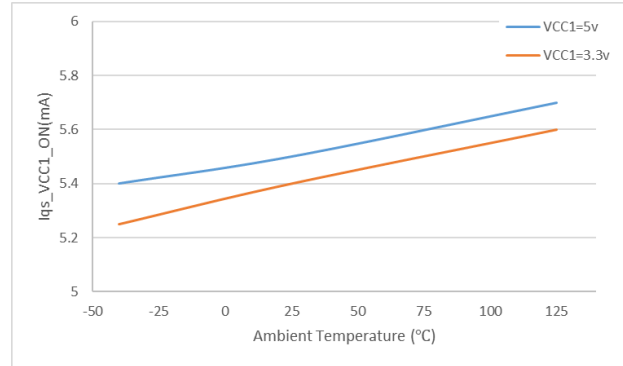


Figure 5.2 VCC1 ON supply current vs temperature

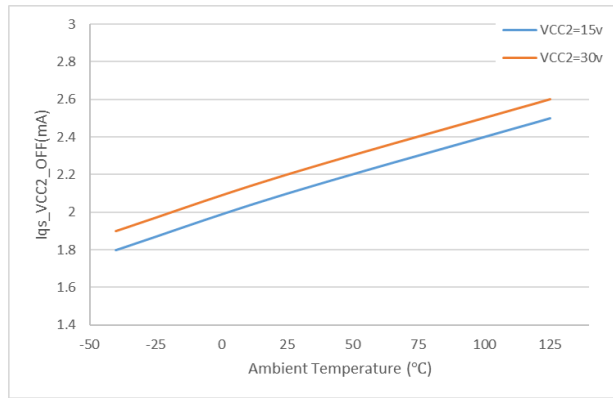


Figure 5.3 VCC2 OFF supply current vs temperature

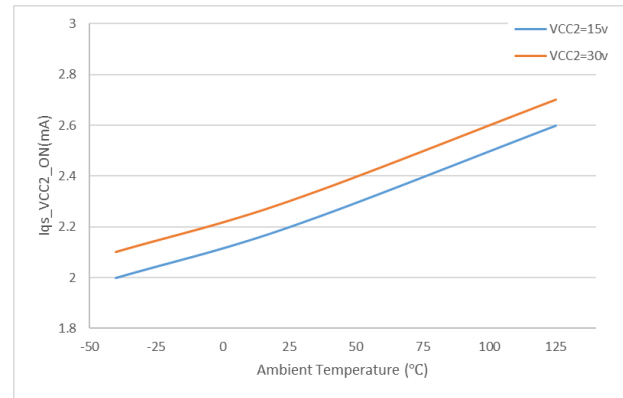


Figure 5.4 VCC2 ON supply current vs temperature

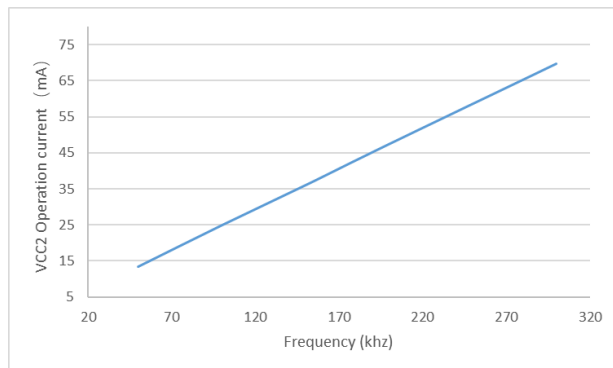


Figure 5.5 VCC2 operating current vs frequency

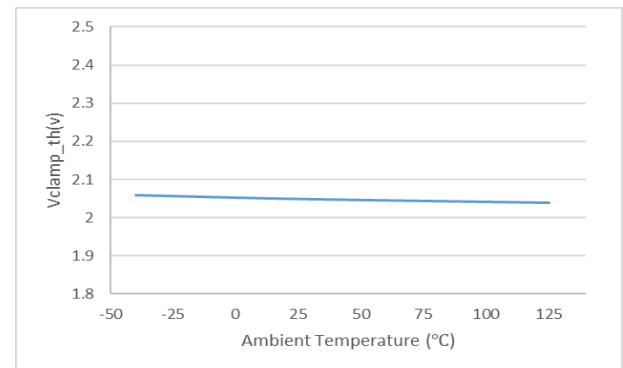


Figure 5.6 miller clamp threshold vs temperature

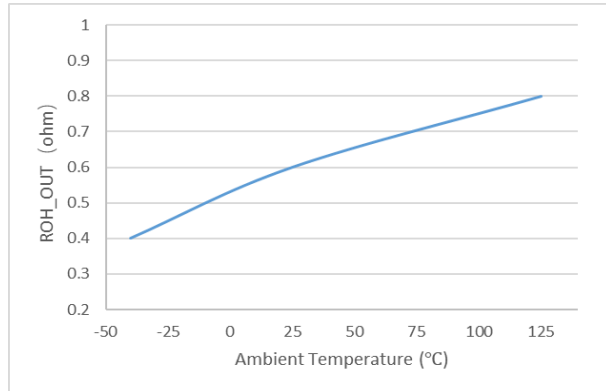


Figure5.7 ROH_OUT vs temperature

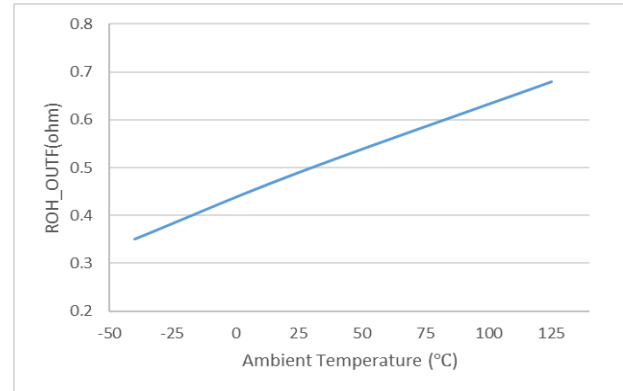


Figure5.8 ROH_OUTF vs temperature

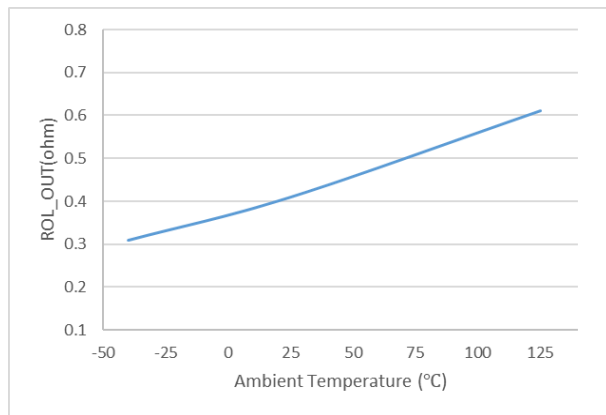


Figure5.9 ROL_OUT vs temperature

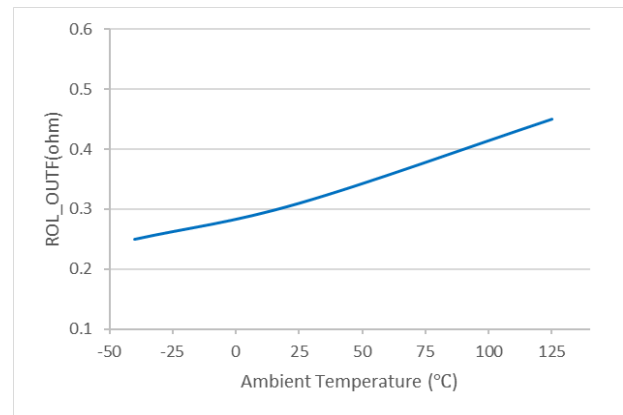


Figure5.10 ROL_OUTF vs temperature

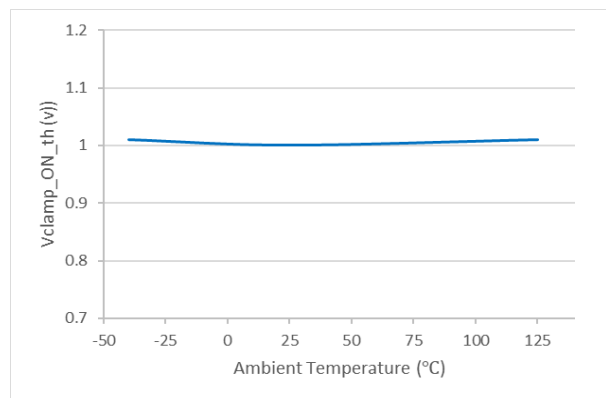


Figure5.11 clamp ON threshold vs temperature

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

<i>Parameters</i>	<i>Symbol</i>	<i>SOW8</i>	<i>Unit</i>	<i>Comments</i>
Min. External Air Gap (Clearance)	CLR	8.0	mm	IEC 60664-1
Min. External Tracking (Creepage)	CPG	8.0	mm	IEC 60664-1
Distance Through the Insulation	DTI	20	um	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

6.2. Insulation Specification for SOW8 Package

Description			Test Condition	Symbol	Value	Unit
Overvoltage Category per IEC60664-1			For Rated Mains Voltage ≤ 150Vrms		I to IV	
			For Rated Mains Voltage ≤ 300Vrms		I to IV	
			For Rated Mains Voltage ≤ 600Vrms		I to IV	
			For Rated Mains Voltage ≤ 1000Vrms		I to III	
Climatic Classification					40/125/21	
Pollution Degree per DIN VDE 0110					2	
Maximum Working Isolation Voltage			AC voltage (sine wave) Time dependent dielectric breakdown (TDDb)test	V _{IOWM}	1500	V _{RMS}
			DC voltage		2121	V _{DC}
Maximum Repetitive Isolation Voltage			AC voltage(bipolar)	V _{IORM}	2121	V _{PEAK}
Apparent Charge			Method a, after Input/output safety test subgroup 2/3, Vini=VIOTM, tini = 60s , Vpd(m)=1.2*VIORM, tm=10s.	q _{pd}	<5	pC
			Method a, after environmental tests subgroup 1, Vini=VIOTM, tini=60s ,Vpd(m)=1.6*VIORM, tm=10s			
			Method b, routine test (100% production) and preconditioning (type test);Vini=1.2*VIOTM, tini=1s Vpd (m)=1.875*VIORM, tm=1s (method b1) or Vpd(m)=Vini, tm=tini(method b2)			
Maximum Transient Isolation Voltage			t = 60s	V _{IOTM}	8000	V _{PEAK}
Maximum impulse voltage			Tested in air, 1.2/50-μs waveform per IEC62368-1	V _{IMP}	6250	V _{PEAK}
Maximum Surge Isolation Voltage			Test method per IEC62368,1.2/50μs waveform, V _{TEST} =V _{IOSM} ×1.6	V _{IOSM}	10000	V _{PEAK}
Isolation Resistance			V _{IO} =500V at T _A =T _S	R _{IO}	>10 ⁹	Ω
			V _{IO} =500V at 100°C≤T _A ≤125°C		>10 ¹¹	Ω
			V _{IO} =500V ,T _A =25°C		>10 ¹²	Ω
Isolation Capacitance			f = 1MHz	C _{IO}	0.8	pF
UL1577						
Maximum Withstanding Isolation Voltage			V _{TEST} = V _{ISO} , t = 60s (qualification); V _{TEST} = 1.2 ×V _{ISO} , t = 1s (100%production)	V _{ISO}	5700	V _{RMS}

6.3. Safety Limiting Values for SOW8 Package

Description	Test Condition	Symbol	Value		Unit
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{JA}=75^{\circ}\text{C/W}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	P_S	Total	1.67	W
			Input Side	0.04	
			Output Side	1.63	
Maximum Safety Current	$R_{JA}=75^{\circ}\text{C/W}$, $V_{CC2}=15\text{V}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	I_S	Output Side	108	mA
	$R_{JA}=75^{\circ}\text{C/W}$, $V_{CC2}=30\text{V}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$		Output Side	54	

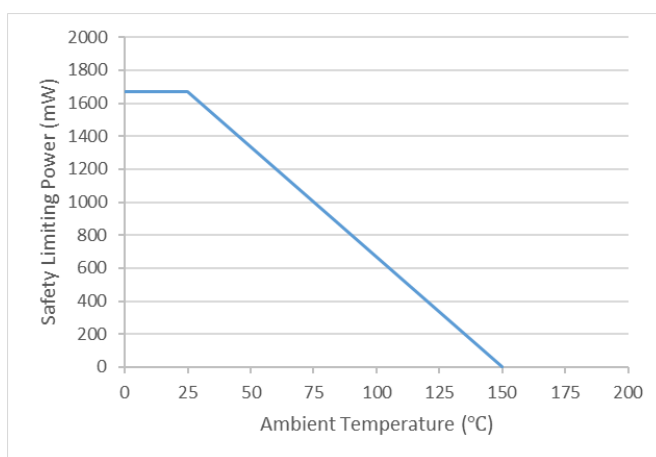


Figure 6.1 Thermal Derating Curve for Limiting Power for SOW8 Package

6.4. Regulatory Information for SOW8 Package

<i>UL</i>		<i>TUV</i>	<i>CQC</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 5700V _{RMS} Isolation Voltage	Single Protection, 5700V _{RMS} Isolation voltage	Reinforced Insulation $V_{IORM}=2121V_{PEAK}$, $V_{IOTM}=8000V_{PEAK}$	Reinforced Insulation
E500602		R 50574061	CQC26001518664

7. Function Description

7.1. Overview

The NSI6601S is a highly reliable isolated gate driver with 12V UVLO, which is suitable to drive MOSFET, IGBT, and SiC. NSI6601S can support 5700V_{RMS} isolation per UL1577. System robustness is supported by 200kV/μs minimum common-mode transient immunity (CMTI).

The functional block diagram of NSI6601S is shown below. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Active pull-down and short circuit clamping features are implemented to protect power transistor.

The isolation barrier inside NSI6601S is based on capacitive isolation. The signal across the isolation barrier is transmitted via OOK (on-off keying) modulation technique with key benefits of high noise immunity and low radiation EMI. The transmitter sends a high-frequency carrier across the isolation barrier to represent one digital state and sends no signal to represent the other digital state. The digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

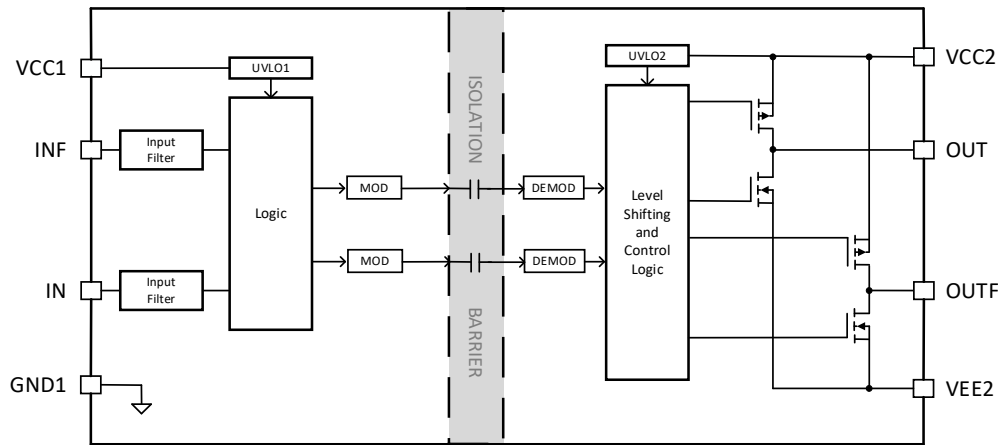


Figure 7.1 NSI6601S Functional Block Diagram

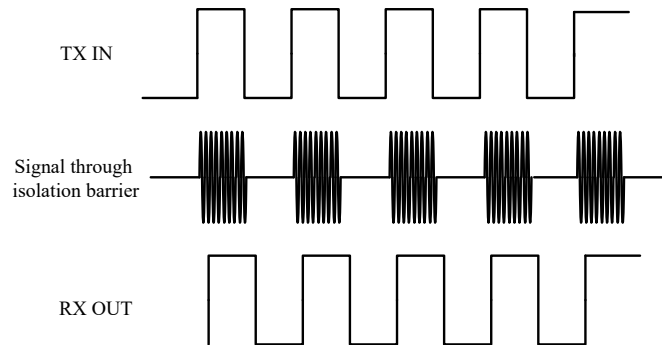


Figure 7.2 OOK based Modulation

7.2. Output Stage

The voltage and current of external power transistor drain to source or collector to emitter change during low to high output signal transition. At that moment, the p-channel MOSFET turns on to provide a transitory boost in the sourcing current during the period of turning the output state from low to high. It results in faster turn on time and lower turn on power loss for external power transistor. This function helps to pull the IGBT or MOSFET gate to the off state when VCC2 is not connected to the power supply. NSI6601S is also designed with an active pulldown function. This feature prevents the false turn-on of OUT pin by clamping the output to V_{ACTPD} when the VCC2 is open.

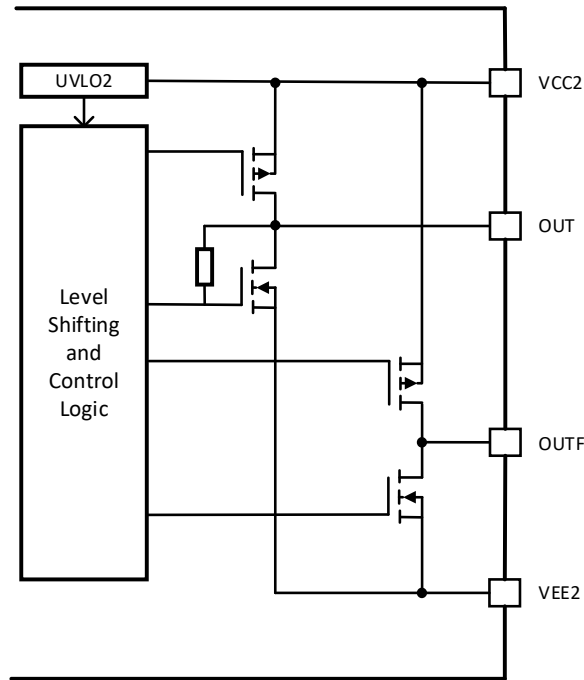


Figure 7.3 NSI6601S Output Stage

7.3. Short Circuit Clamping

Short circuit is used to clamp the driver output voltage as well as to pull the miller clamp pins to a bit higher than VCC2. This function helps to protect the gate of a MOSFET or IGBT from overvoltage breakdown. The short circuit clamping is implemented by the Pmos of OUTF.

7.4. VCC1, and VCC2 Under Voltage Lock Out (UVLO)

The device is equipped with an undervoltage lockout for input and output independently to ensure correct switching of IGBT/SiC. If both VCC1 and VCC2 have increased above the respective levels VCC1_{ON} and VCC2_{ON}, terminal OUT or OUTF will be activated after a UVLO condition for turn-on according to the present state at terminal IN or INF. If any power supply voltage drops below the UVLO threshold, a turn-off signal will be sent to the output chip before power-down. OUTF will keep HIZ to avoid the overshoot of the IGBT/SiC.

The supply voltage VCC2 and related protection functions are always referred to as VEE2. There is no differentiation between unipolar or bipolar supply. A capacitor that is placed near the supply terminals VCC1 and GND1 on the input side, and VCC2 and VEE2 on the output side, avoids accidental triggering of under-voltage lockout events.

The IC is safe with any start-up sequence regarding its supply voltages VCC1 and VCC2. However, it is good practice to have the input side supply voltage start up first, followed by the output side supply.

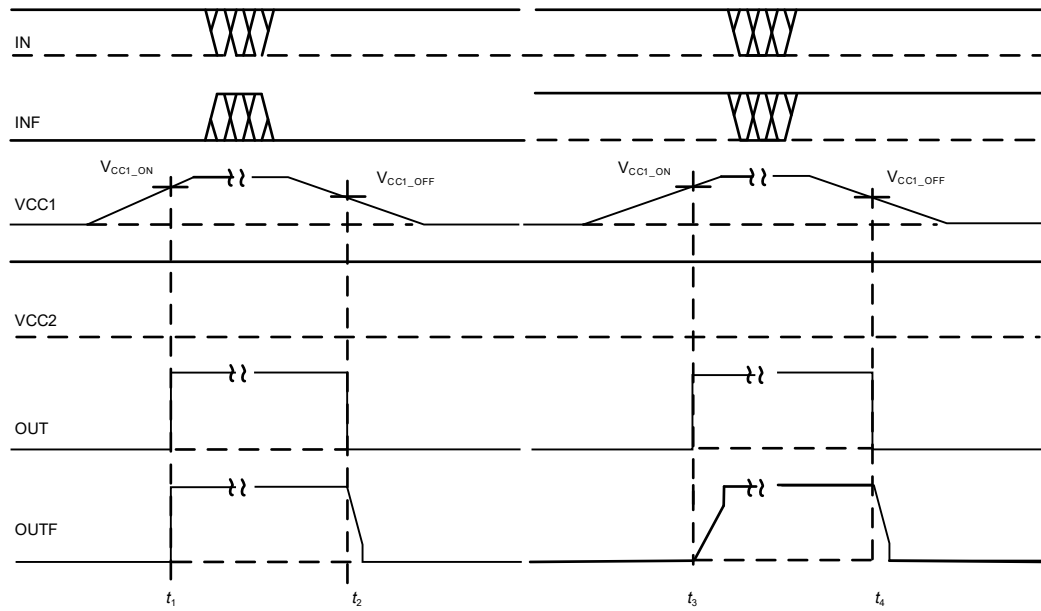


Figure 7.4 VCC1 power supply vs output status

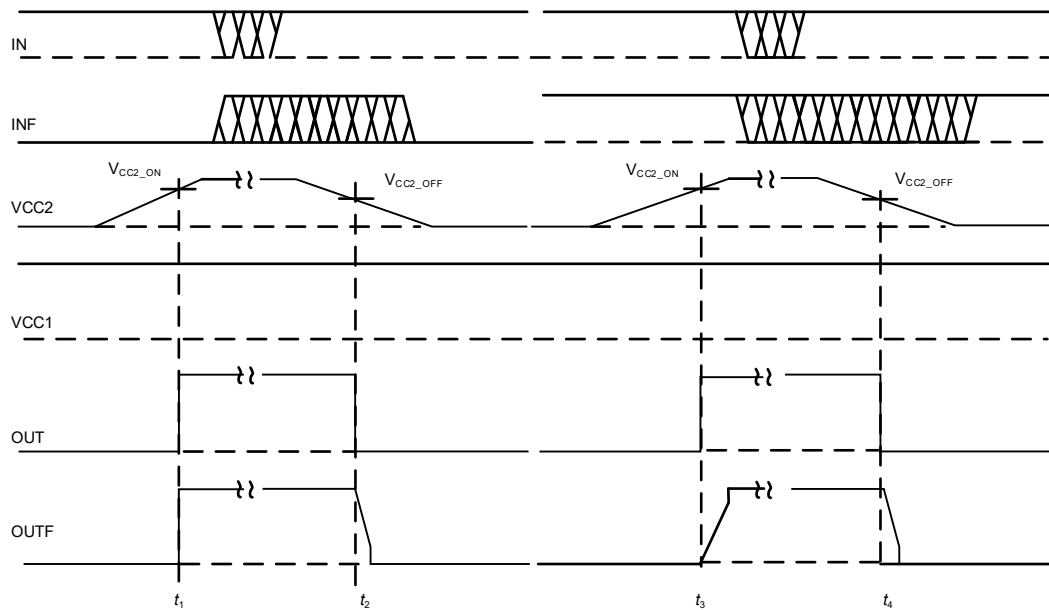


Figure 7.5 VCC2 power supply vs output status

7.5. Input characteristics

The IN and /INF input terminals dictate the operating behavior of the OUT and OUTF output terminals. A PWM signal applied to the IN terminal defines the switching characteristics of OUT and OUTF, while the /INF terminal controls whether only OUT or both OUT and OUTF track the IN input signal. Given that both OUT and OUTF are connected to gate resistors, the /INF terminal further determines if either a single gate resistor or both gate resistors are connected to the IGBT gate.

Both input terminals integrate pull-down resistors, which bias the IC into a safe operating mode if the connection to the system control circuit is interrupted. A short-pulse suppression filter with a dedicated filter time is implemented after the Schmitt trigger; all pulses with a width below t_{IN_min} / t_{INF_min} are suppressed. To enhance the integrated short-pulse suppression function and effectively filter input noise, external RC filters with a time constant of more than 10 ns (e.g., a 100 pF capacitor paired with a 100 Ω resistor) must be used.

7.6. Active Miller Clamp

The active miller clamp function helps to prevent the false turn-on of the power switches caused by the miller current in applications such as half bridge configuration, where switched off IGBT is false triggered during turn on period of the opposite IGBT. It usually happens when a unipolar power supply is used. To avoid such false turn-on of switches a miller clamp allows sinking the miller current across a low impedance path in this dv/dt situation. During turn-off the gate voltage is monitored, and the power-switch gate voltage is clamped to less than $V_{CLAMP_OFF_TH}$ referred to VEE2. The clamp is designed for a miller current in the same range as the nominal output current.

7.7. Slew Rate Control Logic

This timing diagram demonstrates the control logic and timing characteristics of the isolated gate driver, featuring input signals IN and INF as well as output signals OUT and OUTF. The main output OUT strictly toggles synchronously with the PWM edges of input IN. The behavior of the auxiliary output OUTF is jointly determined by the edges of IN and the logic level of INF.

As for NSI6601SRC, when INF is low, both OUT and OUTF are simultaneously pulled up to VCC2 at the rising edge of IN. When INF is high, OUTF remains in a high-impedance state during the turn-on process at the rising edge of IN. OUTF remains high impedance until the OUTF pin detects $V_{CLAMP_ON_TH}$ relative to VCC2, at which point OUTF is clamped to VCC2. When INF is high, both OUT and OUTF are pulled down to VEE2 simultaneously at the falling edge of IN. When INF is low, OUTF remains in a high-impedance state during the turn-off process at the falling edge of IN and stays high-impedance until the OUTF pin detects $V_{CLAMP_OFF_TH}$ relative to VEE2, at which point OUTF is clamped to VEE2.

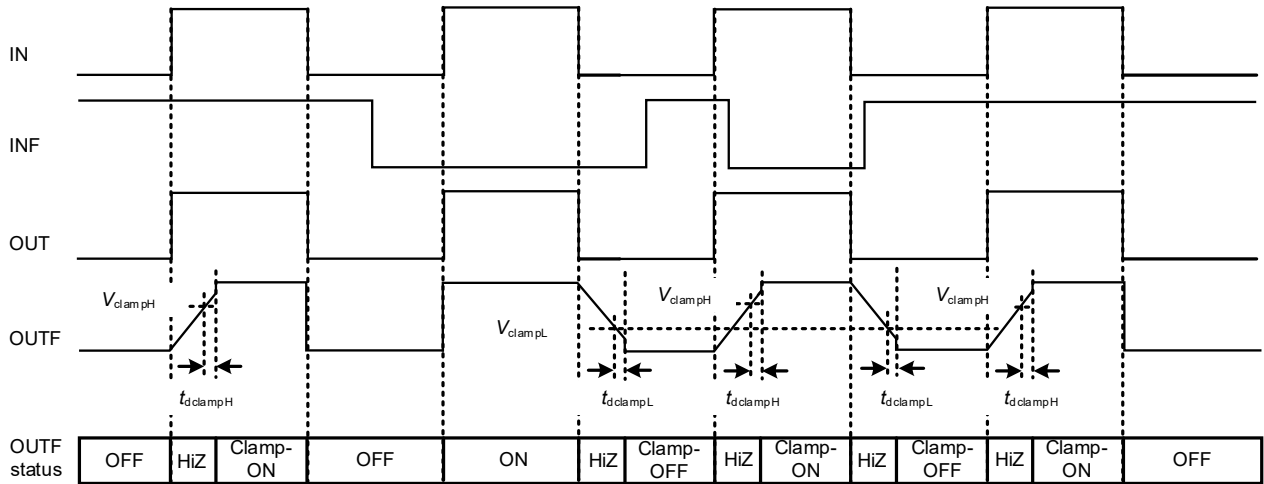


Figure 7.6 NSI6601SRC slew rate control logic

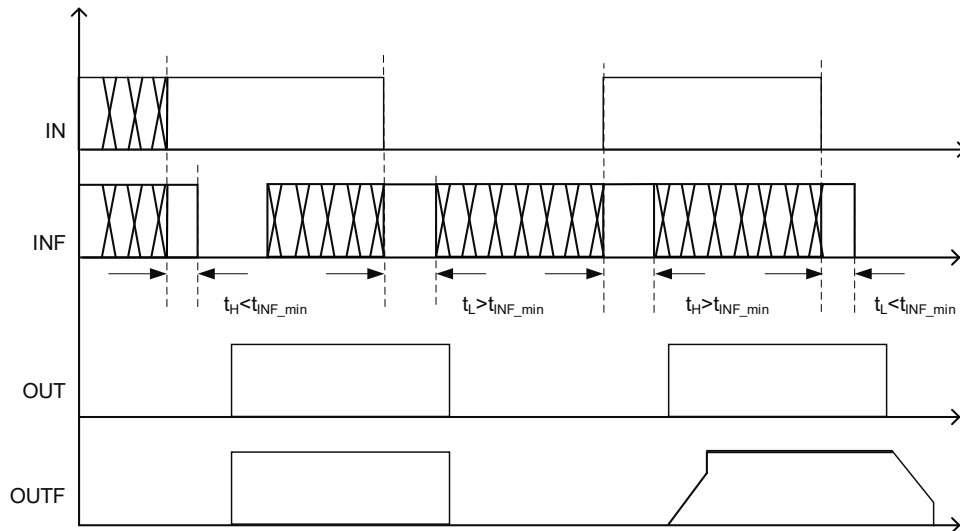


Figure 7.7 NSI6601SRC vs INF minimum pulse time

For the NSI6601SH3, when INF is high, both OUT and OUTF are pulled up to VCC2 simultaneously at the rising edge of IN.

When INF is low, OUTF remains in a high-impedance state during the turn-on process at the rising edge of IN and will not be clamped to VCC2 until the OUTF pin detects $V_{\text{clamp_on_th}}$ relative to VCC2; if $V_{\text{clamp_on_th}}$ is not detected by the OUTF pin after $t_{\text{clp_ON_delay}}$ has elapsed, OUTF will be forcibly clamped to VCC2. When INF is high both OUT and OUTF are pulled down to VEE2 simultaneously at the falling edge of IN. When INF is low, OUTF remains in a high-impedance state during the turn-off process at the falling edge of IN and will not be clamped to VEE2 until the OUTF pin detects $V_{\text{clamp_off_th}}$ relative to VEE2; if $V_{\text{clamp_off_th}}$ is not detected by the OUTF pin after $t_{\text{clp_off_delay}}$ has elapsed, OUTF will be forcibly clamped to VEE2.

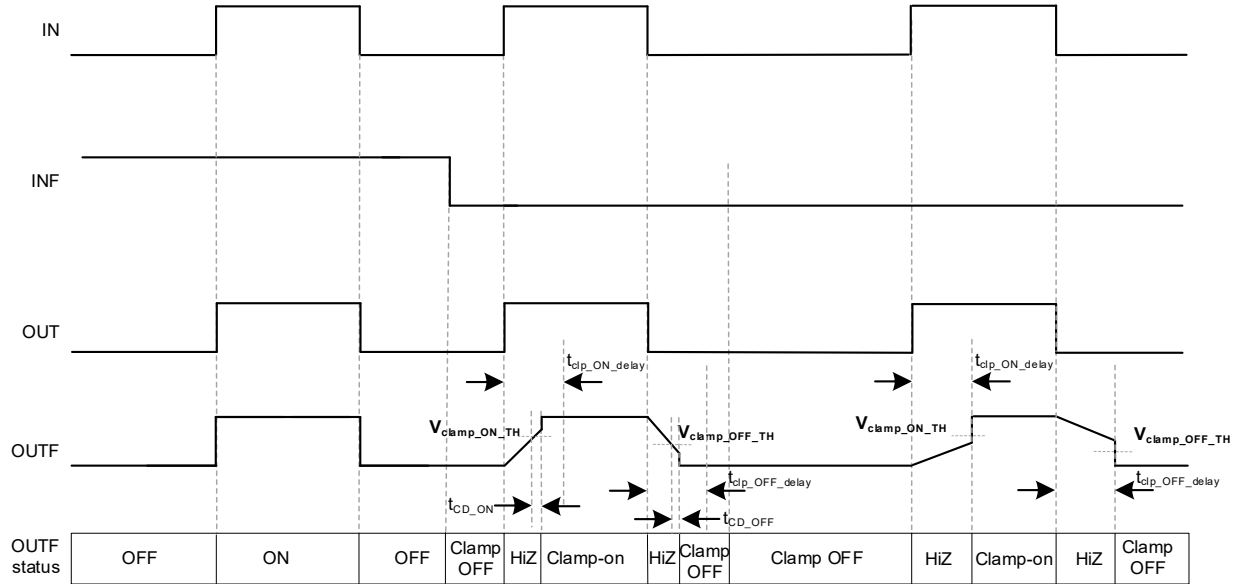


Figure 7.8 NSI6601SH3 slew rate control logic

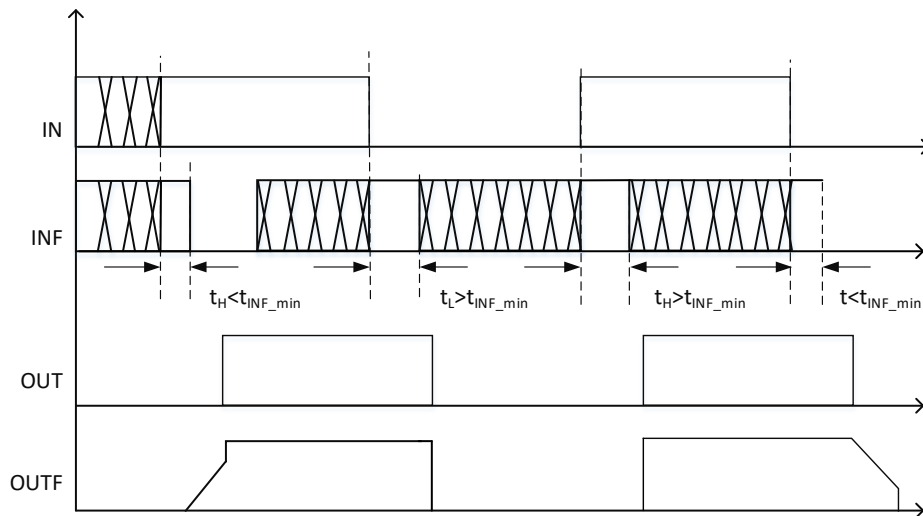


Figure 7.9 NSI6601SH3 vs INF minimum pulse time

For the NSI6601SHC, when INF is LOW, both OUT and OUTF are pulled up to VCC2 simultaneously at the rising edge of IN; when INF is HIGH, OUTF remains in a high-impedance state during the turn-on process at the rising edge of IN.

When INF is LOW, both OUT and OUTF are pulled down to VEE2 simultaneously at the falling edge of IN; when INF is HIGH, OUTF remains in a high-impedance state during the turn-off process at the falling edge of IN.

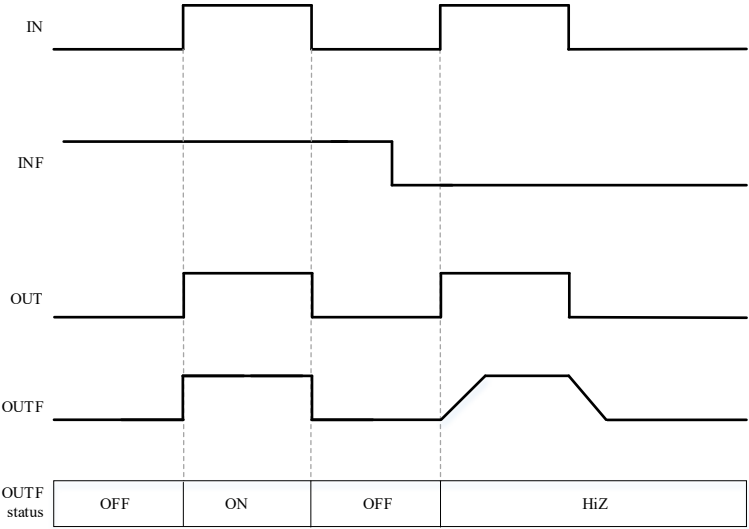


Figure 7.10 NSI6601SHC slew rate control logic

8. Application Note

8.1. Typical Application Circuit

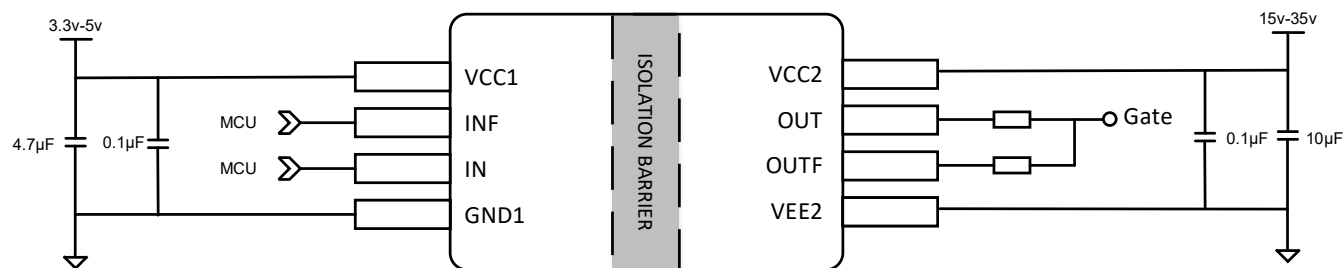


Figure 8.1 NSI6601S Typical Application Circuit

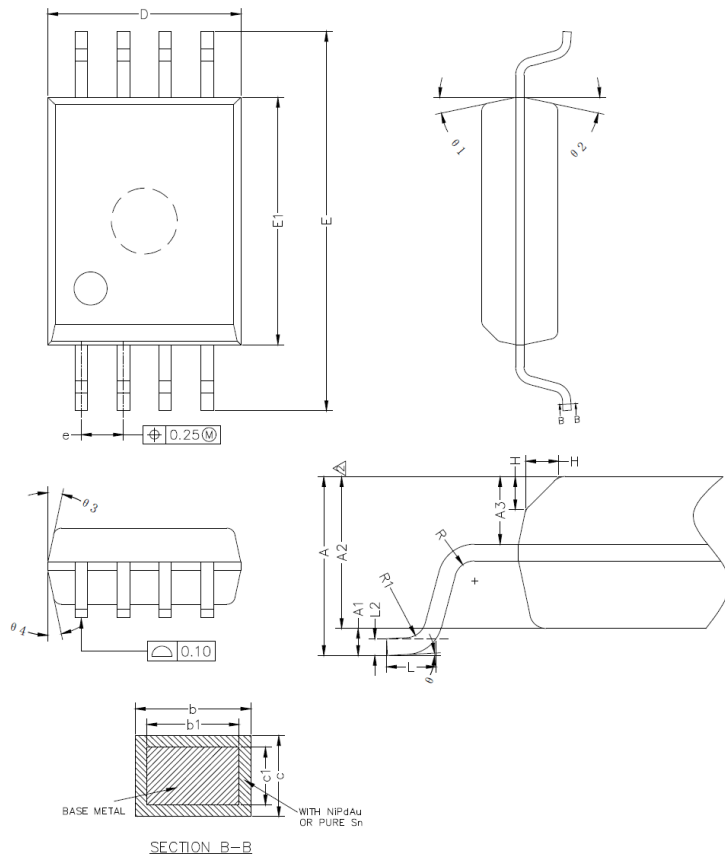
Bypassing capacitors for VCC1 and VCC2 supplies are needed to achieve reliable performance. To filter noise, a 0.1µF/50V ceramic capacitor is recommended to place as close as possible to NSI6601S, both at VCC1 and VCC2 sides. For VCC2 supply, an additional 10µF/50V ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the VCC1 or VCC2 power supply is located long distance from the IC, larger capacitance is needed.

8.2. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI6601S, between VCC1 to GND1, or VCC2 to VEE2.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6601S close to power transistor.
- Place large amount of copper connecting to VEE2 pin and VCC2 pin for thermal dissipation, with priority on VEE2 pin. If the system has multi VEE2 or VCC2 layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

9. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	2.85
A1	0.31	0.41	0.51
A2	2.20	2.30	2.40
A3	0.97	1.02	1.07
b PURE Sn	0.33	—	0.47
NiPdAu	0.33	—	0.44
b1	0.33	0.38	0.43
c PURE Sn	0.22	—	0.32
NiPdAu	0.22	—	0.29
c1	0.22	0.25	0.28
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.17	1.27	1.37
H	0.40	0.50	0.60
L	0.55	0.75	0.90
L1	2.00REF		
L2	0.25BSC		
R	0.07	—	—
R1	0.07	—	—
θ	0°	—	8°
θ 1	10°	12°	14°
θ 2	10°	12°	14°
θ 3	10°	12°	14°
θ 4	10°	12°	14°

NOTES:

1. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. TOP INDEX E-MARK $\phi 1.00 \pm 0.10$, DEPTH 0.10 ± 0.13 , BOTTOM E-MARK $\phi 2.00 \pm 0.10$, DEPTH 0.15 ± 0.13 .

Figure 9.1 SOW8 Package Shape and Dimension in millimeters

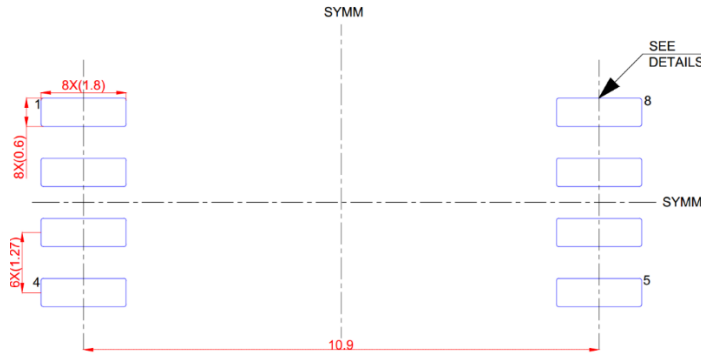


Figure 9.2 Land Pattern Example of SOW8 (mm)

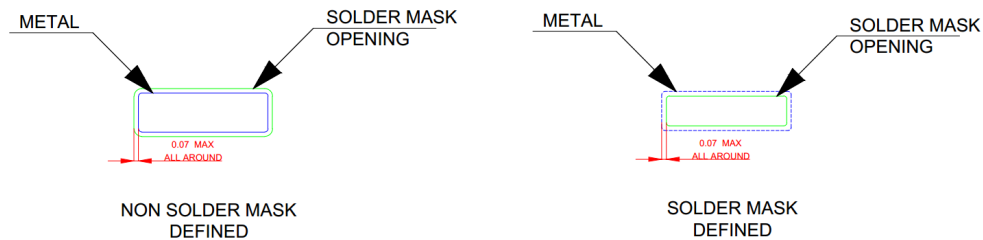


Figure 9.3 Solder Mask Detail of SOW8 (mm)

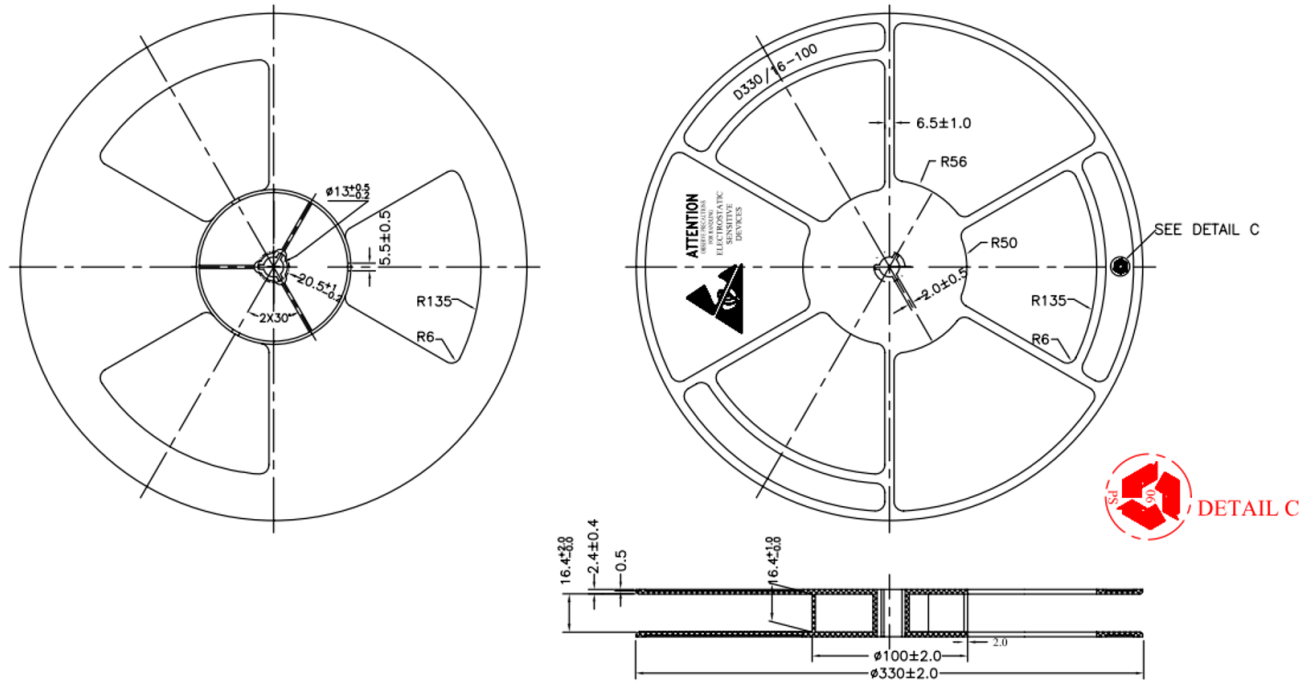
10. Ordering Information

Part Number	INF level of fast-switching		Clamping Feature	Temperature	MSL	Package Type	Category	MPQ	SPQ
	Rising	Falling							
NSI6601SRC-DSWVR	Low	High	Yes	-40 to 125°C	3	SOW8	Industrial	1000	1000
NSI6601SH3-DSWVR	High	High	Yes	-40 to 125°C	3	SOW8	Industrial	1000	1000
NSI6601SHC-DSWVR	Low	Low	No	-40 to 125°C	3	SOW8	Industrial	1000	1000

11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolated Driver Selection Guide
NSI6601S	Click here	Click here	Click here	Click here

12. Tape and Reel Information



Notes:

Material: Polystyrene (Black);

Flatness: Maximum allowable deviation: 3 mm;

Units: All dimensions are in millimeters (mm);

Surface Resistance: 10^5 to 10^{11} ohms per square (Ω/sq);

Unspecified Tolerances: ± 0.25 mm.

Figure 12.1 Tape Information

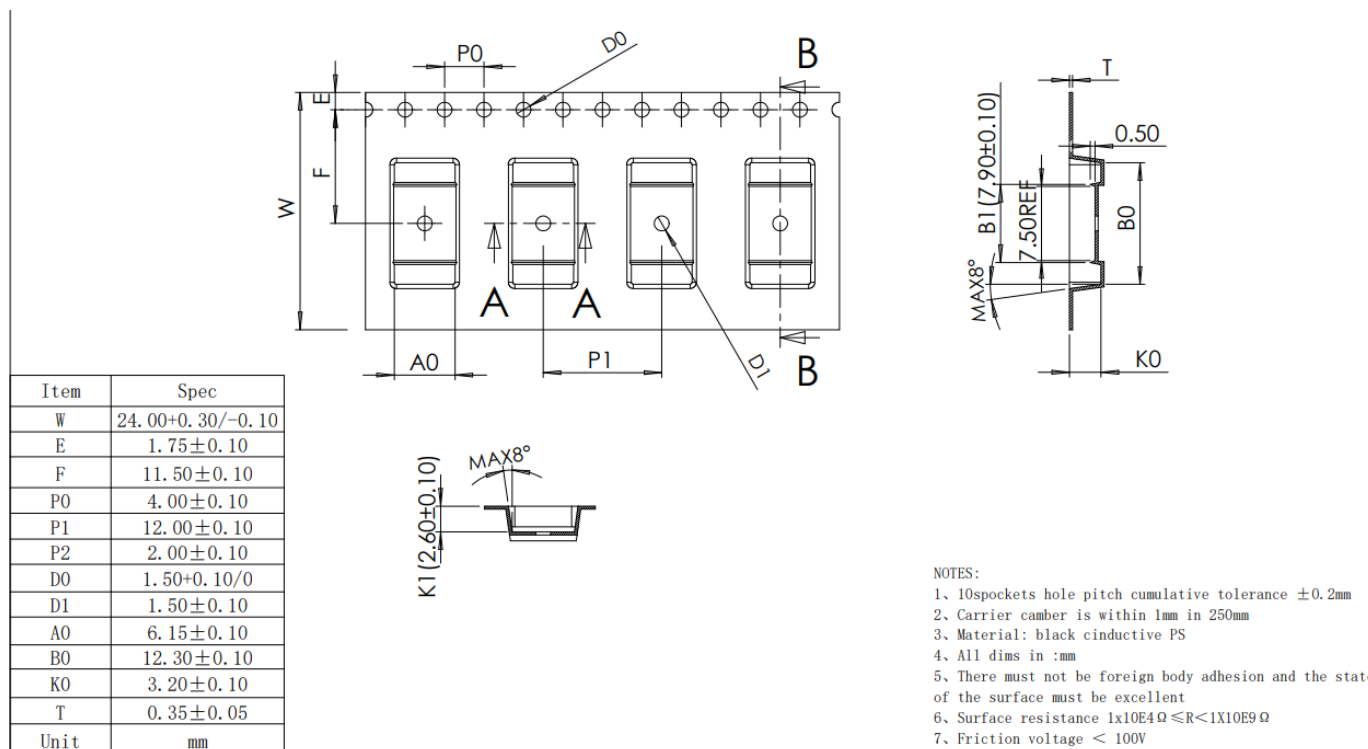


Figure 12.2 Reel Information of SOW8

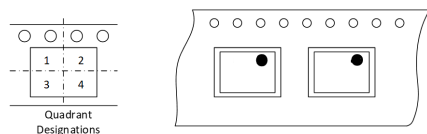


Figure 12.3 Quadrant Designation for Pin1 Orientation in Tape

13. Revision History

Revision		Description	Date
1.0	Initial version		2026/6/2

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