

Product Overview

The NSI6601 is a single-channel isolated gate driver designed to drive IGBTs, power MOSFETs and SiC MOSFETs in many applications. It provides split outputs that control the rise and fall time individually. It can source and sink 5A peak current.

The NSI6601 is available in SOP8 package, which can support 3000V_{RMS} isolation per UL1577. System robustness is supported by 150kV/ μ s minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 28V, while the input-side accepts from 3.1V to 17V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

With high driving current, excellent robustness, wide supply voltage range and fast signal propagation, NSI6601 is suitable for high reliability, power density and efficiency switching power system.

Key Features

- Isolated single-channel driver
- Input side supply voltage: 3.1V to 17V
- Driver side supply voltage: up to 28V with 9V/13V UVLO
- 5A peak source and sink output current
- High CMTI: $\pm 150\text{kV}/\mu\text{s}$
- 78ns typical propagation delay
- Operation ambient temperature: $-40^\circ\text{C} \sim 125^\circ\text{C}$
- RoHS & REACH Compliance:
- AEC-Q100 (Grade 1) qualified for auto-motive application

Safety Regulatory Approvals

- UL recognition: 3000V_{RMS} for 1 minute per UL1577
- DIN VDE V 0884-17:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2022

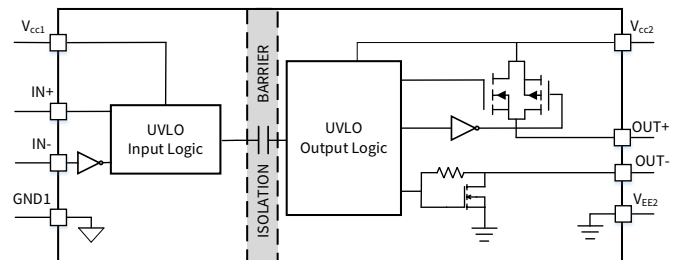
Applications

- Isolated DC/DC and AC/DC Power Supplies
- High Voltage PFC
- Solar Inverters
- Motor Drives and EV Charging
- UPS and Battery Chargers

Device Information

Part Number	UVLO Level	Package	Body Size
NSI6601B-Q1SPR	9V	SOP8	4.9×3.9×1.35mm
NSI6601C-Q1SPR	13V	SOP8	4.9×3.9×1.35mm

Functional Block Diagrams



NSI6601 Block Diagram

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1. Pin Configuration and Functions

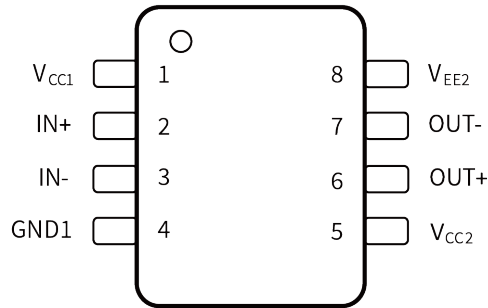


Figure 1.1 NSI6601 Top View

Table 1.1 NSI6601 Pin Configuration and Description

NSI6601 PIN NO.	Symbol	Function
1	V _{CC1}	Input-side supply rail
2	IN+	Non-inverted input signal with internal pull down to GND1
3	IN-	Inverted input signal with internal pull up to V _{CC1}
4	GND1	Input-side ground reference
5	V _{CC2}	Positive output supply rail
6	OUT+	Driver source output
7	OUT-	Driver sink output
8	V _{EE2}	Negative output supply rail

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	$V_{CC1-GND1}$	-0.3	18	V
Input Signal Voltage	$V_{IN+-GND1}, V_{IN--GND1}$	-0.3	18	V
Driver Side Supply Voltage	$V_{CC2-V_{EE2}}$	-0.3	35	V
Output Signal Voltage	V_{OUT+}, V_{OUT-}	$V_{EE2}-0.3$	$V_{CC2}+0.3$	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD <ul style="list-style-type: none"> All pins 	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB <ul style="list-style-type: none"> All pins 	±1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	$V_{CC1-GND1}$	3.3	17	V
Input Signal Voltage	$V_{IN+-GND1}, V_{IN--GND1}$	-0.3	17	V
Driver Side Supply Voltage	$V_{CC2-V_{EE2}}(NSI6601B)$	10	28	V
	$V_{CC2-V_{EE2}}(NSI6601C)$	13.7	28	V
Ambient Temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	NSI6601	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	120	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	38	°C/W

6. Specifications

6.1. DC Electrical Characteristics

(Unless otherwise noted, $V_{CC1}=5V$, $V_{CC2}=15V$, $V_{EE2}=GND2$. Typical values are at $T_A=25^{\circ}C$. All min and max specifications are at $T_A=-40^{\circ}C$ to $125^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Currents						
Input Supply Quiescent Current	I_{CC1}		0.9	1.5	mA	
Output Supply Quiescent Current	I_{CC2}		1.6	3	mA	
Input Side Supply UVLO Threshold						
VCC1 UVLO Rising Threshold	V_{CC1_ON}		2.9	3.1	V	
VCC1 UVLO Falling Threshold	V_{CC1_OFF}	2.55	2.79		V	
VCC1 UVLO Hysteresis	V_{CC1_HYS}		0.11		V	
Driver Side Supply UVLO Threshold						
VCC2 UVLO Rising Threshold	V_{CC2_ON}		9.2	10	V	
VCC2 UVLO Falling Threshold	V_{CC2_OFF}	8	8.5		V	
VCC2 UVLO Hysteresis	V_{CC2_HYS}		0.7		V	
Driver Side Supply UVLO Threshold (NSI6601C, 13V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC_ON}		13.2	13.7	V	
VCC UVLO Falling Threshold	V_{CC_OFF}	11.7	12.3		V	
VCC UVLO Hysteresis	V_{CC_HYS}		0.9		V	
Input Pin Characteristic						
Logic High Input Threshold (IN+, IN-)	V_{IN+H}, V_{IN-H}			$0.7 \times V_{CC1}$	V	
Logic Low Input Threshold (IN+, IN-)	V_{IN+L}, V_{IN-L}	$0.3 \times V_{CC1}$			V	
Input Hysteresis Voltage (IN+, IN-)	V_{hys_IN}		$0.1 \times V_{CC1}$		V	
IN+ Input Current	I_{IN+}		55	100	μA	$V_{IN+}=V_{CC1}$
IN- Input Current	I_{IN-}		55	100	μA	$V_{IN-}=GND1$
Output Pin Characteristic						
High Level Output Voltage	V_{OH}	$V_{CC2}-0.25$	$V_{CC2}-0.14$		V	$I_{OUT+}=-50mA$, $V_{IN+}=High$, $V_{IN-}=Low$
Low Level Output Voltage	V_{OL}		30	60	mV	$I_{OUT+}=50mA$, $V_{IN+}=Low$, $V_{IN-}=High$
Peak Source Output Current	I_{OUT+}		5		A	$V_{CC2}=15V$, pulse width $<10\mu s$

Peak Sink Output Current	I_{OUT-}		5		A	$V_{CC2}=15V$, pulse width $<10\mu s$
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6.2. Switching Characteristics

(Unless otherwise noted, $V_{CC1}=5V$, $V_{CC2}=15V$, $V_{EE2}=GND2$. Typical values are at $T_A=25^{\circ}C$. All min and max specifications are at $T_A=-40^{\circ}C$ to $125^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Minimum Pulse Width	t_{PWmin}		30	70	ns	
Propagation Delay	t_{pLH}	50	78	110	ns	$C_{LOAD}=100pF$
Propagation Delay	t_{pHL}	50	78	110	ns	$C_{LOAD}=100pF$
Pulse Width Distortion $ t_{pLH}-t_{pHL} $	t_{PWD}		2	25	ns	$C_{LOAD}=100pF$
Output Rise Time (20% to 80%)	t_R		9	20	ns	$C_{LOAD}=1nF$
Output Fall Time (80% to 20%)	t_F		8	19	ns	$C_{LOAD}=1nF$
Common Mode Transient Immunity	CMTI	150			kV/ μ s	Verified by design

6.3. Typical Performance Characteristics

(Unless otherwise noted, $V_{CC1}=5V$, $V_{CC2}=15V$, $V_{EE2}=GND2$, $T_A=25^{\circ}C$)

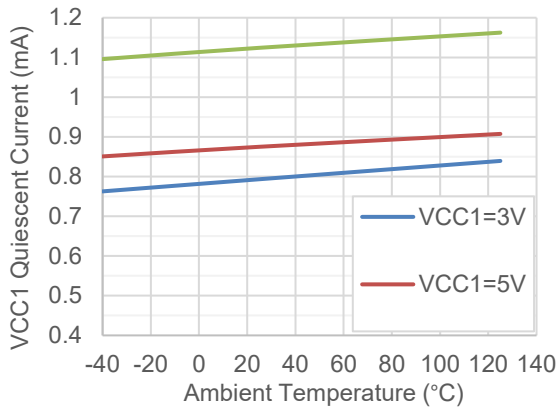


Figure 6.1 Input supply quiescent current versus Temperature

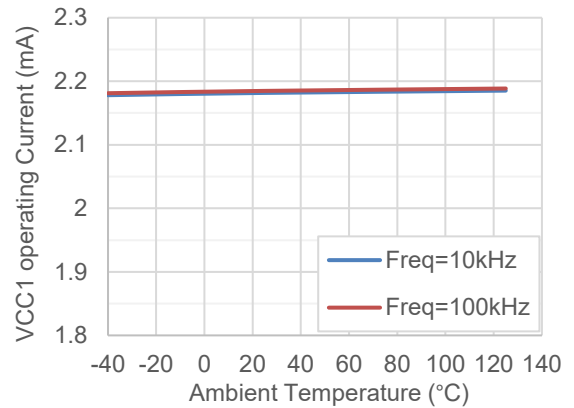


Figure 6.2 Input supply operating current versus Temperature

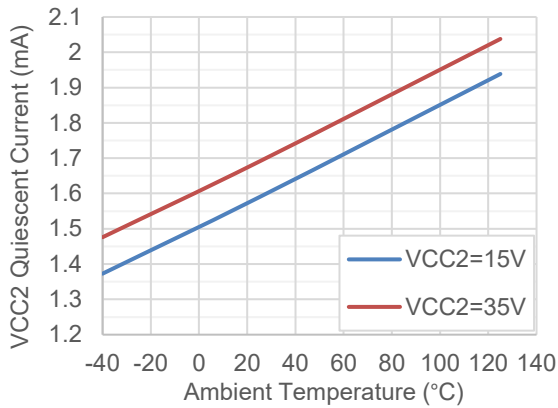


Figure 6.3 Output supply quiescent current versus Temperature

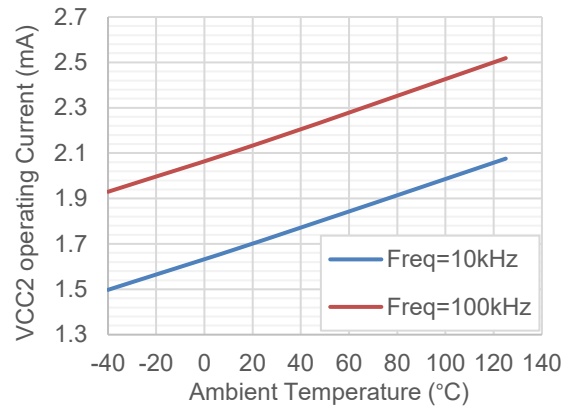


Figure 6.4 Output supply operating current versus Temperature

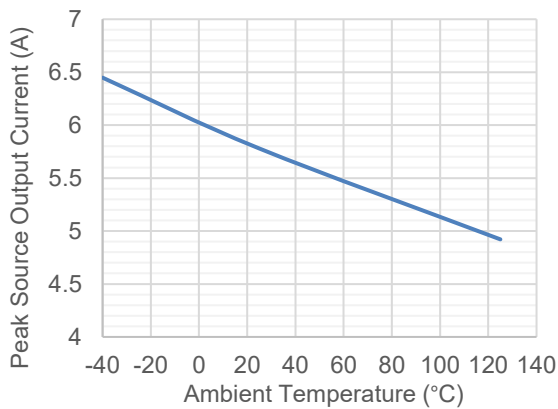


Figure 6.5 Peak source output current versus Temperature

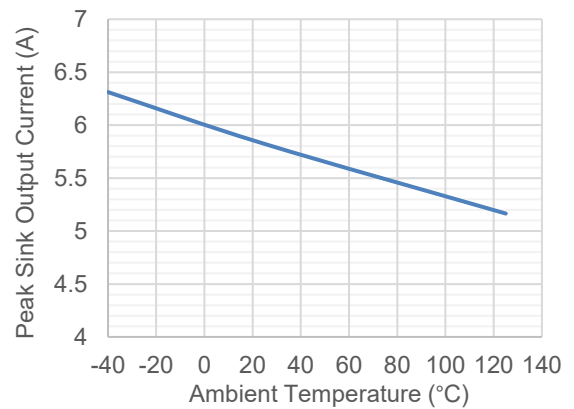


Figure 6.6 Peak sink output current versus Temperature

6.4. Parameter Measurement Information

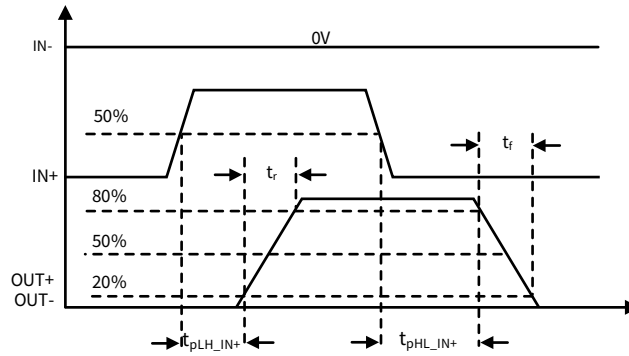


Figure 6.7 Propagation Delay, Rise Time and Fall Time, Non-inverting Configuration

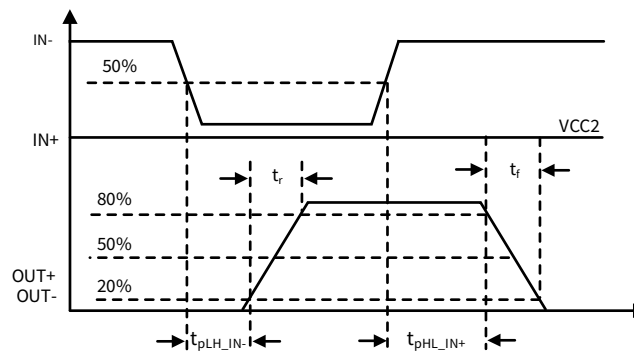


Figure 6.8 Propagation Delay, Rise Time and Fall Time, Inverting Configuration

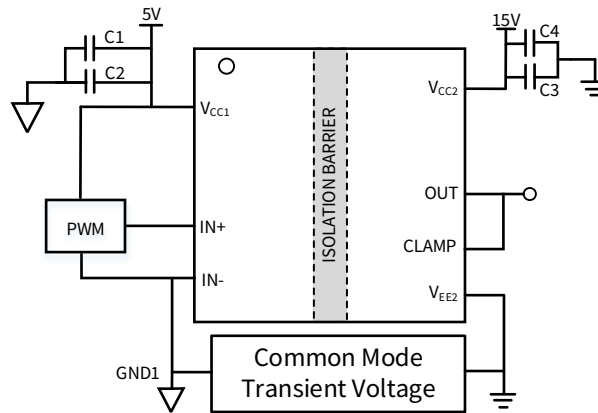


Figure 6.9 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

<i>Parameters</i>	<i>Symbo l</i>	<i>NSI6601</i>	<i>Unit</i>	<i>Comments</i>
Minimum External Air Gap (Clearance)	CLR	4.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	4.0	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	20	µm	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60112

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 150 V_{RMS}$		I to IV	
	For Rated Mains Voltage $\leq 300 V_{RMS}$		I to III	
Climatic Category			40/125/2 1	
Pollution Degree			2	
DIN EN IEC 60747-17(VDE 0884-17)				
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	700	V_{RMS}
	DC voltage		990	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	990	V_{PEAK}
Apparent Charge	Input to Output Test Voltage, Method B1, $V_{pd(m)}=V_{IORM} \times 1.5$, 100% production test, $t_{ini}=t_m=1s$	q_{pd}	<5	pC
	Method A , After Environmental Tests Subgroup 1, $V_{pd(m)}=V_{IORM} \times 1.2$, $t_{ini}=60s$, $t_m=10s$			pC
	After Input and Output Safety Test Subgroup 2 and Subgroup 3, $V_{pd(m)}=V_{IORM} \times 1.2$, $t_{ini}=60s$, $t_m=10s$			pC
Maximum Transient Isolation Voltage	$t = 60s$	V_{IOTM}	4242	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50 μ s waveform per IEC62368-1	V_{imp}	3500	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50 μ s waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	6000	V_{PEAK}
Isolation Resistance	$V_{IO} = 500V$ at $T_A=T_S=25^\circ C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500V$ at $T_A=T_S=150^\circ C$		$>10^9$	Ω
	$V_{IO} = 500V$ at $100^\circ C \leq T_A \leq 125^\circ C$		$>10^{11}$	Ω
Isolation Capacitance	$f = 1MHz$	C_{IO}	1	pF
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1s$ (100% production test)	V_{ISO}	3000	V_{RMS}

7.3. Safety Limiting Values

Description	Test Condition	Symbol	Value	Unit	
Maximum Safety Temperature		T_s	150	°C	
Maximum Safety Power Dissipation	$R_{\theta JA}=120^{\circ}\text{C/W}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	P_s	Total	1.14	W
			Input Side	0.05	
			Output Side	1.09	
Maximum Safety Current	$R_{\theta JA}=110^{\circ}\text{C/W}$, $V_{CC2}=15\text{V}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	I_s	Output Side	73	mA
	$R_{\theta JA}=110^{\circ}\text{C/W}$, $V_{CC2}=30\text{V}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$		Output Side	36	

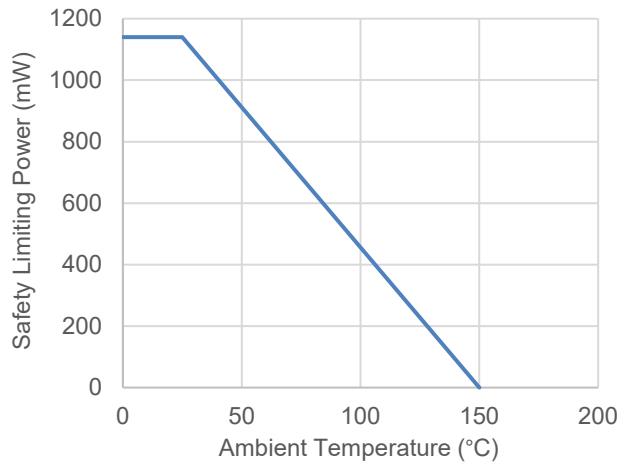


Figure 7.1 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-17

7.4. Regulatory Information

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 3000V _{RMS} Isolation Voltage	Single Protection, 3000V _{RMS} Isolation voltage	Basic Insulation $V_{IORM}=990\text{V}_{PEAK}$, $V_{IOTM}=4242\text{V}_{PEAK}$, $V_{IOSM}=6000\text{V}_{PEAK}$	Basic Insulation
Certificate No.E500602		Certificate No.40050121	CQC20001264940

8. Function Description

8.1. Overview

The NSI6601 is a high reliable power transistor gate driver. It has 9V UVLO version, which is suitable to drive MOSFET, IGBT, or SiC MOSFET. The NSI6601 is available in SOP8 narrow body, which can support 3000V_{RMS} isolation per UL1577. System robustness is supported by 150kV/μs minimum common-mode transient immunity (CMTI).

The isolation barrier inside NSI6601 is based on a capacitive isolation. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI. As shown in Figure 8.2, the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

The functional block diagram of NSI6601 is shown in Figure 8.1. Two Input pins with non-inverting and inverting logic support interlock and shoot through protection. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Split outputs can control the rise and fall time individually. Active pull-down and short circuit clamping features are implemented to protect power transistor.

8.2. Functional Block Diagram

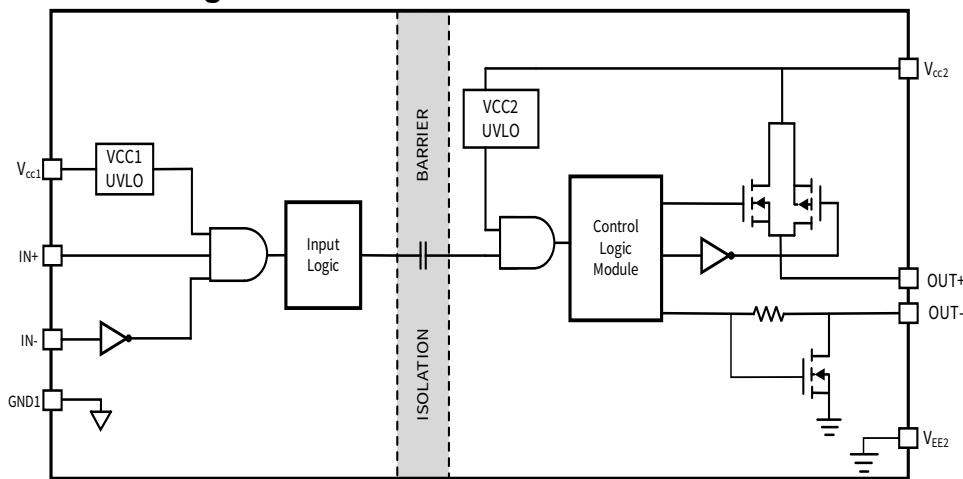


Figure 8.1 NSI6601 Functional Block Diagram

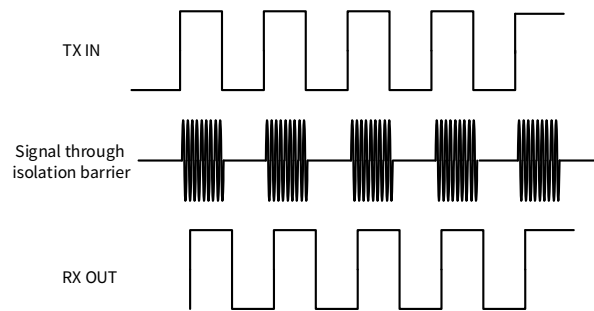


Figure 8.2 OOK Modulation

8.3. Truth Tables

Table 8.1 Driver Function Table ⁽¹⁾

<i>V_{CC1}</i> <i>status</i>	<i>V_{CC2}</i> <i>status</i>	<i>Inputs</i>		<i>Outputs</i>		<i>Comment</i>
		<i>IN+</i>	<i>IN-</i>	<i>OUT+</i>	<i>OUT-</i>	
PU	PU	H	L	H	Hi-Z	
PU	PU	L	H	Hi-Z	L	
PU	PU	H	H	Hi-Z	L	Interlock protection
PU	PU	L	L	Hi-Z	L	
PD	PU	X	X	Hi-Z	L	
PU	PD	X	X	Hi-Z	L	Active pull-down
PD	PD	X	X	Hi-Z	L	Active pull-down

(1) PD = Powered Down; PU = Powered Up; H = Logic High; L = Logic Low; X = Irrelevant

The IN+ pin is internally pulled down to GND1, while IN- pin is internally pulled up to VCC1, making the output of NSI6601 is low by default. To improve noise immunity, grounding an input or tying to VCC1 is recommended.

To control the output during normal operation, PWM from MCU is connected to IN+ pin or IN- pin. A minimum input pulse width is defined to filter occasional glitches.

From the truth table, interlock protection and active pull-down is obtained. See Chapter 8.6 and Chapter 9.2 for detailed description.

8.4. Output Stage

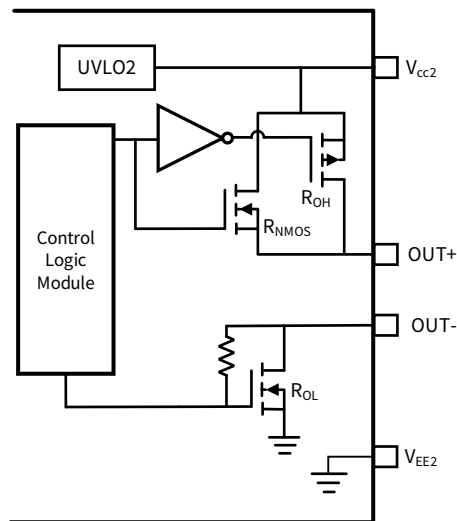


Figure 8.3 NSI6601 Output Stage

Table 8.2 NSI6601 Output Stage On-Resistance

<i>R_{NMOS}</i>	<i>R_{OH}</i>	<i>R_{OL}</i>	<i>Unit</i>
0.8	2.8	0.6	Ω

The NSI6601 has P-channel and N-channel MOSFET in parallel to pull up the OUT+ pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET.

The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSI6601 N-channel MOSFET turns on to pull up OUT+ more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of NSI6601. The equivalent pull-up resistance of NSI6601 is the parallel combination $R_{OH} \parallel R_{NMOS}$. The result is quite small, indicating the strong driving capability of NSI6601. The pull-down structure of NSI6601 is simply composed of an N-channel MOSFET with on-resistance of R_{OL} . The result is quite small, indicating the strong driving capability of NSI6601.

8.5. V_{CC1} , V_{CC2} and Under Voltage Lock Out (UVLO)

To ensure correct switching the device is equipped with an undervoltage lockout for input and output power supply independently. V_{CC1} voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver output can become clamped low. Output supply UVLO is referred to V_{EE2} pin. If $V_{CC2}-V_{EE2}$ falls below the UVLO threshold, OUT- of the gate-driver will be clamped low.

Local bypass capacitors should be placed between the V_{CC2} and V_{EE2} pins, as well as the V_{CC1} and GND1 pins. 220nF to 10 μ F is recommended for device biasing. Additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. The capacitors should be positioned as close to the device as possible for better noise filtering. Low-ESR, ceramic surface-mount capacitors are recommended.

8.6. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC2} is not connected to the power supply. When V_{CC} is floating, the driver output is held low and clamping OUT to approximately 1.8V higher than V_{EE2} .

8.7. Short Circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the miller capacitance. The diode between OUT+ and V_{CC2} pins inside the driver limits this voltage to approximately 0.7V higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10 μ s. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

9. Application Note

9.1. Typical Application Circuit

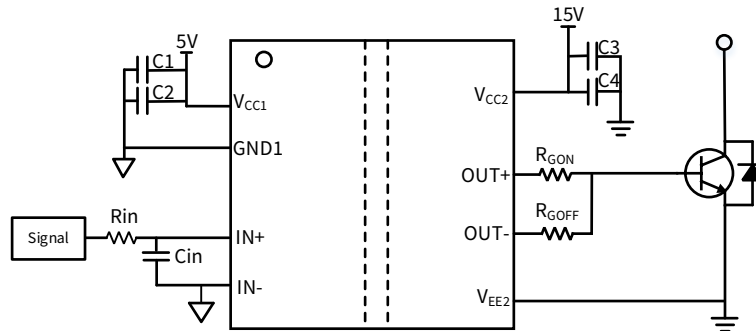


Figure 9.1 NSI6601 Typical Application Circuit

Bypassing capacitors for V_{CC1} and V_{CC2} supplies are needed to achieve reliable performance. To filter noise, $0.1\mu\text{F}/50\text{V}$ ceramic capacitor is recommended to place as close as possible to NSI6601, both at V_{CC1} and V_{CC2} side. For V_{CC2} supply, additional $10\mu\text{F}/50\text{V}$ ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the V_{CC1} or V_{CC2} power supply is located long distance from the IC, bigger capacitance is needed.

The input filter composed by R_{in} and C_{in} can be used if input PWM has ring due to long traces or bad PCB layout. However, it will introduce longer propagation delay.

9.2. Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSI6601 can be used. Interlock protection is possible as shown in Figure 9.2. If the controller has some mistake, leading to negative dead time, the output PWM of NSI6601 is adjusted to avoid power transistor shoot through.

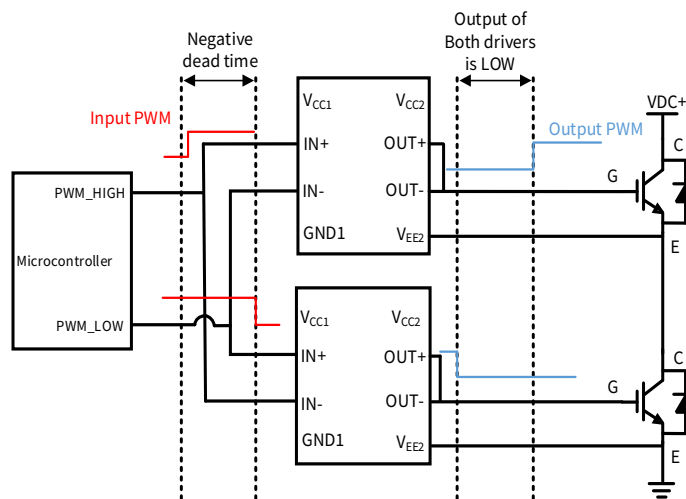


Figure 9.2 Interlock Protection using NSI6601

9.3. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI6601, between V_{CC1} to $GND1$, or V_{CC2} to V_{EE2} .
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6601 close to power transistor.

- Place large amount of copper connecting to V_{EE2} pin and V_{CC2} pin for thermal dissipation, with priority on V_{EE2} pin. If the system has multi V_{EE2} or V_{CC2} layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

10. Package Information

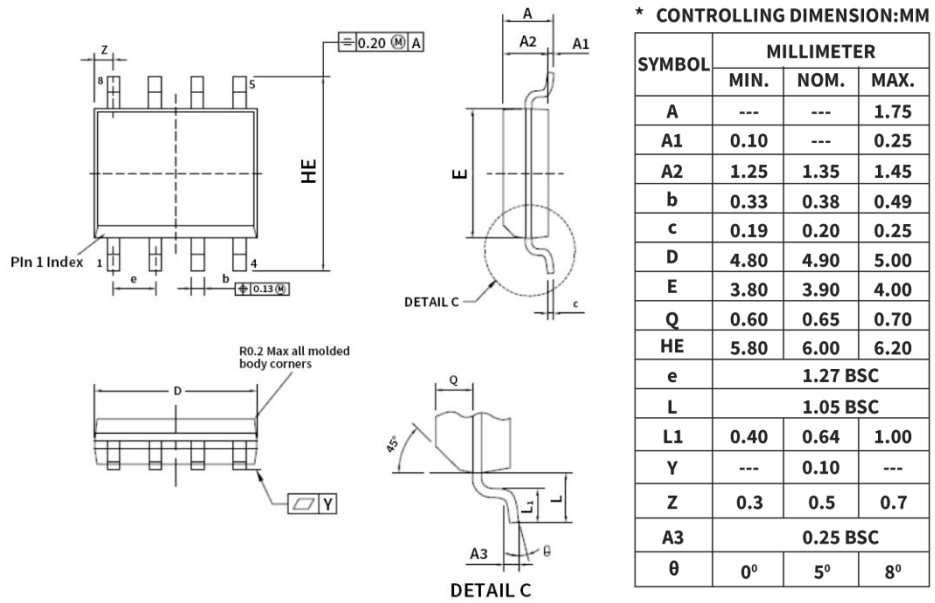


Figure 10.1 Package Shape and Dimension in millimeters

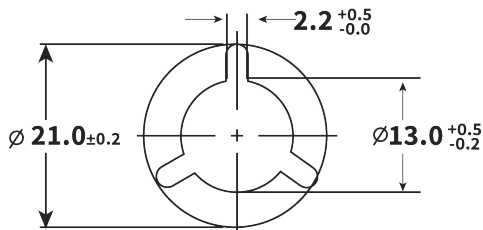
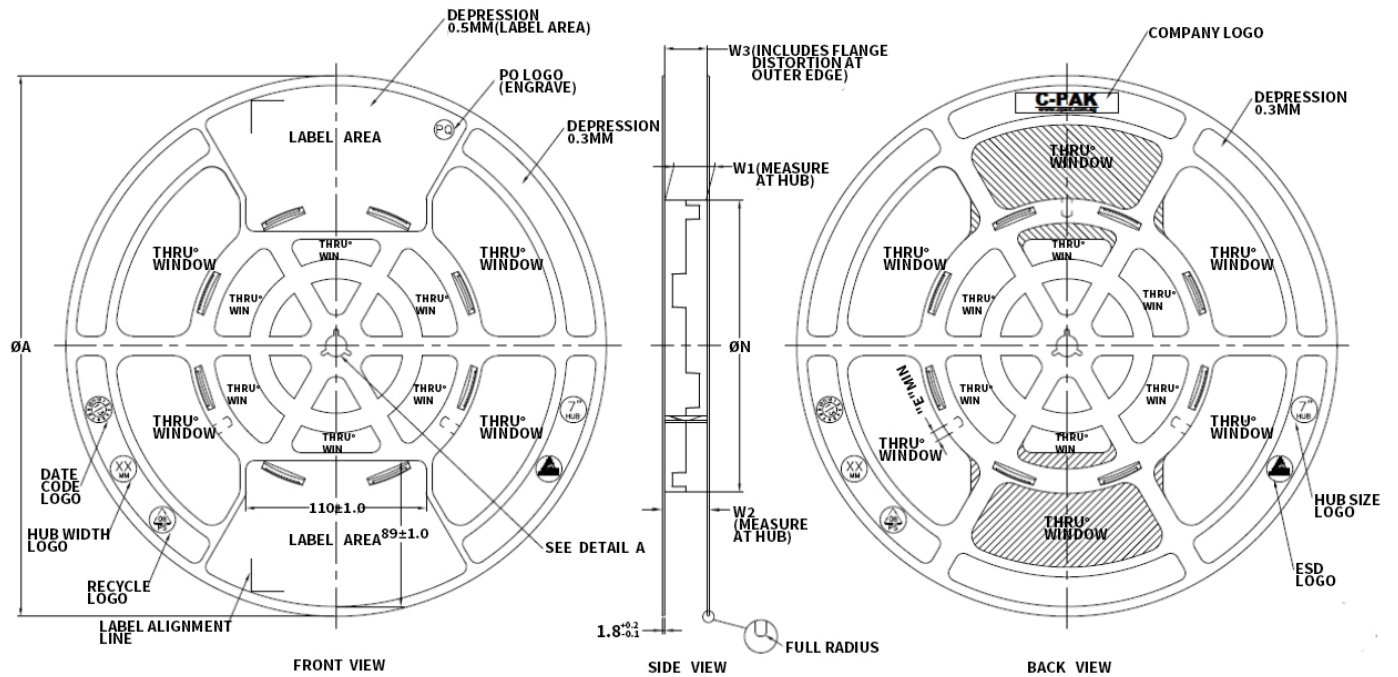
11. Ordering Information

<i>Part Number</i>	<i>Isolation Rating (kV)</i>	<i>UVLO Level</i>	<i>Temperature</i>	<i>MSL</i>	<i>Package Type</i>	<i>SPQ</i>	<i>AEC-Q100</i>
NSI6601B-Q1SPR	3	9V	-40 to 125°C	1	SOP8	2500	YES
NSI6601C-Q1SPR	3	13V	-40 to 125°C	1	SOP8	2500	YES

12. Documentation Support

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolated Driver Selection Guide</i>
NSI6601	tbd	tbd	tbd	tbd

13. Tape and Reel Information



**ARBOR HOLE
DETAIL A
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	$\varnothing A \pm 2.0$	$\varnothing N \pm 2.0$	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^6 TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^5 & BELOW 10^5	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^9 TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 13.1 Tape Information

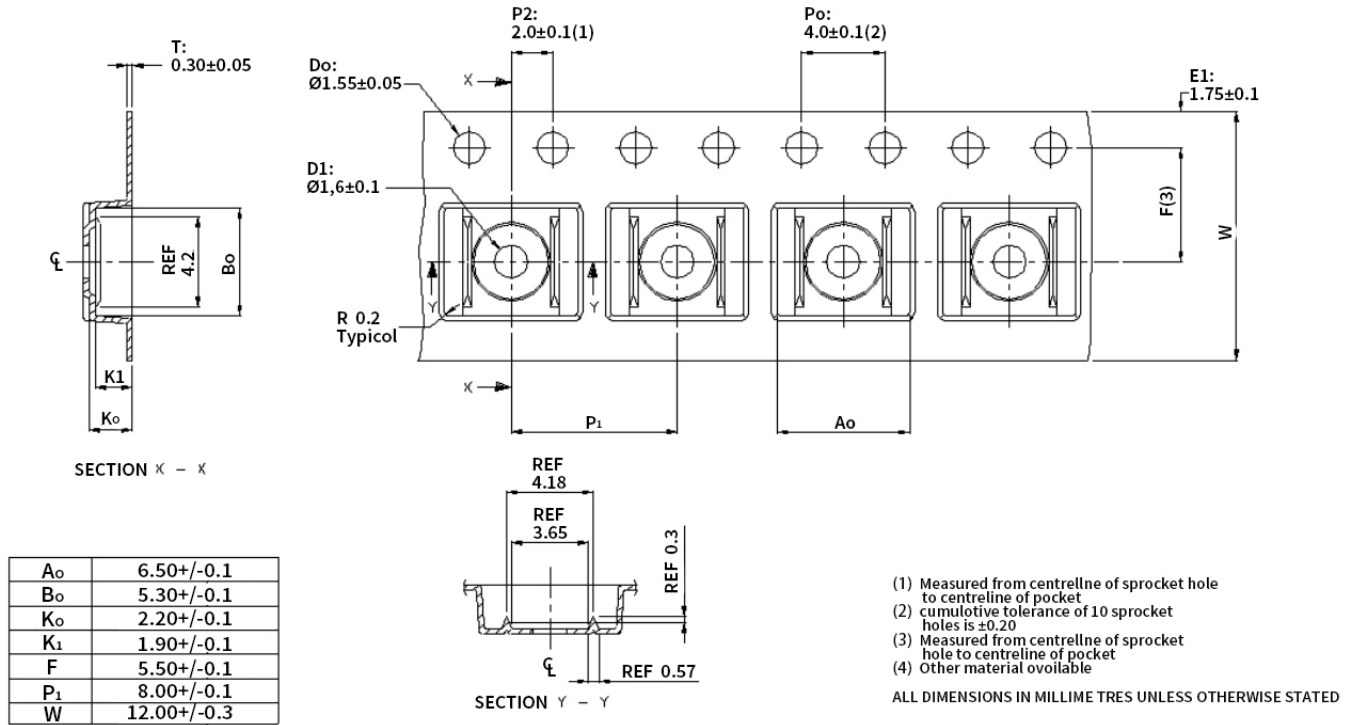


Figure 13.2 Reel Information

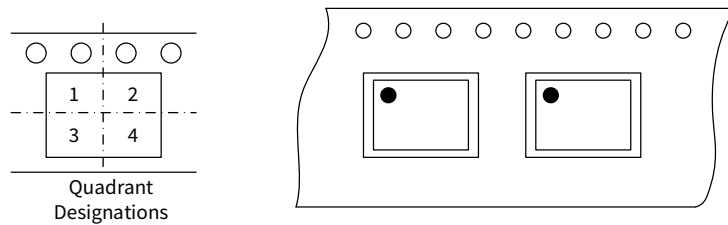


Figure 13.3 Quadrant Designation for Pin1 Orientation in Tape

14. Revision History

Revision	Description	Date
1.0	Initial version	2024/8/2
1.1	Add specifications for NSI6601C	2025/3/27

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