

Product Overview

The NSI36C12R is a high performance isolated amplifier with integrated isolated power supply that accept fully-differential input of $\pm 1V$. The integrated isolated power supply enables single-power operation on the low side of the device without the need for a separate isolated power supply for the high side, effectively reducing the board area. The high input impedance of NSI36C12R makes it highly suitable for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

The device has a ratiometric gain of $V_{REF}/2.56$ and provides a single-ended analog output. V_{REF} defines the clipping output voltage. Apply the supply voltage of the subsequent ADC to V_{REF} to match the entire ADC dynamic input range. The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching as in motor control applications. The input over-threshold protection supports externally adjustable threshold voltage and provides an open-drain protection fault output to simplify system-level design and diagnostics.

Key Features

- Up to 5000V_{rms} Insulation voltage
- $\pm 1V$ linear Input Voltage Range
- Low Offset Error and Drift:
 $\pm 0.5mV$ (Max), $\pm 10\mu V/^\circ C$ (Max)
- Low Gain Error and Drift:
 $\pm 0.3\%$ (Max), $\pm 45ppm/^\circ C$ (Max)
- Low Nonlinearity and Drift:
 $\pm 0.04\%$ (Max), $\pm 1ppm/^\circ C$ (Typ)
- SNR: 80dB (Typ, BW=10kHz), 70dB (Typ, BW=100kHz)
- Wide bandwidth: 340kHz (Typ)

- High CMTI: 150kV/ μs (Typ)
- System-Level Diagnostic Features: integrated isolated power supply detection
- Operation Temperature: $-40^\circ C \sim 125^\circ C$
- AEC-Q100 qualified for automotive applications: Grade 1
- RoHS-Compliant Packages: SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- On Board Chargers
- DC/DC Converters
- Traction Inverters
- Battery Management Units

Device Information

Part Number	Package	Body Size
NSI36C12R-Q1SWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

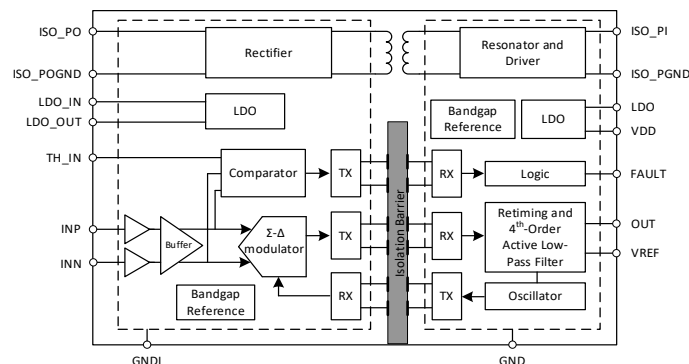


Figure 1. Function Block Diagram of NSI36C12R

INDEX

1. PIN CONFIGURATION AND FUNCTIONS.....	3
2. ABSOLUTE MAXIMUM RATINGS ⁽¹⁾	4
3. ESD RATINGS ⁽¹⁾	4
4. RECOMMENDED OPERATING CONDITIONS.....	4
5. THERMAL INFORMATION.....	5
6. SPECIFICATIONS.....	5
6.1. ELECTRICAL CHARACTERISTICS.....	5
6.2. TIMING DIAGRAMS	8
6.3. TYPICAL PERFORMANCE CHARACTERISTICS	9
7. HIGH VOLTAGE FEATURE DESCRIPTION	15
7.1. INSULATION AND SAFETY RELATED SPECIFICATIONS	15
7.2. INSULATION CHARACTERISTICS.....	15
7.3. REGULATORY INFORMATION	16
8. FUNCTION DESCRIPTION	17
8.1. OVERVIEW	17
8.2. ANALOG INPUT AND OUTPUT	17
8.3. ACCURACY RELATED PARAMETERS	18
8.3.1. Input Offset V_{OS} and Gain Error E_G	18
8.3.2. Input Offset Drift TCV_{OS} and Gain Error Thermal Drift TCE_G	19
8.3.3. Nonlinearity.....	20
8.3.4. Power-Supply Rejection Ratio	20
8.3.5. Common-Mode Rejection Ratio.....	20
8.3.6. Total Error Calculation	20
8.4. ISOLATED POWER	22
8.5. PROTECTION COMPARATOR	22
9. APPLICATION NOTE	23
9.1. TYPICAL APPLICATION CIRCUIT	23
9.2. VREF PIN CONNECTING	24
9.3. HIGH VOLTAGE DIVIDING RESISTOR SELECTION.....	25
9.4. PCB LAYOUT	25
10. PACKAGE INFORMATION	26
11. ORDERING INFORMATION.....	27
12. DOCUMENTATION SUPPORT	27
13. TAPE AND REEL INFORMATION	27
14. REVISION HISTORY	28

1. Pin Configuration and Functions

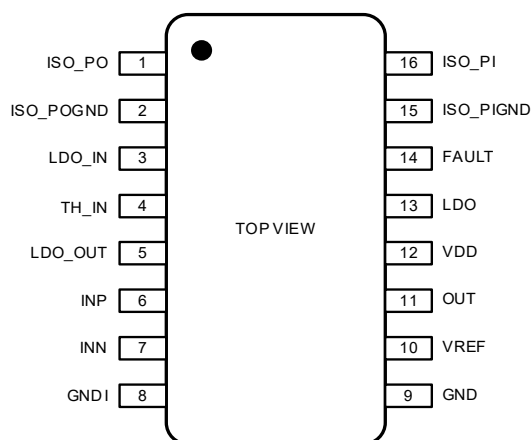


Figure 1.1 NSI36C12R Package

Table 1.1 NSI36C12R Pin Configuration and Description

NSI36C12R PIN NO.	SYMBOL	FUNCTION
1	ISO_PO	Internal isolated power output (need to be connected to the LDO_IN pin)
2	ISO_POGND	Internal isolated power ground reference (need to be connected to the GNDI pin)
3	LDO_IN	Internal input side LDO power input (need to be connected to the ISO_PO pin)
4	TH_IN	Input side protection threshold, need to connect to external threshold voltage
5	LDO_OUT	Internal input side LDO power output
6	INP	Positive analog input (Either INP or INN must have a DC current path to GNDI to define the common-mode input voltage)
7	INN	Negative analog input
8	GNDI	Input side ground reference (need to be connected to the ISO_POGND pin)
9	GND	Output side ground reference (need to be connected to the ISO_PIGND pin)
10	VREF	Reference input, the voltage applied to this pin sets the ratiometric gain and the full-scale output voltage of this device
11	OUT	Analog output
12	VDD	Output side power supply
13	LDO	Internal output side LDO power input (need to be connected to the ISO_PI pin and without external load)
14	FAULT	Over-threshold protection fault output (need to be connected to the pull-up supply)
15	ISO_PIGND	Internal isolated power ground reference (need to be connected to the GND pin)
16	ISO_PI	Internal isolated power input (need to be connected to the LDO pin)

2. Absolute Maximum Ratings⁽¹⁾

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD to GND	-0.3		6.5	V
Analog Input Voltage	INP, INN	GNDI-6		LDO_OUT+0.5	V
Analog Output Voltage	OUT	GND-0.5		VDD+0.5	V
Fault Output Voltage	FAULT	GND-0.5		6.5	V
Analog Input Voltage	TH_IN	GNDI-0.5		3.0	V
Analog Input Voltage	VREF	GND-0.3		VDD+0.5	V
Input current per IO Pin	I _{IN}	-10		10	mA
Junction Temperature	T _J	-40		150	°C
Storage Temperature	T _{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

3. ESD Ratings⁽¹⁾

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD	±4.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB	±1.0	kV

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation or damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply	VDD to GND	3.0	3.3/5	5.5	V
Differential input voltage before clipping output	V _{Clipping}		±1.28		V
Linear differential input full scale voltage	V _{FSR}	-1		1	V
Absolute common-mode input voltage	V _{CM}	-2		V _{LDO_OUT}	V
Operating common-mode input voltage	V _{CM}	-0.8		0.6	V
Reference input voltage	V _{REF}	3	3.3/5	VDD	V
FAULT pull-up supply voltage	V _{FAULT}	0		VDD	V
Operating Ambient Temperature	T _A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	64	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	30	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	33.3	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	10.9	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	28.2	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD = 3.0V ~ 5.5V, INP = -1V to +1V, and INN = GNDI = 0V, T_A = -40°C to 125°C. Unless otherwise noted, Typical values are at VDD = V_{REF} = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Output side supply voltage	VDD	3.0	3.3/5	5.5	V	
Output side supply current	IDD		34.3	46.0	mA	no external load on LDO_OUT, over-threshold protection not triggered, R _{PULLUP} =4.7kΩ to VDD
			35.1	46.5	mA	0.5mA external load on LDO_OUT, over-threshold protection not triggered, R _{PULLUP} =4.7kΩ to VDD
			36.7	48.3	mA	no external load on LDO_OUT, over-threshold protection triggered, R _{PULLUP} =4.7kΩ to VDD
			37.4	48.8	mA	0.5mA external load on LDO_OUT, over-threshold protection triggered, R _{PULLUP} =4.7kΩ to VDD
External load current on Input side LDO	I _E			0.5	mA	
Isolated power output voltage	V _{ISO_PO}	3	3.5	4.6	V	ISO_PO to GNDI
Input side LDO output voltage	V _{LDO_OUT}	3	3.2	3.3	V	LDO_OUT to GNDI
Isolated power output undervoltage detection threshold voltage	V _{ISO_POUV}	2.1	2.3	2.8	V	Isolated power output falling
Input side LDO undervoltage detection threshold voltage	V _{LDO_UV}	2.1	2.3	2.8	V	LDO_OUT falling

Parameters	Symbol	Min	Typ	Max	Unit	Comments
VDD undervoltage detection threshold voltage	VDD _{UV}			2.95	V	
Analog Input						
Input offset voltage	V _{OS}	-0.5	±0.1	0.5	mV	INP = INN = GNDI, at T _A = 25°C
Input offset drift ⁽¹⁾	TCV _{OS}	-10	±2	10	µV/°C	
Common-mode rejection ratio ⁽²⁾	CMRR _{dc}		-100		dB	INP = INN, f _{IN} = 0 Hz, V _{CM min} ≤ VIN ≤ V _{CM max}
	CMRR _{ac}		-86		dB	INP = INN, f _{IN} = 10 kHz, V _{CM min} ≤ VIN ≤ V _{CM max}
Single-ended input resistance	R _{IN}		0.8		GΩ	INN = GNDI
Differential input resistance	R _{IND}		1.2		GΩ	
Input capacitance	C _I		4.5		pF	Single-ended input capacitance, f _{in} =310kHz
Input capacitance	C _{ID}		4.5		pF	Differential input capacitance, f _{in} =310kHz
Input bias current	I _{IB}		1		nA	INP = INN = GNDI, I _{IB} = (I _{IBP} + I _{IBN}) / 2
Input bias current drift ⁽¹⁾	TCI _{IB}		-14		pA/°C	
Reference Input						
Reference input voltage	V _{REF}	3	3.3/5	VDD	V	
Reference input impedance	R _{REFIN}		88		kΩ	
Analog Output						
Nominal Gain			V _{REF} /2.56		V/V	Gain = (V _{REF} /2)/ V _{clipping} , V _{clipping} = 1.28V
Gain error	E _G	-0.3%	±0.05%	0.3%		at T _A = 25°C
Gain error thermal drift ⁽¹⁾	TCE _G	-45	±15	45	ppm/°C	
Nonlinearity		-0.04%	±0.01%	0.04%		
Nonlinearity drift ⁽¹⁾			1		ppm/°C	
Total harmonic distortion ⁽³⁾	THD		-84		dB	V _{IN} = 2Vpp, f _{IN} = 10kHz, BW = 100kHz
Output noise			350		µV _{RMS}	INP = INN = GNDI, BW = 100kHz
Signal to noise ratio	SNR	72	80		dB	V _{IN} = 2Vpp, f _{IN} = 1kHz, BW = 10kHz
	SNR		70		dB	V _{IN} = 2Vpp, f _{IN} = 10kHz, BW = 100kHz, 1MHz filter

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Single-ended clipping output voltage	V_{CLout}	0		V_{REF}	V	$ V_{IN} = V_{INP} - V_{INN} > V_{Clipping}$ $V_{REF} \leq VDD$
		0		VDD	V	$ V_{IN} = V_{INP} - V_{INN} > V_{Clipping}$ $V_{REF} \geq VDD$
Output bandwidth	BW		340		kHz	
Power supply rejection ratio ⁽²⁾	PSRR _{dc}		-99		dB	PSRR vs VDD, from 3.0~5.5V at DC
	PSRR _{ac}		-66		dB	PSRR vs VDD, 100mV and 10kHz ripple
Output capacitance	C_{LOAD}		500		pF	
Output resistance	R_{OUT}		0.3		Ω	
Output limit current	I_{lim}		± 20		mA	
Common-mode transient immunity	CMTI	100	150		kV/ μ s	Common-mode transient immunity
Protection Comparator						
Protection Comparator input Threshold	V_{TH_IN}	0.4	1	1.2	V	
Protection Comparator input Threshold error	T_{He_OV}	-40		40	mV	For positive comparator, $T_{He_OV} = V_{IT+pos} * - V_{TH_IN}^{(4)}$ For negative comparator, $T_{He_OV} = V_{IT-neg} * - (- V_{TH_IN})^{(5)}$
Protection Comparator input hysteresis voltage	V_{HYS_OV}		40		mV	Rising threshold -Falling threshold, $V_{HYS_OV} = V_{IT+-} V_{IT-} $
Fault output voltage at failsafe state	V_{f_Fault}		HiZ		V	
Low-level output voltage	V_{OL}	0	30	300	mV	$I_{SINK}=4mA$
Open-drain output leakage current	I_{LKG}		200		nA	$V_{PULLUP}=5V$
Fault pull up resistor	R_{PULLUP}	1	4.7	10	k Ω	
Output current limit	I_{sink}			12	mA	VDD=5V, sinking
Output resistance	R_{OUT}		5.5		Ω	
Common-mode transient immunity	CMTI	100	150		kV/ μ s	For protection comparator, $R_{PULLUP}=4.7k\Omega$ to VDD
Timing						
Rising time of OUT	t_r		1.3		μ s	
Falling time of OUT	t_f		1.3		μ s	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
INP, INN to OUT signal delay (50% - 50%)	t_{PD}		1.4	1.8	μs	
Propagation delay of fault	t_{PD_Fault}		0.6	1	μs	$V_{od}=100mV$, $C_L=15pF$, fault trigger and release delay
Fault output fall time	t_{f_Falut}		2		ns	$C_L=15pF$
Analog setting time	t_{AS}		0.9		ms	VDD step to 3.0 V, to OUT valid, 0.1% settling

- (1) The temperature drift is calculated within the whole temperature range (-40°C to 125°C).
- (2) Input referred.
- (3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).
- (4) $V_{IT+_{pos}}$ is the positive-going trip threshold (refer to input voltage) for positive trip threshold, $V_{IT-_{pos}}$ is the negative-going trip threshold (refer to input voltage) for positive trip threshold, refer to Figure 6.2.
- (5) $V_{IT-_{neg}}$ is the negative-going trip threshold (refer to input voltage) for negative trip threshold, $V_{IT+_{neg}}$ is the positive-going trip threshold (refer to input voltage) for negative trip threshold, refer to Figure 6.2.

6.2. Timing Diagrams

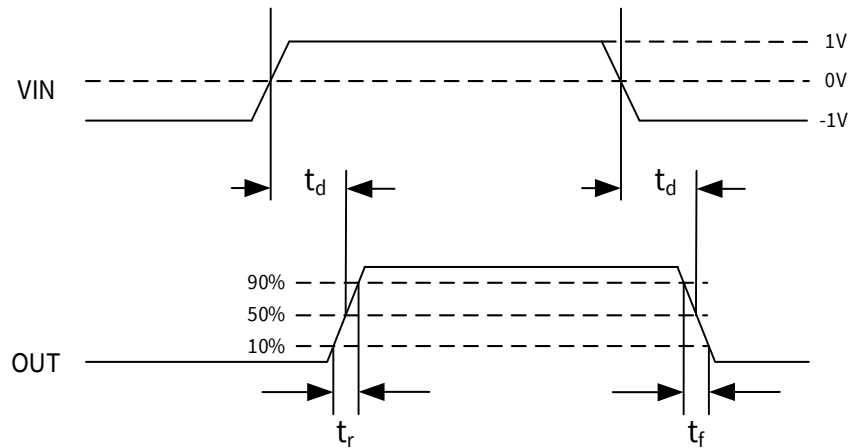


Figure 6.1 Propagation Delay and Output Fall Time Definition

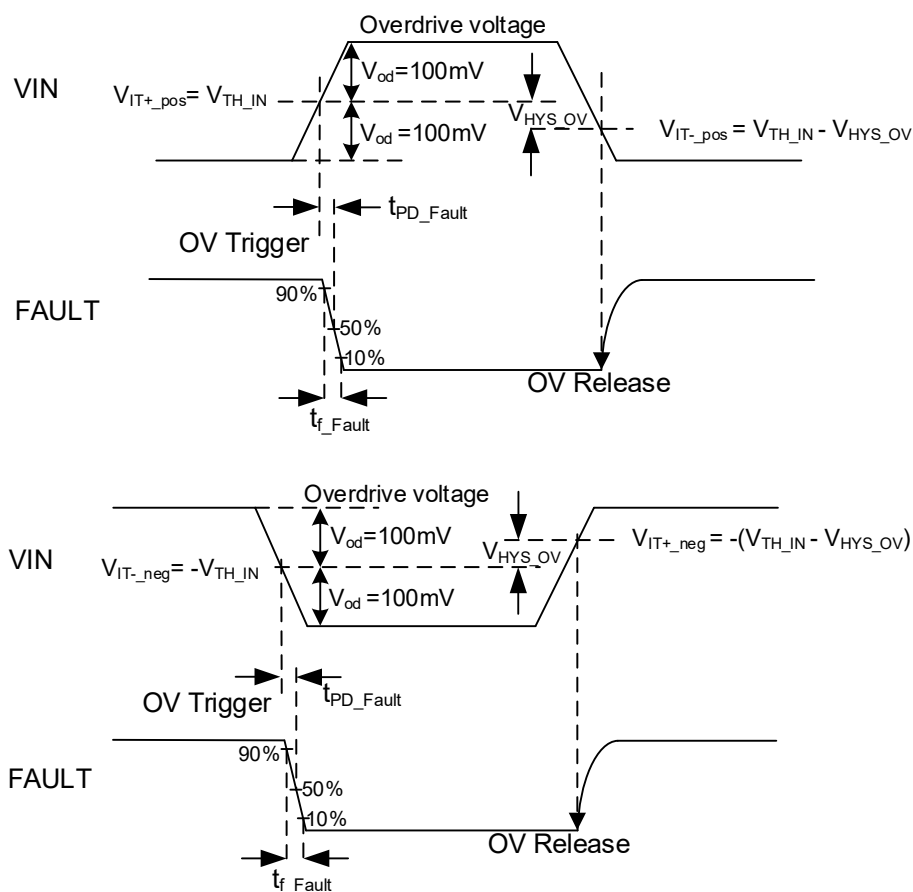


Figure 6.2 Propagation Delay and Output Fall Time Definition for Protection Comparator

6.3. Typical Performance Characteristics

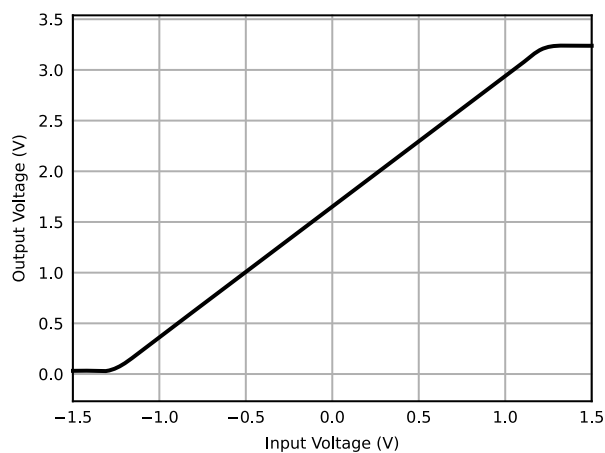


Figure 6.3 Output Voltage vs Input Voltage ($V_{REF} = V_{DD} = 3.3\text{V}$)

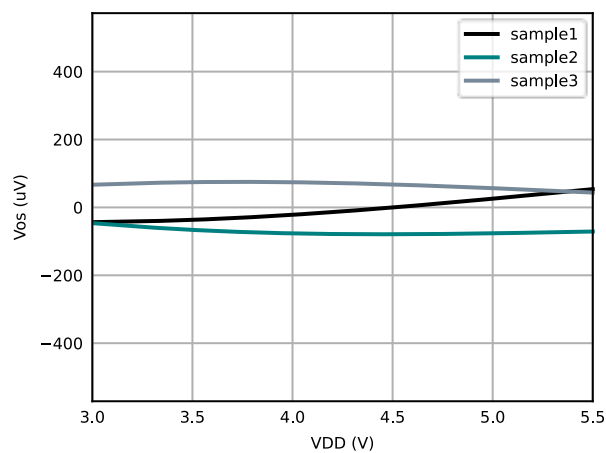


Figure 6.4 Input Offset Voltage vs Supply Voltage

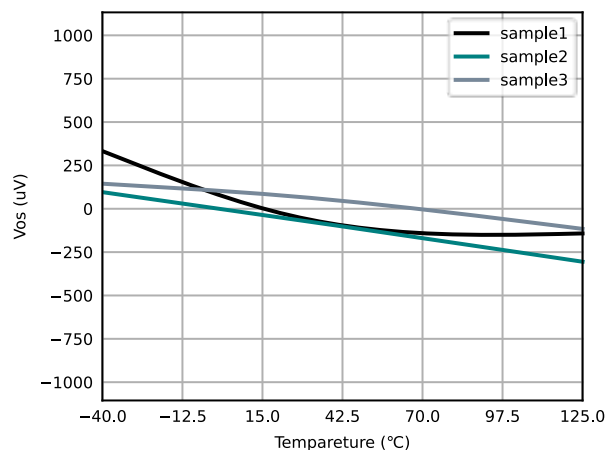


Figure 6.5 Input Offset Voltage vs Temperature

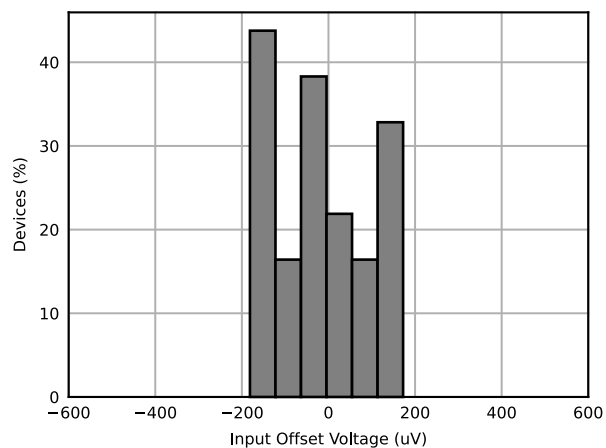


Figure 6.6 Input Offset Voltage Distribution ⁽¹⁾

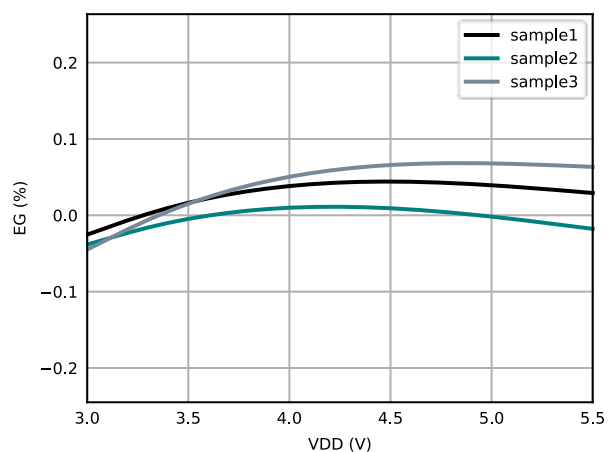


Figure 6.7 Gain Error vs Supply Voltage

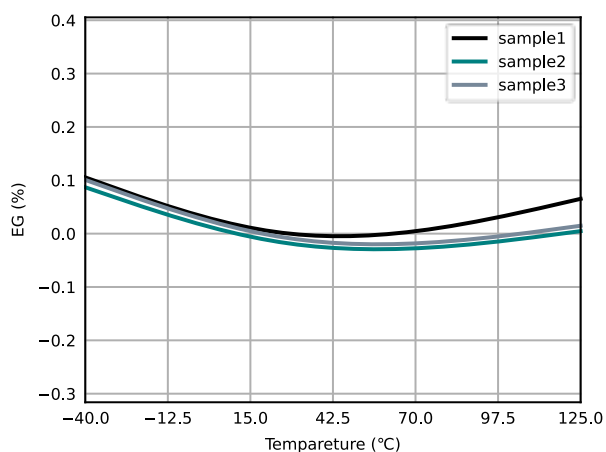


Figure 6.8 Gain Error vs Temperature

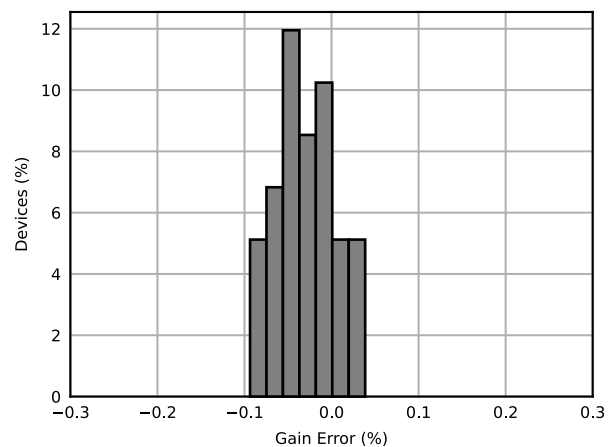


Figure 6.9 Gain Error Distribution ⁽¹⁾

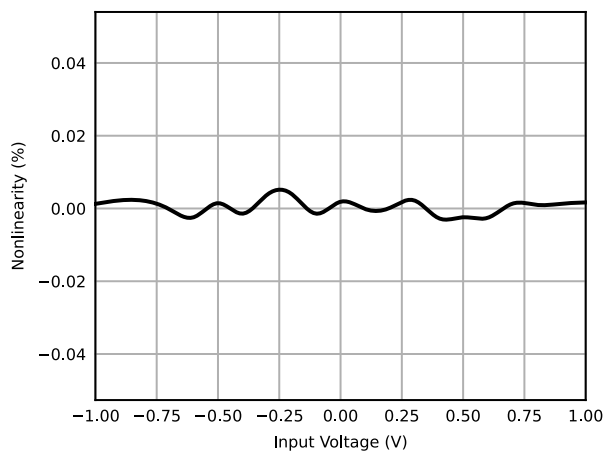


Figure 6.10 Nonlinearity vs Input Voltage

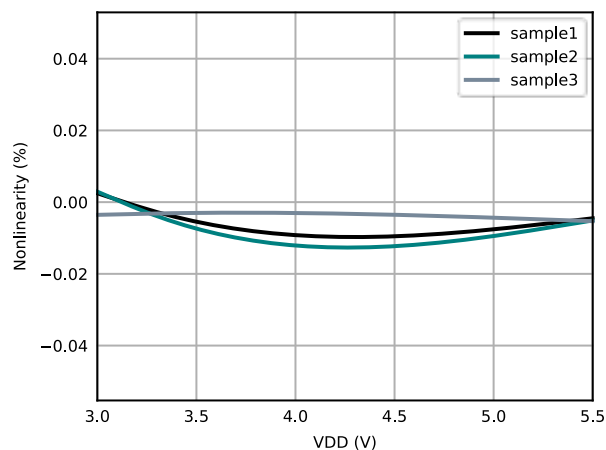


Figure 6.11 Nonlinearity vs Supply Voltage

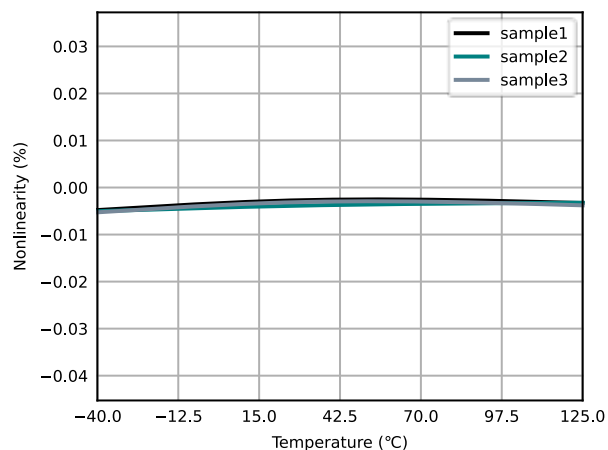


Figure 6.12 Nonlinearity vs Temperature

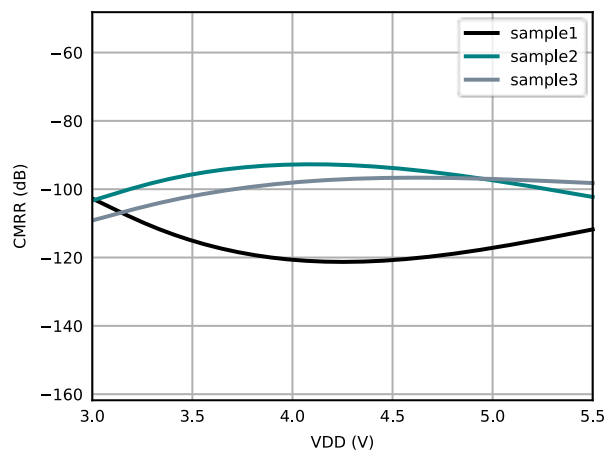


Figure 6.13 Common-Mode Rejection Ratio vs Supply Voltage ($V_{REF} = VDD$)

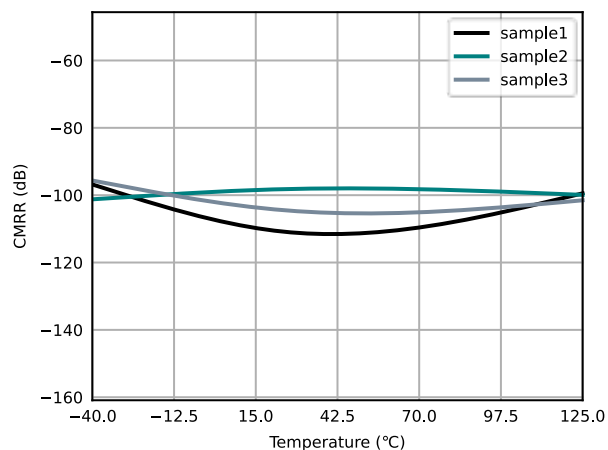


Figure 6.14 Common-Mode Rejection Ratio vs Temperature

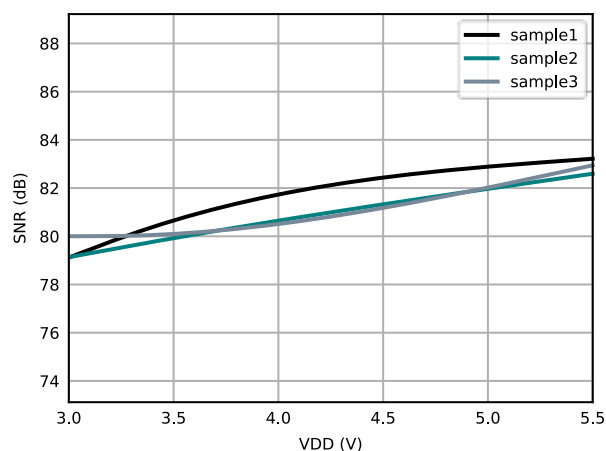


Figure 6.15 Signal to Noise Ratio vs Supply Voltage ($V_{REF} = VDD$)

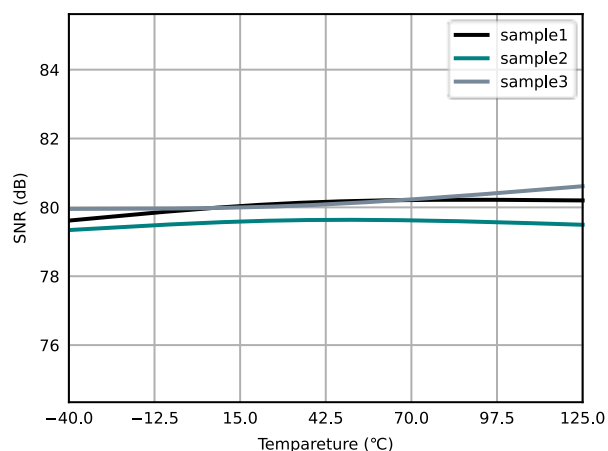


Figure 6.16 Signal to Noise Ratio vs Temperature

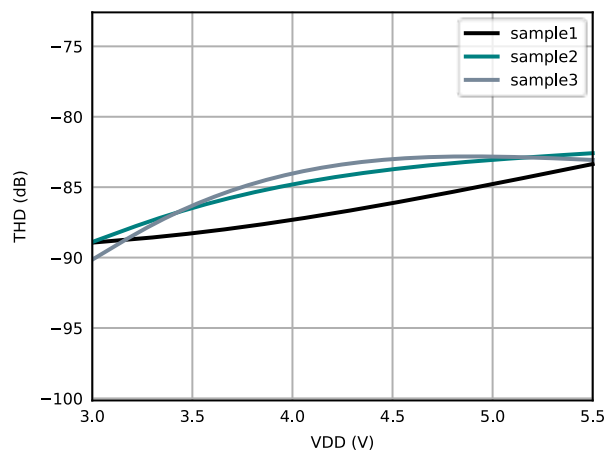


Figure 6.17 Total Harmonic Distortion vs Supply Voltage ($V_{REF} = VDD$)

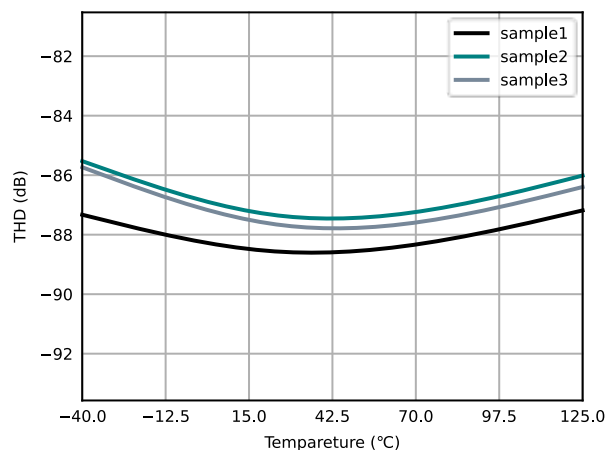


Figure 6.18 Total Harmonic Distortion vs Temperature

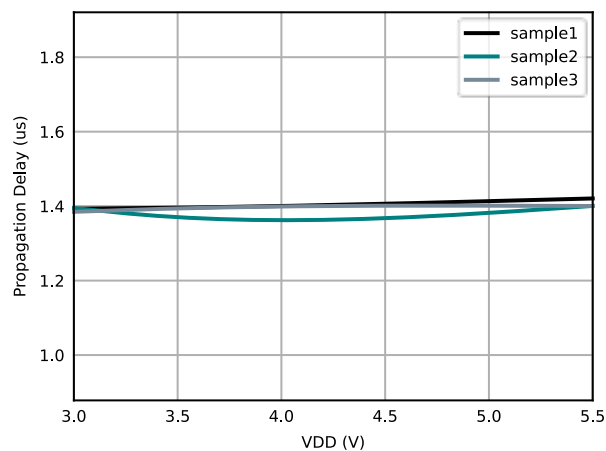


Figure 6.19 Input and Output Signal Delay time vs Supply Voltage

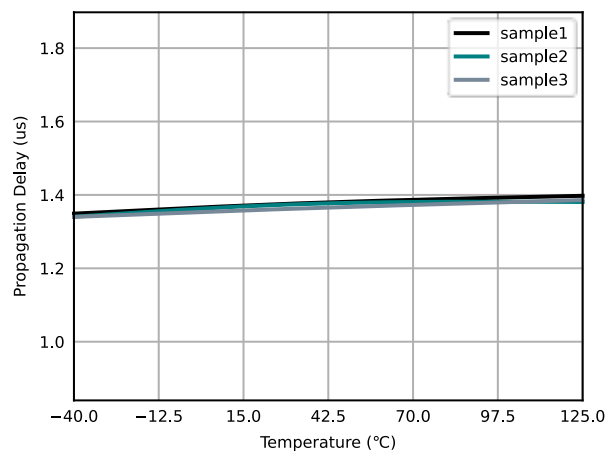


Figure 6.20 Input and Output Signal Delay time vs Temperature

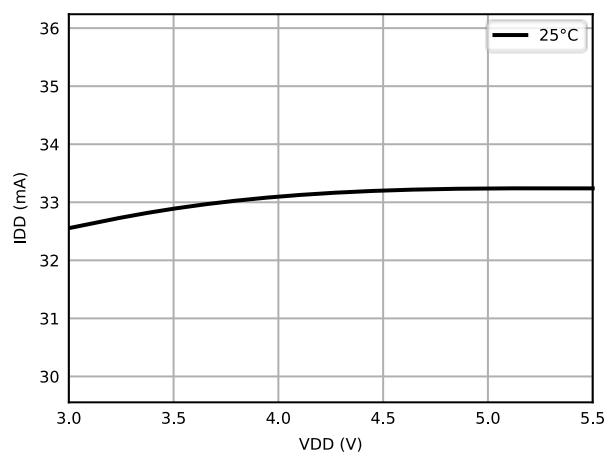


Figure 6.21 Input Supply Current vs Supply Voltage ($I_E = 0.5mA$, over-threshold protection not triggered)

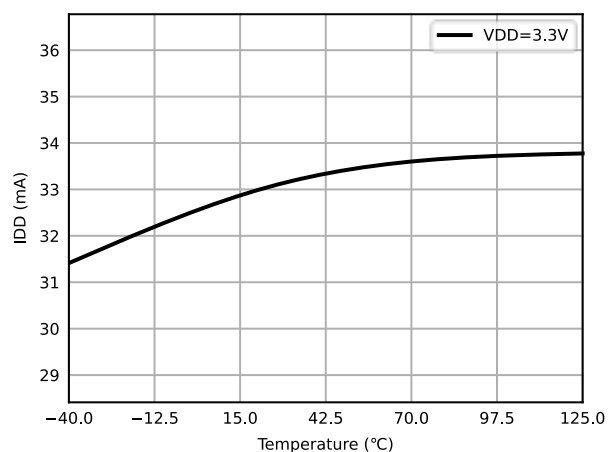


Figure 6.22 Input Supply Current vs Temperature ($I_E = 0.5mA$, over-threshold protection not triggered)

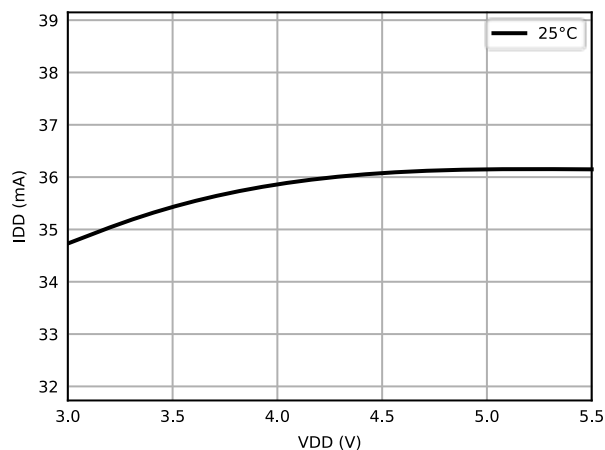


Figure 6.23 Input Supply Current vs Supply Voltage ($I_E=0.5\text{mA}$, over-threshold protection triggered)

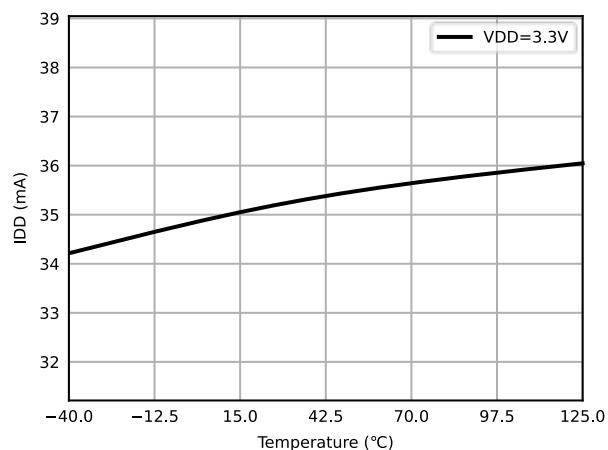


Figure 6.24 Input Supply Current vs Temperature ($I_E=0.5\text{mA}$, over-threshold protection triggered)

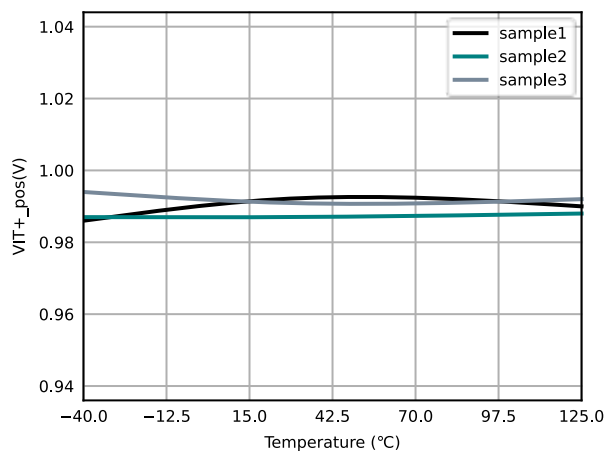


Figure 6.25 V_{IT+_pos} vs Temperature ($V_{TH_IN}=1\text{V}$)

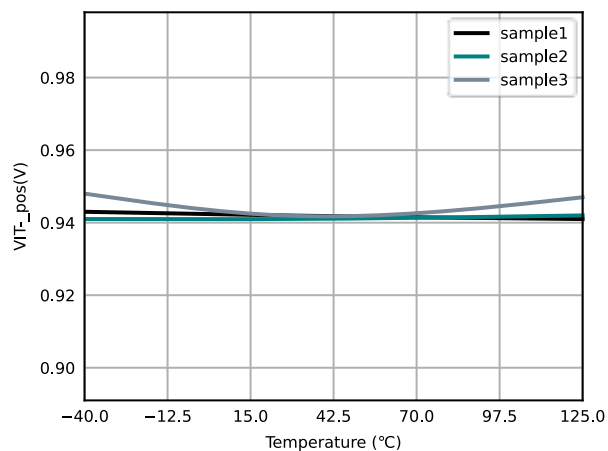


Figure 6.26 V_{IT-_pos} vs Temperature ($V_{TH_IN}=1\text{V}$)

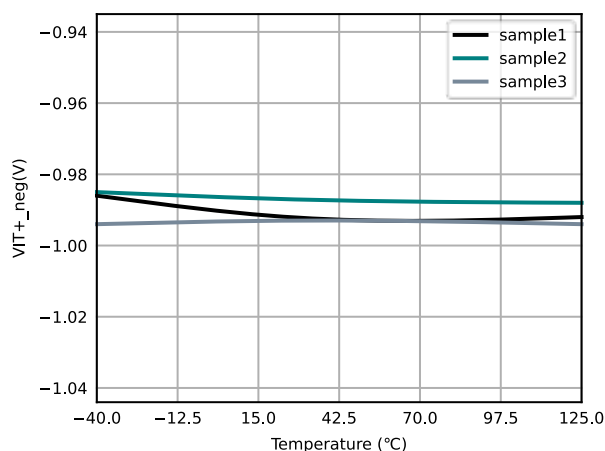


Figure 6.27 V_{IT+_neg} vs Temperature ($V_{TH_IN}=1\text{V}$)

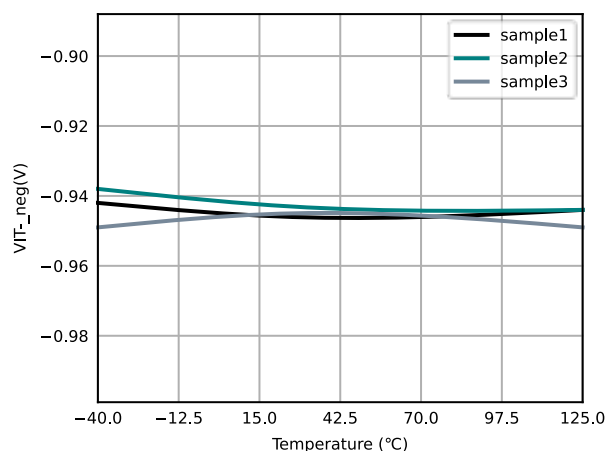


Figure 6.28 V_{IT-_neg} vs Temperature ($V_{TH_IN}=1\text{V}$)

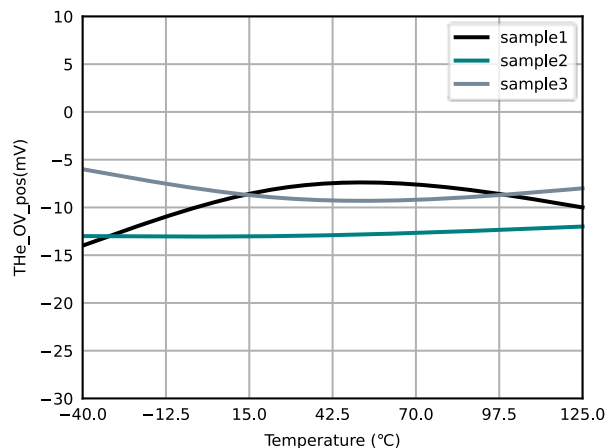


Figure 6.29 THe_ov_pos vs Temperature

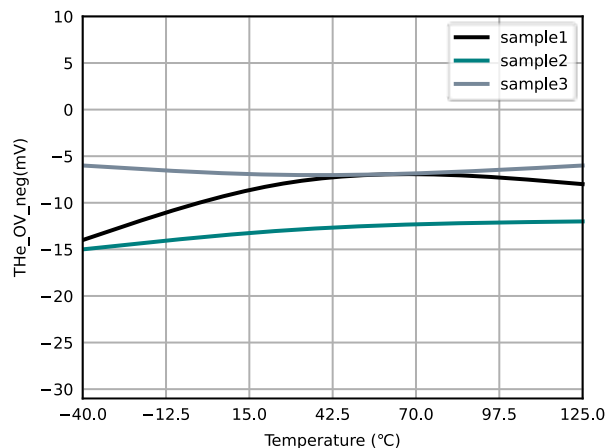


Figure 6.30 THe_ov_neg vs Temperature

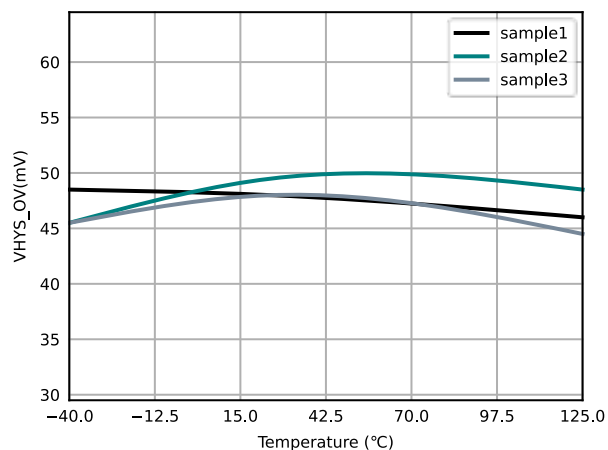


Figure 6.31 VHYS_OV vs Temperature

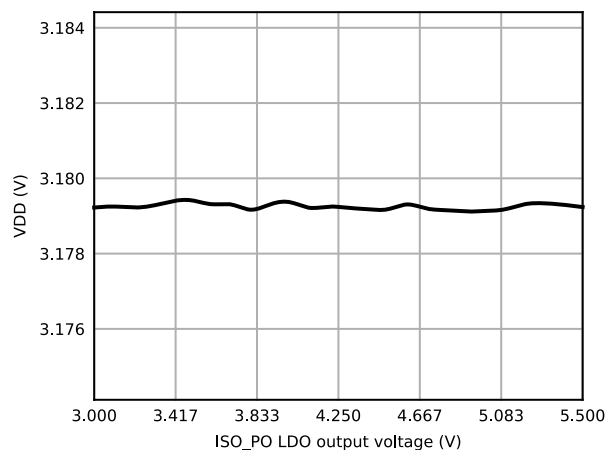


Figure 6.32 ISO-PO LDO Regulation

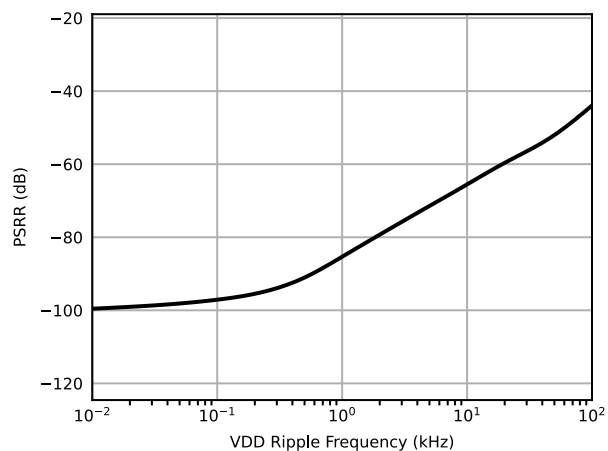


Figure 6.33 Power-Supply Rejection Ratio vs VDD Input Frequency

(1) According to the test results of 30 pcs samples.

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Clearance	CLR	8	mm	IEC 60664-1
Minimum External Creepage	CPG	8	mm	IEC 60664-1
Distance Through Insulation	DTI	26	μm	Distance through insulation (internal clearance – capacitive signal isolation)
		75	μm	Distance through insulation (internal clearance – transformer power isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 150\text{Vrms}$	I to IV
	For Rated Mains Voltage $\leq 300\text{Vrms}$	I to IV
	For Rated Mains Voltage $\leq 600\text{Vrms}$	I to IV
	For Rated Mains Voltage $\leq 1000\text{Vrms}$	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{s}$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{s}$			pC
	Method b, $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{s}$			pC

Description	Test Condition	Symbol	Value	Unit
	$V_{pd(m)} = 1.875 \cdot V_{IORM}$, $t_m = 1s$ (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)			
Maximum transient isolation voltage	$t = 60s$	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50 μs waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50 μs waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$, $T_{amb} = 25^\circ C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500V$, $100^\circ C \leq T_{amb} \leq 125^\circ C$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500V$, $T_{amb} = T_s$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	pF
Safety total power dissipation	$V_I = 5.5V$, $T_J = 150^\circ C$, $T_A = 25^\circ C$	P_s	1954	mW
Safety input, output, or supply current	$R_{\theta JA} = 64^\circ C/W$ for SOW16, $V_I = 5.5V$, $T_J = 150^\circ C$, $T_A = 25^\circ C$	I_s	355	mA
Maximum safety temperature		T_s	150	$^\circ C$
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1s$	V_{ISO}	5000	V_{RMS}

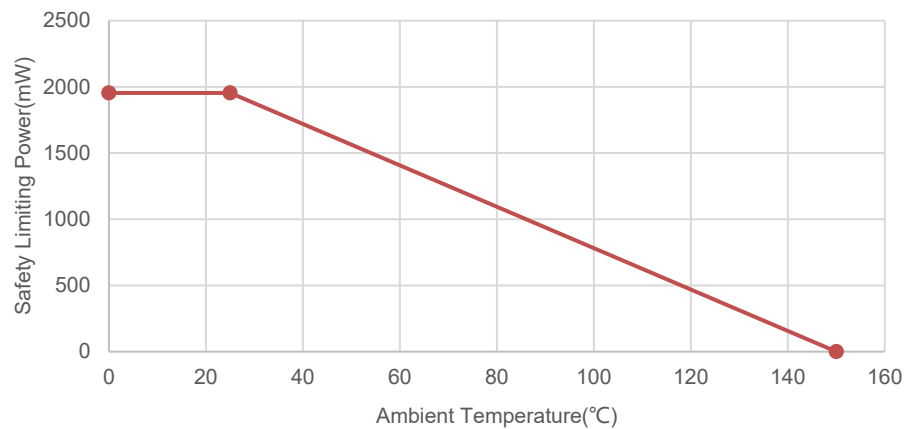


Figure 7.1 NSI36C12R Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI36C12R is approved by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1

UL	VDE	CQC	TUV
Single Protection, 5000V _{rms} Isolation voltage	Reinforce Insulation V _{IORM} =2121 V _{PEAK} V _{IOTM} =8000 V _{PEAK} V _{IOSM} =10000 V _{PEAK}	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	R50574061

8. Function Description

8.1. Overview

The NSI36C12R is a high-performance isolated amplifier with integrated isolated power supply and input over-threshold protection function. The device accepts fully-differential input of $\pm 1V$. The integrated isolated power supply enables single-power operation on the low side of the device without the need for a separate isolated power supply for the high side, effectively reducing the board area. The fully-differential input is ideally suited for AC voltage monitoring in high voltage applications where isolation is required.

The low-side power supply VDD feeds power to the isolated power supply input through an LDO with external connection from the LDO pin to the ISO_PI pin. The output of the isolated power supply is regulated by an LDO with external connection from the ISO_PO pin to the LDO_IN pin, to power the high-side circuit.

The analog input is continuously sampled by a second-order Σ - Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated input and output side voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the output side, which has a ratiometric single-ended output. The ratiometric gain is defined by the input voltage of VREF as $V_{REF}/2.56$.

In addition, the NSI36C12R integrates an input over-threshold protection function. VIN is compared with the threshold voltage V_{TH_IN} . The output of the comparator is sent to the output side through a separate isolation channel to achieve fast propagation delay (600ns Typ). The over-threshold signal can be monitored on the FAULT pin.

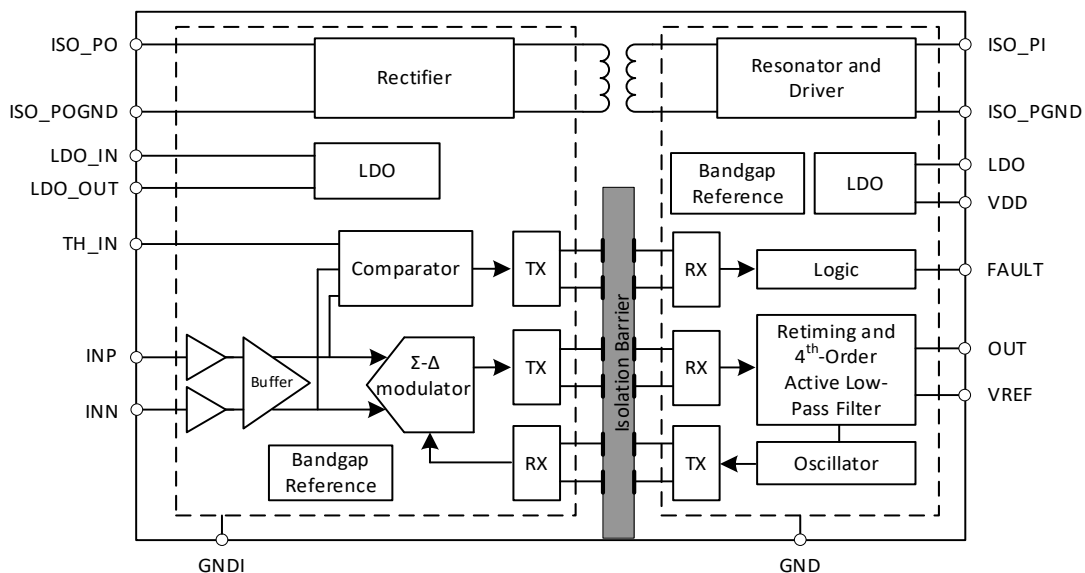


Figure 8.1 Function Block Diagram of NSI36C12R

8.2. Analog Input and Output

There are two restrictions on the analog input signals (INP and INN).

- If the input voltage exceeds the range $GNDI-6V$ to $LDO_OUT+0.5V$, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

The NSI36C12R provides a single-ended analog output voltage proportional to the input voltage. The output is referred to GND and is galvanically isolated from the input of the device. The output is designed to connect directly to the input of an ADC.

The full-scale output voltage is set by the VREF pin. The gain of NSI36C12R can be configured by the voltage on pin VREF as below:

- The reference input voltage range of VREF is from 3.0 V to VDD. The VREF pin must not be connected to GND.
- When VREF is connected to an external reference voltage above 3V, the NSI36C12R has a dynamic output voltage range proportional to the voltage of VREF. The input to output curve is shown in Figure 8.2.
- For linear input range ($|V_{IN}| \leq |V_{FSR}|$), the analog output of NSI36C12R has a ratiometric gain of $V_{REF} / 2.56$. The device outputs a voltage equal to:

$$V_{OUT} = (V_{INP} - V_{INN}) * V_{REF} / 2.56 + V_{REF} / 2$$

When the input exceeds the linear full-scale range, the output continues to follow the input, but the linear performance will decline. If an input signal exceeding the clipping input range is applied to the NSI36C12R ($|V_{IN}| \geq |V_{Clipping}|$), the analog output will be clipped.

When the undervoltage of the integrated isolated power supply output ISO_PO or the high-side LDO output LDO_OUT is detected, the output voltage is 0V.

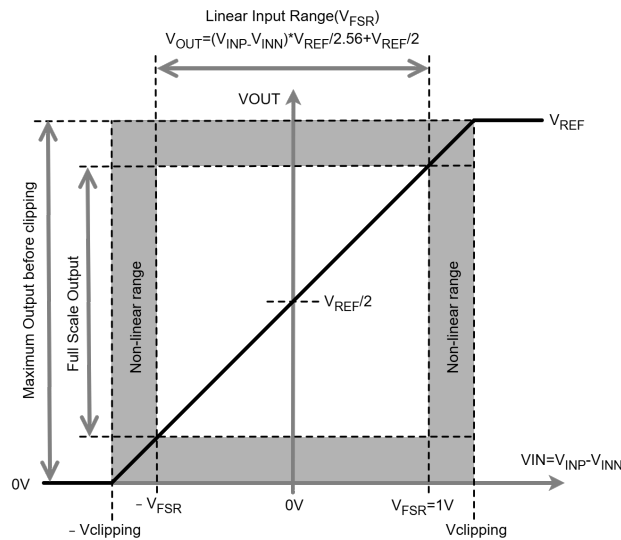


Figure 8.2 Input to Output Transfer Curve of the NSI36C12R

8.3. Accuracy Related Parameters

Parameters related to the accuracy performance are explained in this section, including V_{OS} and its drift, E_G and its drift, Nonlinearity. Other immunity parameters that affect accuracy like CMRR and PSRR are also included.

8.3.1. Input Offset V_{OS} and Gain Error E_G

V_{OS} and E_G are the most significant factor influencing accuracy. The ideal curve and actual curve are shown in Figure 8.3.

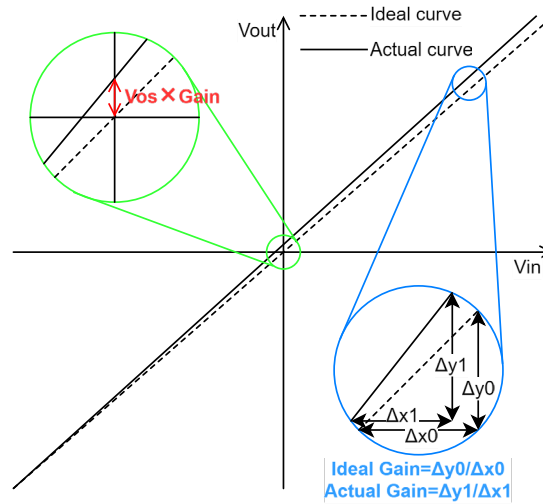


Figure 8.3 Vos and EG diagram

V_{OS} means the input offset voltage when input is 0V. The tested output should be divided by nominal gain as V_{OS} is defined as the offset voltage referred to input (See Equation 1).

$$V_{OS} = V_o / \text{Nominal Gain} \quad \text{Equation 1}$$

where

- V_o is the output voltage tested when input is 0V.
- Nominal Gain is $V_{REF} / 2.56$ for NSI36C12R.

Gain is the magnification of the amplifier, and the definition formula is shown in Equation 2. EG means the difference between actual and ideal slope. It should be noted that EG is tested across the whole input range to minimize test error (See Equation 3).

$$\text{Gain} = \frac{\Delta y1}{\Delta x1} = \frac{V_{o1} - V_{o2}}{V_{in1} - V_{in2}} \quad \text{Equation 2}$$

$$E_G = \frac{\text{Gain} - \text{Nominal Gain}}{\text{Nominal Gain}} \times 100\% \quad \text{Equation 3}$$

where V_{in1} and V_{in2} are the lower and upper limit of the input FSR separately, V_{o1} and V_{o2} are the output voltage corresponding to V_{in1} and V_{in2} .

8.3.2. Input Offset Drift TCV_{OS} and Gain Error Thermal Drift TCE_G

Input offset drift TCV_{OS} means the drift of V_{OS} over the whole operating temperature range, which is calculated as Equation 4.

$$TCV_{OS} = \frac{V_{OS_{max}} - V_{OS_{min}}}{\text{TempRange}} \quad \text{Equation 4}$$

where

- $V_{OS_{max}}$ and $V_{OS_{min}}$ is the maximum and minimum offset voltage over the whole operating ambient temperature range.
- TempRange covers the whole operating temperature, from -40°C to 125°C .

Gain error thermal drift TCE_G is the drift of E_G over the whole operating temperature range, which is calculated as Equation 5.

$$TCE_G = \frac{E_{G_{max}} - E_{G_{min}}}{\text{TempRange}} \quad \text{Equation 5}$$

where $E_{G_{max}}$ and $E_{G_{min}}$ is the maximum and minimum Gain Error over the whole temperature.

Both TCV_{OS} and TCE_G should be multiplied by the direction of temperature drift.

8.3.3. Nonlinearity

Nonlinearity describes the deviation between the actual output and the ideal linear output. Calculate the peak-to-peak value of the error between the actual output and the fitting curve, and nonlinearity is expressed as the ratio of half of the peak-to-peak error to the full-scale range of the output voltage (See Equation 6).

$$\text{Nonlinearity} = \frac{\text{Error_pkpk}}{2 \times V_{\text{OFSR}}} \times 100\% \quad \text{Equation 6}$$

where

- Error_pkpk is the peak-to-peak value of the error between the actual output and the fitting curve.
- V_{OFSR} represents the full-scale range of the output voltage ($2 \times V_{\text{REF}} / 2.56 \text{ V}$ for NSI36C12R).

8.3.4. Power-Supply Rejection Ratio

Power-Supply Rejection Ratio (PSRR) describes the level of the output error (input inferred) which is affected by the variation of power supply. PSRR is defined in dB and calculated as Equation 7.

$$\text{PSRR} = 20 \times \log_{10} \left(\frac{V_{\text{O_var}}}{\text{Nominal Gain} \times V_{\text{DD_var}}} \right) \quad \text{Equation 7}$$

Where $V_{\text{O_var}}$ and $V_{\text{DD_var}}$ are respectively the variation value of the output voltage and the supply voltage.

8.3.5. Common-Mode Rejection Ratio

Common-Mode Rejection Ratio (CMRR) quantifies the ability of a differential amplifier to suppress the variation of the common mode signals while amplifying the differential-mode signals. CMRR is calculated as:

$$\text{CMRR} = 20 \times \log_{10} \left(\frac{V_{\text{O_var}}}{\text{Nominal Gain} \times V_{\text{CM_var}}} \right) \quad \text{Equation 8}$$

where CMRR is the input-referred voltage variation in dB and $V_{\text{CM_var}}$ is the variation value of the input common-mode voltage.

8.3.6. Total Error Calculation

The total error is contributed by parameters discussed above. It is helpful to know the respective contribution of all different parameters when something is wrong about system current sensing. This section will introduce the calculation method of total error.

Parameters which mainly affect sensing accuracy are V_{os} , EG and Nonlinearity and their drift. PSRR and CMRR are not a dominant factor in most cases. However, PSRR can be a concern when the power supply has high-frequency ripple, in which case a larger decoupling capacitor and a better layout are highly recommended (Refer to Section 9.3).

The error introduced by V_{os} and its drift can be calculated as:

$$\text{Error_Vos} = \frac{V_{\text{os_max}} + \text{TCV}_{\text{os}} \times \Delta T}{V_{\text{IN}}} \times 100\% \quad \text{Equation 9}$$

where

- $V_{\text{os_max}}$ is the maximum value of input offset voltage at 25°C, which is $\pm 0.5 \text{ mV}$ for NSI36C12R.
- TCV_{os} is the maximum drift of input offset voltage over the whole working temperature, which is $10 \text{ uV}/^\circ\text{C}$ for NSI36C12R.
- ΔT is the range of temperature variation.
- V_{IN} is the input voltage in the application.

The error introduced by E_{G} and TCE_{G} can be calculated as:

$$\text{Error_E}_G = E_{\text{G}} + \text{TCE}_{\text{G}} \times \Delta T \quad \text{Equation 10}$$

where

- E_{G} is the maximum value of Gain Error when the temperature is 25°C, which is $\pm 0.3\%$ for NSI36C12R.
- TCE_{G} is the maximum drift of Gain Error over the whole temperature, which is $\pm 45 \text{ ppm}/^\circ\text{C}$ for NSI36C12R.

The error introduced by Nonlinearity is $\text{Nonlinearity}_{\text{max}}$, the maximum value of Nonlinearity in the entire temperature range, - 40°C to 125°C, which is $\pm 0.04\%$ for NSI36C12R. The total error sensing error is expressed as:

$$\text{Total_Error} = \sqrt{\text{Error_Vos}^2 + \text{Error_E}_G^2 + \text{Nonlinearity}_{\text{max}}^2} \quad \text{Equation 11}$$

For example, consider an NSI36C12R with the sensing input voltage of $\pm 1\text{V}$ and a -40°C to 85°C temperature range. The total error calculation is shown in Table 8.1.

Table 8.1 Total Error Calculation of NSI36C12R (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at $V_{\text{in}}=\pm 1\text{V}$	Error at $V_{\text{in}}=\pm 0.1\text{V}$
Input offset error	Error_Vos	$\text{Error_Vos} = \frac{V_{\text{osmax}} + \text{TCV}_{\text{os}} \times \Delta T}{V_{\text{IN}}} \times 100\%$ $= \frac{\pm 0.5\text{mV} \pm 10\mu\text{V}/^\circ\text{C} \times 65^\circ\text{C}}{V_{\text{IN}}} \times 100\%$	$\pm 0.115\%$	$\pm 1.15\%$
Gain error	Error_EG	$\text{Error_E}_G = E_G + \text{TCE}_G \times \Delta T$ $= \pm 0.3\% \pm 45\text{ppm}/^\circ\text{C} \times 65^\circ\text{C}$	$\pm 0.593\%$	$\pm 0.593\%$
Nonlinearity	Nonlinearity _{max}	$\text{Nonlinearity}_{\text{max}} = \pm 0.04\%$	$\pm 0.04\%$	$\pm 0.04\%$
Total error	Total_Error	Total_Error $= \sqrt{\text{Error_Vos}^2 + \text{Error_E}_G^2 + \text{Nonlinearity}_{\text{max}}^2}$	$\pm 0.606\%$	$\pm 1.295\%$

Since the input offset voltage is independent of input voltage, it becomes the dominant factor of the total error when the input voltage is low. To improve the system accuracy, especially in low-input applications, it is recommended to perform software zero-point calibration and gain error calibration. With system-level calibration, the total error can also be reduced significantly. The reduced error is calculated according to Table 8.2.

Table 8.2 Total Error Calculation with Software Calibration (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at $V_{\text{in}}=\pm 1\text{V}$	Error at $V_{\text{in}}=\pm 0.1\text{V}$
Input offset error	Error_Vos	$\text{Error_Vos} = \frac{\text{TCV}_{\text{os}} \times \Delta T}{V_{\text{IN}}} \times 100\%$ $= \frac{10\mu\text{V}/^\circ\text{C} \times 65^\circ\text{C}}{V_{\text{IN}}} \times 100\%$	$\pm 0.065\%$	$\pm 0.65\%$
Gain error	Error_EG	$\text{Error_E}_G = \text{TCE}_G \times \Delta T = \pm 45\text{ppm}/^\circ\text{C} \times 65^\circ\text{C}$	$\pm 0.293\%$	$\pm 0.293\%$
Nonlinearity	Nonlinearity _{max}	$\text{Nonlinearity}_{\text{max}} = \pm 0.04\%$	$\pm 0.04\%$	$\pm 0.04\%$
Total error	Total_Error	Total_Error $= \sqrt{\text{Error_Vos}^2 + \text{Error_E}_G^2 + \text{Nonlinearity}_{\text{max}}^2}$	$\pm 0.303\%$	$\pm 0.714\%$

The maximum total error with and without calibration is show in Figure 8.4, considering 1V input as full load, NSI36C12R can achieve <1% error at more than 10% load ($|V_{\text{in}}| \geq 100\text{mV}$) with software calibration, and <1% error at more than 20% load ($|V_{\text{in}}| \geq 200\text{mV}$) without software calibration.

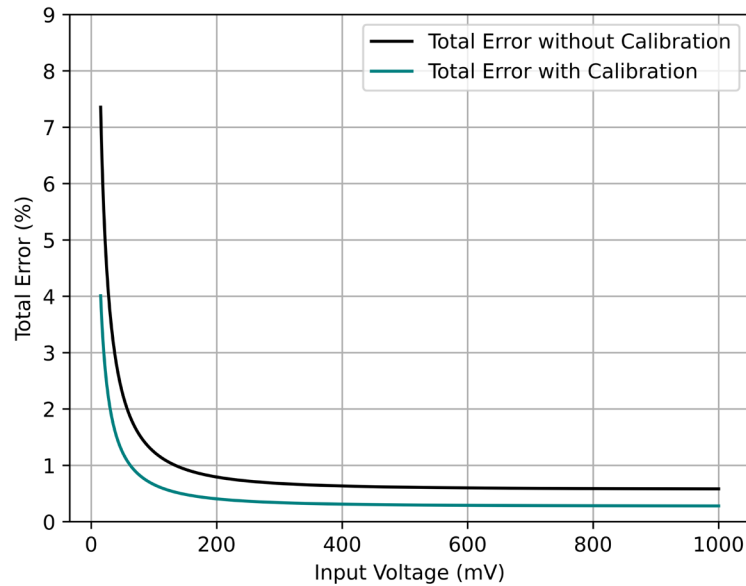


Figure 8.4 Total Error Over -40°C to 85°C vs Input Voltage

8.4. Isolated Power

The NSI36C12R integrates an isolated DC/DC power supply that includes the following components as shown in Figure 8.1:

- Low-side low-dropout regulator (LDO) to provide stable voltage for the input of the isolated DC/DC converter.
- Isolated DC/DC converter with the primary resonator and driver, an air-core transformer, and the secondary rectifier. The converter does not output a constant voltage and it is not recommended to drive additional load.
- High-side LDO to convert the isolated DC/DC converter output to a stable voltage and supply for the high-side signal circuitry. The high-side LDO can provide a limited current of 0.5mA for external load.

The isolated DC/DC power supply uses a spread spectrum clocking technique and optimized transformer design to improve the electro-magnetic interference (EMI) performance.

8.5. Protection Comparator

The NSI36C12R provides an input over-threshold protection function. The function block diagram of the internal window comparator is shown in Figure 8.5. The differential input voltage signal is amplified by a buffer at the input stage and then sent to a window comparator to be compared with the threshold voltage $\pm V_{TH_IN}$. The desired threshold voltage of the window comparator V_{TH_IN} can be set by applying an external voltage to the TH_IN pin according to

$$V_{TH_IN} = V_{OV} \quad \text{Equation 12}$$

where V_{OV} is the desired overcurrent threshold of the differential input sensing voltage.

The comparison window is centered around 0V. The over-threshold signal is transferred across the isolation barrier and monitored on the pin FAULT. The FAULT pin is an open-drain output with a weak pull-up resistor $R3 = 175k\Omega$ ($VDD = 5V$) to VDD inside the chip, providing a defined state when external pull-up resistor is not used. In practical applications, the FAULT pin needs to be pulled up to VDD through an external resistor.

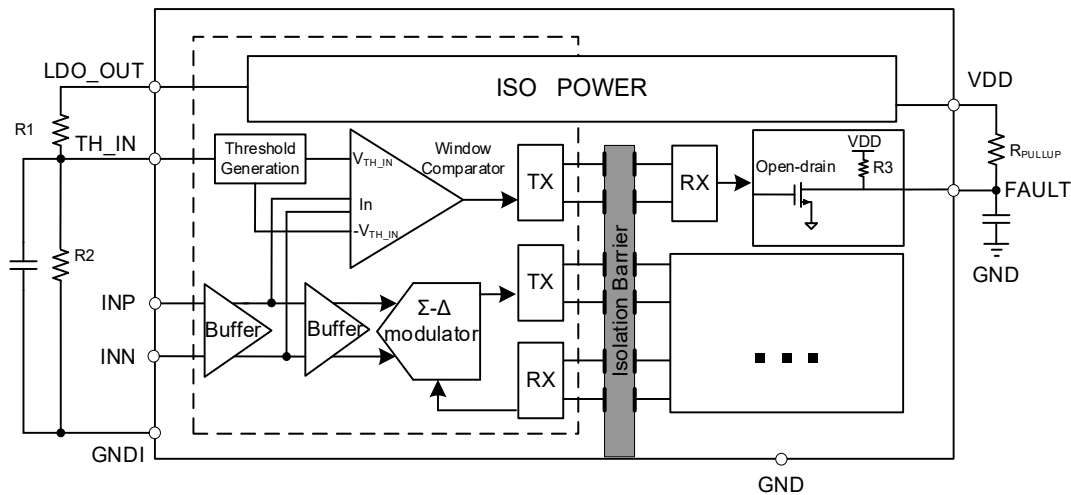


Figure 8.5 Function Block Diagram of Window Comparator

The switching characteristic of input over-threshold protection function is shown in Figure 8.6. If $|VIN| < V_{TH_IN} - V_{HYS_OV}$, the FAULT pin is in a high-impedance state and pulled up to high level externally. The FAULT pin is actively pulled low when $|VIN| > V_{TH_IN}$, which means the over-threshold protection is triggered. The hysteresis voltage V_{HYS_OV} (typical value of 45mV) makes the comparator have better immunity in noisy environment without the need to add a positive feedback circuit to create hysteresis.

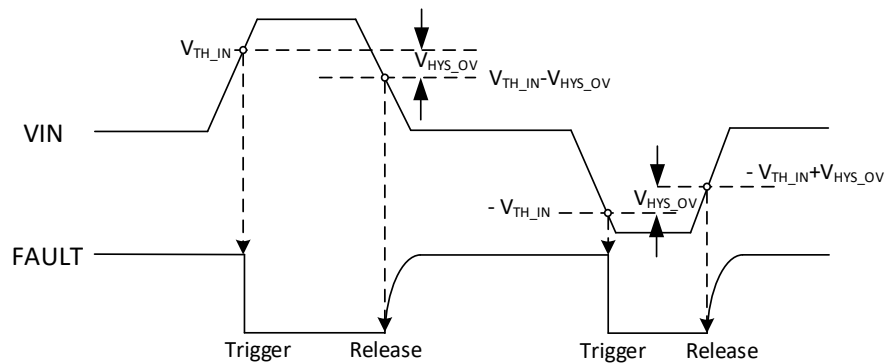


Figure 8.6 Switching Characteristic of Input Over-threshold Protection Function

It should be noted that the CMTI (Common-mode transient immunity) performance of the open-drain output is related to the pullup resistance R_{PULLUP} and load capacitance. When a common-mode transient event with high dV/dt occurs, the open-drain output may be pulled down because of interference signal coupled from parasitic capacitance between the high side and the low side. The lower pullup resistance enhances immunity. Additionally, a capacitor can be placed between the FAULT pin and GND pin to improve the CMTI performance. However, the load capacitance extends the output fall time and is preferably less than 1nF.

The protection comparator threshold voltage is recommended to be set by dividing the LDO_OUT voltage, as is shown in Figure 8.5. Adjusting the resistance of the voltage divider network, R1 and R2, can change the threshold voltage V_{TH_IN} . The resistance of the voltage divider should not be too small because the maximum external load current on the LDO_OUT pin is 0.5mA. The input resistance of the TH_IN pin is $>1G\Omega$, which has almost no impact on overcurrent threshold accuracy. Additionally, the protection comparator threshold voltage can also be set by an external reference voltage.

9. Application Note

9.1. Typical Application Circuit

The following key features make NSI36C12R the ideal solution for isolated AC and DC voltage sensing applications.

- Reinforced isolation barrier supports a working voltage up to 1500Vrms, provides extremely high reliability for dangerous high voltage systems.

- Excellent common mode transient immunity (CMTI, 150kV/us typ) ensures that the device provides accurate and reliable measurements even in the presence of high-power switching.
- Isolated power supply integrated, reduces the need of external isolated high-side supply, simplifies design and reduces area.
- Excellent DC accuracy and low drift, high linearity over FSR, limited sensitivity to external magnetic fields, make sure the device can provide extremely high sensing accuracy.
- Fast over-threshold protection integrated, the output of the comparator is sent to the output side through a separate isolation channel, ensure robust protection and fast propagation delay (600ns typ), help to reduce customer discrete OVP circuit on board.
- Single-ended output reduces external differential to single-ended amplifier, apply the supply voltage of the subsequent ADC to VREF to match the entire ADC dynamic input range, the ratiometric single-ended output help to reduce area and improve accuracy.

Figure 9.1 shows the typical application circuit of NSI36C12R. The output of the low-side LDO (LDO pin) need to be connected to the isolated power supply input (ISO_PI pin). The isolated power supply output (ISO_PO pin) need to be connected to the input of the high-side LDO (LDO_IN pin). In this way, the high-side amplifier circuitry is powered by an isolated power supply. The necessary filter and bypass capacitors should be added to the device power supply pins, the output side power supply (VDD pin), the isolated power supply input (ISO_PI pin) and output (ISO_PO pin), and the input/output of the high-side LDO (LDO_IN and LDO_OUT pin). The recommended capacitance can refer to Figure 9.1.

The AC voltage of the frequency inverter is divided by a resistance network, and the divided voltage is applied to the input of the NSI36C12R through a RC filter. The protection comparator threshold voltage is set by dividing the LDO_OUT voltage. Adjusting the resistance of the voltage divider network can change the threshold voltage. The resistance of the voltage divider should not be too small because the maximum external load current on Input side LDO is 0.5mA.

The device has a ratiometric gain of $V_{REF}/2.56$ and provides a single-ended analog output. V_{REF} defines the clipping output voltage. Apply the supply voltage of the subsequent ADC to VREF to match the entire ADC dynamic input range. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

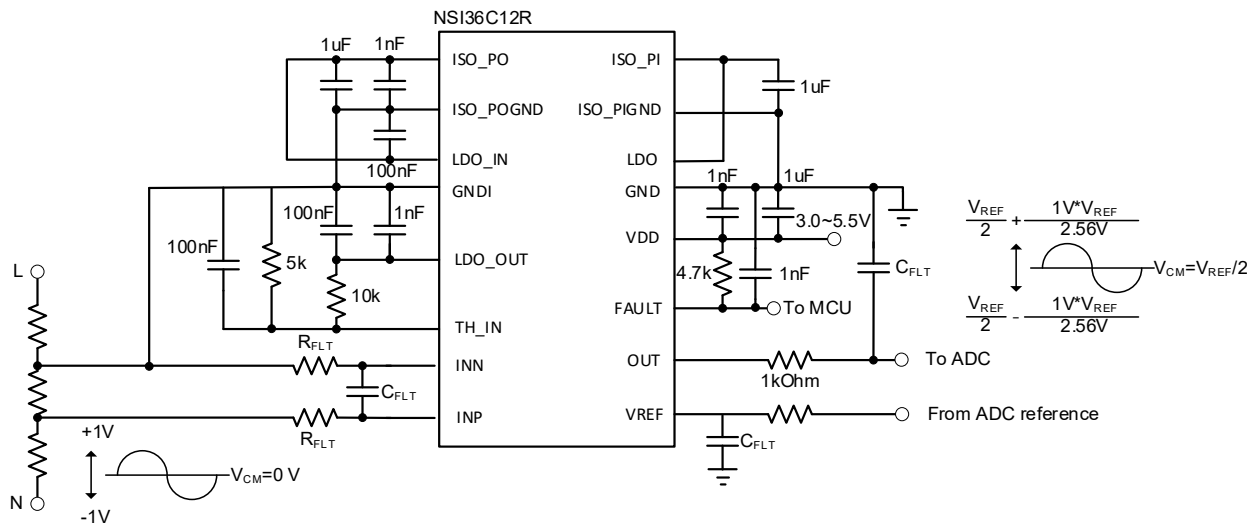


Figure 9.1 Typical application circuit

9.2. VREF Pin Connecting

The VREF pin is used to set the ratiometric gain. The reference input has a finite input impedance as shown in Section 6.1. The effect of this impedance must be considered when driving the VREF pin from a high-impedance source.

Figure 9.2 shows different options for connecting the VREF pin. In the first example, the VREF pin is shorted to VDD to obtain an output voltage that matches the dynamic input range of the subsequent ADC. A 100nF capacitor between the VREF and GND pins is used to filter out high-frequency noise at the reference input. In the second example, the VREF pin is driven by a buffered resistive divider that derives the reference voltage from VDD. In the third example, the VREF pin is driven by an external voltage source.

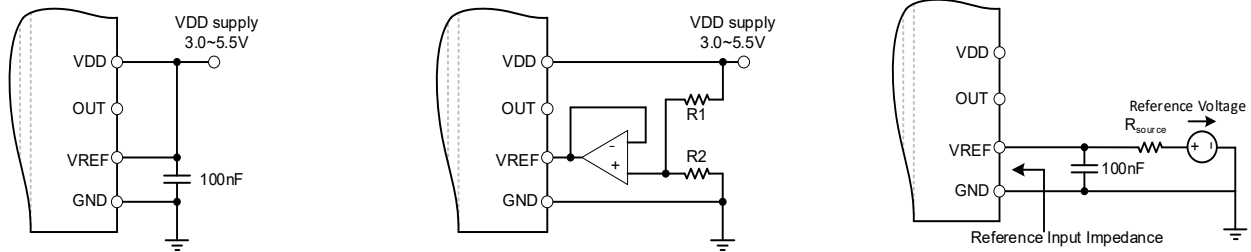


Figure 9.2 Typical application circuit

9.3. High Voltage Dividing Resistor Selection

Two restrictions should be considered when choosing the proper value of the voltage-dividing resistors:

- The current through the resistor should be within its rated range. Using Ohm law to calculate the cross current ($I_{cross} = V_{max}/R_{total}$);
- The divided input voltage value should not exceed the linear input range of NSI36C12R, in which case the output may be clipped.

9.4. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- The filter and bypass capacitors of VDD, ISO_PO, ISO_PI and LDO_OUT pins should be placed as close as possible to the pins respectively. For multiple filter capacitors of the same pin, capacitors with smaller values should be placed closer to the pin to filter out high-frequency noise better. An additional 1~10 μ F capacitor may be used for the power supply pin VDD in noisy conditions.
- Kelvin rules are recommended for the connection between sense resistor to NSI36C12R. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the sensing resistor close to the input and keep the layout of both connections symmetrical and the traces running very close to each other to the input of the NSI36C12R. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.
- To suppress radiation on the power lines, place Ferrite Beads respectively in series with the line of VDD and GND for filter. The ferrite Beads, together with decoupling capacitors, can filter and isolate noise well. In the layout area, the ferrite beads need to effectively separate the chip layout area from peripheral circuit without overlap in different PCB layers. Ferrite Beads can also be added in series with the differential input to suppress radiation on the input signal lines.
- Keep the trace lengths of the wiring as short as possible and don't place a ground plane in the high-voltage domain, which minimizes the antenna on this node to minimize radiated emissions.

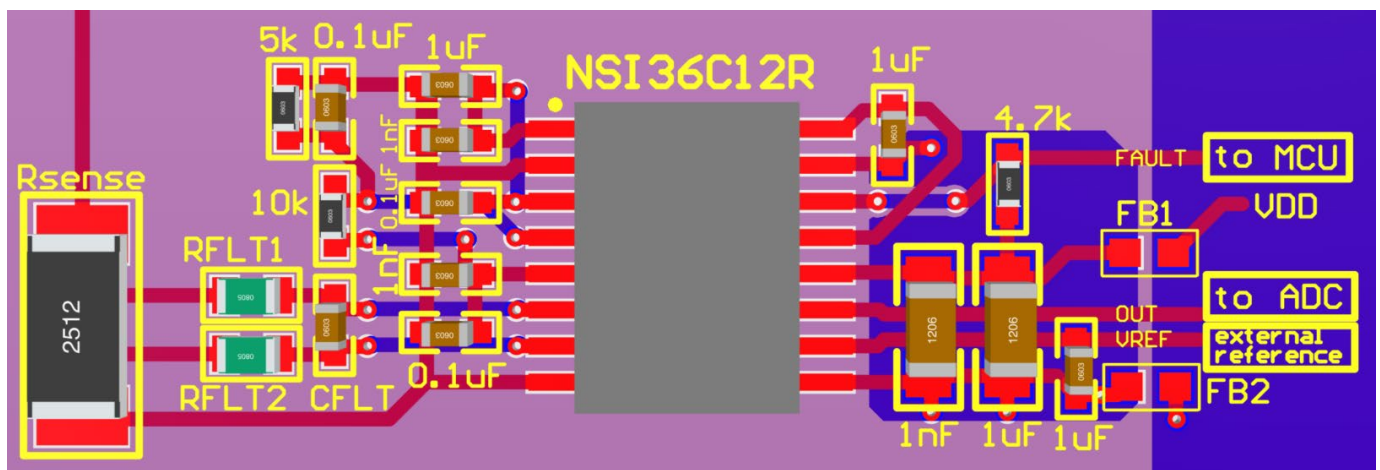
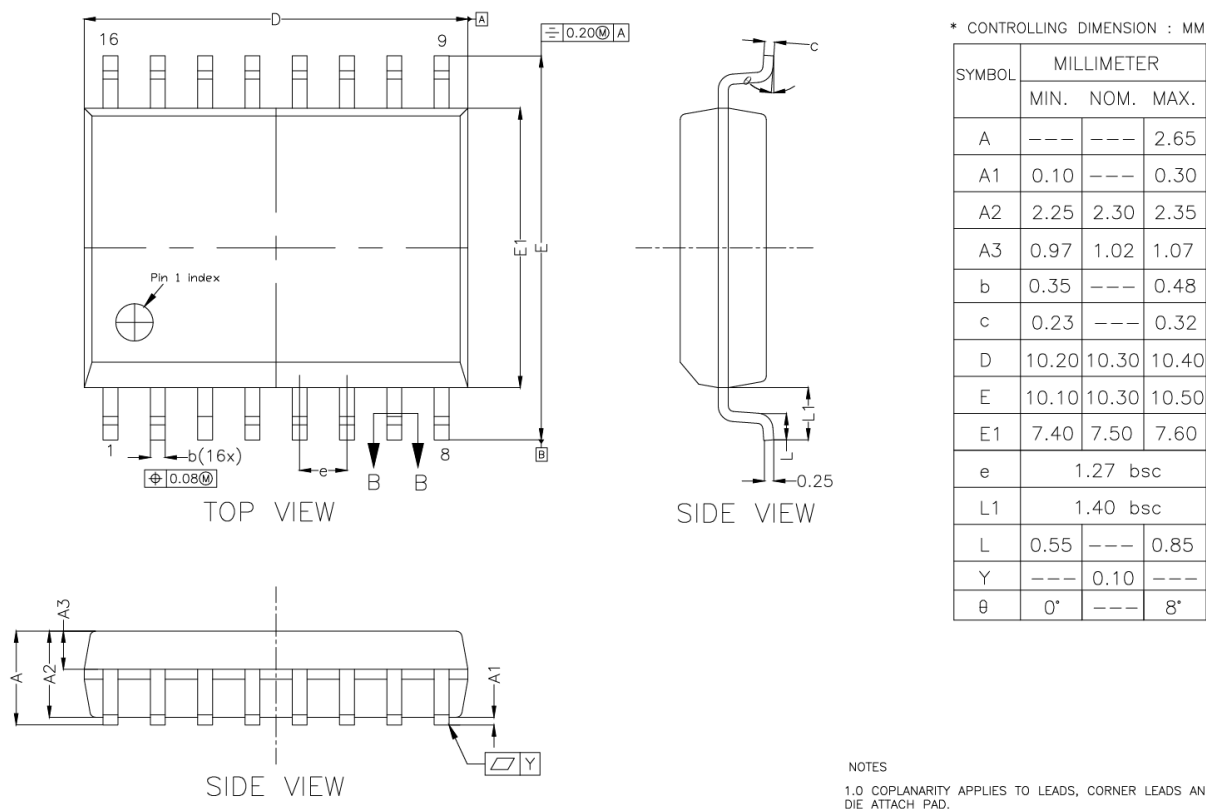


Figure 9.3 PCB layout example of NSI36C12R

10. Package Information



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOW16 package shape and dimension in millimeters

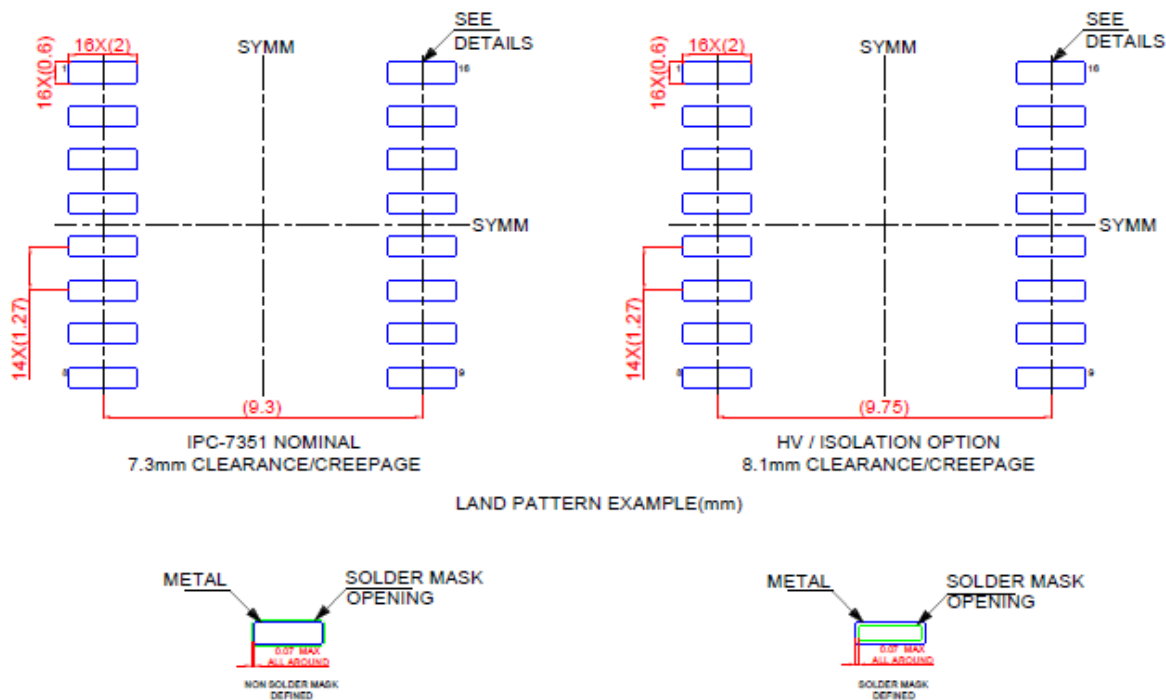


Figure 10.2 SOW16 Package Board Layout Example

Part No.	Isolation Rating (kV)	Linear Input Range(V)	MSL	Device Marking	Temperature	Automotive	Package Type	Package Drawing	SPQ	MPQ
NSI36C12R-Q1SWR	5	-1 ~ 1	Level-3	NSI36C12RQ	-40 to 125°C	YES	SOP16 (300mil)	SOW16	1500	1500

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolator selection guide</i>
NSI36C12R-Q1	Click here	Click here	Click here	Click here

Technical drawing of a circular wafer carrier (cassette) showing top and side views with dimensions and labels.

Top View:

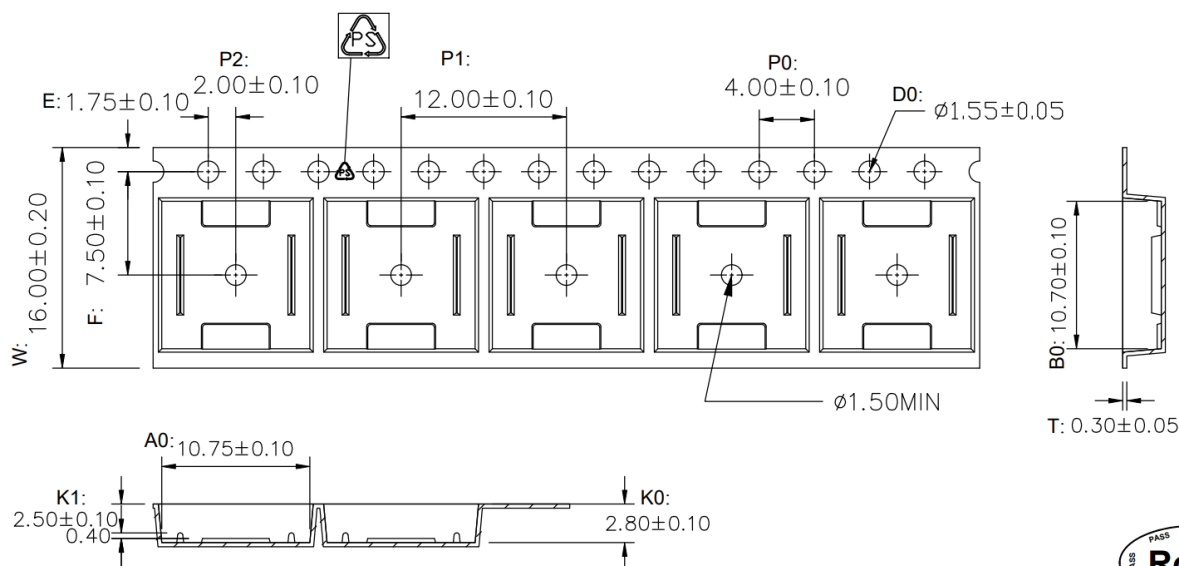
- Overall diameter: $\phi 21.00^{+0.8}_{-0.6}$
- Inner diameter: $\phi 13.20^{+0.3}_{-0.2}$
- Radial dimension from center to inner edge: $2.20^{+0.3}_{-0.3}$
- Radial dimension from center to outer edge: 28.98
- Label: TX16-04-EC1
- Warning: ATTENTION OBSERVER PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES
- Gate locations marked with "gate" and symbols.

Side View:

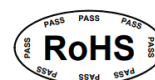
- Overall height: $H2$
- Inner height: $H1$
- Width: W

NOTES:
1.MATERIAL:DISSIPATIVE(BLACK)
2.FLANGE WARPAGE:3 MM MAXIMUM
3.ALL DIMENSIONS ARE IN MM
4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5.GENERAL TOLERANCE: ±0.25 MM

Page 27



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 378 Meters.(復巻 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : $10^5 \sim 10^{10} \Omega/\square$



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

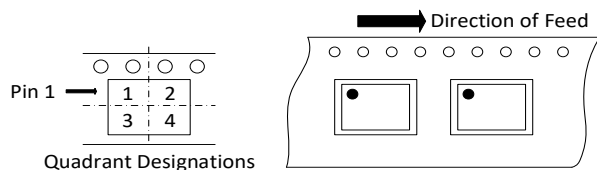


Figure 13.2 Tape Information of SOP16(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Version.	2026/05/08

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’s products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd