High Reliability Reinforced Isolated Amplifier with Integrated Isolated Power Supply

NOVOSENSE

Product Overview

The NSI3611D is a high-performance isolated amplifier with integrated isolated power supply. The device accepts a single-ended input signal range from 0V to 2V. The integrated isolated power supply enables single-power operation on the low side of the device without the need for a separate isolated power supply for the high side, effectively reducing the board area. The high input impedance of NSI3611D makes it highly suitable for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

The device has a fixed gain of 1 and provides a differential analog output. The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The integrated isolated power supply detection and the open-drain diagnosis output simplify system-level design and diagnostics.

Key Features

- Up to 5000V_{rms} Insulation voltage
- 0V~2V linear Input Voltage Range
- Low Offset Error and Drift:
  ±1.2mV (Max), ±20μV/°C (Max)
- Low Gain Error and Drift:
  ±0.25% (Max), ±45ppm/°C (Max)
- Low Nonlinearity and Drift:
  ±0.04% (Max), ±1ppm/°C (Typ)
- SNR: 78dB (Typ, BW=10kHz), 66dB (Typ, BW=100kHz)
- Wide bandwidth: 340kHz (Typ)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Features: integrated isolated power supply detection
- Operation Temperature: -40°C ~125°C
- RoHS-Compliant Packages: SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Server Power Supply Units
- Uninterruptible Power Suppliers
- Energy Storage Systems
- Solar Inverters
- Charging Piles
- Motor Drives

Device Information

Part Number	*Package*	*Body Size*
NSI3611D-DSWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

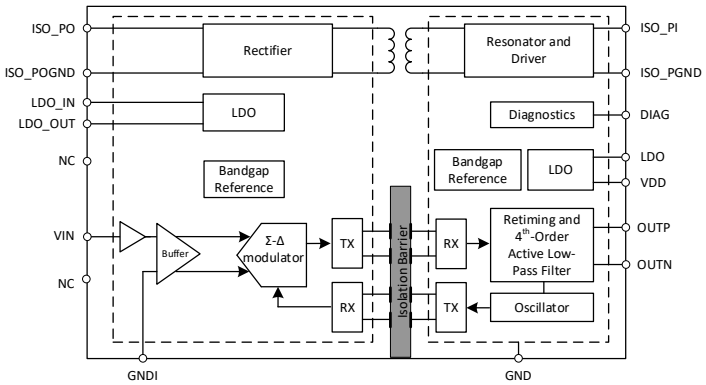

Figure 1. Function Block Diagram of NSI3611D

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1. Pin Configuration and Functions

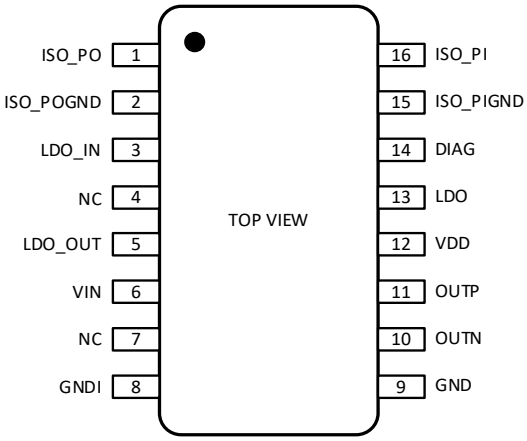


Figure 1.1 NSI3611D Package

Table 1.1 NSI3611D Pin Configuration and Description

NSI3611D PIN NO.	*SYMBOL*	*FUNCTION*
1	ISO_PO	Internal isolated power output (need to be connected to the LDO_IN pin)
2	ISO_POGND	Internal isolated power ground reference (need to be connected to the GNDI pin)
3	LDO_IN	Internal input side LDO power input (need to be connected to the ISO_PO pin)
4	NC	Not internal connected, leave this pin floating or connect to GNDI
5	LDO_OUT	Internal input side LDO power output
6	VIN	Single-ended analog input
7	NC	Not internal connected, leave this pin floating or connect to GNDI
8	GNDI	Input side ground reference (need to be connected to the ISO_POGND pin)
9	GND	Output side ground reference (need to be connected to the ISO_PIGND pin)
10	OUTN	Negative analog output
11	OUTP	Positive analog output
12	VDD	Output side power supply
13	LDO	Internal output side LDO power input (need to be connected to the ISO_PI pin and without external load)
14	DIAG	Open-drain diagnosis output (need to be connected to the pull-up supply or floating)
15	ISO_PIGND	Internal isolated power ground reference (need to be connected to the GND pin)
16	ISO_PI	Internal isolated power input (need to be connected to the LDO pin)

2. Absolute Maximum Ratings (1)

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD to GND	-0.3		6.5	V
Analog Input Voltage	VIN	GNDI-6		LDO_OUT+0.5	V
Analog Output Voltage	OUTP, OUTN	GND-0.5		VDD+0.5	V
Digital Output Voltage	DIAG	GND-0.5		6.5	V
Input current per output Pin	I_{IN}	-10		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

3. ESD Ratings (1)

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±4.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±1.0	kV

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply	VDD to IGND	3.0	3.3	5.5	V
Input voltage before clipping output	$V_{Clipping}$		2.5		V
Linear differential input full scale voltage	V_{FSR}	0		2	V
DIAG pull-up supply voltage	V_{DIAG}	0		VDD	V
Operating Ambient Temperature	T_A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	64	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	30	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	33.3	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	10.9	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	28.2	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD = 3.0V ~ 5.5V, VIN = 0V to 2V, T_A = -40°C to 125°C. Unless otherwise noted, Typical values are at VDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Output side supply voltage	VDD	3.0	3.3	5.5	V	
Output side supply current	IDD		31.3	42	mA	no external load on LDO_OUT
Output side supply current	IDD		32.6	43.2	mA	1mA external load on LDO_OUT
External load current on Input side LDO	I_E			1	mA	
Isolated power output voltage	V_{ISO_PO}	3	3.5	4.6	V	ISO_PO to GNDI
Input side LDO output voltage	V_{LDO_OUT}	3	3.2	3.3	V	LDO_OUT to GNDI
Isolated power output undervoltage detection threshold voltage	V_{ISO_POUV}	2.1	2.3	2.8	V	
Input side LDO undervoltage detection threshold voltage	V_{LDO_UV}	2.1	2.3	2.8	V	
VDD undervoltage detection threshold voltage	VDD_{UV}			2.95	V	
Analog Input						
Input offset voltage	V_{OS}	-1.2	±0.1	1.2	mV	VIN=0V, at T_A = 25°C
Input offset drift (1)	TCV_{OS}	-20	1	20	μV/°C	
Single-ended input resistance	R_{IN}	0.1	1		GΩ	
Input capacitance	C_I		4.5		pF	Single-ended input capacitance, fin=310kHz
Input bias current	I_{IB}		1		nA	VIN=0V, at TA = 25°C

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input bias current drift (1)	TCI_{IB}		-14		pA/°C	
Analog Output						
Nominal Gain			1		V/V	
Gain error	E_G	-0.25%	±0.05%	0.25%		at T_A = 25°C
Gain error thermal drift (1)	TCE_G	-45	±15	45	ppm/°C	
Nonlinearity		-0.04%	±0.01%	0.04%		
Nonlinearity drift (1)			1		ppm/°C	
Total harmonic distortion (3)	THD		-85		dB	VIN =2Vpp, f_{IN} = 10kHz, BW = 100kHz
Output noise			300		μV_{RMS}	VIN = 0V, BW = 100kHz
Signal to noise ratio	SNR	72	78		dB	VIN =2Vpp, f_{IN} = 1kHz, BW = 10kHz
	SNR		66		dB	VIN =2Vpp, f_{IN} = 10kHz, BW = 100kHz, 1MHz filter
Common-mode output voltage	V_{CMout}	1.35	1.42	1.48	V	
Differential clipping output voltage	V_{CLout}		2.4		V	V_{OUT} = (V_{OUTP} – V_{OUTN}), V_{IN} > $V_{Clipping}$
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.55	-2.5	V	
Output bandwidth	BW		340		kHz	
Power supply rejection ratio (2)	$PSRR_{dc}$		-92		dB	PSRR vs VDD, from 3.0~5.5V at DC
	$PSRR_{ac}$		-84		dB	PSRR vs VDD, 100mV and 10kHz ripple
Output resistance	R_{OUT}		0.3		Ω	
Output capacitance	C_{LOAD}		500		pF	
Output limit current	I_{lim}		±20		mA	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t_r		1.1		μs	
Falling time of OUTP, OUTN	t_f		1.1		μs	
VIN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.4	1.8	μs	
Analog setting time	t_{AS}		0.9		ms	VDD step to 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) The temperature drift is calculated within the whole temperature range (-40°C to 125°C).

(2) Input referred.

(3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).

6.2. Timing Diagrams

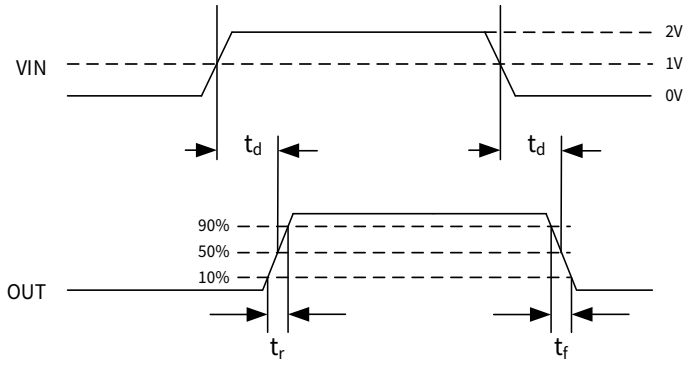


Figure 6.1 Propagation Delay and Output Fall Time Definition

6.3. Typical Performance Characteristics

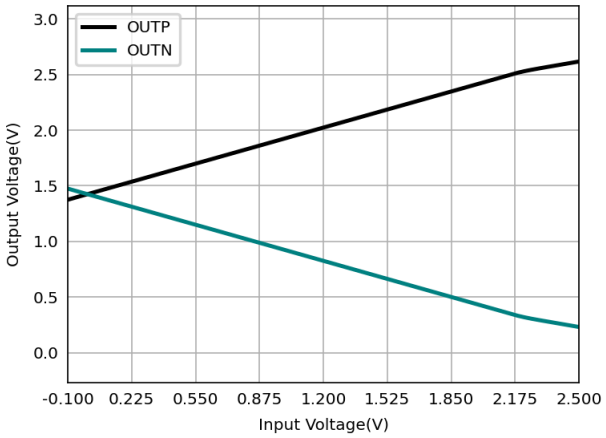


Figure 6.2 Output vs Input Voltage

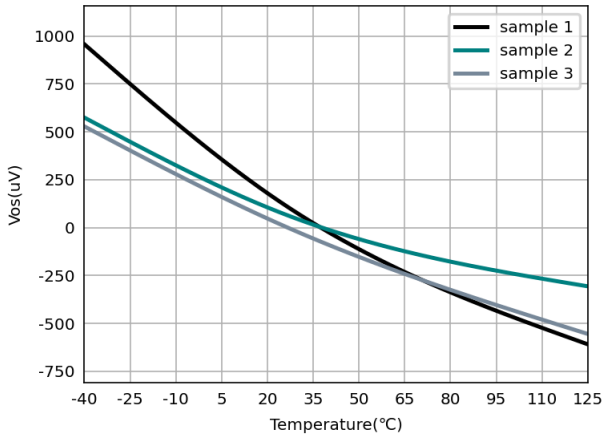


Figure 6.3 Input Offset Voltage vs Temperature

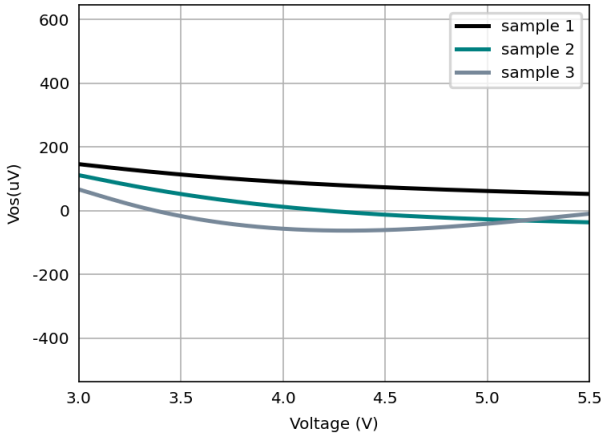


Figure 6.4 Input Offset Voltage vs Supply Voltage

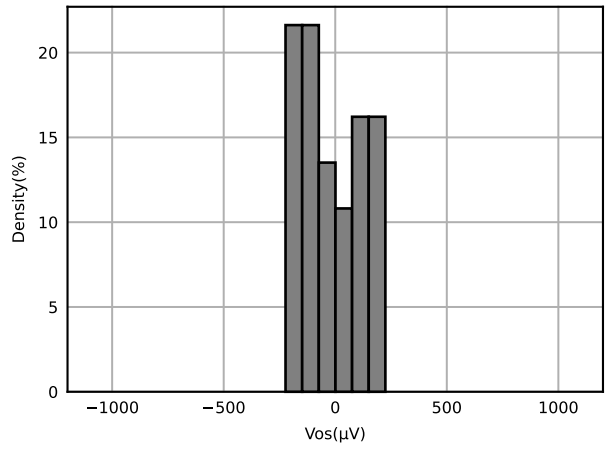


Figure 6.5 Input Offset Voltage Distribution (1)

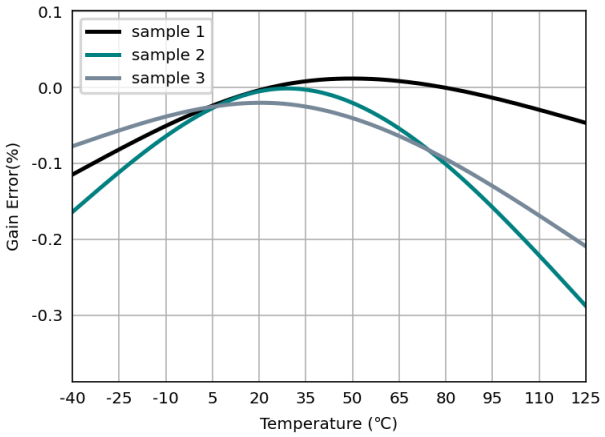


Figure 6.6 Gain Error vs Temperature

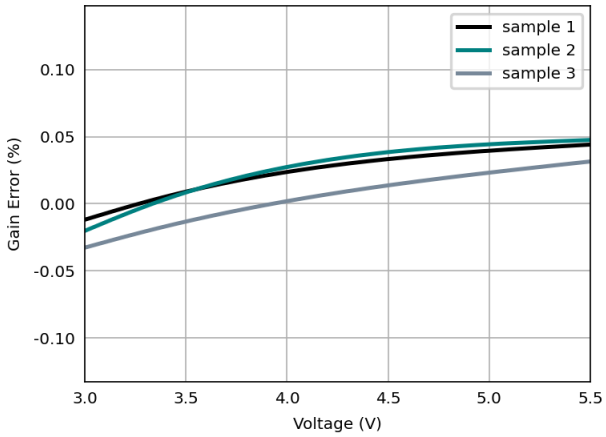


Figure 6.7 Gain Error vs Supply Voltage

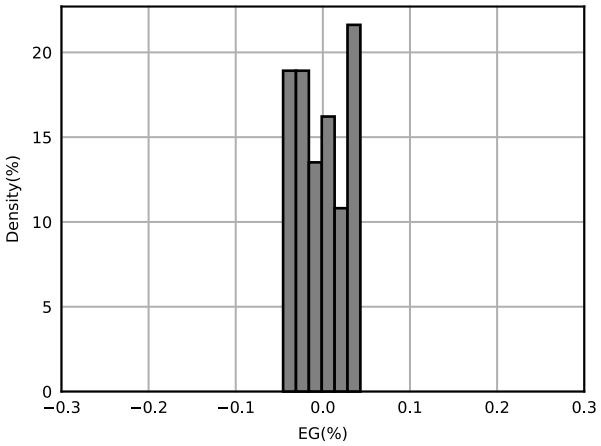


Figure 6.8 Gain Error Distribution (1)

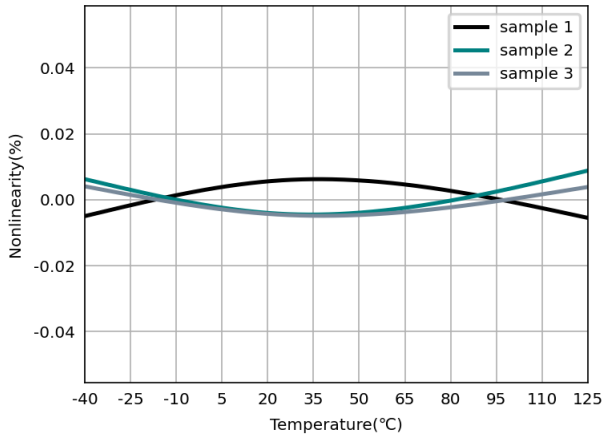


Figure 6.9 Nonlinearity vs Temperature

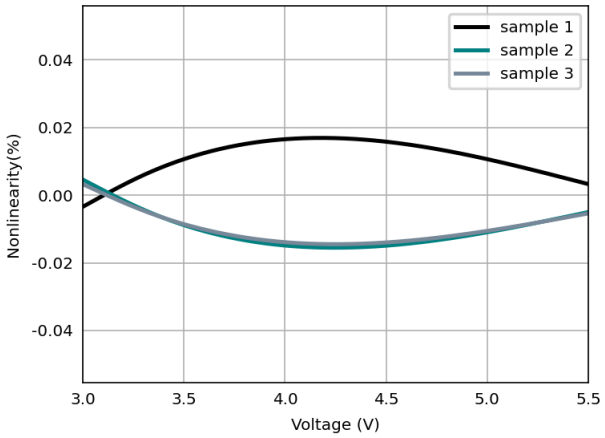


Figure 6.10 Nonlinearity vs Supply Voltage

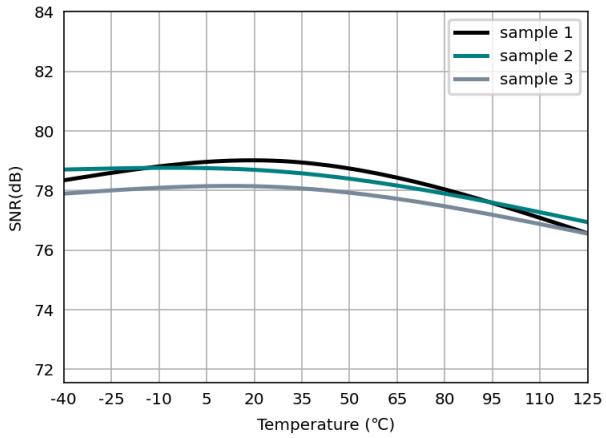


Figure 6.11 Signal to Noise Ratio vs Temperature

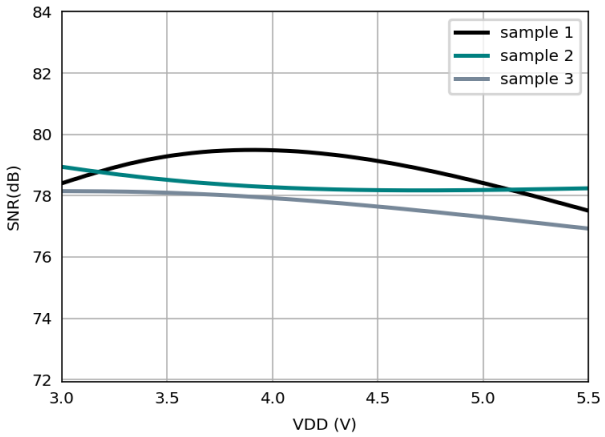


Figure 6.12 Signal to Noise Ratio vs Supply Voltage

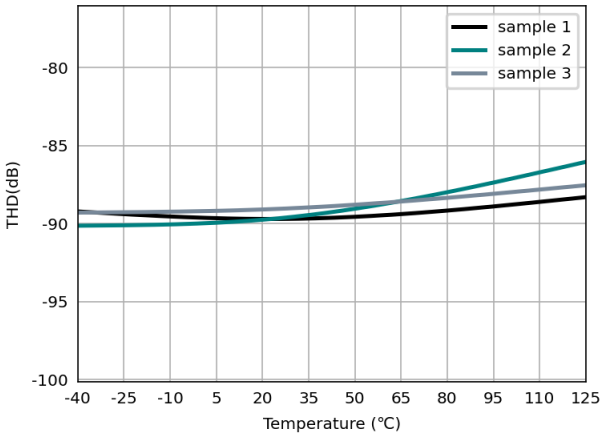


Figure 6.13 Total Harmonic Distortion vs Temperature

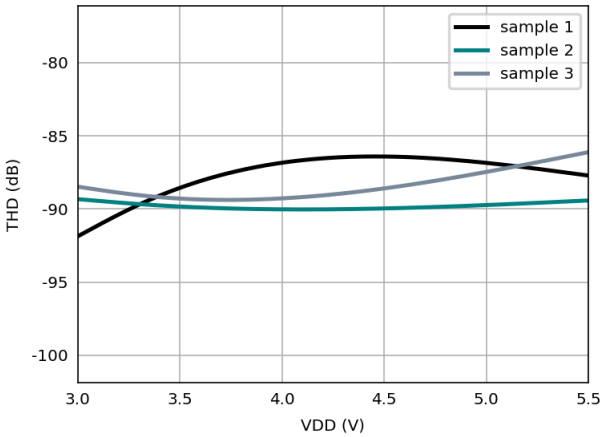


Figure 6.14 Total Harmonic Distortion vs Supply Voltage

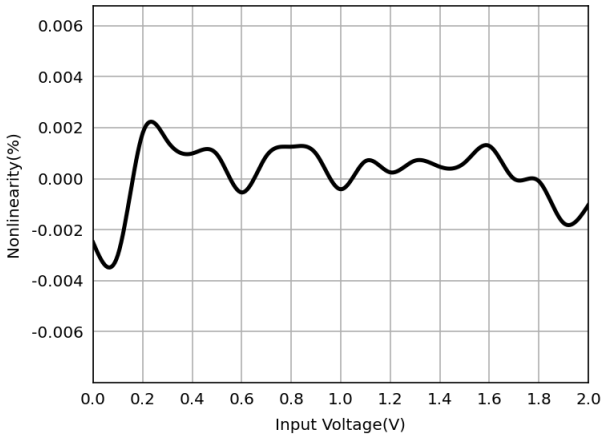


Figure 6.15 Nonlinearity vs Input Voltage

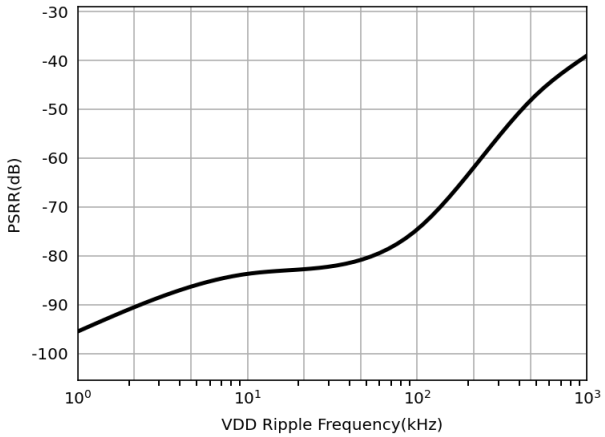


Figure 6.16 Power-Supply Rejection Ratio vs VDD Input Frequency

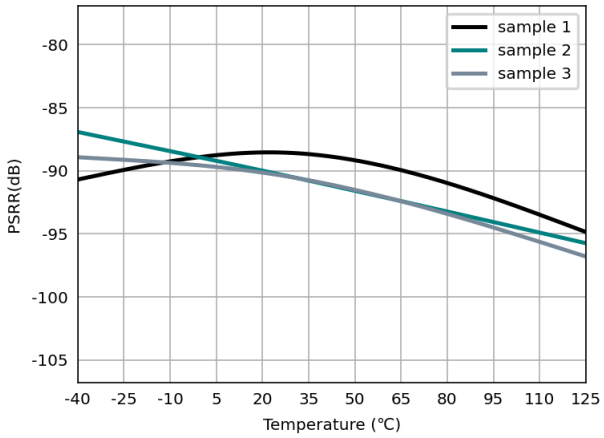


Figure 6.17 Power-Supply Rejection Ratio vs Temperature

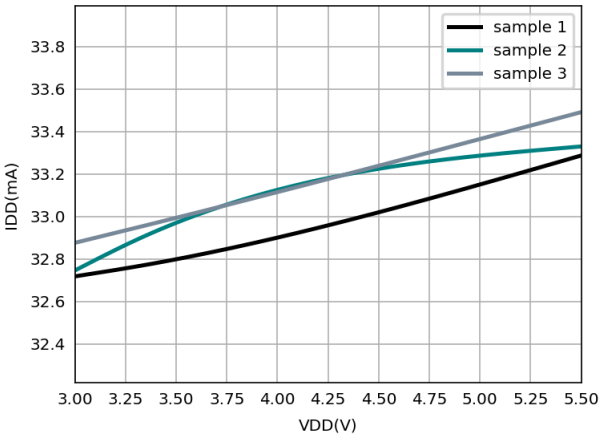


Figure 6.18 Input Supply Current vs Supply Voltage (IE=1mA)

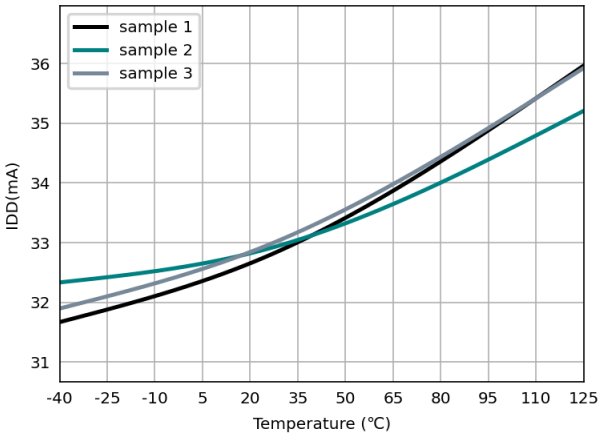


Figure 6.19 Input Supply Current vs Temperature (IE=1mA)

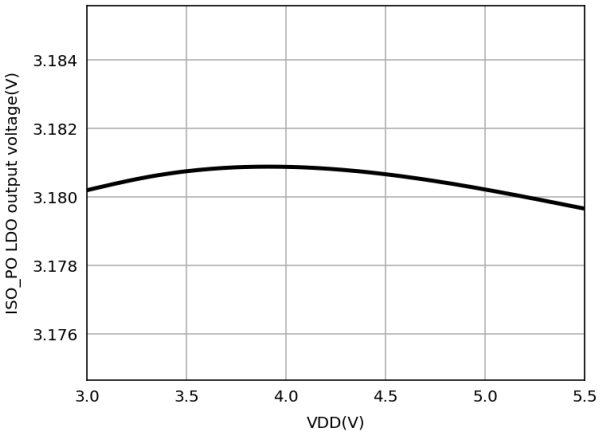


Figure 6.20 ISO-PO LDO Regulation

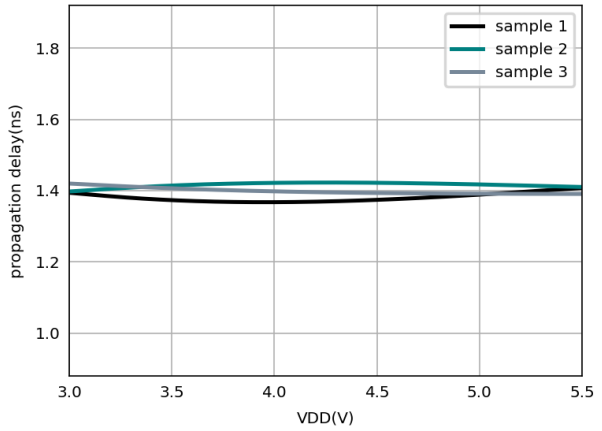


Figure 6.21 Input and Output Signal Delay time vs Supply Voltage

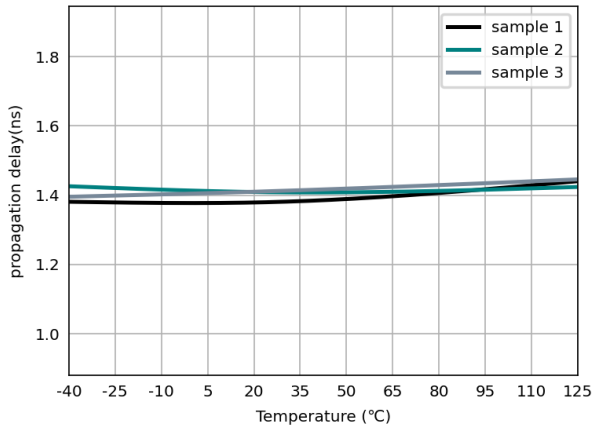


Figure 6.22 Input and Output Signal Delay time vs Temperature

(1) According to the test results of 30 pcs samples.

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	26	μm	Distance through insulation (internal clearance – capacitive signal isolation)
		75	μm	Distance through insulation (internal clearance – transformer power isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s , $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s ,$V_{pd(m)}=1.6*V_{IORM}$, t_m=10s			pC
	Method b, $V_{ini}=1.2*V_{IOTM}$, t_{ini}=1s			pC

Description	Test Condition	Symbol	Value	Unit
	$V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=V_{ini}, t_m=t_{ini}(method b2)			
Maximum transient isolation voltage	t = 60sec	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, V_{IOSM}≥V_{IMP} × 1.3	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25°C	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100°C ≤ T_{amb} ≤ 125°C	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Ps	1524	mW
Safety input, output, or supply current	θ_{JA} = 82°C/W for SOW8, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Is	277	mA
Maximum safety temperature		Ts	150	°C
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s	V_{ISO}	5000	V_{RMS}

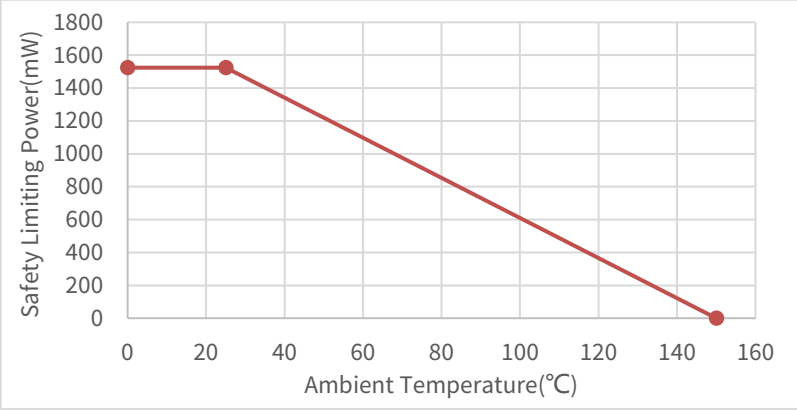


Figure 7.1 NSI3611D Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI3611D are approved by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121 V_{PEAK} V_{IOTM}=8000 V_{PEAK} V_{IOSM}=10000 V_{PEAK}	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264939	R50574061

8. Function Description

8.1. Overview

The NSI3611D is a high-performance isolated amplifier with integrated isolated power supply. The device accepts a single-ended input signal range from 0V to 2V. The integrated isolated power supply enables single-power operation on the low side of the device without the need for a separate isolated power supply for the high side, effectively reducing the board area. The high input impedance of NSI3611D makes it highly suitable for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

The low-side power supply VDD feeds power to the isolated power supply input through an LDO with external connection from the LDO pin to the ISO_PI pin. The output of the isolated power supply is regulated by an LDO with external connection from the ISO_PO pin to the LDO_IN pin, to power the high-side circuit. The integrated isolated power supply enables single-power operation on the low side of the device without the need for a separate isolated power supply for the high side, effectively reducing the board area.

The analog input is continuously sampled by a second-order Σ-Δ modulator in the device, which is driven by a pre-stage buffer in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated input and output side voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the output side and has a differential output.

The integrated isolated power supply detection and the open-drain diagnosis output simplify system-level design and diagnostics.

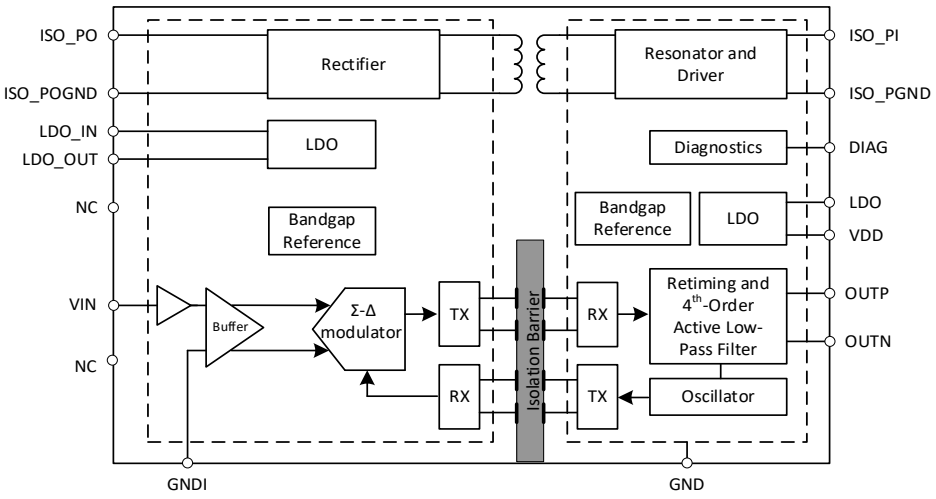


Figure 8.1 Function Block Diagram of NSI3611D

8.2. Analog Input and output

There are two restrictions on the analog input signal (VIN).

- If the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR).

For linear input range, the analog output of NSI3611D has a fixed gain of 1. If an input signal exceeding the clipping input range is applied to the NSI3611D ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically 2.4V).

In addition, NSI3611D integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated when the undervoltage of the integrated isolated power supply output ISO_PO or the high-side LDO output LDO_OUT is detected. Use the maximum $V_{FAILSAFE}$ voltage -2.5V as a reference value for the fail-safe detection on the system level.

8.3. Accuracy Related Parameters

Parameters related to the accuracy performance are explained in this section, including Vos and its drift, EG and its drift, Nonlinearity. Other immunity parameters that affect accuracy like CMRR and PSRR are also included.

8.3.1. Input offset V_{OS} and Gain Error E_G

Vos and EG are the most significant factor influencing accuracy. The ideal curve and actual curve are shown in Figure 8.2.

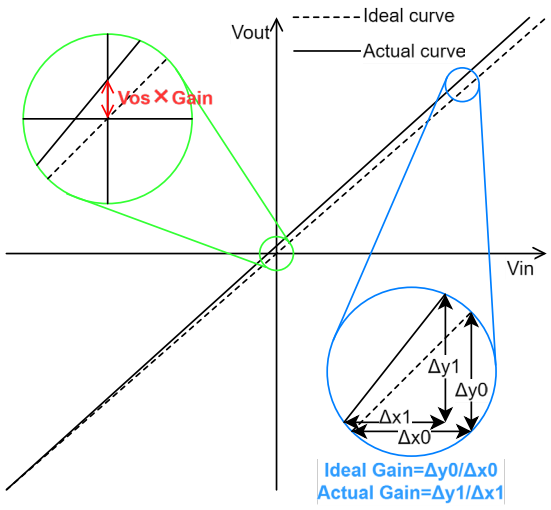


Figure 8.2 Vos and EG diagram

V_{OS} means the input offset voltage when input is 0V. The tested output should be divided by nominal gain as Vos is defined as the offset voltage referred to input (See Equation 1).

$$\mathrm{Vos} = \mathrm{Vo}/\mathrm{Nominal\ Gain} \qquad \text{Equation 1}$$

where

- Vo is the output voltage tested when input is 0V.
- Nominal Gain is 1 for NSI3611D.

Gain is the magnification of the amplifier, and the definition formula is shown in Equation 2. EG means the difference between actual and ideal slope. It should be noted that EG is tested across the whole input range to minimize test error (See Equation 3).

$$\mathrm{Gain} = \frac{\Delta y1}{\Delta x1} = \frac{\mathrm{Vo1} - \mathrm{Vo2}}{\mathrm{Vin1} - \mathrm{Vin2}} \qquad \text{Equation 2}$$

$$E_G = \frac{\text{Gain} - \text{Nominal Gain}}{\text{Nominal Gain}} \times 100\% \quad \text{Equation 3}$$

where Vin1 and Vin2 are the lower and upper limit of the input FSR separately, Vo1 and Vo2 are the output voltage corresponding to Vin1 and Vin2.

8.3.2. Input offset drift TCV_{OS} and Gain error thermal drift TCE_G

Input offset drift TCV_{OS} means the drift of V_{OS} over the whole operating temperature range, which is calculated as Equation 4.

$$\text{TCVos} = \frac{\text{Vos}_{\max} - \text{Vos}_{\min}}{\text{TempRange}} \quad \text{Equation 4}$$

where

- Vos_{max} and Vos_{min} is the maximum and minimum offset voltage over the whole operating ambient temperature range.
- TempRange covers the whole operating temperature, from -40°C to 125°C.

Gain error thermal drift TCE_G is the drift of E_G over the whole operating temperature range, which is calculated as Equation 5.

$$\text{TCE}_G = \frac{\text{E}_{\text{Gmax}} - \text{E}_{\text{Gmin}}}{\text{TempRange}} \quad \text{Equation 5}$$

where E_{Gmax} and E_{Gmin} is the maximum and minimum Gain Error over the whole temperature.

Both TCV_{OS} and TCE_G should be multiplied by the direction of temperature drift.

8.3.3. Nonlinearity

Nonlinearity describes the deviation between the actual output and the ideal linear output. Calculate the peak-to-peak value of the error between the actual output and the fitting curve, and nonlinearity is expressed as the ratio of half of the peak-to-peak error to the full-scale range of the output voltage (See Equation 6).

$$\text{Nonlinearity} = \frac{\text{Error\_pkpk}}{2 \times \text{V}_{\text{OFSR}}} \times 100\% \quad \text{Equation 6}$$

where

- Error_pkpk is the peak-to-peak value of the error between the actual output and the fitting curve.
- V_{OFSR} represents the full-scale range of the output voltage (2V for NSI3611D).

8.3.4. Power-Supply Rejection Ratio

Power-Supply Rejection Ratio (PSRR) describes the level of the output error (input inferred) which is affected by the variation of power supply. PSRR is defined in dB and calculated as Equation 7.

$$\text{PSRR} = 20 \times \log_{10}\left(\frac{\text{V}_{\text{O\_var}}}{\text{Nominal Gain} \times \text{VDD}_{\text{var}}}\right) \quad \text{Equation 7}$$

Where V_{O_var} and VDD_{var} are respectively the variation value of the output voltage and the supply voltage.

8.3.5. Common-Mode Rejection Ratio

Common-Mode Rejection Ratio (CMRR) quantifies the ability of a differential amplifier to suppress the variation of the common mode signals while amplifying the differential-mode signals. CMRR is calculated as:

$$\text{CMRR} = 20 \times \log_{10}\left(\frac{\text{V}_{\text{O\_var}}}{\text{Nominal Gain} \times \text{V}_{\text{CM\_var}}}\right) \quad \text{Equation 8}$$

where CMRR is the input-referred voltage variation in dB and V_{CM_var} is the variation value of the input common-mode voltage.

8.3.6. Total Error Calculation

The total error is contributed by parameters discussed above. It is helpful to know the respective contribution of all different parameters when something is wrong about system current sensing. This section will introduce the calculation method of total error.

Parameters which mainly affects sensing accuracy are Vos, EG and Nonlinearity and their drift. PSRR and CMRR are not a dominant factor in most case. However, PSRR can be a concern when the power supply has high-frequency ripple, in which case a larger decoupling capacitor and a better layout is highly recommended (Refer to Section 9.3).

The error introduce by Vos and its drift can be calculated as:

$$\text{Error\_Vos} = \frac{\text{Vos}_{\max} + \text{TCV}_{\text{os}} \times \Delta T}{V_{IN}} \times 100\% \quad \text{Equation 9}$$

where

- $\text{Vos}_{\max}$ is the maximum value of input offset voltage at 25°C, which is ±1.2mV for NSI3611D.
- TCV_{os} is the maximum drift of input offset voltage over the whole working temperature, which is 20uV/°C for 3611D
- ΔT is the range of temperature variation.
- V_{IN} is the input voltage in the application.

The error introduced by E_G and TCE_G can be calculated as：

$$\text{Error\_E}_G = \text{E}_G + \text{TCE}_G \times \Delta T \quad \text{Equation 10}$$

where

- E_G is the maximum value of Gain Error when the temperature is 25°C, which is ±0.25% for NSI3611D.
- TCE_G is the maximum drift of Gain Error over the whole temperature, which is ±50ppm/°C for NSI3611D.

The error introduced by Nonlinearity is $\text{Nonlinearity}_{\max}$, the maximum value of Nonlinearity in the entire temperature range, - 40°C to 125°C, which is ±0.04% for NSI3611D. The total error sensing error is expressed as:

$$\text{Total\_Error} = \sqrt{\text{Error\_Vos}^2 + \text{Error\_E}_G{}^2 + \text{Nonlinearity}_{\max}{}^2} \quad \text{Equation 11}$$

For example, consider an NSI3611D with the sensing input voltage of 0~2V and a - 40°C to 85°C temperature range. The total error calculation is shown in Table 8.1.

Table 8.1 Total Error Calculation of NSI3611D (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at Vin=2V	Error at Vin=0.1V
Input offset error	Error_Vos	$\text{Error\_Vos} = \frac{\text{Vos}_{\max} + \text{TCV}_{\text{os}} \times \Delta T}{V_{IN}} \times 100\% = \frac{\pm 1.2\text{mV} \pm 30\mu\text{V/°C} * 65\text{°C}}{V_{IN}} \times 100\%$	±0.158%	±3.15%
Gain error	Error_E_G	$\text{Error\_E}_G = \text{E}_G + \text{TCE}_G \times \Delta T = \pm 0.25\% \pm 45\text{ppm/°C} \times 65\text{°C}$	±0.543%	±0.543%
Nonlinearity	$\text{Nonlinearity}_{\max}$	$\text{Nonlinearity}_{\max} = \pm 0.04\%$	±0.04%	±0.04%
Total error	Total_Error	$\text{Total\_Error} = \sqrt{\text{Error\_Vos}^2 + \text{Error\_E}_G{}^2 + \text{Nonlinearity}_{\max}{}^2}$	±0.567%	±3.197%

Since the input offset voltage is independent of input voltage, it becomes the dominant factor of the total error when the input voltage is low. To improve the system accuracy, especially under low-input applications, it is recommended to perform software zero-point calibration and gain error calibration. With system-level calibration, the total error can also be reduced significantly. The reduced error is calculated as Table 8.2.

Table 8.2 Total Error Calculation with Software Calibration (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at Vin=2V	Error at Vin=0.1V
Input offset error	Error_Vos	$\text{Error\_Vos} = \frac{\text{TCV}_{\text{os}} \times \Delta\text{T}}{\text{V}_{IN}} \times 100\% = \frac{30\mu\text{V/°C} * 65\text{°C}}{\text{V}_{IN}} \times 100\%$	±0.098%	±1.95%
Gain error	Error_E_G	$\text{Error\_E}_G = \text{TCE}_G \times \Delta\text{T} = \pm 45\text{ppm/°C} \times 65\text{°C}$	±0.293%	±0.293%
Nonlinearity	$\text{Nonlinearity}_{\text{max}}$	$\text{Nonlinearity}_{\text{max}} = \pm 0.04\%$	±0.04%	±0.04%
Total error	Total_Error	$\text{Total\_Error} = \sqrt{\text{Error\_Vos}^2 + \text{Error\_E}_G{}^2 + \text{Nonlinearity}_{\text{max}}{}^2}$	±0.312%	±1.972%

The maximum total error with and without calibration is show in Figure 8.3.

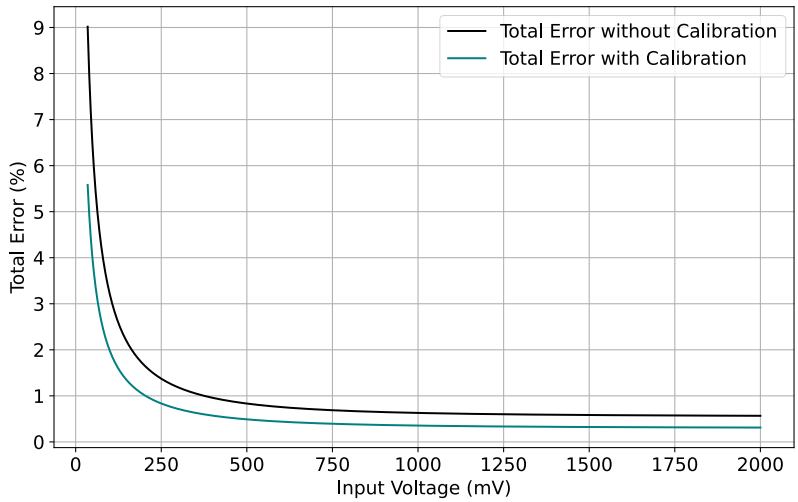


Figure 8.3 Total Error Over - 40°C to 85°C vs Input Voltage

8.4. Isolated power

The NSI3611D integrates an isolated DC/DC power supply that includes the following components as shown in Figure 8.1:

- Low-side low-dropout regulator (LDO) to provide stable voltage for the input of the isolated DC/DC converter.
- Isolated DC/DC converter with the primary resonator and driver, an air-core transformer, and the secondary rectifier. The converter does not output a constant voltage and it is not recommended to drive additional load.
- High-side LDO to convert the isolated DC/DC converter output to a stable voltage and supply for the high-side signal circuitry. The high-side LDO can provide a limited current of 1mA for external load.

The isolated DC/DC power supply uses a spread spectrum clocking technique and optimized transformer design to improve the electro-magnetic interference (EMI) performance.

8.5. Diagnostic Output

The open-drain diagnosis output DIAG helps confirm whether the device is in normal operation and simplifies system-level design and diagnostics. The DIAG pin needs to be connected to the pull-up supply through a resister. If the device operates normally, the DIAG pin is in a high-impedance state and pulled up to high level externally. The DIAG pin is actively pulled

low when the undervoltage of the integrated isolated power supply output ISO_PO or the high-side LDO output LDO_OUT is detected. The failsafe mode is activated correspondingly. The amplifier outputs a negative differential voltage $V_{FAILSAFE}$.

The diagnostic output feature is only activated when the NSI3611D is properly powered on, which means the DIAG pin will not be pull down during power up procedure.

The DIAG pin can be floating if not used.

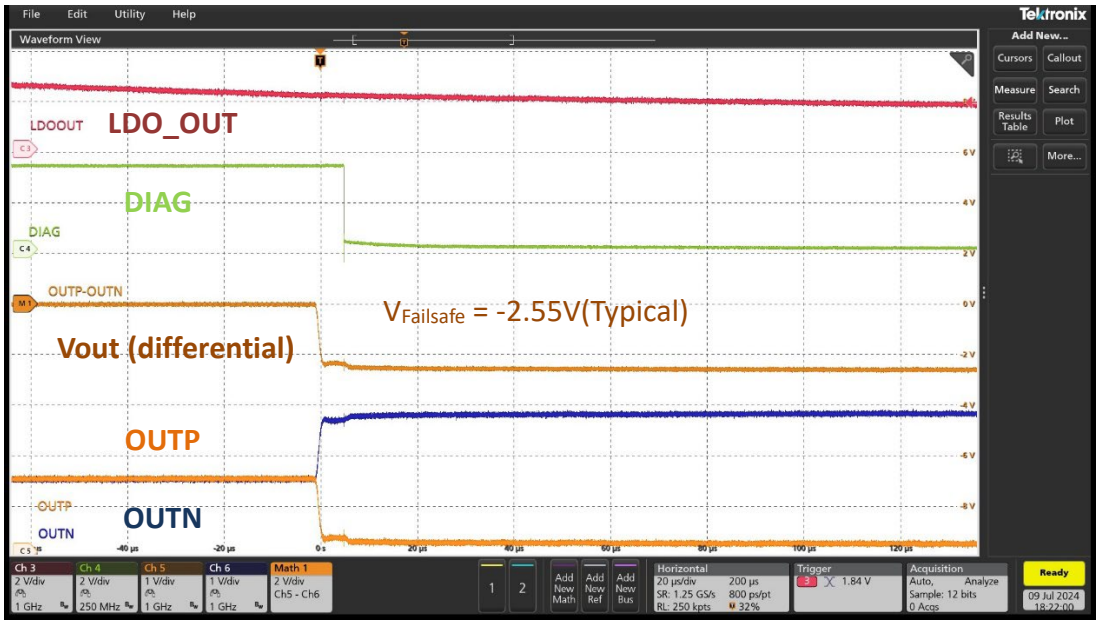


Figure 8.4 Typical Failsafe output

9. Application Note

9.1. Typical Application Circuit

The following key features make NSI3611D is the ideal solution for isolated voltage sensing applications.

- Reinforced isolation barrier supports a working voltage up to 1500Vrms, provide extremely high reliability for dangerous high voltage systems.
- Excellent common mode transient immunity (CMTI, 150kV/us typ) ensures the device to provide accurate and reliable measurements even in the presence of high-power switching.
- Isolated power supply integrated, reduces the need of external isolated high-side supply compared to traditional NSI1311, simplifies design and reduces area.
- Excellent DC accuracy and low drift, high linearity over FSR, make sure the device can provide extremely high sensing accuracy.

The typical application circuit is shown in Figure 9.1. The output of the low-side LDO (LDO pin) need to be connected to the isolated power supply input (ISO_PI pin). The isolated power supply output (ISO_PO pin) need to be connected to the input of the high-side LDO (LDO_IN pin). In this way, the high-side amplifier circuitry is powered by an isolated power supply. The necessary filter and bypass capacitors should be added to the device power supply, the isolated power supply input (ISO_PI pin) and output (ISO_PO pin), and the input of the high-side LDO (LDO_IN pin).The recommended capacitance can refer to Figure 9.1.

The bus voltage of the frequency inverter is divided by a resistance network, and the divided voltage is applied to the input of the NSI3611D through a RC filter. Suggest to add >1kΩ resistor on the OUTP and OUTN pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

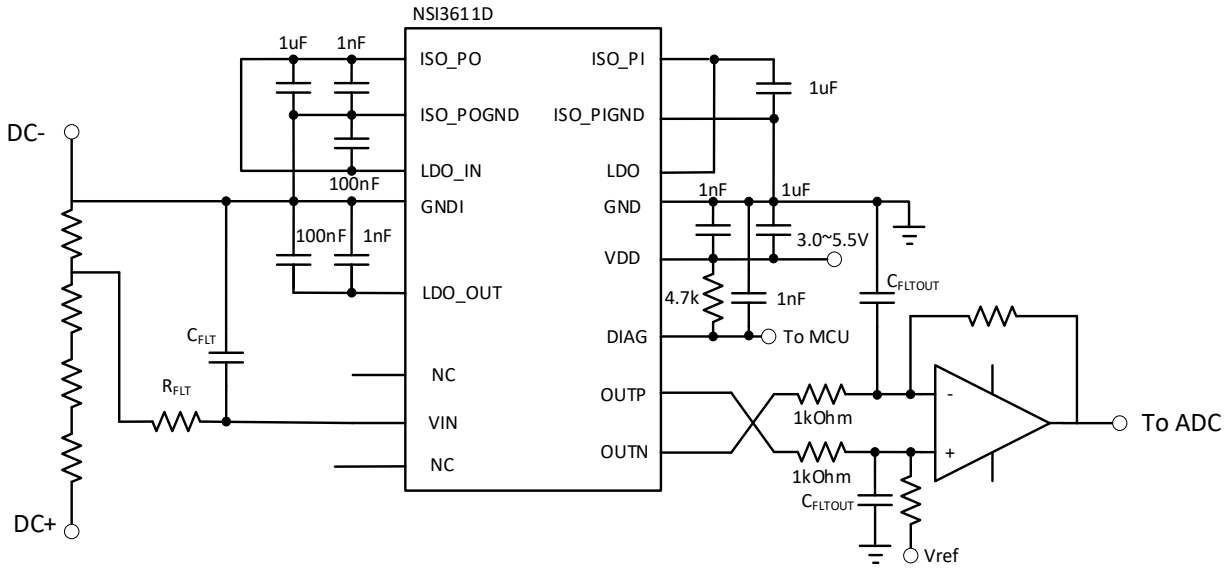


Figure 9.1 Typical application circuit

9.2. High Voltage Dividing Resistor Selection

Two restrictions should be considered when choosing the proper value of the voltage-dividing resistors:

- The current through the resistor should be within its rated range. Using Ohm law to calculate the cross current (Icross = Vmax/Rtotal);
- The divided input voltage value should not exceed the linear input range of NSI3611D, in which case the output may be clipped.

9.3. How to design input conditioning circuit

The high voltage in system is divided by a resistance network, and the divided voltage is applied to the input of the NSI3611D through a RC filter to ensure best performance. The RC filter is shown as R_{FLT} and C_{FLT} in Figure 9.1. The characteristics of this filter are dictated by the input topology and sensing frequency of the ADC, customers can adjust the filter design by demand.

The cut-o frequency of the RC filter is as below:

$$f_C = \frac{1}{2\pi R_{FLT} C_{FLT}}$$

9.4. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- The filter and bypass capacitors of VDD, ISO_PO, ISO_PI and LDO_OUT pins should be placed as close as possible to the pins respectively. For multiple filter capacitors of the same pin, capacitors with smaller values should be placed closer to the pin to filter out high-frequency noise better. An additional 1~10μF capacitor may be used for the power supply pin VDD in noisy conditions.
- Kelvin rules is recommended for the connection between sense resistor to NSI3611D. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the sensing resistor close to the input and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI3611D. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.
- To suppress radiation on the power lines, place Ferrite Beads respectively in series with the line of VDD and GND for filter. The ferrite Beads, together with decoupling capacitors, can filter and isolate noise well. In the layout area, the ferrite beads need to effectively separate the chip layout area from peripheral circuit without overlap in different PCB layers. Ferrite Beads can also be added in series with the differential input to suppress radiation on the input signal lines.

- Keep the trace lengths of the wiring as short as possible and don't place a ground plane in the high-voltage domain, which minimizes the antenna on this node to minimize radiated emissions.

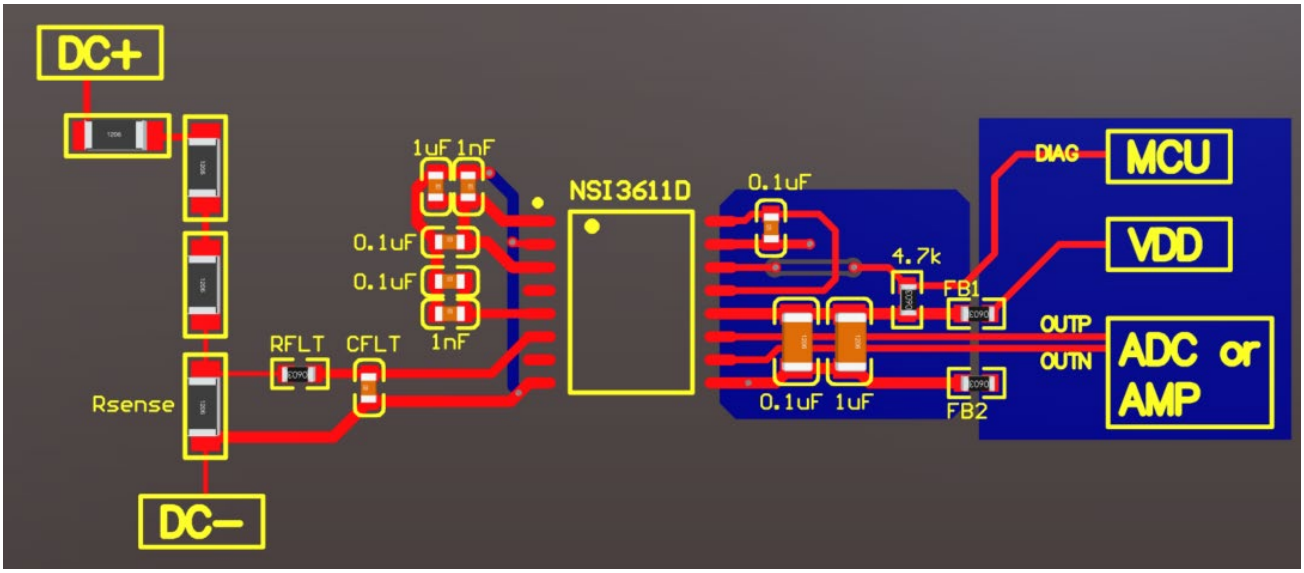
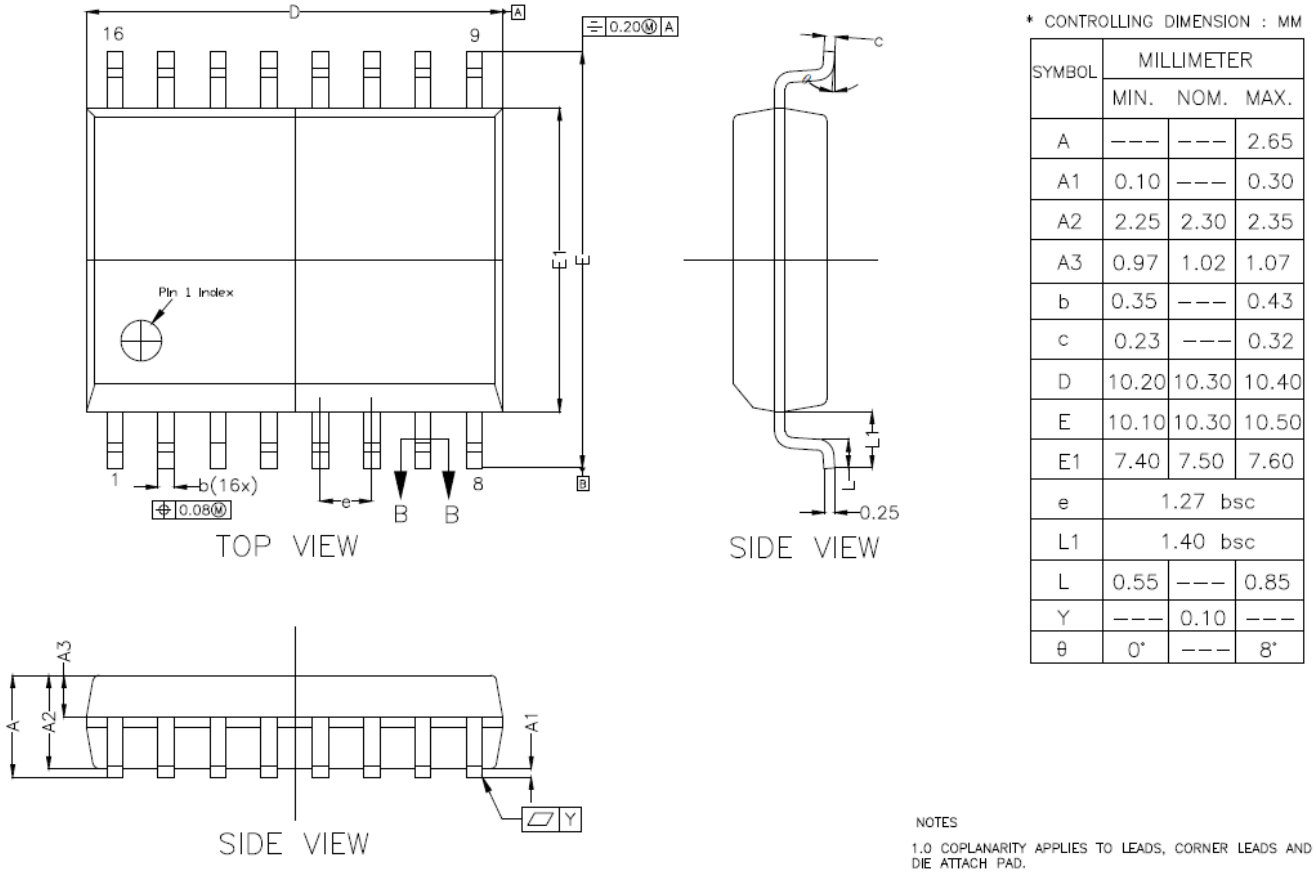


Figure 9.2 PCB layout example of NSI3611D

10. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOW16 package shape and dimension in millimeters

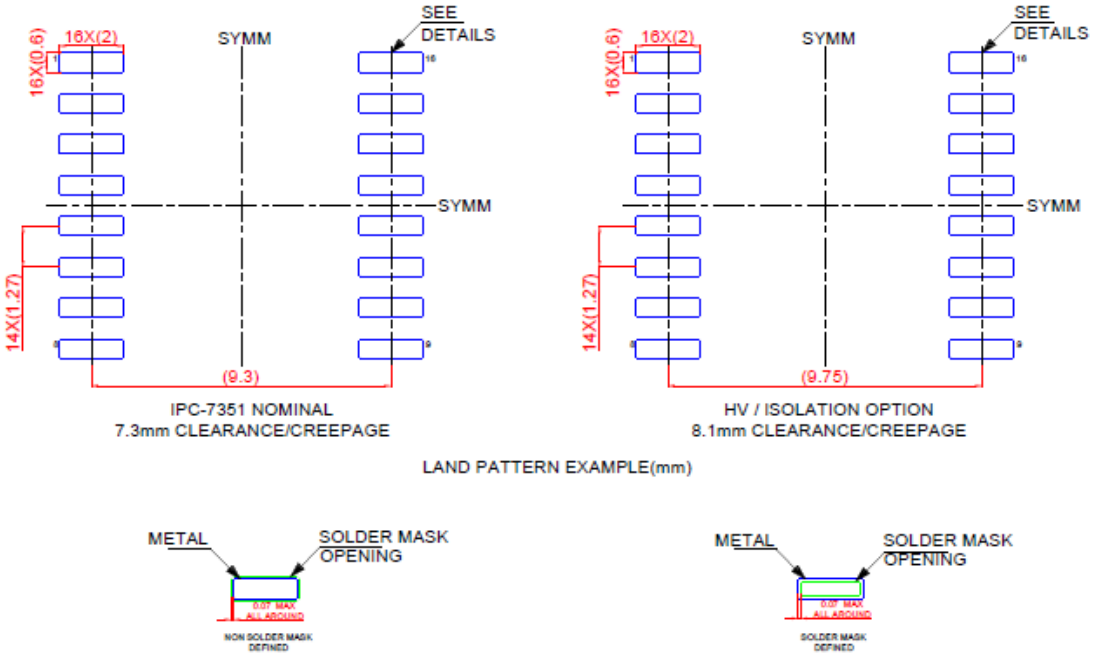


Figure 10.2 SOW16 Package Board Layout Example

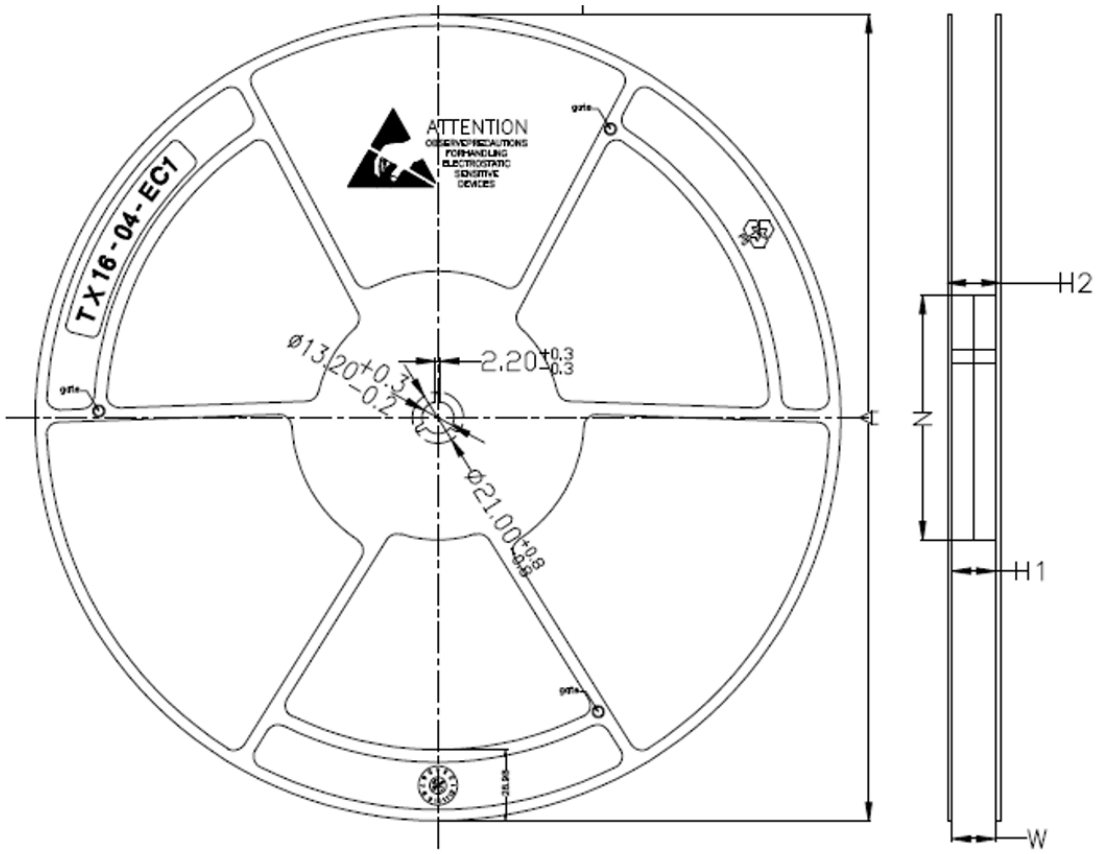
11. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(V)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SPQ
NSI3611D -DSWR	5	0 ~ 2	Level-3	-40 to 125°C	NO	SOP16 (300mil)	SOW16	1500

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI3611D	Click here	Click here	Click here	Click here

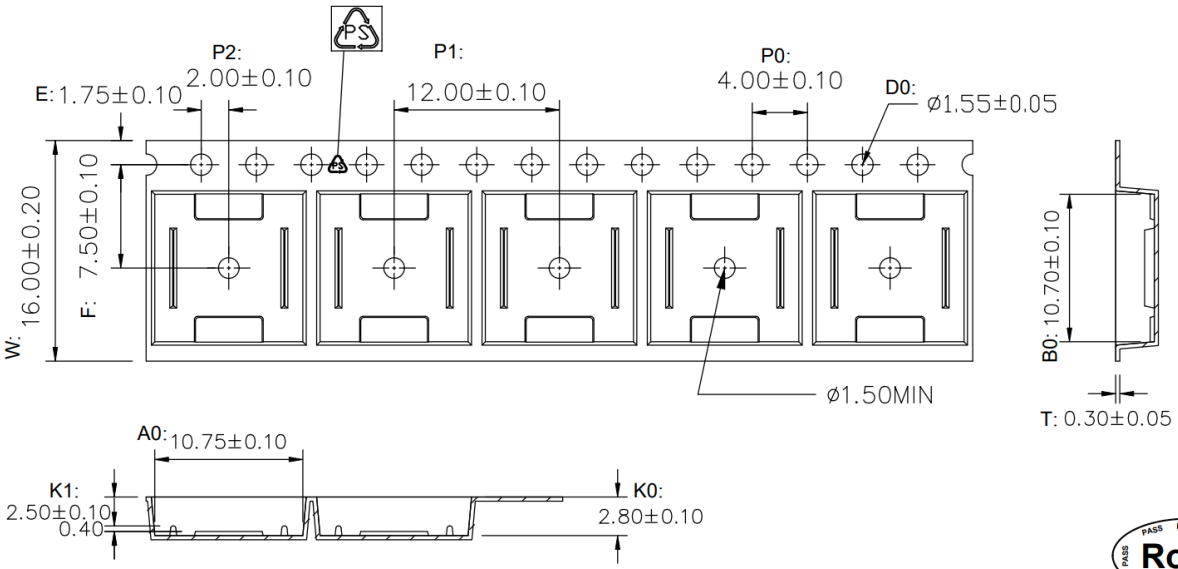
13. Tape and Reel Information



PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA +2 −2	øN +2 −2	H1 +2 −0	H2 +1 −1	W +3.5 −0.2
16MM	330	100	16.4	20.6	16.4

NOTES:
1. MATERIAL: DISSIPATIVE(BLACK)
2. FLANGE WARPAGE: 3 MM MAXIMUM
3. ALL DIMENSIONS ARE IN MM
4. ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5. GENERAL TOLERANCE: ±0.25 MM

Figure 13.1 Reel Information



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :10^{5} ~ 10^{10} Ω/□

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

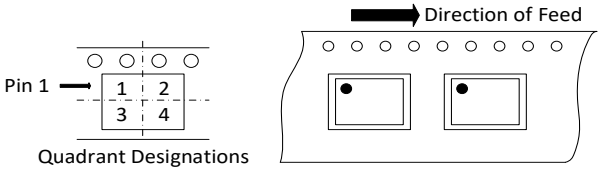


Figure 13.2 Tape Information of SOP16(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Version.	2025/11/7

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