

Product Overview

The NSI1611D0x-Q1 is a high-performance isolated amplifier with output separated from input based on NOVOSENSE capacitive isolation technology, which provides the amplifier with exceptional resistance to magnetic interference.

The device accepts an input range from -0.1V to 4V (-0.1V to 2V for NSI1611D02-Q1) and provides a differential output with the fixed gain of 0.5 (1 for NSI1611D02-Q1). The NSI1611D0x-Q1 features high input impedance, making it an ideal choice for applications where large resistive dividers are used or when connecting any high-impedance voltage signal source to the input.

The low offset and gain drift ensure the accuracy over the entire temperature range. The high common-mode transient immunity ensures that the device is reliable even in the presence of high-power switching such as in motor control applications.

The fail-safe function (missing VDD1 detection) simplifies system-level design and diagnostics.

Key Features

- Up to 5700V_{rms} Insulation voltage
- linear Input Voltage Range:
 - NSI1611D02-Q1: -0.1V to 2V
 - NSI1611D04-Q1: -0.1V to 4V
- Low Offset Error and Drift:
 - NSI1611D02-Q1: $\pm 0.8\text{mV}$ (Max), $\pm 20\mu\text{V}/^\circ\text{C}$ (Max)
 - NSI1611D04-Q1: $\pm 1.5\text{mV}$ (Max), $\pm 40\mu\text{V}/^\circ\text{C}$ (Max)
- Low Gain Error and Drift:
 - $\pm 0.25\%$ (Max), $\pm 45\text{ppm}/^\circ\text{C}$ (Max)
- Low Nonlinearity and Drift:
 - $\pm 0.04\%$ (Max), $\pm 1\text{ppm}/^\circ\text{C}$ (Typ)
- SNR: 82dB (Typ, BW = 10kHz), 71dB (Typ, BW = 100kHz)
- Wide bandwidth: 330kHz (Typ)
- High CMTI: 150kV/ μs (Typ)
- System-Level Diagnostic Features: input side power supply detection

- Operation Temperature: $-40^\circ\text{C} \sim 125^\circ\text{C}$
- AEC-Q100 Qualified for Automotive Applications: Grade 1
- RoHS-Compliant Packages: SOP8(300mil)

Safety Regulatory Approvals

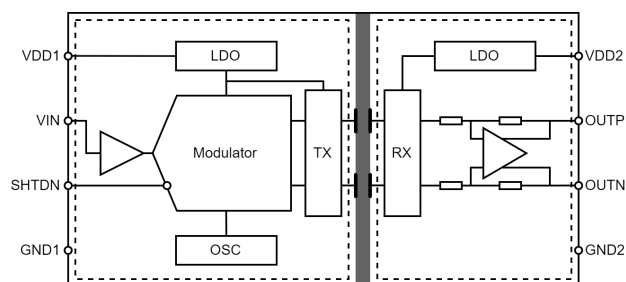
- UL recognition: 5700V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

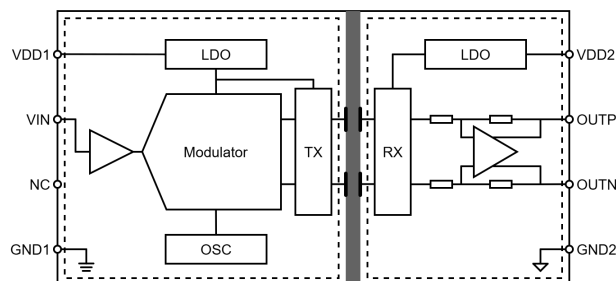
- Traction Inverters
- Onboard Chargers
- DC/DC inverters
- Battery Management Units

Device Information

Part Number	Package	Body Size
NSI1611D02-Q1SWVR	SOP8 (300mil)	5.85mm × 7.50mm
NSI1611D04-Q1SWVR	SOP8 (300mil)	5.85mm × 7.50mm



NSI1611D02-Q1



NSI1611D04-Q1

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1. Pin Configuration and Functions

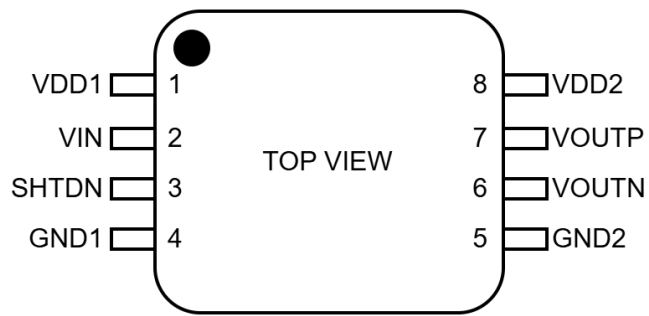


Figure 1.1 NSI1611D02-Q1 Package

Table 1.1 NSI1611D02-Q1 Pin Configuration and Description

NSI1611D02-Q1 PIN NO.	SYMBOL	FUNCTION
1	VDD1	Input side power supply
2	VIN	Single ended analog input
3	SHTDN	Shutdown input, active high, pulled up internally(100kΩ typ), recommended to connect to GND1 if shutdown mode is not needed
4	GND1	Input side ground
5	GND2	Output side ground
6	VOUTN	Negative output of differential output
7	VOUTP	Positive output of differential output
8	VDD2	Output side power supply

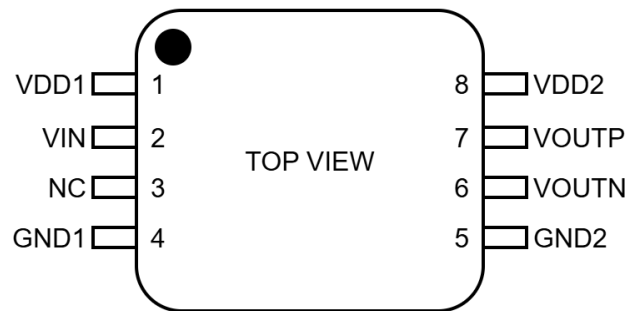


Figure 1.2 NSI1611D04-Q1 Package

Table 1.1 NSI1611D04-Q1 Pin Configuration and Description

NSI1611D04-Q1 PIN NO.	SYMBOL	FUNCTION
1	VDD1	Input side power supply
2	VIN	Single ended analog input
3	NC	Not internally connected, tied to GND1 recommended
4	GND1	Input side ground
5	GND2	Output side ground
6	VOUTN	Negative output of differential output
7	VOUTP	Positive output of differential output
8	VDD2	Output side power supply

2. Absolute Maximum Ratings⁽¹⁾

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDDx to GNDx	-0.3		6.5	V
Analog Input Voltage	V _{IN}	GND-0.5		VDD1+0.5	V
Digital Input Voltage	SHTDN ⁽²⁾	GND-0.5		VDD1+0.5	V
Analog Output Voltage	OUTP, OUTN	GND-0.5		VDD2+0.5	V
Input current per IO Pin	I _{IN}	-10		10	mA
Junction Temperature	T _J	-40		150	°C
Storage Temperature	T _{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

(2) Only for NSI1611D02-Q1

3. ESD Ratings ⁽¹⁾

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD	±2.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB	±1.0	kV

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation or damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
NSI1611D02-Q1					
Power supply voltage	VDD1 to GND1	3.0	5	5.5	V
	VDD2 to GND2	3.0	3.3	5.5	V
Maximum input voltage before clipping output	V _{Clipping}		2.15		V
Linear input full scale voltage	V _{FSR} ⁽¹⁾	-0.1		2	V
Digital Input Voltage	SHTDN	GND1		VDD1	V
Operating ambient temperature	T _A	-40		125	°C
NSI1611D04-Q1					
Power supply voltage	VDD1 to GND1	4.5	5	5.5	V
	VDD2 to GND2	3.0	3.3	5.5	V
Maximum input voltage before clipping output	V _{Clipping}		4.3		V

<i>Parameters</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
Linear input full scale voltage	$V_{FSR}^{(1)}$	-0.1		4	V
Operating ambient temperature	T_A	-40		125	°C

(1) Though the device has the ability to output voltage down to -0.1V, all accuracy related specifications are tested and guaranteed within the range of 0~2V for NSI1611D02-Q1 or 0~4V for NSI1611D04-Q1.

5. Thermal Information

<i>Parameters</i>	<i>Symbol</i>	<i>SOP8(300mil)</i>	<i>Unit</i>
Junction-to-ambient thermal resistance	$R_{\theta JA}$	86	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	4	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	42	°C/W

6. Specifications

6.1. Electrical Characteristics of NSI1611D02-Q1

(Minimum and maximum specifications apply across the following conditions: VDD1 = 3.0 ~ 5.5V, VDD2 = 3.0 ~ 5.5V, INP = 0V to 2V, and SHTDN = 0V, T_A = -40°C to 125°C. Unless otherwise noted, Typical values are measured at VDD1 = 5V VDD2 = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Input side supply voltage	VDD1	3.0	5.0	5.5	V	
Input side supply current	IDD1		6.3	9	mA	SHTDN is low
			1		μA	SHTDN is high
Output side supply voltage	VDD2	3.0	3.3	5.5	V	
Output side supply current	IDD2		2.9	4	mA	SHTDN is low
VDD1 undervoltage detection threshold voltage	VDD1 _{UV}	2.6	2.7	2.8	V	VDD1 falling threshold
		2.3	2.4	2.5	V	VDD1 rising thershold
VDD2 undervoltage detection threshold voltage	VDD2 _{UV}	2.5	2.7	2.8	V	VDD2 falling threshold
		2.2	2.4	2.6	V	VDD2 rising thershold
Analog Input						
Input offset voltage	V _{OS}	-0.8	±0.3	0.8	mV	V _{IN} = GND1, at T _A = 25°C
Input offset drift ⁽¹⁾	TCV _{OS}	-20	1	20	μV/°C	
Single-ended input resistance ⁽⁴⁾	R _{IN}		1		GΩ	
Input capacitance ⁽⁵⁾	C _I		5		pF	Single-ended input capacitance, f _{IN} =250kHz
Input bias current ⁽⁴⁾	I _{IB}	-10	±2	10	nA	V _{IN} = GND1
Digital Input						
Shutdown input	V _{IH}	0.7*VDD1			V	
	V _{IL}			0.3*VDD1	V	
Analog Output						
Nominal Gain			1		V/V	
Gain error	E _G	-0.25	±0.05	0.25	%	at T _A = 25°C
Gain error thermal drift ⁽¹⁾	TCE _G	-45	±10	45	ppm/°C	
Nonlinearity		-0.04	±0.01	0.04	%	
Nonlinearity drift ⁽¹⁾			1		ppm/°C	
Total harmonic distortion ⁽³⁾	THD		-85		dB	V _{IN} = 0~2Vpp, f _{IN} = 10kHz, BW = 100kHz
Output noise			270		μV _{RMS}	V _{IN} = GNDI, BW = 100kHz

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Signal to noise ratio	SNR		82		dB	$V_{IN} = 0 \sim 2V_{pp}$, $f_{IN} = 1\text{kHz}$, $BW = 10\text{kHz}$
	SNR		71		dB	$V_{IN} = 0 \sim 2V_{pp}$, $f_{IN} = 10\text{kHz}$, $BW = 100\text{kHz}$
Common-mode output voltage	V_{CMout}	1.39	1.44	1.49	V	
Differential clipping output voltage	$V_{clipout}$		2.15		V	$V_{OUT} = (V_{OUTP} - V_{OUTN})$, $V_{IN} \geq V_{Clipping}$
Failsafe differential output voltage	$V_{FAILSAFE}$		-3	-2.5	V	
Output bandwidth ⁽⁴⁾	BW		330		kHz	
Power supply rejection ratio ⁽²⁾ of VDD1 ⁽⁴⁾	PSRR _{dc}		-90		dB	PSRR vs VDD1, from 3.0~5.5V at DC
	PSRR _{ac}		-80		dB	PSRR vs VDD1, 100mV and 10kHz ripple
Power supply rejection ratio ⁽²⁾ of VDD2 ⁽⁴⁾	PSRR _{dc}		-90		dB	PSRR vs VDD2, from 3.0~5.5V at DC
	PSRR _{ac}		-80		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance ⁽⁴⁾	R_{OUT}		0.2		Ω	
Output limit current ⁽⁴⁾	I_{lim}		± 14		mA	
Common-mode transient immunity ⁽⁴⁾	CMTI	100	150		kV/ μ s	Common-mode transient immunity
Timing						
Rising time of OUTP - OUTN ⁽⁴⁾	t_r		1.3		μ s	
Falling time of OUTP- OUTN ⁽⁴⁾	t_f		1.3		μ s	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.6	1.9	μ s	
Analog setting time ⁽⁴⁾	t_{AS}		50	100	μ s	VDD step to 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) The temperature drift is calculated within the whole temperature range (-40°C to 125°C).

(2) Input referred.

(3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).

(4) Not test covered, guaranteed by characterization.

(5) Not test covered, guaranteed by design.

6.2. Electrical Characteristics of NSI1611D04-Q1

(Minimum and maximum specifications apply across the following conditions: VDD1 = 4.5 ~ 5.5V, VDD2 = 3.0 ~ 5.5V, INP = 0V to 4V, T_A = -40°C to 125°C. Unless otherwise noted, Typical values are measured at VDD1 = 5V VDD2 = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Input side supply voltage	VDD1	4.5	5.0	5.5	V	
Input side supply current	IDD1		6.3	9	mA	
Output side supply voltage	VDD2	3.0	3.3	5.5	V	
Output side supply current	IDD2		2.8	4	mA	
VDD1 undervoltage detection threshold voltage	VDD1 _{UV}	3.8	4.0	4.2	V	VDD1 falling threshold
		3.7	3.8	3.9	V	VDD1 rising thershold
VDD2 undervoltage detection threshold voltage	VDD2 _{UV}	2.6	2.7	2.8	V	VDD2 falling threshold
		2.3	2.4	2.5	V	VDD2 rising thershold
Analog Input						
Input offset voltage	V _{OS}	-1.5	±0.3	1.5	mV	V _{IN} = GND1, at T _A = 25°C
Input offset drift ⁽¹⁾	TCV _{OS}	-40	1	40	μV/°C	
Single-ended input resistance ⁽⁴⁾	R _{IN}		1		GΩ	
Input capacitance ⁽⁵⁾	C _I		5		pF	Single-ended input capacitance, f _{IN} =250kHz
Input bias current ⁽⁴⁾	I _{IB}	-10	±2	10	nA	V _{IN} = GND1
Analog Output						
Nominal Gain			0.5		V/V	
Gain error	E _G	-0.25	±0.05	0.25	%	at T _A = 25°C
Gain error thermal drift ⁽¹⁾	TCE _G	-40	±10	40	ppm/°C	
Nonlinearity		-0.04	±0.01	0.04	%	
Nonlinearity drift ⁽¹⁾			1		ppm/°C	
Total harmonic distortion ⁽³⁾	THD		-85		dB	V _{IN} = 0~4Vpp, f _{IN} = 10kHz, BW = 100kHz
Output noise			270		μV _{RMS}	V _{IN} = GNDI, BW = 100kHz
Signal to noise ratio	SNR		82		dB	V _{IN} = 0~4Vpp, f _{IN} = 1kHz, BW = 10kHz
	SNR		71		dB	V _{IN} = 0~4Vpp, f _{IN} = 10kHz, BW = 100kHz
Common-mode output voltage	V _{CMout}	1.39	1.44	1.49	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Differential clipping output voltage	$V_{clipout}$		2.15		V	$V_{OUT} = (V_{OUTP} - V_{OUTN})$, $V_{IN} \geq V_{Clipping}$
Failsafe differential output voltage	$V_{FAILSAFE}$		-3	-2.5	V	
Output bandwidth ⁽⁴⁾	BW		330		kHz	
Power supply rejection ratio ⁽²⁾ of VDD1 ⁽⁴⁾	PSRR _{dc}		-90		dB	PSRR vs VDD1, from 3.0~5.5V at DC
	PSRR _{ac}		-80		dB	PSRR vs VDD1, 100mV and 10kHz ripple
Power supply rejection ratio ⁽²⁾ of VDD2 ⁽⁴⁾	PSRR _{dc}		-90		dB	PSRR vs VDD2, from 3.0~5.5V at DC
	PSRR _{ac}		-80		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance ⁽⁴⁾	R_{OUT}		0.2		Ω	
Output limit current ⁽⁴⁾	I_{lim}		± 14		mA	
Common-mode transient immunity ⁽⁴⁾	CMTI	100	150		kV/ μ s	Common-mode transient immunity
Timing						
Rising time of OUTP-OUTN ⁽⁴⁾	t_r		1.3		μ s	
Falling time of OUTP-OUTN ⁽⁴⁾	t_f		1.3		μ s	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.6	1.9	μ s	
Analog setting time ⁽⁴⁾	t_{AS}		50	100	μ s	VDD step to 5.0 V, to OUTP, OUTN valid, 0.1% settling

(1) The temperature drift is calculated within the whole temperature range (-40°C to 125°C).

(2) Input referred.

(3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).

(4) Not test covered, guaranteed by characterization.

(5) Not test covered, guaranteed by design.

6.3. Timing Diagrams

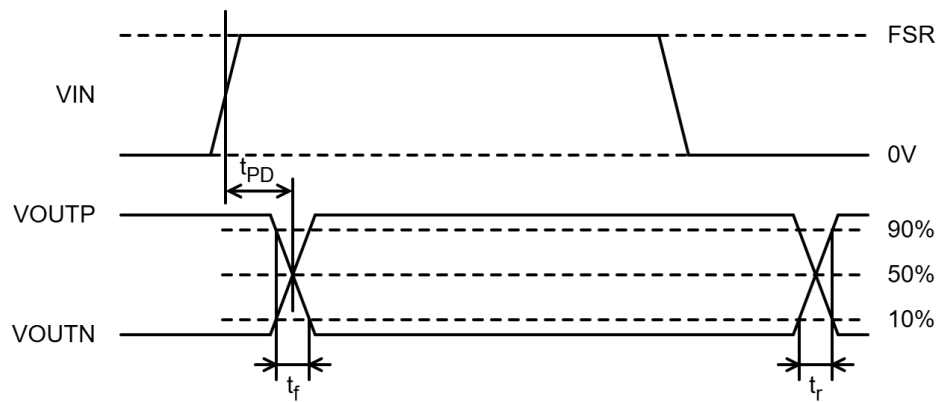


Figure 6.1 Propagation Delay and Output Fall Time Definition

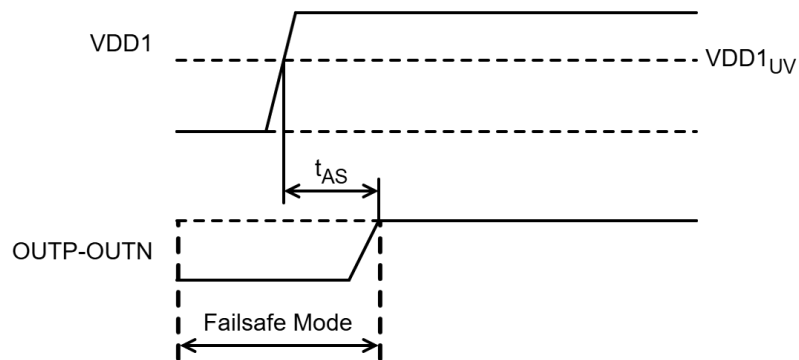


Figure 6.2 Analog Setting Time Definition ($V_{DD2} > V_{DD2_{UV}}$, $V_{IN} = 0$)

6.1. Typical Performance Characteristics of NSI1611D02-Q1

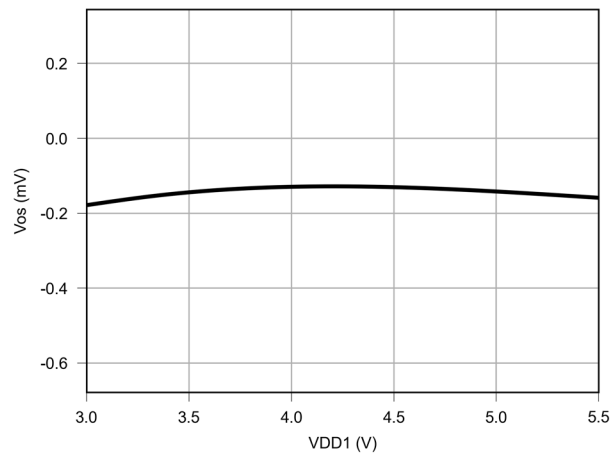


Figure 6.3 Input Offset Voltage vs High Side Supply Voltage

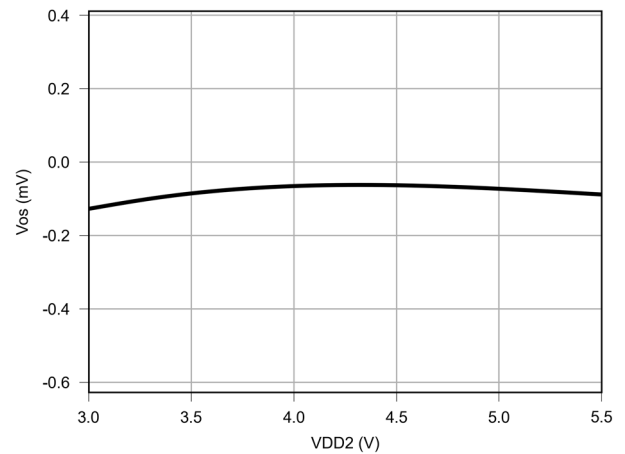


Figure 6.4 Input Offset Voltage vs Low Side Supply Voltage

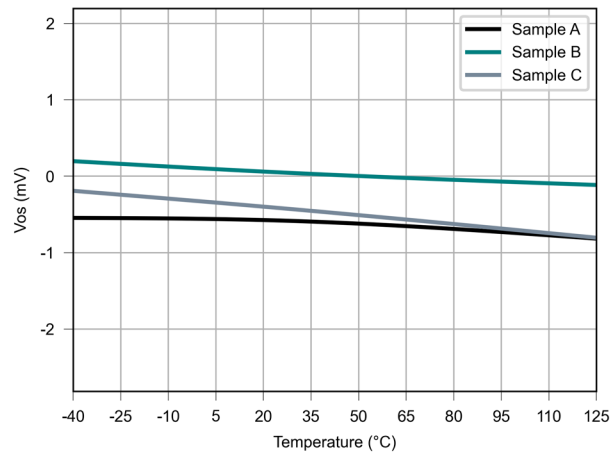


Figure 6.5 Input Offset Voltage vs Temperature

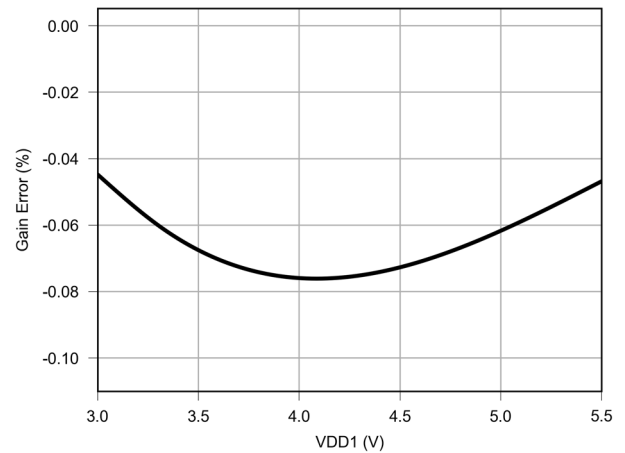


Figure 6.6 Gain Error vs High Side Supply Voltage

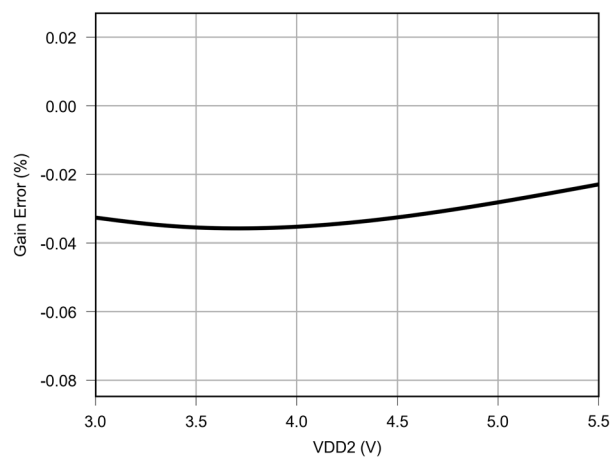


Figure 6.7 Gain Error vs Low Side Supply Voltage

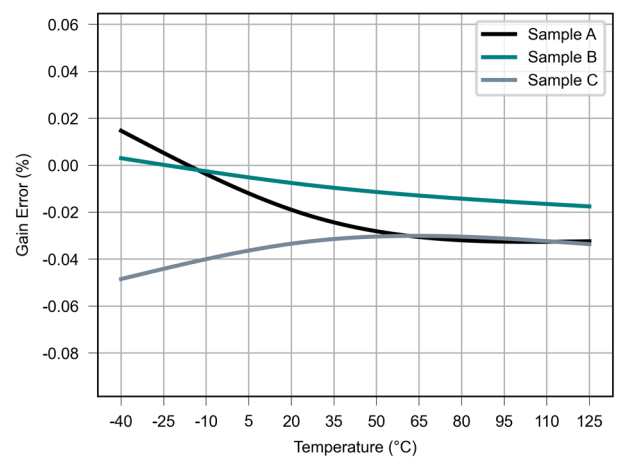


Figure 6.8 Gain Error vs Temperature

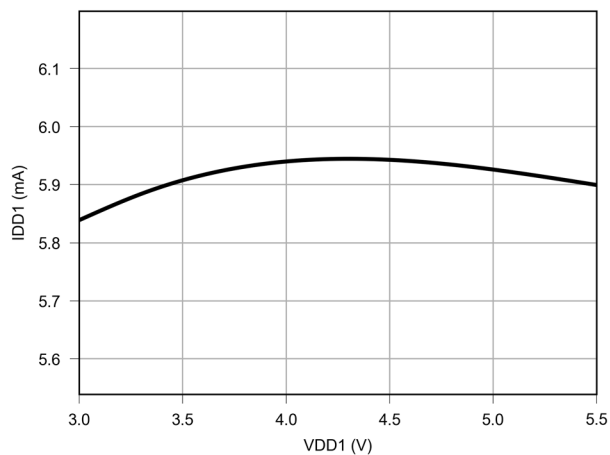


Figure 6.9 High Side Supply Current vs Supply Voltage

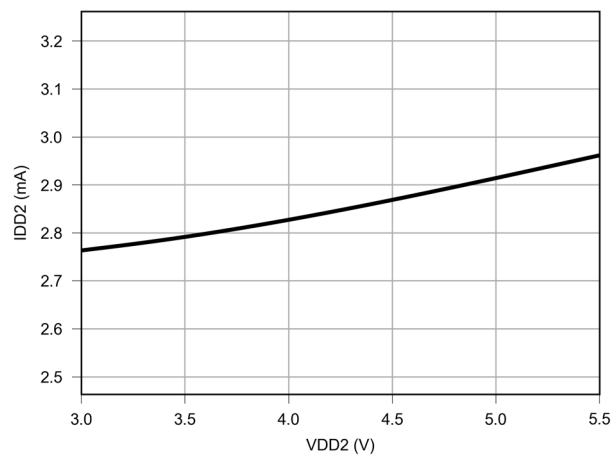


Figure 6.10 Low Side Supply Current vs Supply Voltage

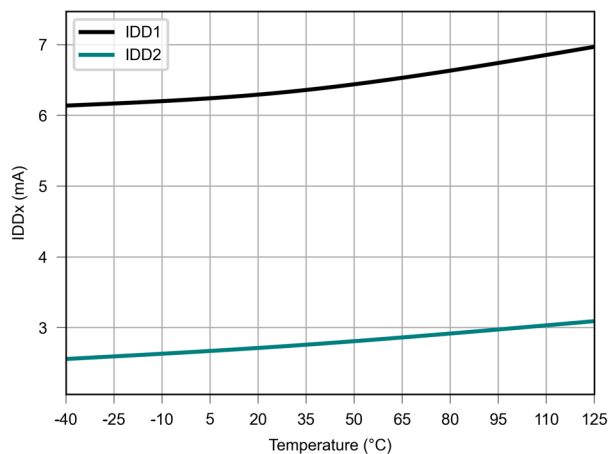


Figure 6.11 Supply Current vs Temperature

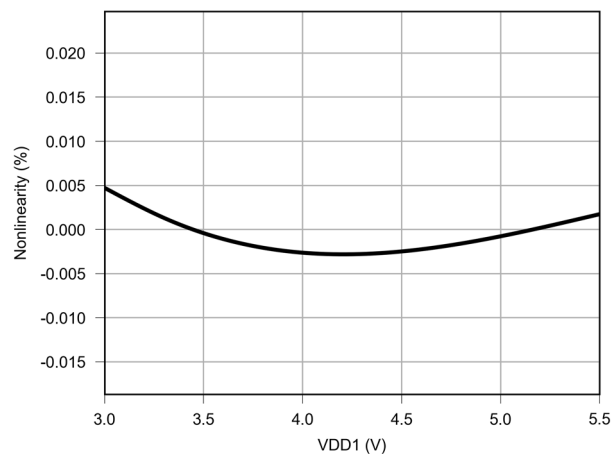


Figure 6.12 Nonlinearity vs High Side Input Voltage

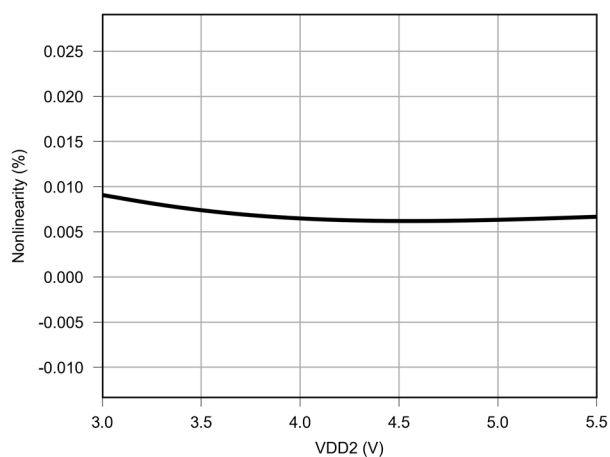


Figure 6.13 Nonlinearity vs Low Side Input Voltage

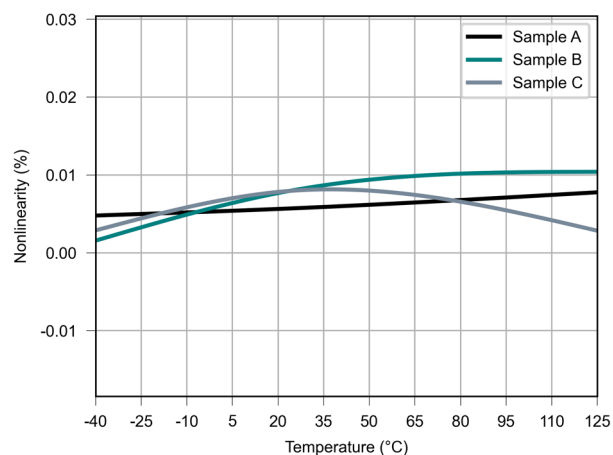


Figure 6.14 Nonlinearity vs Temperature

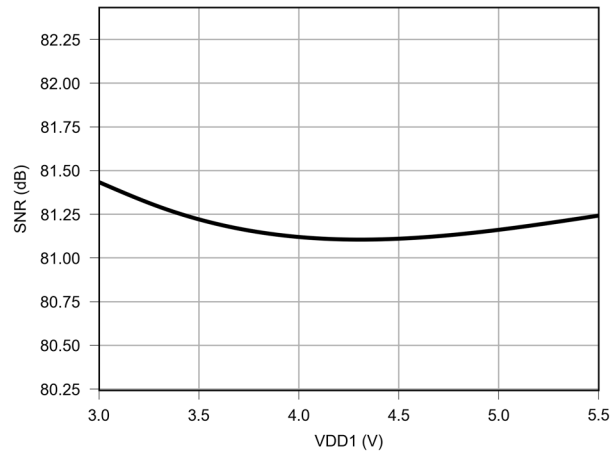


Figure 6.15 SNR vs High Side Supply Voltage

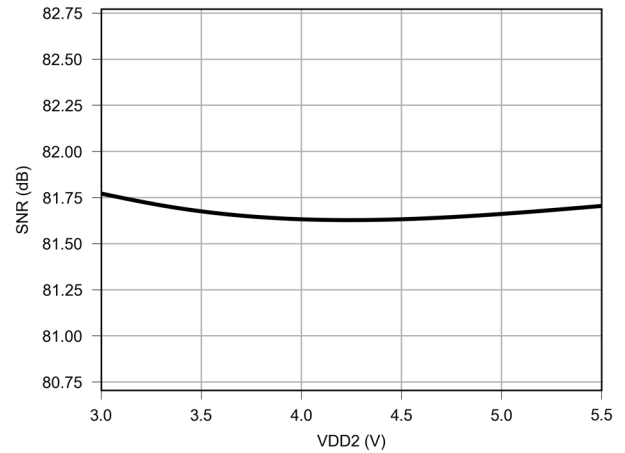


Figure 6.16 SNR vs Low Side Supply Voltage

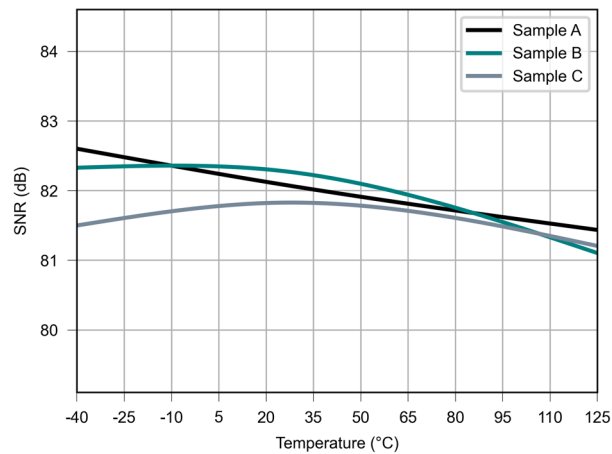


Figure 6.17 SNR vs Temperature

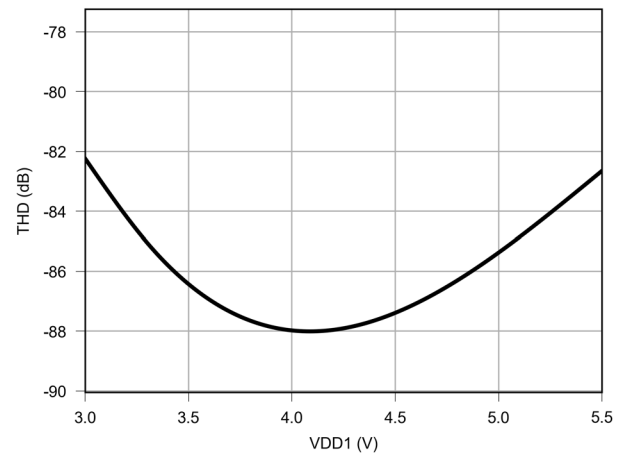


Figure 6.18 THD vs High Side Supply Voltage

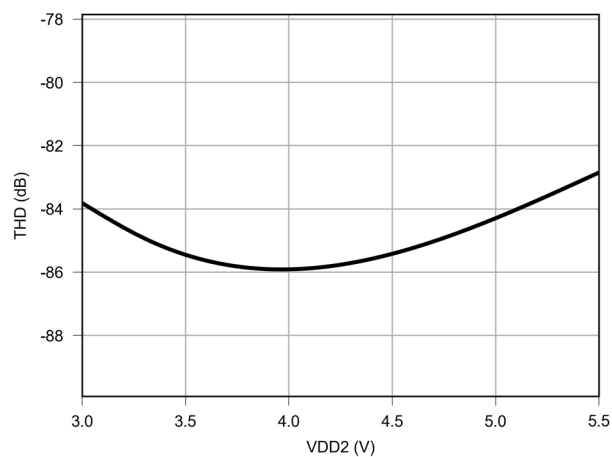


Figure 6.19 THD vs Low Side Supply Voltage

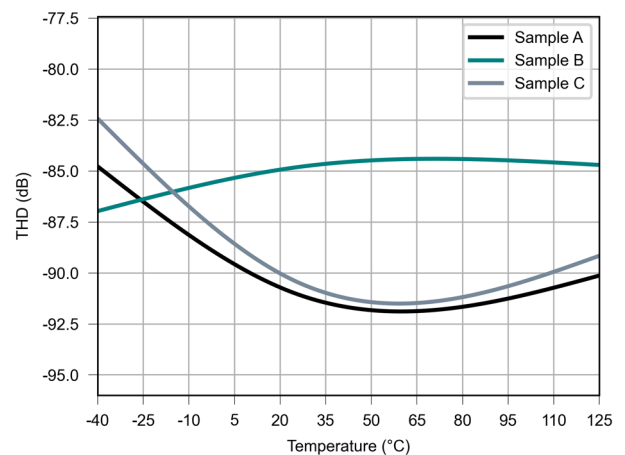


Figure 6.20 THD vs Temperature

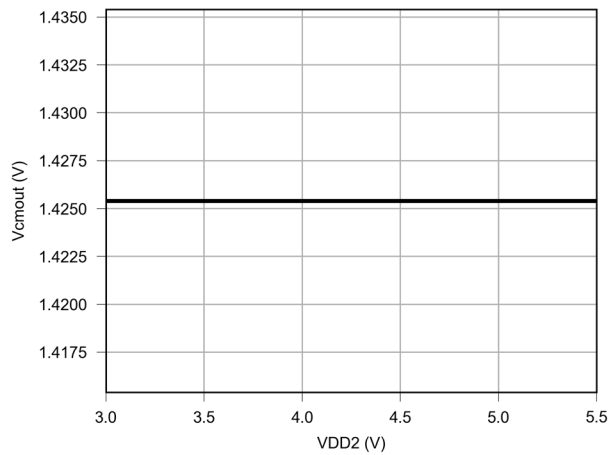


Figure 6.21 Output Common Voltage vs VDD2

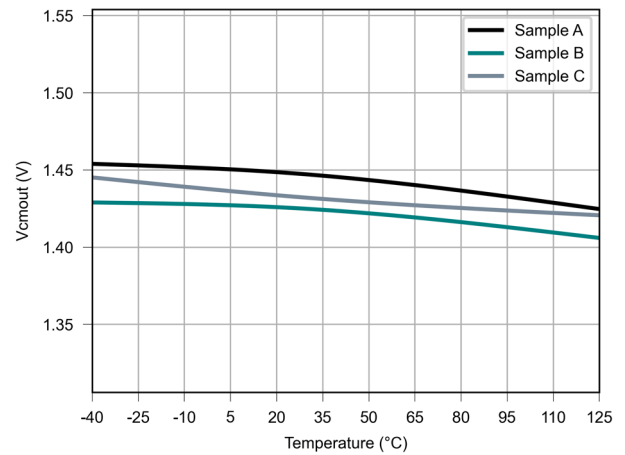


Figure 6.22 Output Common Voltage vs Temperature

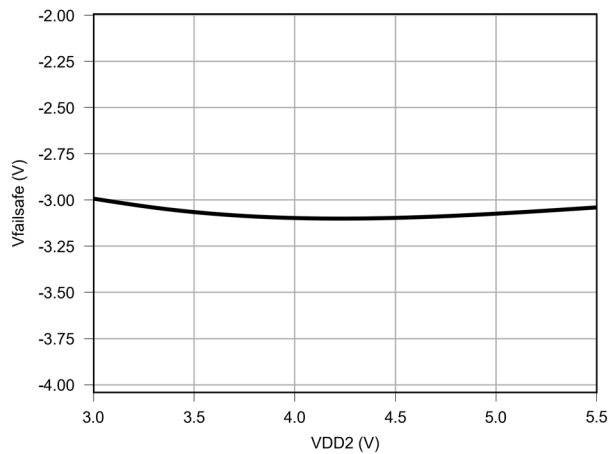


Figure 6.23 Fail-safe Output Voltage vs VDD2

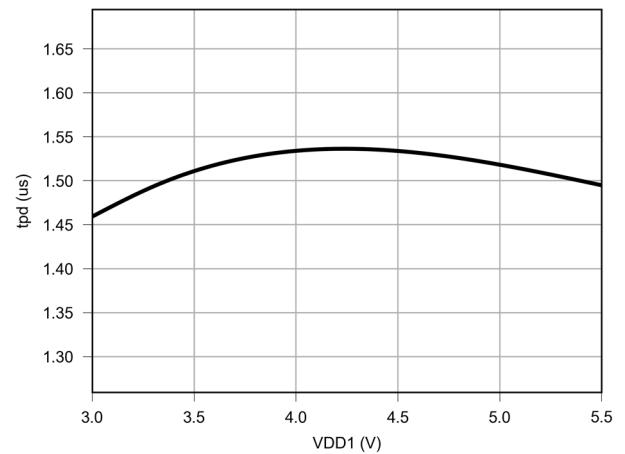


Figure 6.24 Propagation Delay vs VDD1

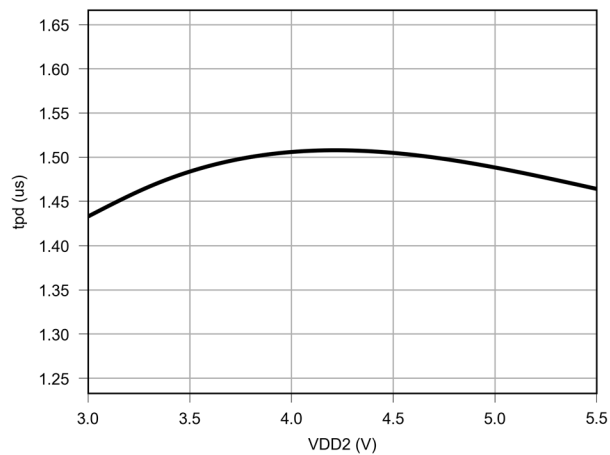


Figure 6.25 Propagation Delay vs VDD2

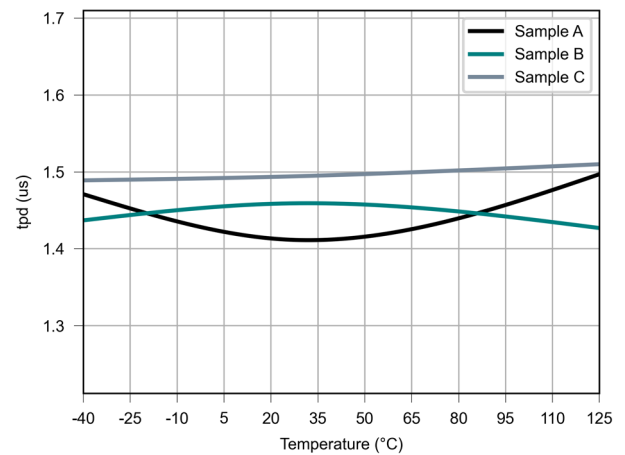


Figure 6.26 Propagation Delay vs Temperature

6.2. Typical Performance Characteristics of NSI1611D04-Q1

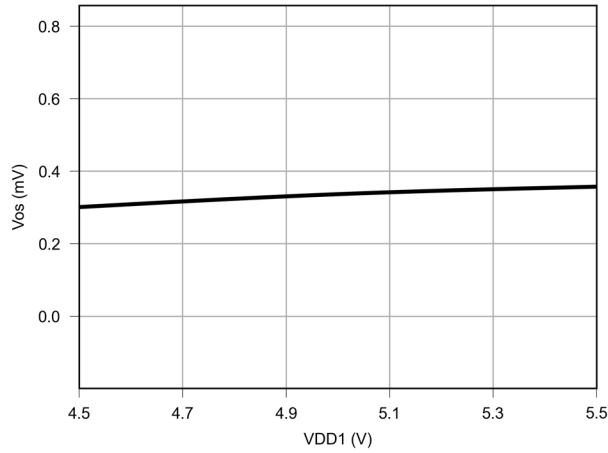


Figure 6.27 Input Offset Voltage vs High Side Supply Voltage

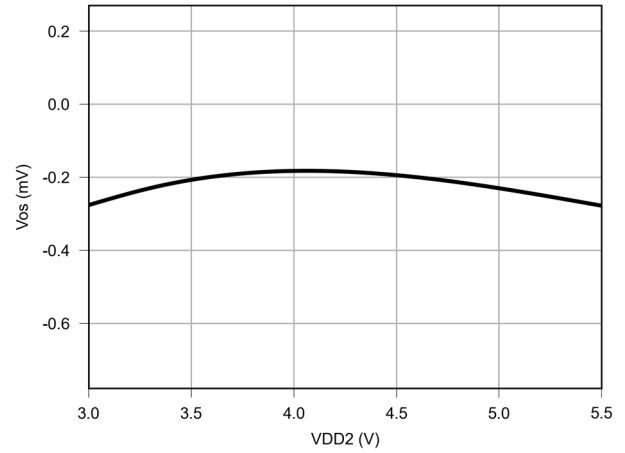


Figure 6.28 Input Offset Voltage vs Low Side Supply Voltage

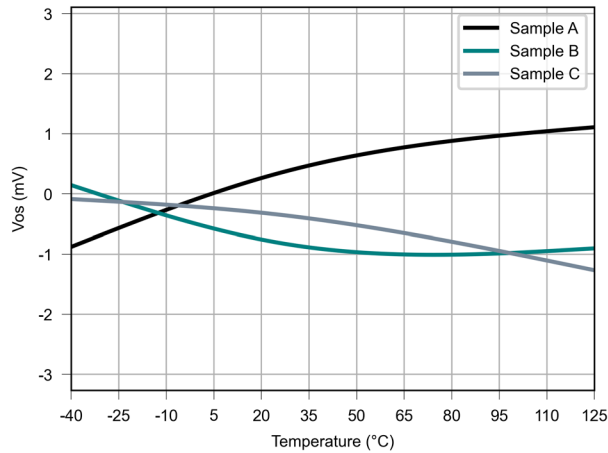


Figure 6.29 Input Offset Voltage vs Temperature

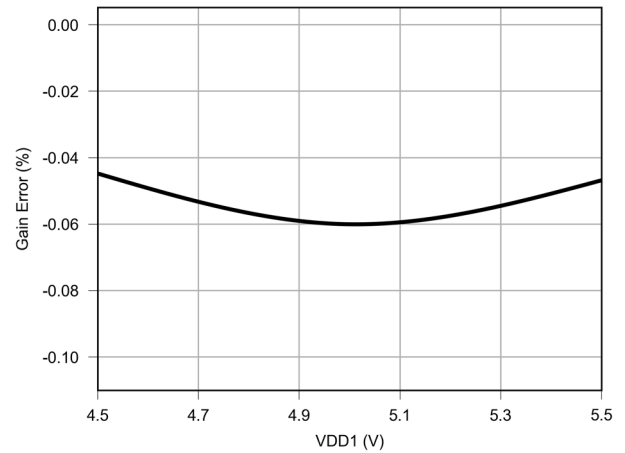


Figure 6.30 Gain Error vs High Side Supply Voltage

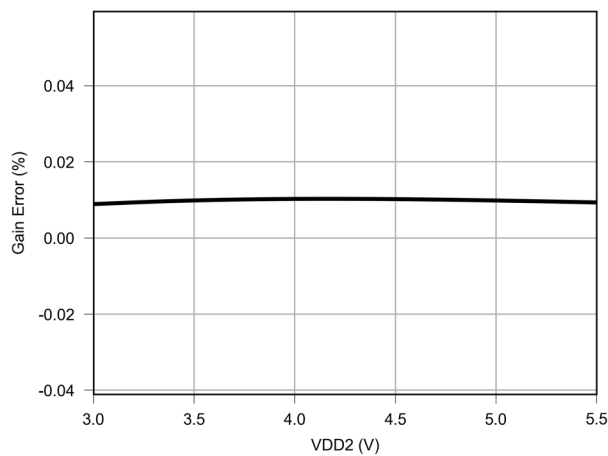


Figure 6.31 Gain Error vs Low Side Supply Voltage

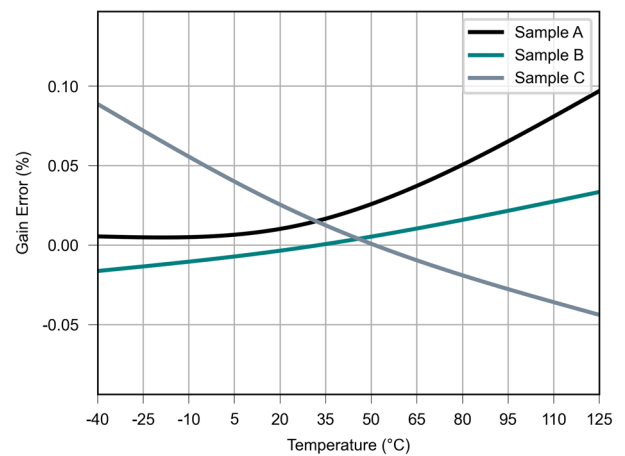


Figure 6.32 Gain Error vs Temperature

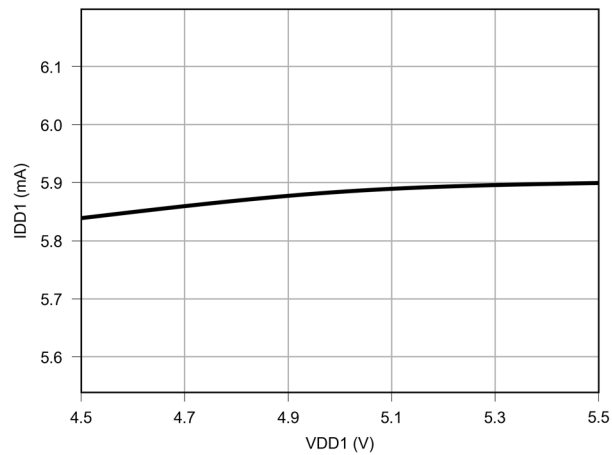


Figure 6.33 High Side Supply Current vs Supply Voltage

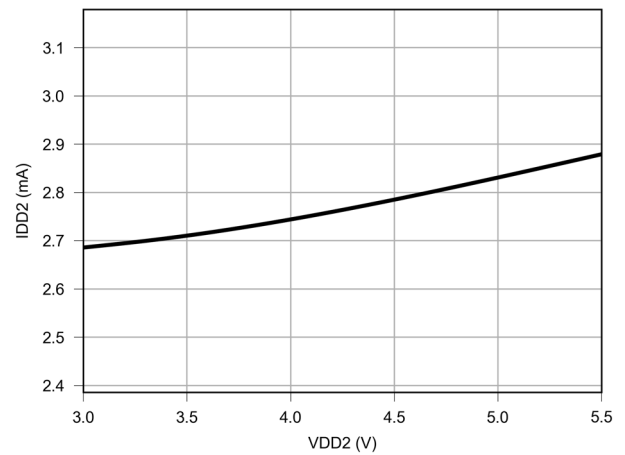


Figure 6.34 Low Side Supply Current vs Supply Voltage

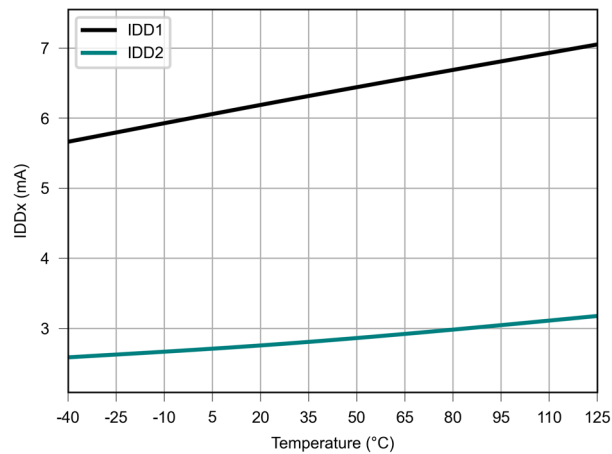


Figure 6.35 Supply Current vs Temperature

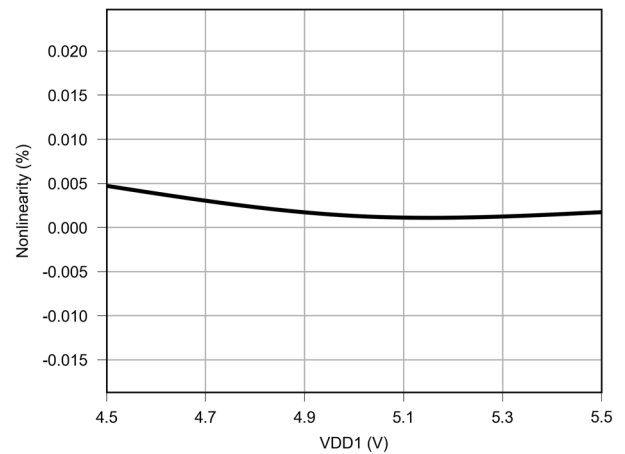


Figure 6.36 Nonlinearity vs High Side Input Voltage

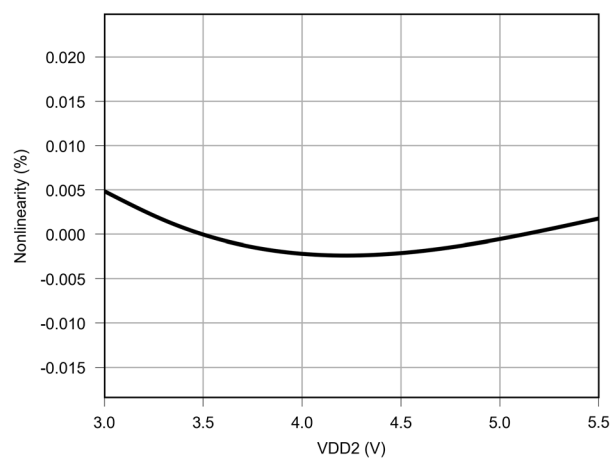


Figure 6.37 Nonlinearity vs Low Side Input Voltage

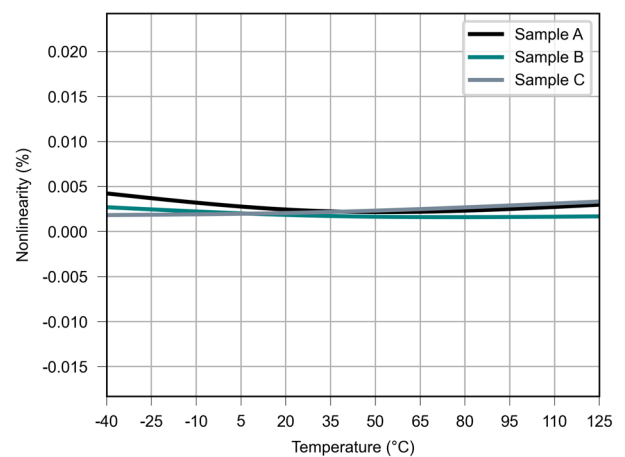


Figure 6.38 Nonlinearity vs Temperature

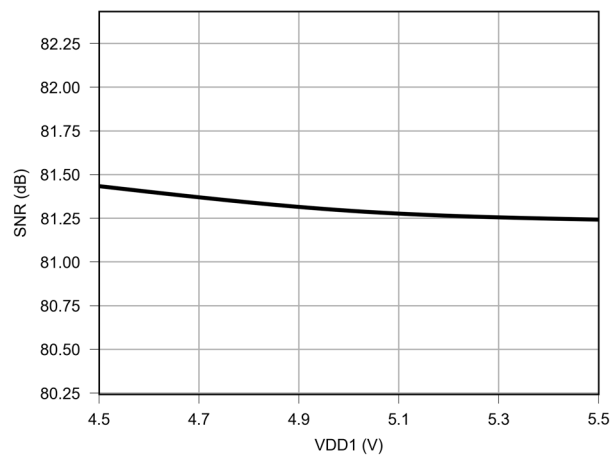


Figure 6.39 SNR vs High Side Supply Voltage

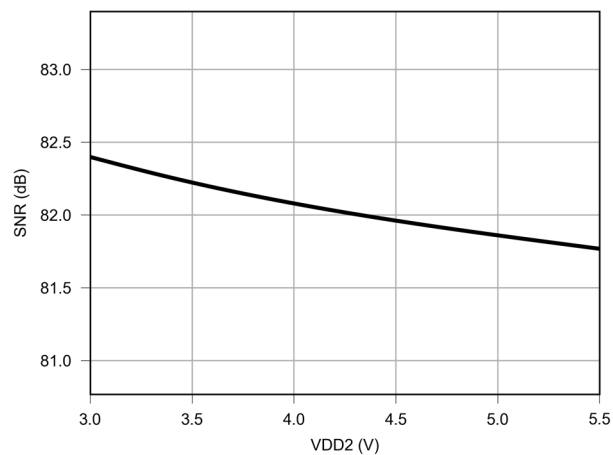


Figure 6.40 SNR vs Low Side Supply Voltage

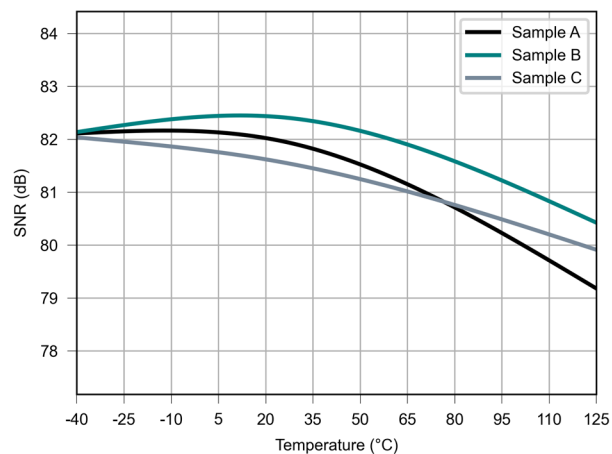


Figure 6.41 SNR vs Temperature

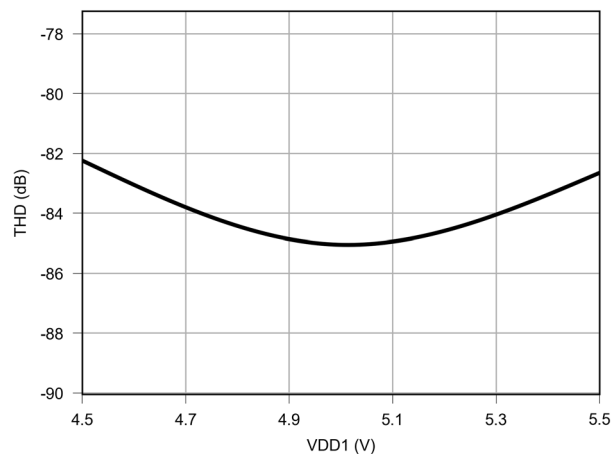


Figure 6.42 THD vs High Side Supply Voltage

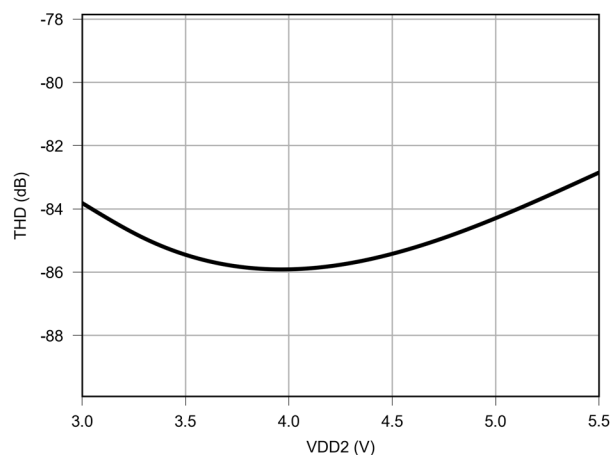


Figure 6.43 THD vs Low Side Supply Voltage

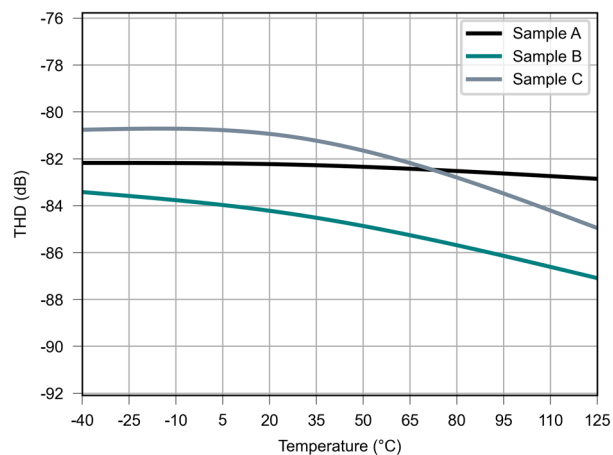


Figure 6.44 THD vs Temperature

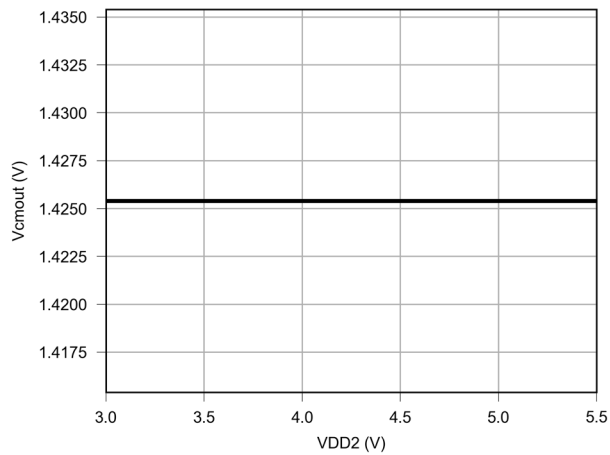


Figure 6.45 Output Common Voltage vs VDD2

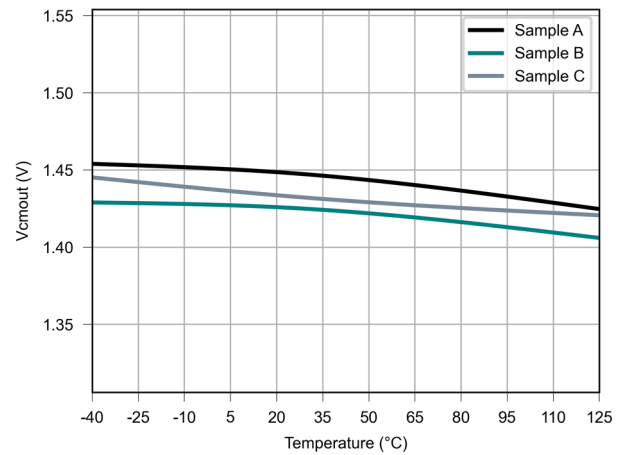


Figure 6.46 Output Common Voltage vs Temperature

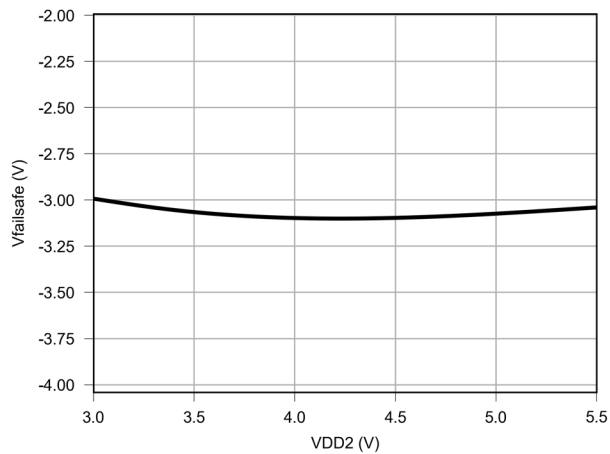


Figure 6.47 Fail-safe Output Voltage vs VDD2

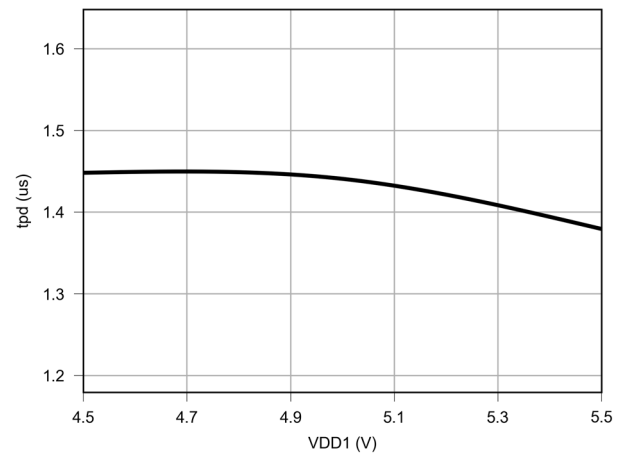


Figure 6.48 Propagation Delay vs VDD1

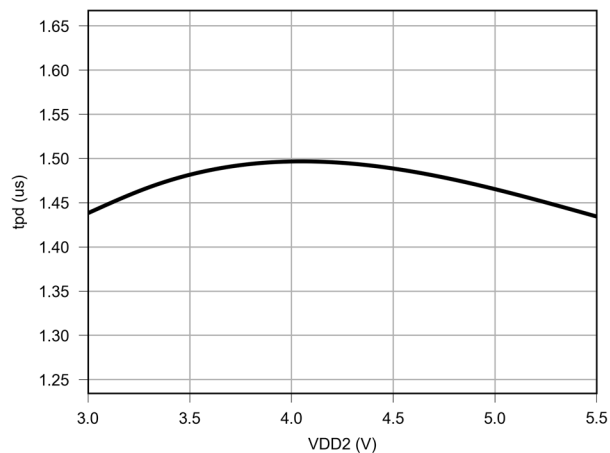


Figure 6.49 Propagation Delay vs VDD2

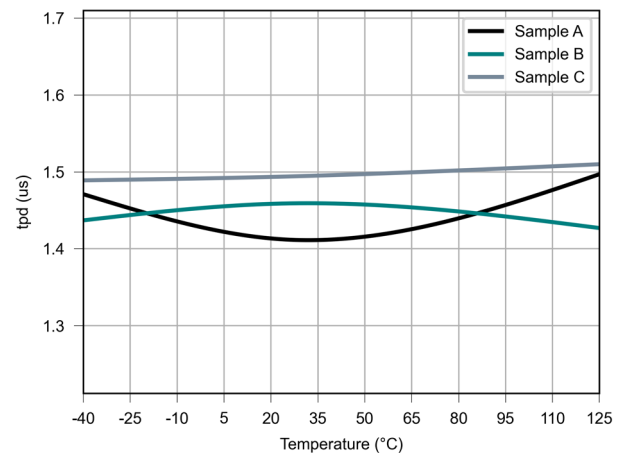


Figure 6.50 Propagation Delay vs Temperature

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Clearance	CLR	8.5	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8.5	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	18	μm	Distance through insulation (internal clearance – capacitive signal isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 150\text{Vrms}$	I to IV
	For Rated Mains Voltage $\leq 300\text{Vrms}$	I to IV
	For Rated Mains Voltage $\leq 600\text{Vrms}$	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	1500	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1060	V_{RMS}
	DC Voltage		1500	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{ s}$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{ s}$			pC
	Method b, $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{ s}$ $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Maximum transient isolation voltage	$t=60\text{ sec}$	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	7700	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}

Description	Test Condition	Symbol	Value	Unit
Isolation resistance	$V_{IO} = 500V, T_{amb} = 25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500V, 100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500V, T_{amb} = T_s$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	pF
Safety total power dissipation	$V_I = 5.5V, T_J = 150^{\circ}C, T_A = 25^{\circ}C$	P_s	1430	mW
Safety input, output, or supply current	$\theta_{JA} = 82^{\circ}C/W$ for SOW8, $V_I = 5.5V, T_J = 150^{\circ}C, T_A = 25^{\circ}C$	I_s	260	mA
Maximum safety temperature		T_s	150	$^{\circ}C$
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}, t = 60\text{ s (qualification)},$ $V_{TEST} = 1.2 \times V_{ISO}, t = 1\text{ s}$	V_{ISO}	5700	V_{RMS}

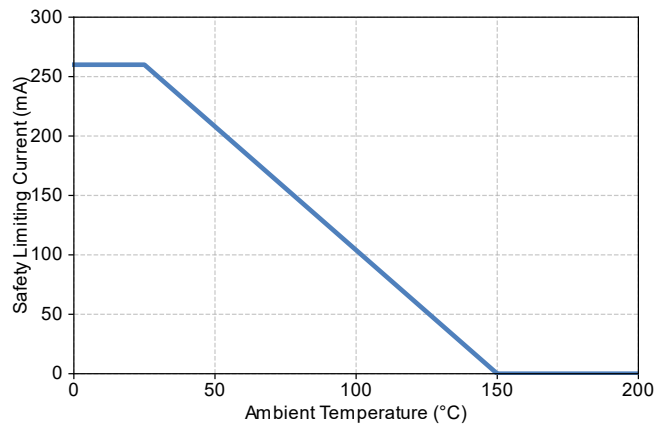


Figure 7.1 NSI1611D0x-Q1 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI1611D0x-Q1SWVR are approved or pending approval by the organizations listed in table.

UL		CQC		TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	Certified According to EN IEC 62368-1	DIN EN IEC 60747-17 (VDE 0884-17)
Single Protection, 5700V _{rms} Isolation voltage	Single Protection, 5700V _{rms} Isolation voltage	Reinforced insulation	5700V _{rms} for 1min	Reinforce Insulation $V_{IORM} = 1414\text{ V}_{PEAK}$ $V_{IOTM} = 8000\text{ V}_{PEAK}$ $V_{IOSM} = 10000\text{ V}_{PEAK}$
Pending	Pending	Pending	Pending	Pending

8. Function Description

8.1. Overview of NSI1611D02-Q1

The NSI1611D02-Q1 is a high-performance isolated amplifier with an input range of $-0.1\sim 2V$ and a differential output. The buffer at the input port ensures the input impedance is high enough for large resistive dividers input. Subsequently, the analog signal is modulated to a digital bitstream to transfer through the isolation barrier. Both the modulator and the isolator drivers (designated as TX in the functional block diagram) are clocked by the inside oscillator. The isolator receiver (designated as RX in the functional block diagram) receives the modulated waveform and restores it to an analog form. Finally, the analog output is driven by a fully differential amplifier.

The shutdown mode is activated when pin SHTDN is pulled high or left floating as it is internally pulled high. The output of the NSI1611D02-Q1 enters a failsafe mode to indicate the abnormal state of input side, which is described in detail in Section 8.5.

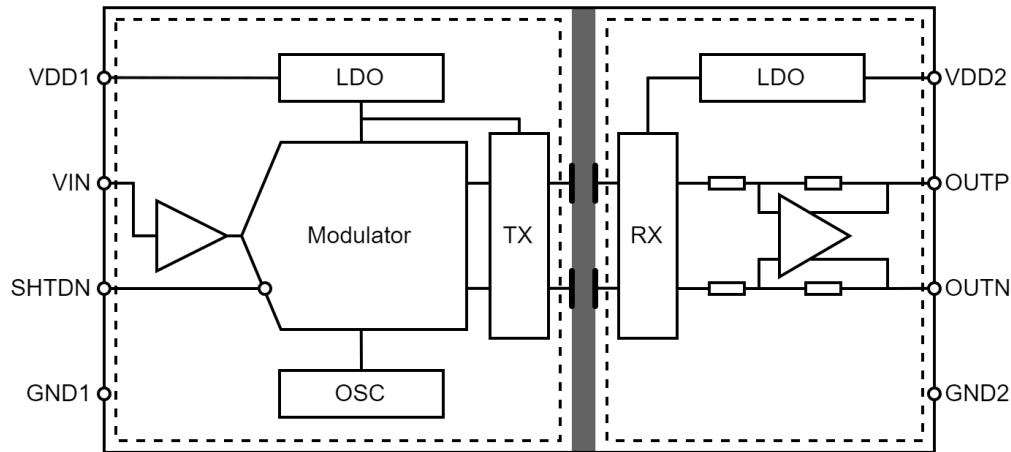


Figure 8.1 Function Block Diagram of NSI1611D02-Q1

8.2. Overview of NSI1611D04-Q1

The NSI1611D04-Q1 is a high-performance isolated amplifier with an input range of $-0.1\sim 4V$ and a differential output. The buffer at the input port ensures the input impedance is high enough for large resistive dividers input. Subsequently, the analog signal is modulated to a digital bitstream to transfer through the isolation barrier. Both the modulator and the isolator drivers (designated as TX in the functional block diagram) are clocked by the inside oscillator. The isolator receiver (designated as RX in the functional block diagram) receives the modulated waveform and restores it to an analog form. Finally, the analog output is driven by a fully differential amplifier.

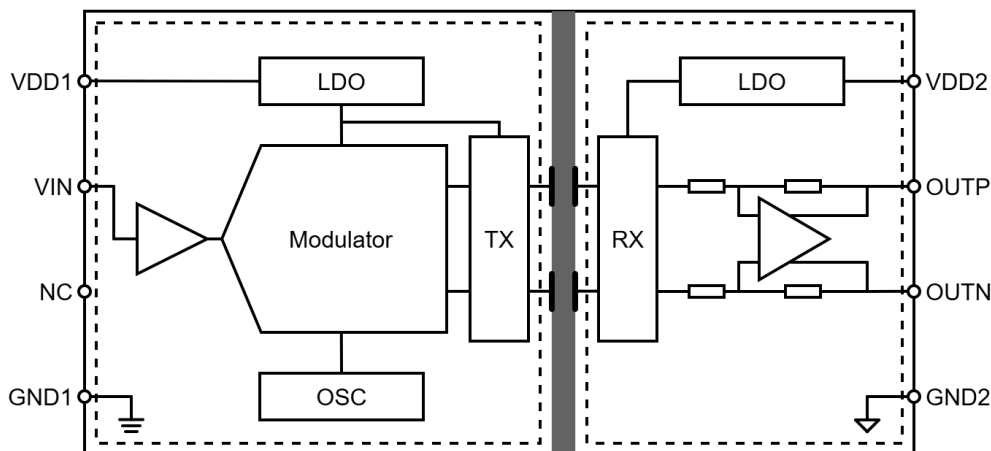


Figure 8.2 Function Block Diagram of NSI1611D04-Q1

8.3. Analog Input

There are two restrictions on the analog input signals V_{IN}

- If the input voltage exceeds the range from $GND1-6V$ to $VDD1+0.5V$, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (V_{FSR}), V_{FSR} is -0.1V to 2V for NSI1611D02-Q1 and -0.1V to 4V for NSI1611D04-Q1, specified in Recommended Operating Conditions section.

8.4. Analog Output

For linear input range, the analog output of NSI1611D02-Q1 has a fixed gain of 1, and NSI1611D04-Q1 has a fixed gain of 0.5. If an input signal exceeding the clipping input range is applied to the NSI1611D0x-Q1 ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically, 2.15V for positive clipping), as shown in Figure 8.3.

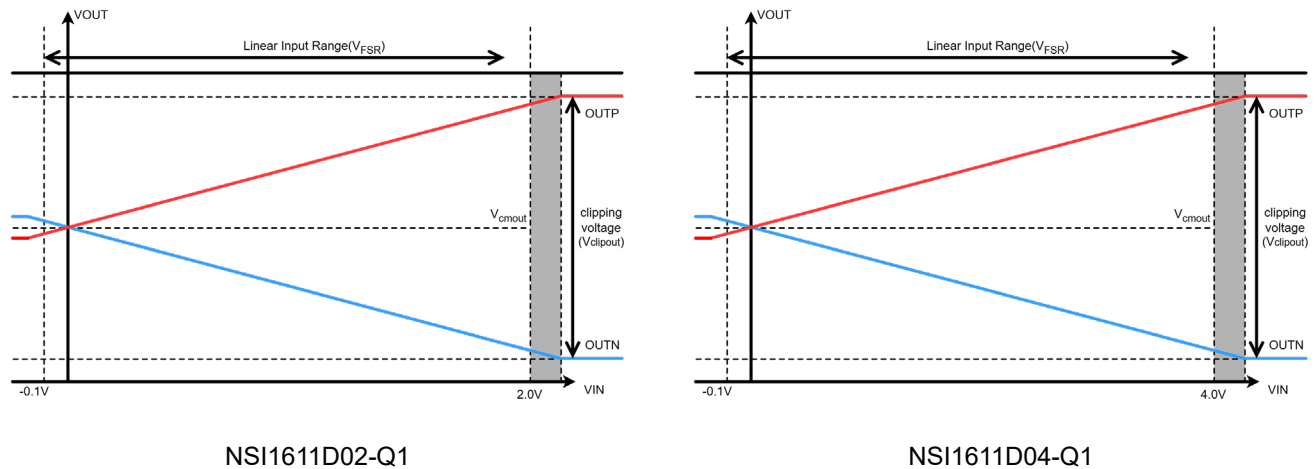


Figure 8.3 Output curve of NSI1611D0x-Q1

In addition, NSI1611D0x-Q1 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage shown in Figure, which does not occur under normal device operation and will only be activated in following conditions:

- When the high-side supply $VDD1$ is missing.
- When the undervoltage of high-side supply $VDD1$ is detected ($VDD1 < VDD1_{UV}$).
- When pin SHTDN is pulled high or left floating

8.5. Device Operating States

The NSI1611D0x-Q1 can operate in the following states:

- **Missing low-side power supply state:** This state is entered when the low-side supply ($VDD2$) drops below the $VDD2_{UV}$ threshold. In this state, the device is unresponsive, and the output (OUT) is in a high-impedance (Hi-Z) state.
- **Missing high-side power supply state:** When the low-side of the device ($VDD2$) is properly powered and within the recommended operating conditions, but the high-side power supply ($VDD1$) is below the $VDD1_{UV}$ threshold, the OUT pin is driven to GND2. The waveform of OUT refers to Figure 8.4 when $VDDx$ is missing.
- **Analog input overrange state:** With both $VDD1$ and $VDD2$ operating within the recommended conditions, if the analog input voltage (V_{IN}) exceeds the maximum clipping voltage ($V_{clipping_MAX}$), the device outputs $V_{clipping}$ at the OUT pin.
- **Normal operating state:** When $VDD1$, $VDD2$, and V_{IN} all fall within their respective recommended operating ranges, the device enters normal operation, and the output delivers a voltage proportional to the input voltage and $REFIN$ voltage according to Function⁽¹⁾

OPERATING STATES	VDD1	VDD2	V_{IN}	DESCRIPTION
Missing low-side power supply state	No effect	$VDD2 < VDD2_{UV}$	No effect	The outputs (OUTP and OUTN) are in high-impedance (Hi-Z) state.
Missing high-side power	$VDD1 < VDD1_{UV}$	Valid ⁽¹⁾	No effect	The OUT pin is driven to

supply state				GND2.
Analog input overrange state	Valid ⁽¹⁾	Valid ⁽¹⁾	$V_{IN} > V_{cliping}$	The device outputs $V_{clipout}$
Normal operating state	Valid ⁽¹⁾	Valid ⁽¹⁾	Valid ⁽¹⁾	The device outputs a voltage proportional to the input voltage.

(1) Valid denotes operation within the recommended operating conditions.

Figure 8.4 illustrates the operating states under different combination of power supply states.

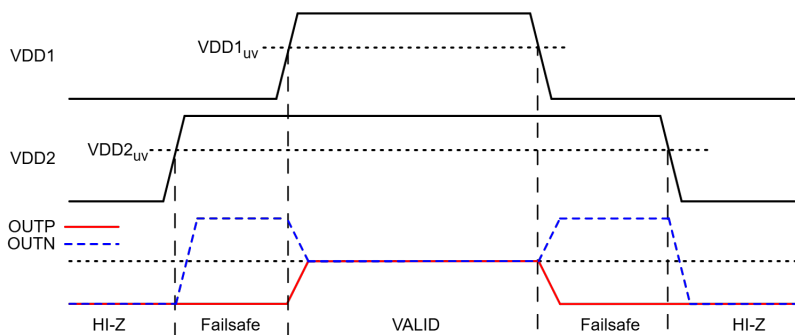


Figure 8.4 Typical Output When Input is 0V

9. Application Note

9.1. Typical Application Circuit of NSI1611D02-Q1

Figure 9.1 illustrates a typical application example of NSI1611D02-Q1. On the input side, the HV_BUS voltage is divided down to 0~2V level across the bottom resistor of a high-impedance resistive divider. VDD1 needs a power supply from 3.0V to 5.5V. A 0.1uF capacitor and a 10uF capacitor in parallel on VDD1 and VDD2 are highly recommended to improve EOS and stability. On the output side, NSI1611D02-Q1 provides differential output for ADC input.

The SHTDN pin should be directly connected to GND1 if shutdown mode is not needed.

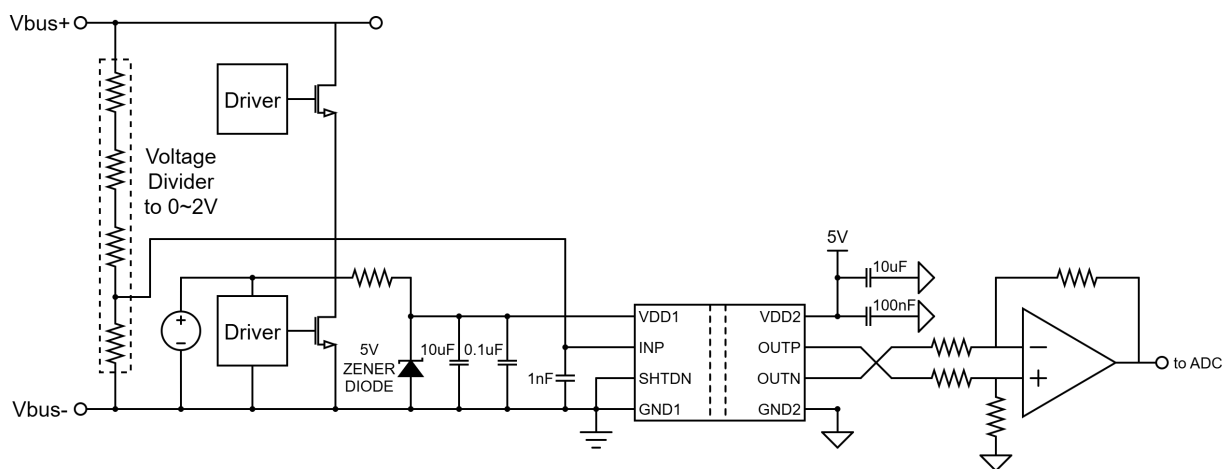


Figure 9.1 Typical Application Circuits of NSI1611D02-Q1

9.1. Typical Application Circuit of NSI1611D04-Q1

Figure 9.2 illustrates a typical application example of NSI1611D04-Q1. On the input side, the HV_BUS voltage is divided down to 0~4V level across the bottom resistor of a high-impedance resistive divider. VDD1 needs a power supply from 4.5V to 5.5V. A 0.1uF capacitor and a 10uF capacitor in parallel on VDD1 and VDD2 are highly recommended to improve EOS and stability. On the output side, NSI1611D04-Q1 provides differential output for ADC input.

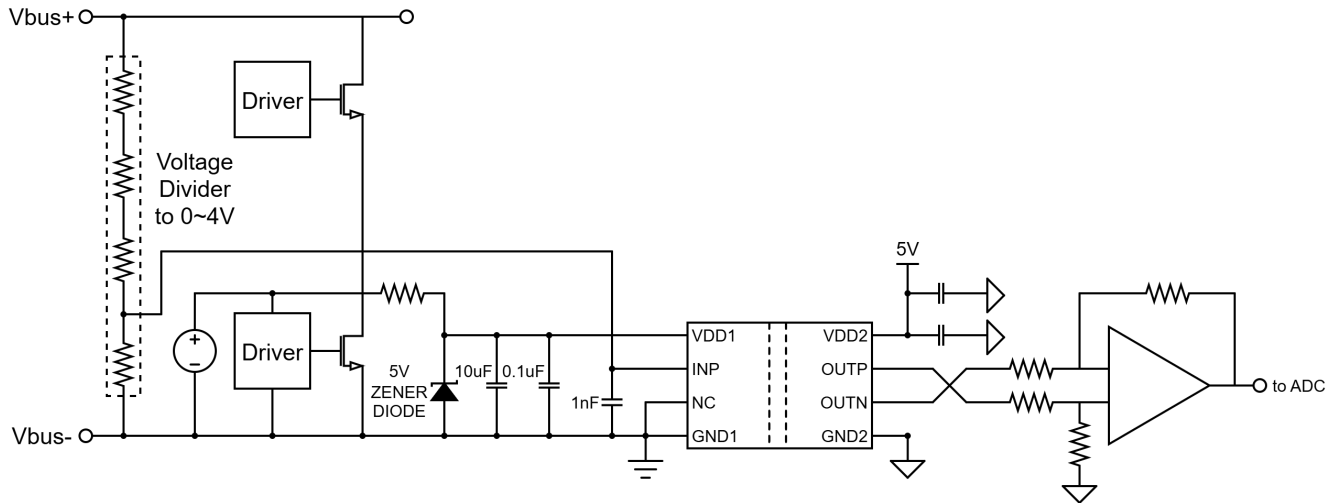


Figure 9.2 Typical Application Circuits of NSI1611D04-Q1

9.2. High Voltage Dividing Resistor Selection

Two restrictions should be considered when choosing the proper value of the voltage-dividing resistors:

- The current through the resistor should be within its rated range. Using Ohm law to calculate the cross current ($I_{cross} = V_{max}/R_{total}$);
- The divided input voltage value should not exceed the linear input range of NSI1611D0x-Q1, in which case the output may be clipped.

9.3. Accuracy Related Parameters

Parameters related to the accuracy performance are explained in this section, including V_{os} and its drift, EG and its drift, Nonlinearity. Other immunity parameters that affect accuracy like CMRR and PSRR are also included.

9.3.1. Input Offset V_{os} and Gain Error E_g

V_{os} and EG are the most significant factor influencing accuracy. The ideal curve and actual curve are shown in Figure 9.3.

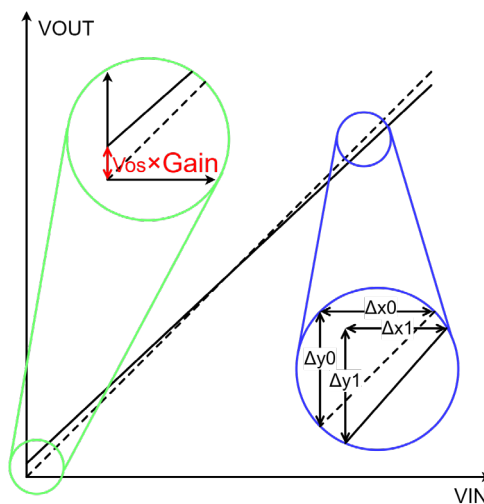


Figure 9.3 V_{os} and EG diagram

V_{os} means the input offset voltage when input is 0V. The tested output should be divided by nominal gain as V_{os} is defined as the offset voltage referred to input (See Equation 1).

$$V_{os} = V_o / \text{Nominal Gain}$$

Equation 1

where

- V_o is the output voltage tested when input is 0V.
- Nominal Gain is 0.5 for NSI1611D04-Q1 and 1.0 for NSI1611D02-Q1.

Gain is the magnification of the amplifier, and the definition formula is shown in Equation 2. EG means the difference between actual and ideal slope. It should be noted that EG is tested across the whole input range to minimize test error (See Equation 3).

$$\text{Gain} = \frac{\Delta y_1}{\Delta x_1} = \frac{V_{o1} - V_{o2}}{V_{in1} - V_{in2}}$$

Equation 2

$$E_G = \frac{\text{Gain} - \text{Nominal Gain}}{\text{Nominal Gain}} \times 100\%$$

Equation 3

where V_{in1} and V_{in2} are the lower and upper limit of the input FSR separately, V_{o1} and V_{o2} are the output voltage corresponding to V_{in1} and V_{in2} .

9.3.2. Input Offset Drift TCV_{OS} and Gain Error Thermal Drift TCE_G

Input offset drift TCV_{OS} means the drift of V_{OS} over the whole operating temperature range, which is calculated as Equation 4.

$$TCV_{os} = \frac{V_{os_{max}} - V_{os_{min}}}{\text{TempRange}}$$

Equation 4

where

- $V_{os_{max}}$ and $V_{os_{min}}$ is the maximum and minimum offset voltage over the whole operating ambient temperature range.
- TempRange covers the whole operating temperature, from -40°C to 125°C.

Gain error thermal drift TCE_G is the drift of E_G over the whole operating temperature range, which is calculated as Equation 5.

$$TCE_G = \frac{E_{G_{max}} - E_{G_{min}}}{\text{TempRange}}$$

Equation 5

where $E_{G_{max}}$ and $E_{G_{min}}$ is the maximum and minimum Gain Error over the whole temperature.

Both TCV_{OS} and TCE_G should be multiplied by the direction of temperature drift.

9.3.3. Nonlinearity

Nonlinearity describes the deviation between the actual output and the ideal linear output. Calculate the peak-to-peak value of the error between the actual output and the fitting curve, and nonlinearity is expressed as the ratio of half of the peak-to-peak error to the full-scale range of the output voltage (See Equation 6).

$$\text{Nonlinearity} = \frac{\text{Error_pkpk}}{2 \times V_{OFSR}} \times 100\%$$

Equation 6

where

- Error_pkpk is the peak-to-peak value of the error between the actual output and the fitting curve.
- V_{OFSR} represents the full-scale range of the output voltage (4V for NSI1611D04-Q1 and 2V for NSI1611D02-Q1).

9.3.4. Power-Supply Rejection Ratio

Power-Supply Rejection Ratio (PSRR) describes the level of the output error (input inferred) which is affected by the variation of power supply. PSRR is defined in dB and calculated as Equation 7.

$$\text{PSRR} = 20 \times \log_{10} \left(\frac{V_{O_var}}{\text{Nominal Gain} \times V_{DD_var}} \right)$$

Equation 7

Where V_{O_var} and V_{DD_var} are respectively the variation value of the output voltage and the supply voltage.

9.3.5.Common-Mode Rejection Ratio

Common-Mode Rejection Ratio (CMRR) quantifies the ability of a differential amplifier to suppress the variation of the common mode signals while amplifying the differential-mode signals. CMRR is calculated as:

$$CMRR=20\times\log_{10}\left(\frac{V_{O_var}}{\text{Nominal Gain}\times V_{CM_var}}\right) \quad \text{Equation 8}$$

where CMRR is the input-referred voltage variation in dB and V_{CM_var} is the variation value of the input common-mode voltage.

9.3.6.Total Error Calculation

The total error is contributed by parameters discussed above. It is helpful to know the respective contribution of all different parameters when something is wrong about system current sensing. This section will introduce the calculation method of total error.

Parameters which mainly affects sensing accuracy are V_{os} , EG and Nonlinearity and their drift. PSRR and CMRR are not a dominant factor in most cases. However, PSRR can be a concern when the power supply has high-frequency ripple, in which case a larger decoupling capacitor and a better layout are highly recommended (Refer to Section 9.4).

The error introduced by V_{os} and its drift can be calculated as:

$$\text{Error_Vos}=\frac{V_{os_max}+TCV_{os}\times\Delta T}{V_{IN}}\times100\% \quad \text{Equation 9}$$

where

- V_{os_max} is the maximum value of input offset voltage at 25°C, which is $\pm1.5\text{mV}$ for NSI1611D04-Q1 and $\pm0.8\text{mV}$ for NSI1611D02-Q1.
- TCV_{os} is the maximum drift of input offset voltage over the whole working temperature, which is $\pm40\text{ }\mu\text{V}/^{\circ}\text{C}$ for NSI1611D04-Q1 and $\pm20\text{ }\mu\text{V}/^{\circ}\text{C}$ for NSI1611D02-Q1.
- ΔT is the range of temperature variation.
- V_{IN} is the input voltage in the application.

The error introduced by E_G and TCE_G can be calculated as:

$$\text{Error_E}_G=E_G+TCE_G\times\Delta T \quad \text{Equation 10}$$

where

- E_G is the maximum value of Gain Error when the temperature is 25°C, which is $\pm0.25\%$ for both NSI1611D04-Q1 and NSI1611D02-Q1.
- TCE_G is the maximum drift of Gain Error over the whole temperature, which is $\pm45\text{ppm}/^{\circ}\text{C}$ for both NSI1611D04-Q1 and NSI1611D02-Q1.
- The error introduced by Nonlinearity is $\text{Nonlinearity}_{max}$, the maximum value of Nonlinearity in the entire temperature range, - 40°C to 125°C, which is $\pm0.04\%$ for NSI1611D0x-Q1. The total error sensing error is expressed as:

$$\text{Total_Error}=\sqrt{\text{Error_Vos}^2+\text{Error_E}_G^2+\text{Nonlinearity}_{max}^2} \quad \text{Equation 11}$$

For example, consider an NSI1611D04-Q1 with the sensing input voltage of 0~4V and a - 40°C to 85°C temperature range. The total error calculation is shown in Table 1.

Table 8.1 Total Error Calculation of NSI1611D04-Q1 (-40°C to 85°C)

Error Component	Symbol	Equation	Error at $V_{IN}=0.4\text{V}$	Error at $V_{IN}=4.0\text{V}$
Input offset error	Error_Vos	$\text{Error_Vos}=\frac{V_{os_max}+TCV_{os}\times\Delta T}{V_{IN}}\times100\%$ $=\frac{\pm1.5\text{mV}\pm40\mu\text{V}/^{\circ}\text{C}\times60^{\circ}\text{C}}{V_{IN}}\times100\%$	$\pm0.975\%$	$\pm0.0975\%$
Gain error	Error_E _G	$\text{Error_E}_G=E_G+TCE_G\times\Delta T=\pm0.25\%\pm45\text{ppm}/^{\circ}\text{C}\times60^{\circ}\text{C}$	$\pm0.52\%$	$\pm0.52\%$

Nonlinearity	Nonlinearity _{max}	Nonlinearity _{max} = ±0.04%	±0.04%	±0.04%
Total error	Total_Error	Total_Error = $\sqrt{\text{Error_Vos}^2 + \text{Error_E}_G^2 + \text{Nonlinearity}_{\text{max}}^2}$	±1.10%	±0.53%

Table 8.2 Total Error Calculation of NSI1611D02-Q1 (-40°C to 85°C)

Error Component	Symbol	Equation	Error at V _{IN} =0.2V	Error at V _{IN} =2.0V
Input offset error	Error_Vos	$\text{Error_Vos} = \frac{\text{Vos}_{\text{max}} + \text{TCV}_{\text{os}} \times \Delta T}{V_{\text{IN}}} \times 100\%$ $= \frac{\pm 0.8\text{mV} \pm 20\mu\text{V}/^\circ\text{C} \times 60^\circ\text{C}}{V_{\text{IN}}} \times 100\%$	±1.0%	±0.10%
Gain error	Error_E _G	Error_E _G = E _G + TCE _G × ΔT = ±0.25% ± 45ppm/°C × 60°C	±0.52%	±0.52%
Nonlinearity	Nonlinearity _{max}	Nonlinearity _{max} = ±0.04%	±0.04%	±0.04%
Total error	Total_Error	Total_Error = $\sqrt{\text{Error_Vos}^2 + \text{Error_E}_G^2 + \text{Nonlinearity}_{\text{max}}^2}$	±1.13%	±0.531%

Since the input offset voltage is independent of input voltage, it becomes the dominant factor of the total error when the input voltage is low. To improve the system accuracy, especially under low-input applications, it is recommended to perform software zero-point calibration and gain error calibration. With system-level calibration, the total error can also be reduced significantly. The reduced error is calculated as Table 8.2.

Table 8.3 Total Error Calculation with Software Calibration of NSI1611D0x-Q1 (-40°C to 85°C)

Error Component	Symbol	Equation	Error at V _{IN} =0.4 V	Error at V _{IN} =4.0V
Input offset error	Error_Vos	$\text{Error_Vos} = \frac{\text{TCV}_{\text{os}} \times \Delta T}{V_{\text{IN}}} \times 100\%$ $= \frac{40\mu\text{V}/^\circ\text{C} \times 60^\circ\text{C}}{V_{\text{IN}}} \times 100\%$	±0.60%	±0.06%
Gain error	Error_E _G	Error_E _G = TCE _G × ΔT = ±45ppm/°C × 60°C	±0.27%	±0.27%
Nonlinearity	Nonlinearity _{max}	Nonlinearity _{max} = ±0.04%	±0.04%	±0.04%
Total error	Error	Total_Error = $\sqrt{\text{Error_Vos}^2 + \text{Error_E}_G^2 + \text{Nonlinearity}_{\text{max}}^2}$	±0.66%	±0.28%

The maximum total error with and without calibration is show in Figure 8.3, considering 0~4V input as full input range, NSI1611D04-Q1 can achieve <0.7% error at more than 10% input voltage(V_{IN}≥0.4V) with software calibration, and <1.2% error at more than 10% load(V_{IN}≥0.4V) without software calibration.

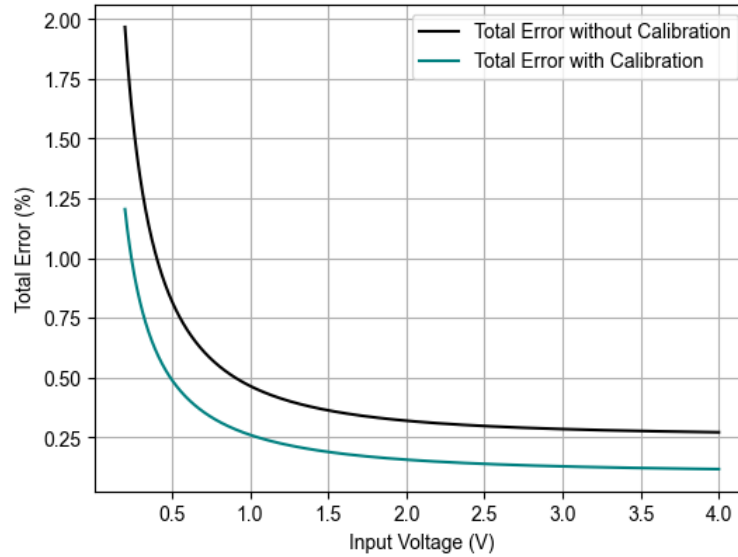


Figure 9.4 Total Error Over - 40°C to 85°C vs Input Voltage

9.4. PCB Layout

Figure 9.5 shows a typical layout example of NSI1611D0x-Q1. To enhance power supply noise immunity and EOS robustness, it is recommended to use a low-ESR 100nF capacitor (C2, C4) in parallel with a low-ESR 1 μ F capacitor (C1, C3). These capacitors should be positioned as close as possible to the power supply pins, and the smaller-value capacitors should be in the inner place as they usually have a lower ESR and better immunity to high-frequency interference.

An additional capacitor (C5) is recommended to be added in parallel with lower side divided resistor (R3). The capacitor is also recommended to be positioned as close as possible to the input pin VIN.

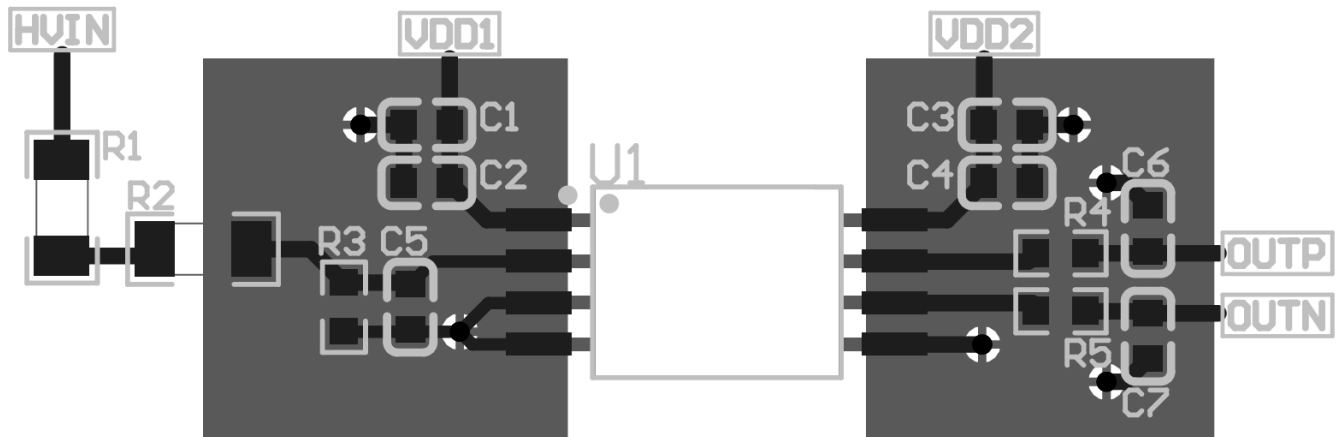
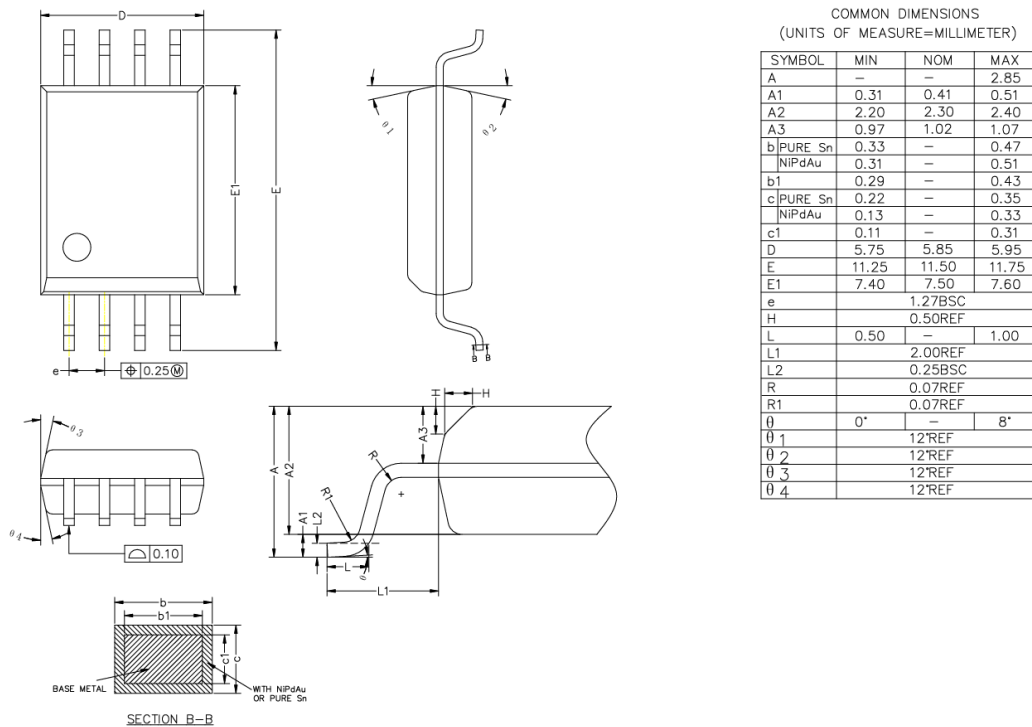


Figure 9.5 PCB layout example of NSI1611D0x-Q1

10. Package Information



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOW8 package shape and dimension in millimeters

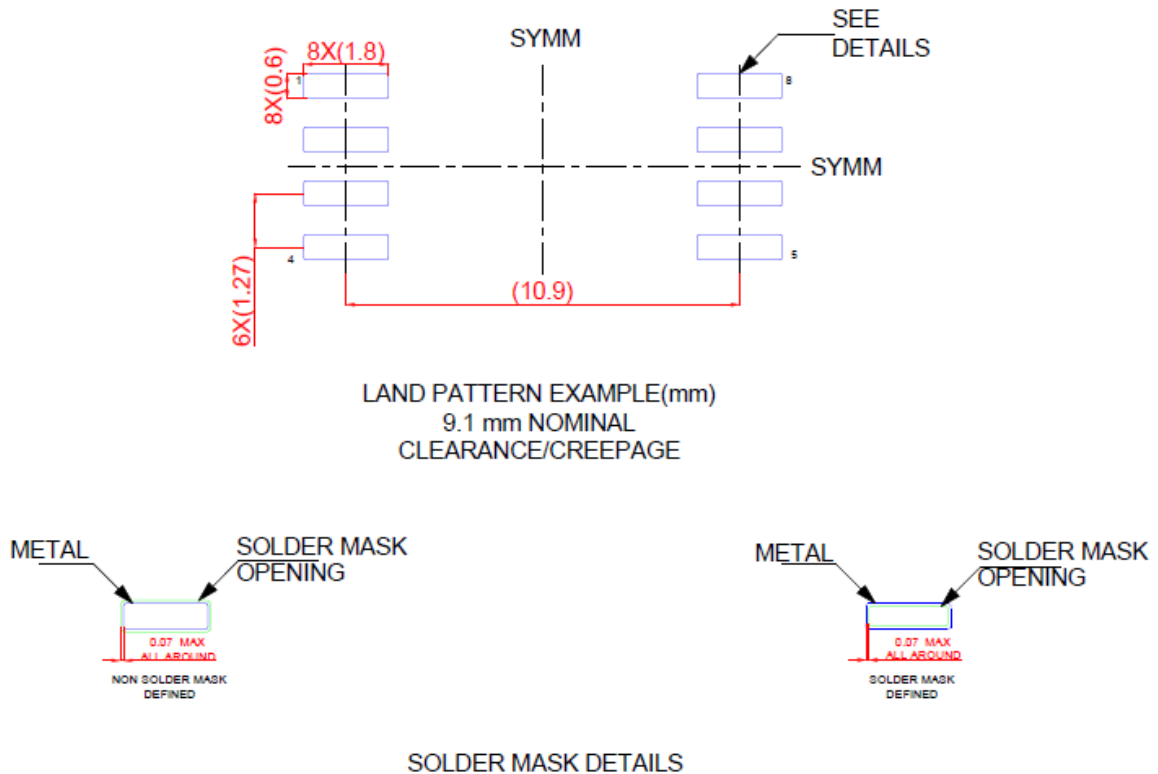


Figure 10.2 SOW8 Package Board Layout Example

11. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range	MSL	Device Marking	Temperature	Package Type	Package Drawing	SPQ	MPQ
NSI1611D02-Q1SWVR	5.7	-0.1~2V	Level-3	NSi1611D02Q	-40 to 125°C	SOP8 (300mil)	SOW8	1000	1000
NSI1611D04-Q1SWVR	5.7	-0.1~4V	Level-3	NSi1611D04Q	-40 to 125°C	SOP8 (300mil)	SOW8	1000	1000

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents
NSI1611D02-Q1SWVR	Click here	Click here	Click here
NSI1611D04-Q1SWVR	Click here	Click here	Click here

13. Tape and Reel Information

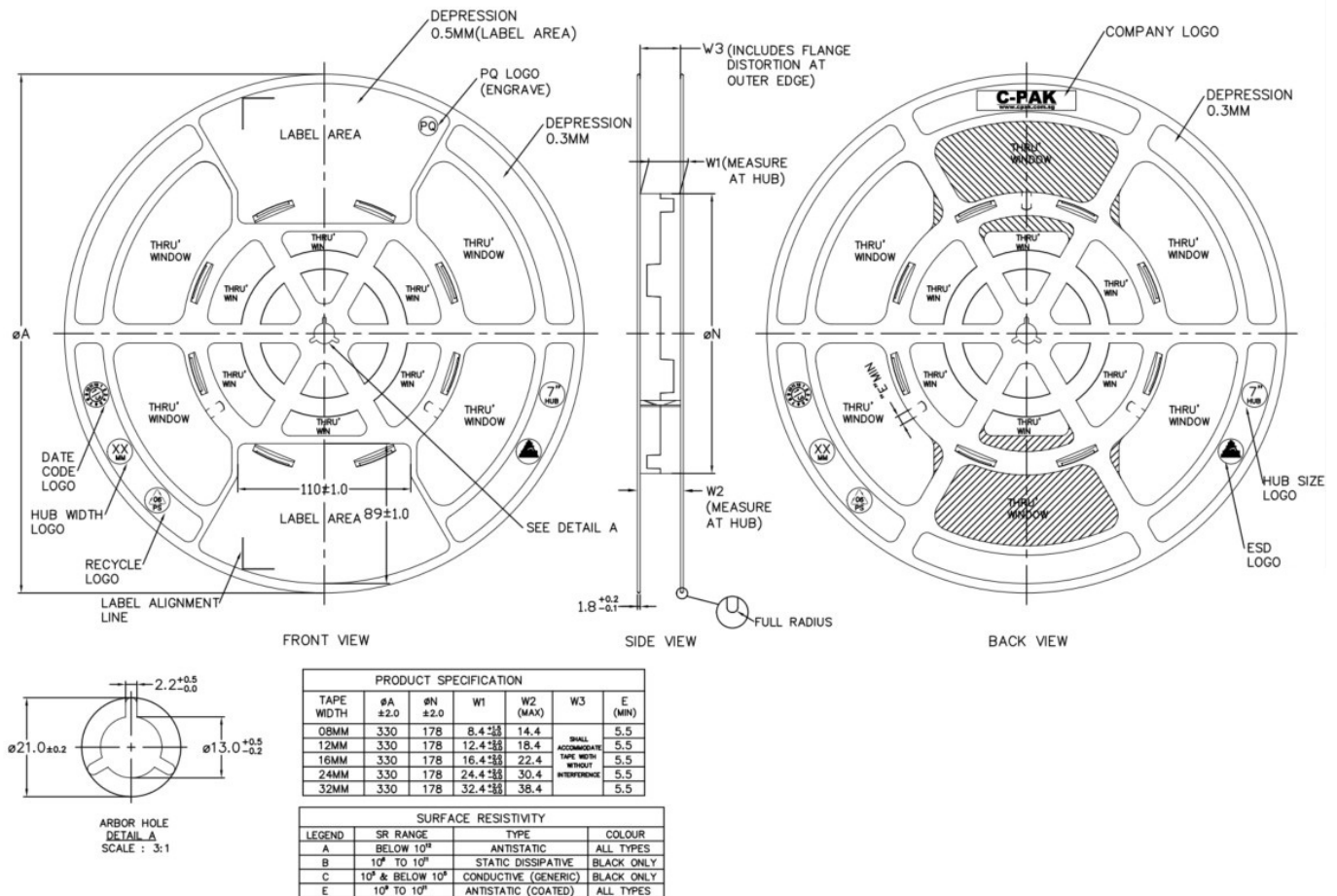


Figure 13.1 Tape Information

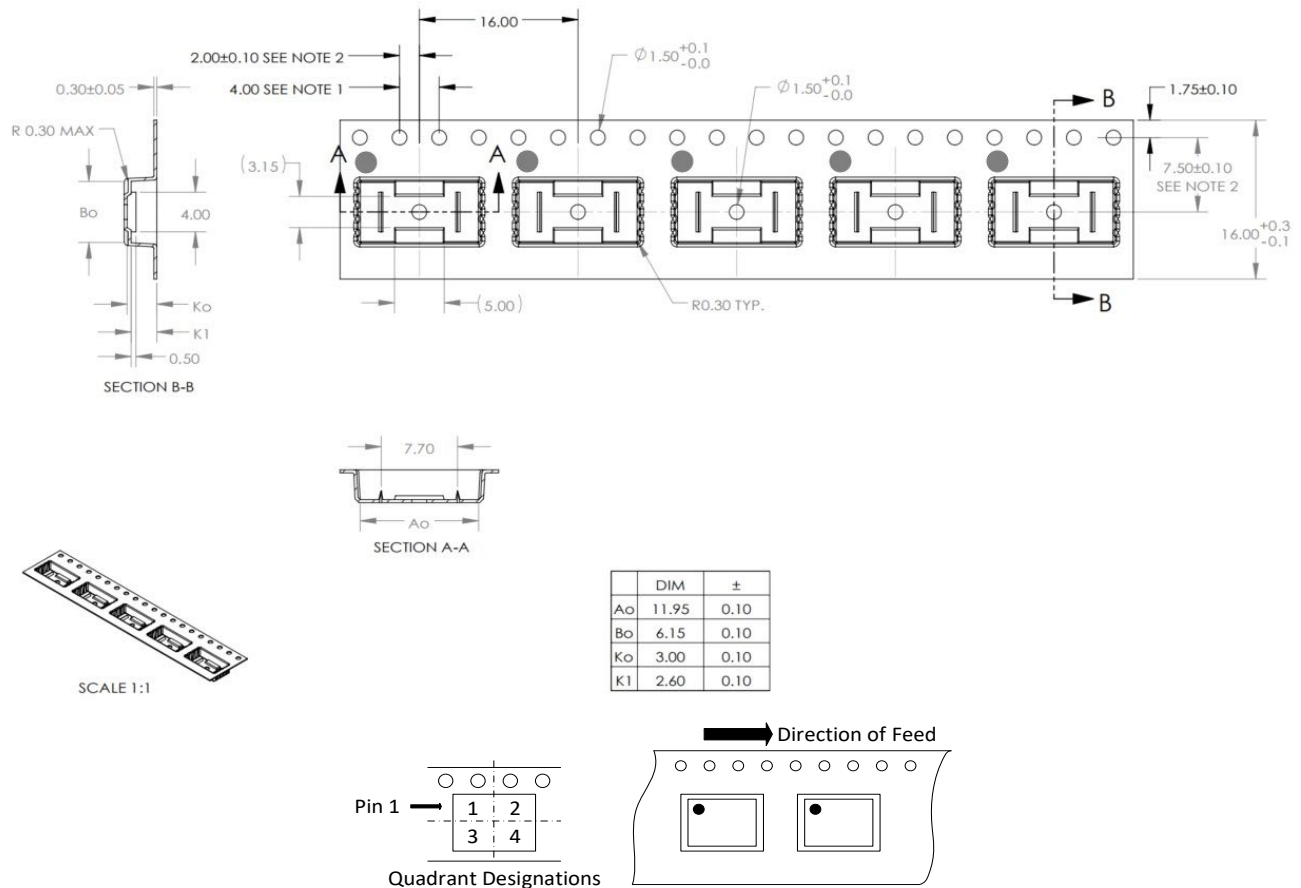


Figure 13.2 Reel Information of SOP8(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Release.	2025/12/26

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