

Product Overview

NSI1316 is a high performance Σ - Δ modulator with output separated from input based on the NOVOSENSE capacitive isolation technology. The isolation barrier has high resistance to magnetic interference, which benefits applications under high common voltage transient. The wide input voltage of $\pm 1\text{V}$ and high input resistance make NSI1316 suitable for high voltage sensing with large resistive dividers. The analog input voltage is amplified and continuously sampled by a second-order Σ - Δ modulator and converted to a high speed, single bit data stream. The output data is synchronous to the external clock with a frequency range from 5MHz to 21MHz. By using an appropriate digital filter (such as sinc3 filter) to decimate the bitstream, the device can achieve 16 bits resolution and an 82dB signal to noise ratio (SNR) at 78.125kSPS with a 20MHz master clock.

The fail-safe function supports missing AVDD detection and simplifies system-level design and diagnostics.

Key Features

- Up to 5000V_{RMS} Insulation Voltage
- Clock frequency: 5MHz to 21MHz
- Wide input voltage range: $\pm 1\text{V}$ linear
- High input resistance: 1.2G Ω (typical)
- Power supply voltage: 3.0V to 5.5V
- Excellent DC Performance:
 - Offset Error: $\pm 0.6\text{mV}$ (max)
 - Offset Drift: $\pm 10 \mu\text{V}/^\circ\text{C}$ (max)
 - Gain Error: $\pm 0.3\%$ (max)
 - Gain Drift: $\pm 40\text{ppm}/^\circ\text{C}$ (max)
- SNR: 82dB (typ)
- THD: -85dB (typ)

- High CMTI: 150kV/ μs
- High system level EMC performance:
- System-Level Diagnostic Features:
 - AVDD Monitoring
- Operation temperature: $-40^\circ\text{C} \sim 125^\circ\text{C}$
- RoHS-Compliant Packages: SOP8(300mil)

Safety Regulatory Approvals

- UL recognition per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- On Board chargers
- DC/DC Converters
- Traction Inverters

Device Information

Part Number	Package	Body Size
NSI1316-DSWVR	SOW-8(300mil)	5.85mm×7.50mm

Functional Block Diagrams

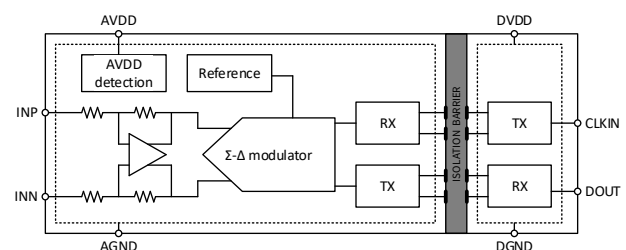


Figure 1. NSI1316 Block Diagram

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1. Pin Configuration and Functions

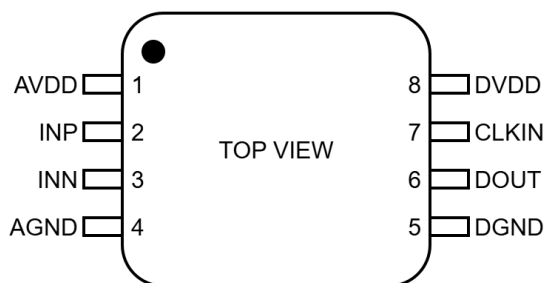


Figure 1.1 NSI1316 Package (Not to scale)

Table 1.1 NSI1316 Pin Configuration and Description

NSI1316 PIN NO.	SYMBOL	FUNCTION
1	AVDD	Power supply for analog side
2	INP	Positive analog input
3	INN	Negative analog input
4	AGND	Analog ground reference
5	DGND	Digital ground reference
6	DOUT	Σ - Δ modulator data output
7	CLKIN	Σ - Δ modulator clock input
8	DVDD	Power supply for digital side

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply	xVDD to GND	-0.3		6.5	V
Analog Input Voltage	INP, INN	AGND-0.5		AVDD+0.5	V
Digital Input Voltage	CLKIN	DGND-0.5		DVDD+0.5	V
Digital Output Voltage	DOUT	DGND-0.5		DVDD+0.5	V
Output current per Output Pin	I _{IN}	-10		10	mA
Operating Temperature	T _{opr}	-40		125	°C
Junction Temperature	T _j	-40		150	°C
Storage Temperature	T _{stg}	-50		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Analog Side Power Supply	AVDD	3.0	5.0	5.5	V
Digital Side Power Supply	DVDD	3.0	3.3	5.5	V
Differential input voltage before clipping output	V _{Clipping}		±1.28		V
Linear differential input full scale voltage	V _{FSR}	-1		1	V
Operating common-mode input voltage	V _{CM}	-0.8		0.6	V
Operating Ambient Temperature	T _A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP8(300mil)	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	86	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	4	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	42	°C/W

6. Specifications

6.1. Electrical Characteristics

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -1V to 1V, and INN = AGND = 0V, TA = -40°C to 125°C and sinc3 filter with OSR=256. Unless otherwise noted, Typical values are at CLKIN=20MHz, AVDD = 5V, DVDD = 3.3V, TA = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		8.2	12	mA	
Digital Side Supply Current	IDVDD		2.5	5	mA	
AVDD undervoltage detection threshold voltage	AVDD _{UV}			2.6	V	AVDD falling threshold
DVDD undervoltage detection threshold voltage	DVDD _{UV}			2.4	V	DVDD falling threshold
Analog Input						
Common-mode rejection ratio	CMRR _{dC}		-100		dB	INP = INN, f _{IN} = 0 Hz, VCM min ≤ V _{IN} ≤ VCM max
	CMRR _{aC}		-86		dB	INP = INN, f _{IN} = 10 kHz, VCM min ≤ V _{IN} ≤ VCM max
Single-ended input resistance	R _{IN}	0.1	0.8		GΩ	INN = AGND
Differential input resistance	R _{IND}	0.1	1.2		GΩ	
Input capacitance	C _I		2		pF	
Input bias current	I _{IB}	-10	2.5	10	nA	INP = INN = AGND, I _{IB} = (I _{IBP} + I _{IBN}) / 2
Input bias current drift	TCI _{IB}		±1		nA/°C	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input offset current	I _{IO}		10		nA	I _{IO} = I _{IIBP} - I _{IIBN}
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	E _O	-0.6	±0.2	0.6	mV	INP = INN = AGND T _A = 25°C
Offset error thermal drift	TCE _O	-10	±2	10	μV/°C	
Gain error	E _G	-0.3%	±0.1%	0.3%		T _A = 25°C
Gain error thermal drift	TCE _G	-40	±10	40	ppm/°C	
Power supply rejection ratio	PSRR		-96		dB	PSRR vs AVDD, at DC
			-90		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR	75	82		dB	f _{IN} = 1kHz
Signal to noise and distortion	SINAD	75	81		dB	f _{IN} = 1kHz
Total harmonic distortion	THD		-86	-80	dB	f _{IN} = 1kHz
Spurious-free dynamic range	SFDR	80	100		dB	f _{IN} = 1kHz
Digital Input / Output						
Input current	I _{IN}	0		7	μA	DGND ≤ V _{IN} ≤ DVDD
Input capacitance	C _{IN}		5		pF	
Output load capacitance	C _{LOAD}		30		pF	
High-level input voltage	V _{IH}	0.7×DVDD		DVDD+0.3	V	
Low-level input voltage	V _{IL}	-0.3		0.3×DVDD	V	
High-level output voltage	V _{OH}	DVDD-0.1			V	I _{OH} = -20μA
		DVDD-0.4			V	I _{OH} = -4mA
Low-level output voltage	V _{OL}			0.1	V	I _{OL} = 20μA
				0.4	V	I _{OL} = 4mA
Timing						
CLKIN clock frequency	f _{CLKIN}	5		21	MHz	
CLKIN clock period	t _{CLKIN}	47.6		200	ns	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
CLKIN clock high time	t_{HIGH}	20	25	120	ns	
CLKIN clock low time	t_{LOW}	20	25	120	ns	
DOUT rising time	t_r			5	ns	$C_{\text{LOAD}} = 15\text{pF}$
DOUT falling time	t_f			5	ns	$C_{\text{LOAD}} = 15\text{pF}$
DOUT hold time after rising edge of CLKIN	t_H	3.5			ns	$C_{\text{LOAD}} = 15\text{pF}$
Rising edge of CLKIN to DOUT valid delay	t_D			15	ns	$C_{\text{LOAD}} = 15\text{pF}$
Analog setting time	t_{AS}		0.5		ms	AVDD step to 3.0 V with DVDD ≥ 3.0 V, to DOUT valid, 0.1% settling

- (1) The temperature drift is calculated within the whole temperature range (-40°C to 125°C).
- (2) Input referred.
- (3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).
- (4) Not test covered, guaranteed by characterization.
- (5) Not test covered, guaranteed by design.

6.2. Timing Diagrams

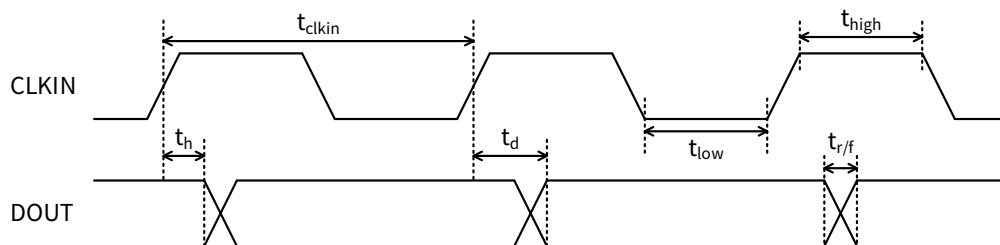


Figure 6.1 Digital Input and Output Timing Definition

6.3. Typical Performance Characteristics

(AVDD = 5.0V, DVDD = 3.3V, INP = -1V to 1V, INN = AGND = 0V, TA = 25°C and CLKIN=20MHz, sinc3 filter with OSR=256. Unless otherwise noted)

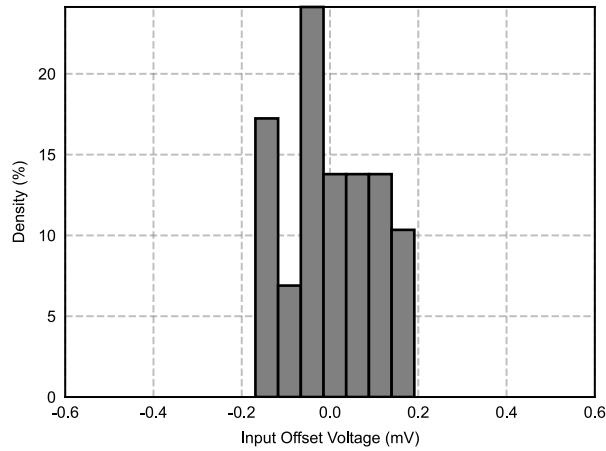


Figure 6.2 Offset Error Histogram

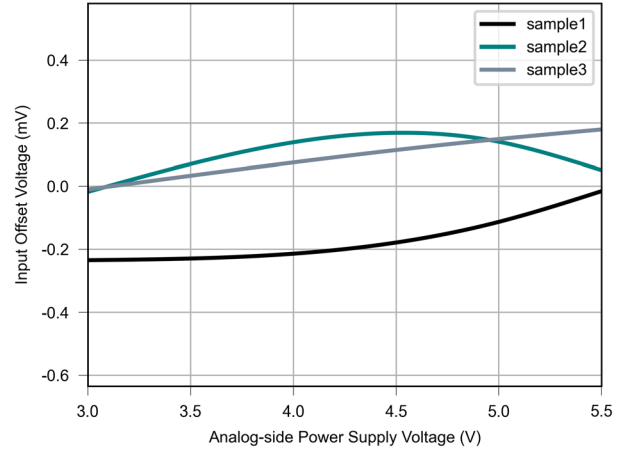


Figure 6.3 Offset Error vs Analog-Side Supply Voltage

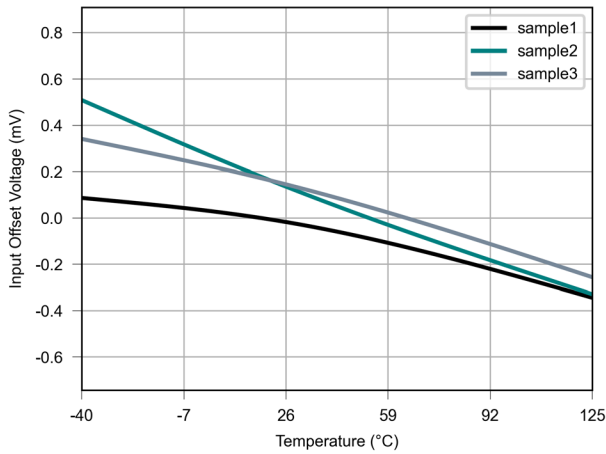


Figure 6.4 Offset Error vs Temperature

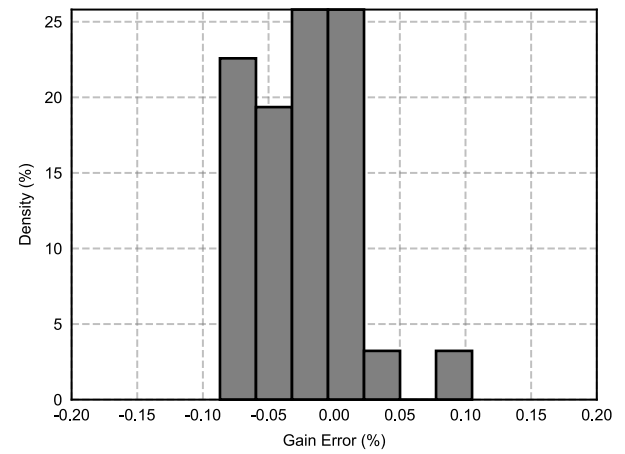


Figure 6.5 Gain Error Histogram

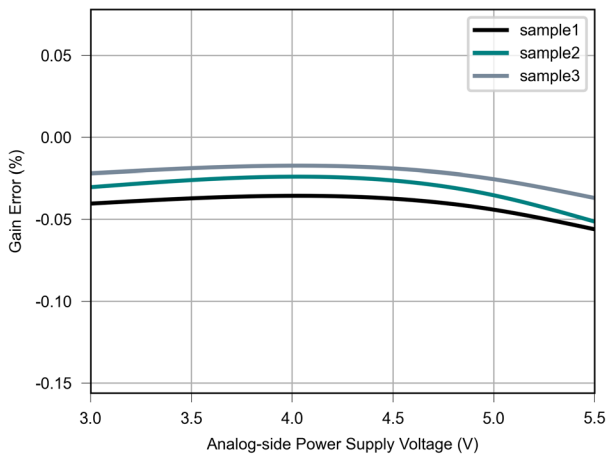


Figure 6.6 Gain Error vs Analog-side Supply Voltage

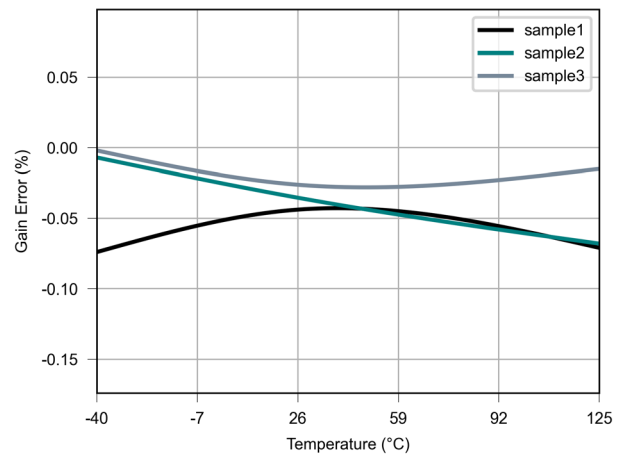


Figure 6.7 Gain Error vs Temperature

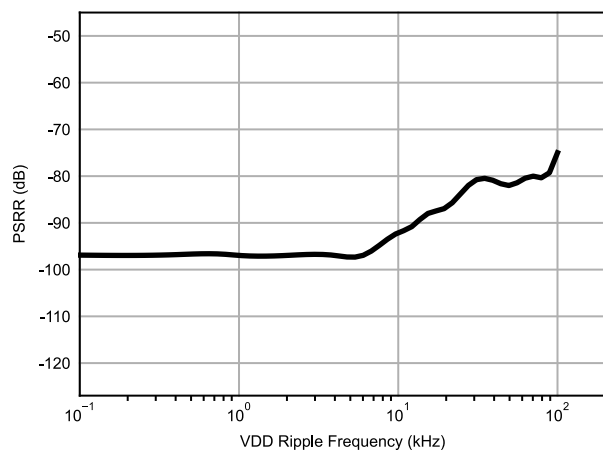


Figure 6.8 PSRR vs Ripple Frequency

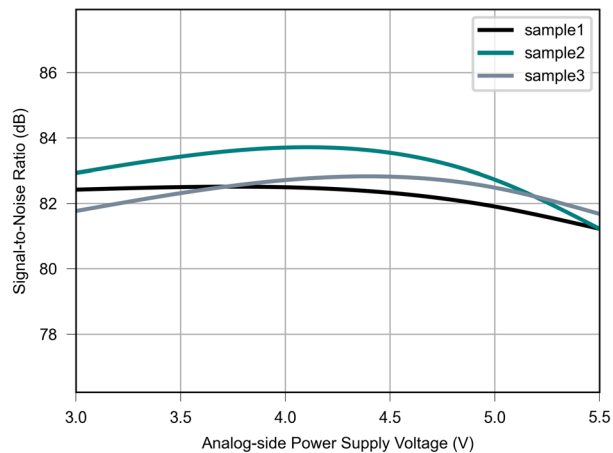


Figure 6.9 SNR vs Analog-Side Supply

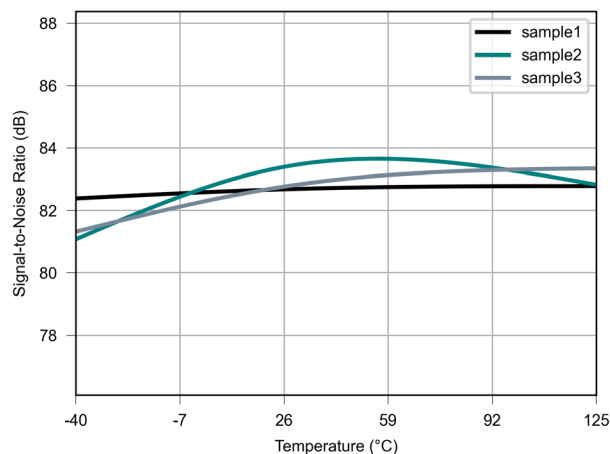


Figure 6.10 SNR vs Temperature

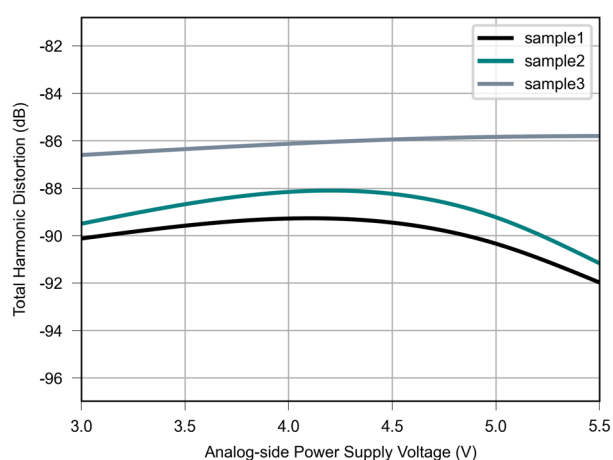


Figure 6.11 THD vs Analog-Side Supply Voltage

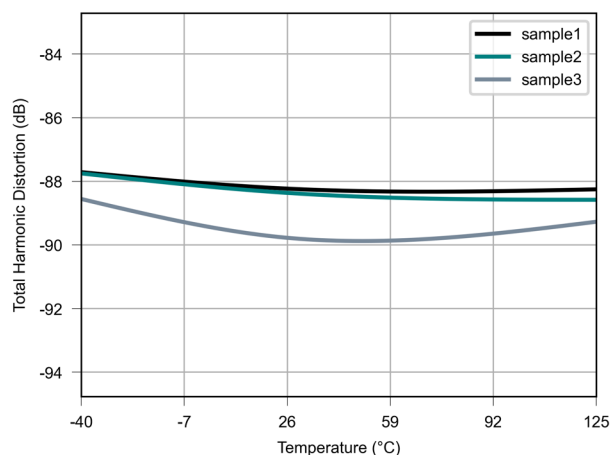


Figure 6.12 THD vs Temperature

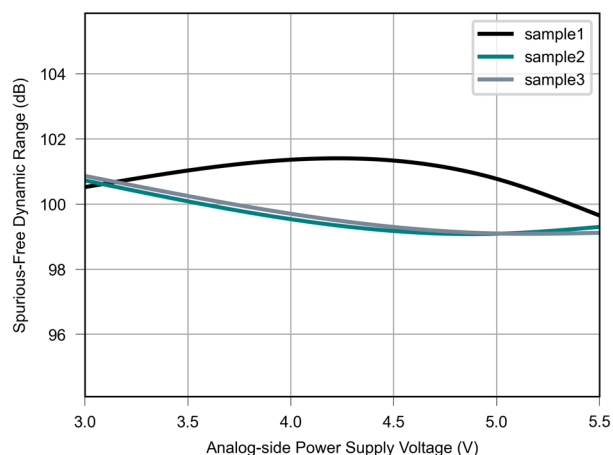


Figure 6.13 SFDR vs Analog-Side Supply Voltage

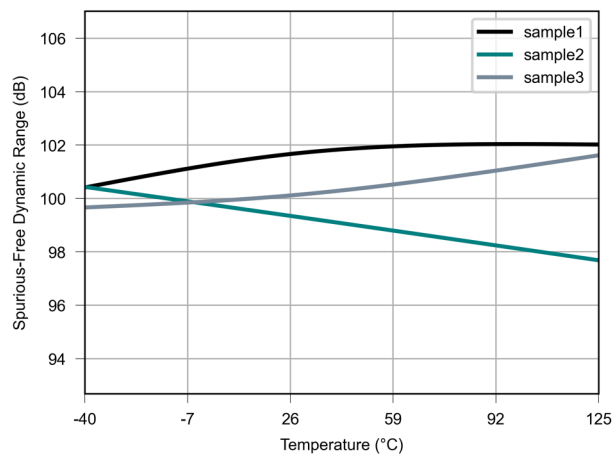


Figure 6.14 SFDR vs Temperature

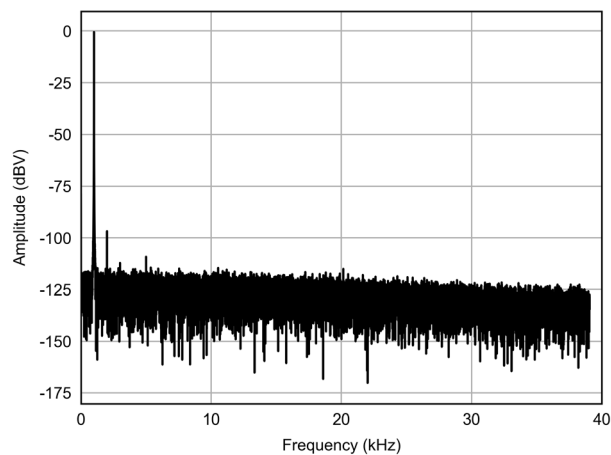


Figure 6.15 Frequency Spectrum with 1-kHz Input Signal

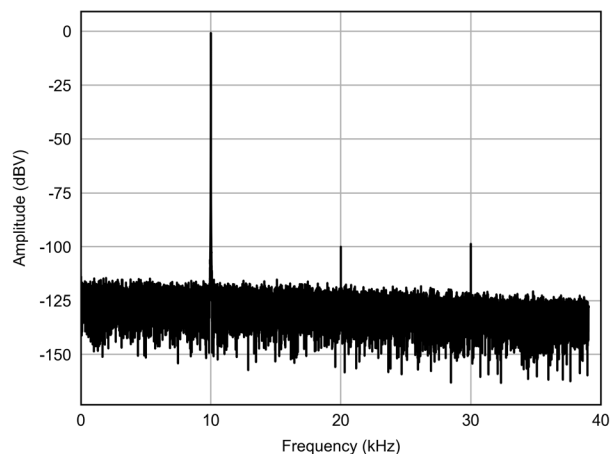


Figure 6.16 Frequency Spectrum with 10-kHz Input Signal

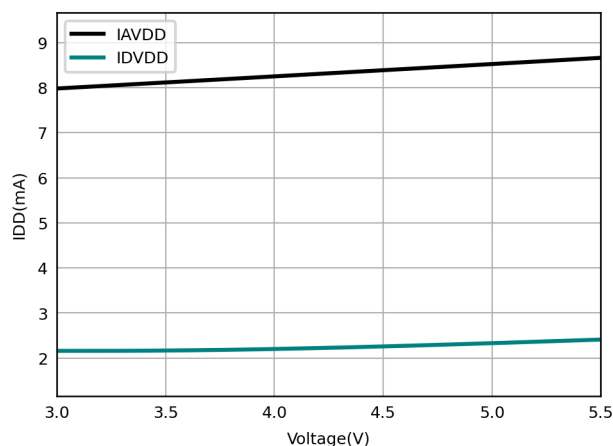


Figure 6.17 Supply Current vs Supply Voltage

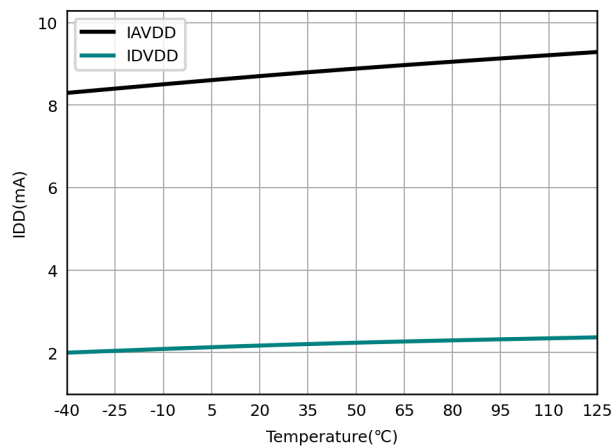


Figure 6.18 Supply Current vs Temperature

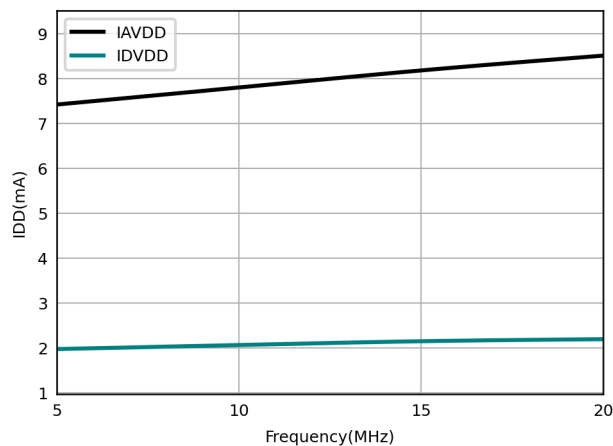


Figure 6.19 Supply Current vs Clock Frequency

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	28	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 150\text{Vrms}$	I to IV
	For Rated Mains Voltage $\leq 300\text{Vrms}$	I to IV
	For Rated Mains Voltage $\leq 600\text{Vrms}$	I to IV
	For Rated Mains Voltage $\leq 1000\text{Vrms}$	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{s}$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{s}$			pC
	Method b, routine test (100% production) and preconditioning (type			pC

Description	Test Condition	Symbol	Value	Unit
	test); $V_{ini}=1.2 \cdot V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.875 \cdot V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			
Maximum transient isolation voltage	$t = 60sec$	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50- μs waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50- μs waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$, $T_A=25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500V$, $100^{\circ}C \leq T_A \leq 125^{\circ}C$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500V$, $T_A=T_s$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	pF
Safety total power dissipation	$V_I = 5.5V$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	P_s	1430	mW
Safety input, output, or supply current	$\theta_{JA} = 86^{\circ}C/W$ for SOP8, $V_I = 5.5V$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	I_s	260	mA
Maximum safety temperature		T_s	150	$^{\circ}C$
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60 s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1 s$ (100% production test)	V_{ISO}	5000	V_{RMS}

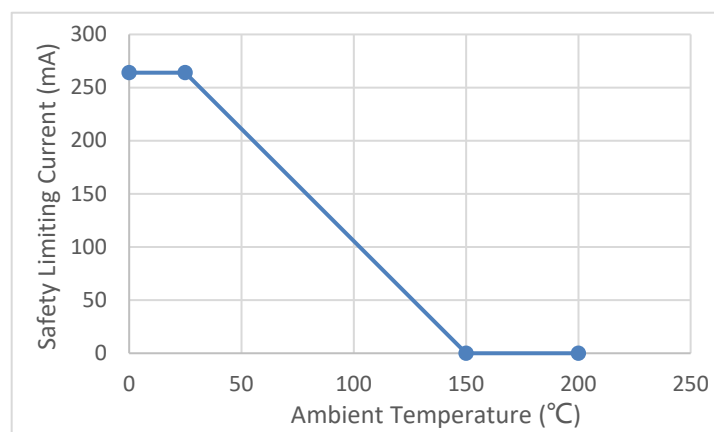


Figure 6.20 NSI1316 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-17

7.3. Regulatory Information

The NSI1316-DSWVR are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforce Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	Reinforced insulation	5000V _{rms} for 1min
E500602	E500602	40052820	CQC20001264938	R50574061

8. Function Description

8.1. Overview

The NSI1316 is a high-performance isolated modulator that accepts fully-differential input. The wide range fully-differential input is ideally suited for high voltage sensing in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ - Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference, the modulator converts the analog input signal to a digital bitstream. The drivers (called TX/RX in the Functional Block Diagram) accept clock from outside and transfer across isolation barrier to the modulator. The output of the modulator is also transferred across the isolation barrier through the drivers TX/RX, as shown in the Functional Block Diagram.

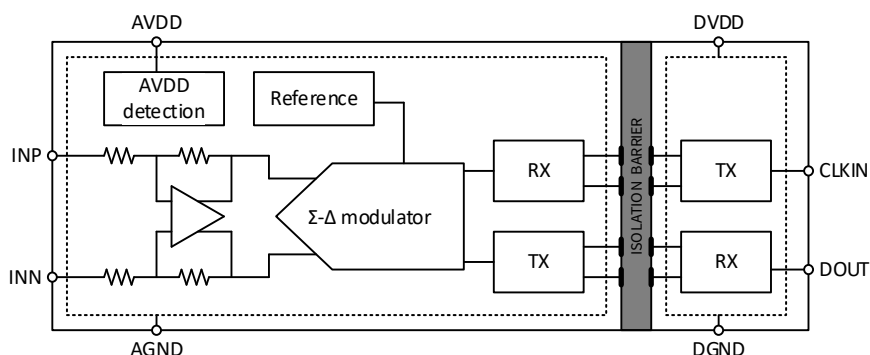


Figure 8.1 Function Block Diagram

8.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range from AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Digital Input

The digital input refers to clock signal which provides the clock for modulator conversion and output data frame clock. The clock signal should be supplied by an external source with a frequency range from 5MHz to 21MHz.

8.4. Digital Output

The digital output provides a stream of ones and zeros that can accurately represent the analog input voltage. Within the linear input range, the density of ones in the bitstream is proportional to the input voltage.

Ideally for a 0V input signal, the modulator outputs a bitstream with 50% high time. For a 1V input signal, the modulator outputs a bitstream with 89.06% high time. For a -1V input signal, the modulator outputs a bitstream with 10.94% high time.

If the input signal is greater than or equal to 1.28V, the modulator clips with a stream of all ones. If the input signal is less than or equal to -1.28V, the output of the modulator clips with a stream of all zeros. In this case, however, the NSI1316 generates a single 0 (if the input is at positive full-scale) or 1 (if the input is at negative full-scale) every 128 clock cycles to indicate proper device function (see section 8.5 for more details).

Due to quantization noise of internal Σ - Δ modulator, the digital output frequency is not fixed, but the density of high time is fixed based on input voltage. Typical modulator digital output characteristics are as below.

Table 8.1 Input Voltage with Ideal Corresponding Density of High Time at Modulator Data Output, and ADC Code

Analog input	Input voltage	Density of high time	Digital output code(16-bit unsigned decimation)
+Differential input voltage before clipping output	+1.28V	99.22%	65024

+Linear differential input full scale voltage	+1V	89.06%	58368
Zero	0V	50%	32768

Ideal density of 1s in the output bitstream for any input voltage(except for full-scale input, as described in section 8.5) at modulator data output can be calculated with:

$$\frac{V_{IN} + V_{CLIPPING}}{2 \times V_{CLIPPING}}$$

Similarly, the ADC code can be calculated, assuming a 16-bit unsigned decimation filter.

8.5. Device Functional Modes

NSI1316 operates normally when the power supplies AVDD and DVDD are applied and clock input signal CLKIN is within the valid range. NSI1316 also integrates several diagnostic features to indicate the occurrence of abnormal states, including fail-safe output and clipping output.

- When the undervoltage of AVDD is detected ($AVDD < AVDD_{UV}$), DOUT pin outputs a bitstream of all logic zeros, as shown in Figure 8.2.

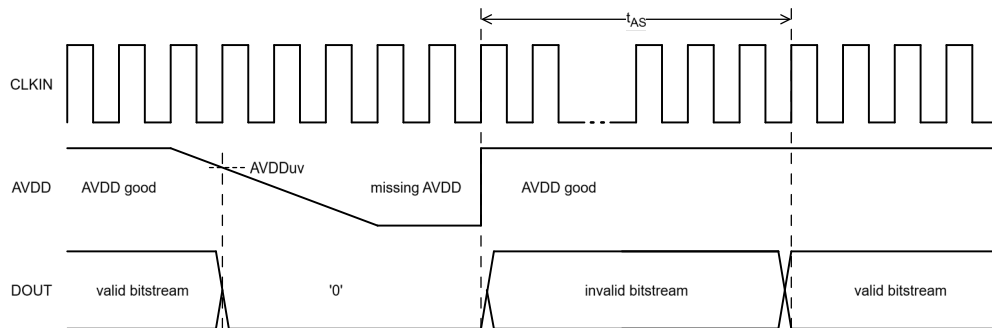


Figure 8.2 Fail-safe output

- If an overrange input signal is applied to the NSI1316 ($V_{IN} \geq V_{CLIPPING}$), the output generates a single 0 or 1 every 128 clock cycles, as shown in Figure 8.3.

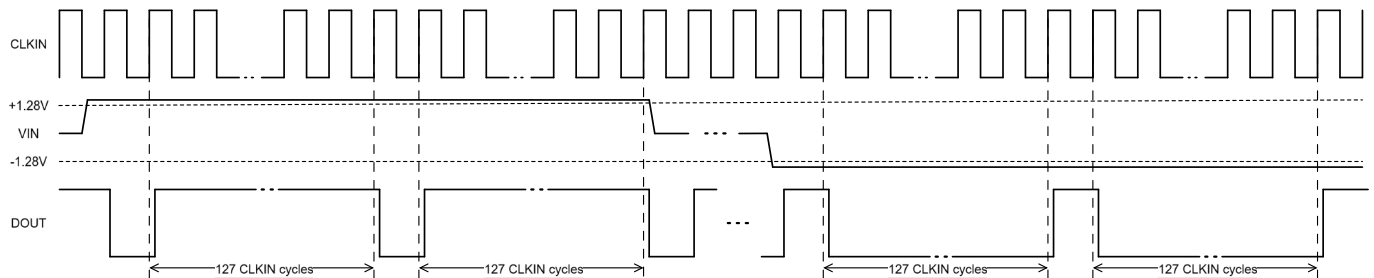


Figure 8.3 Overage output

- If the input clock signal is lost, the DATA output will remain in its previous state until the next clock rising edge arrives, as shown in Figure 8.4

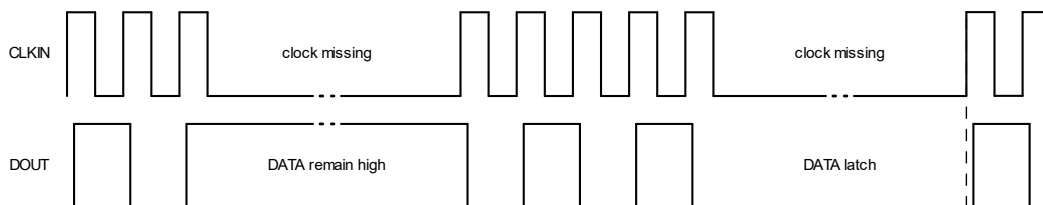


Figure 8.4 Clock missing behavior

Table 8.2 lists all operating modes of NSI1316.

Table 8.2 Device Operational Modes

<i>OPERATING CONDITION</i>	<i>AVDD</i>	<i>DVDD</i>	<i>INP-INN</i>	<i>CLKIN</i>	<i>DEVICE STATE</i>
Normal	Valid	Valid	Valid	Valid	The device outputs bit stream normally
Fail-safe state	$AVDD < AVDD_{uv}$	Valid	Any	Any	The device outputs a data stream of all '0'.
Input positive overrange	Valid	Valid	$INP-INN > +1.28$	Valid	The device outputs one '0' every 128 clock inputs.
Input negative overrange	Valid	Valid	$INP-INN < -1.28$	Valid	The device outputs one '1' every 128 clock inputs.
Clock missing	Valid	Valid	Valid	missing	DOUT remains the state last rising edge comes.

9. Application Note

9.1. Typical Application Circuit

Isolated Σ - Δ modulators are widely used in all kinds of power supplies, traction motors and photovoltaic inverters because of their high accuracy of AC and DC. Figure 9.1 shows a simplified schematic of an inverter using NSI1316 for bus and phase voltage feedback. The ground of controller side is isolated from high voltage side through NSI1316 and NSI1306 to ensure safety of operation.

The clock signal of different modulators can be connected to one source to achieve synchronization between different feedback channels.

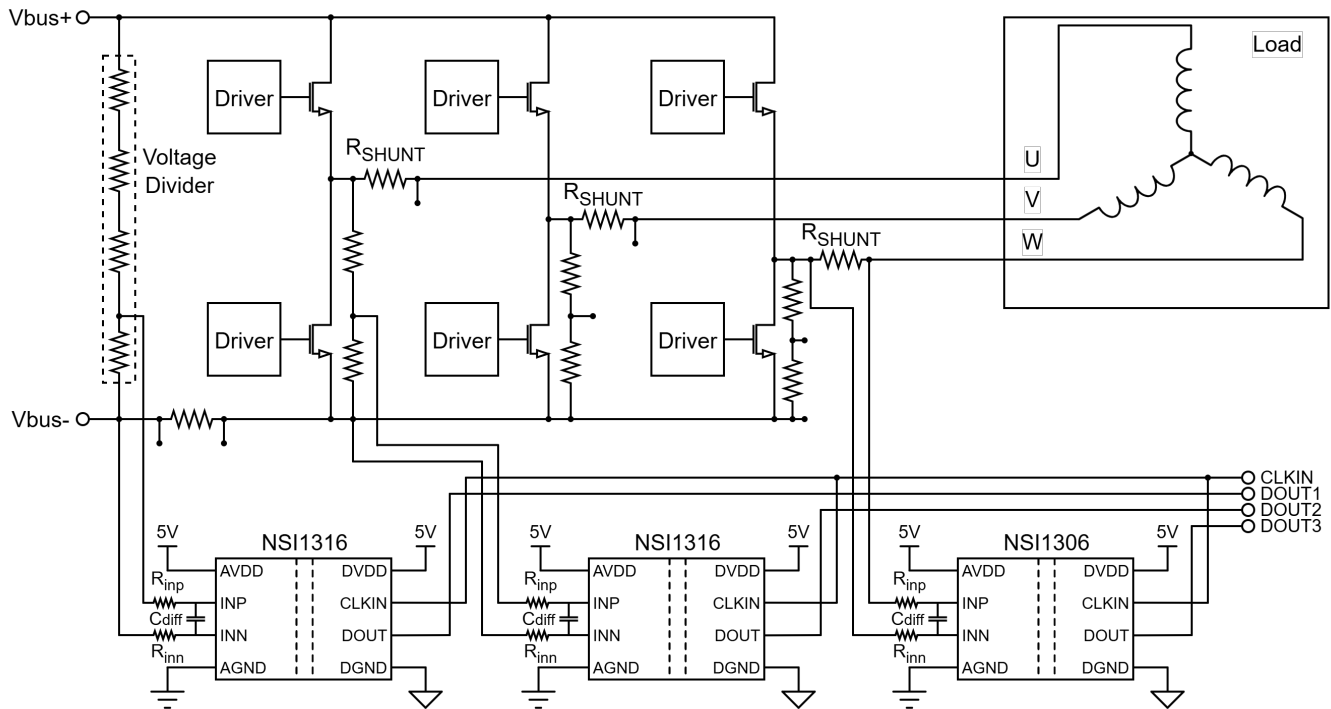


Figure 9.1 Typical Application of NSI1316 in Inverter System

9.2. Digital Filter Implementation

The Σ - Δ modulator has noise-shaping characteristics. Most of the quantization noise is pushed from a low frequency to a higher frequency to improve DC and low frequency AC accuracy. An appropriate filter should be utilized to achieve the highest accuracy.

In order to reduce higher-frequency quantization noise, the modulator output is fed to the digital low-pass filter. Subsequently, the signal of interest passes through to the output of the digital filter, while much of the higher-frequency quantization noise is filtered out.

The digital filter serves another function – decimation. It creates a digital output code from the bitstream that the modulator outputs. The ratio of the modulator rate (f_{MOD}) of the delta-sigma modulator to its output data rate (f_{DR}) is the oversampling ratio (OSR). The relationship between f_{DR} and f_{MOD} is:

$$f_{DR} = f_{MOD} / OSR \quad \text{Equation 9.1}$$

A sinc3 filter is recommended since it's simple and requires less hardware resources. Equation 9.2 describes the transfer function of a sinc filter.

$$H(Z) = \left(\frac{1}{DR} \frac{(1-Z^{-DR})}{(1-Z^{-1})} \right)^N \quad \text{Equation 9.2}$$

where:

DR is the decimation rate;

N is the sinc filter order.

The filter can be implemented in an FPGA or DSP. The sinc filter creates a digital output code by taking a multi-order moving average of the modulator output over a certain number of modulator clock periods.

The higher the decimation rate, the higher the conversion accuracy, and the lower the output data rate. So, there is a trade-off between accuracy and data rate. All the characterization in this datasheet is tested with a sinc3 filter with an oversampling ratio (OSR) of 256.

The output data size is expressed in Equation 9.3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ Size = N \times \log_2 DR \quad \text{Equation 9.3}$$

The filter characteristics for a third-order sinc filter are summarized in Table 9.1.

Table 9.1 Sinc3 Filter Characteristics for 20 MHz CLKIN

Decimation Rate (DR)	Data Output Rate (kHz)	Data Size (bits)	Filter Response (kHz)
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

9.3. PCB Layout

Figure 9.2 Shows a layout example of NSI1316. There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1316 requires a 0.1μF(C1 and C2) bypass capacitor between AVDD and AGND, DVDD and DGND. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF(C3 and C4) capacitor may be used.
- Place the sense resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1316. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.
- It is recommended to add an input capacitor C5 to the input INP pin, the value of capacitor depending on the interference conditions in the actual system.

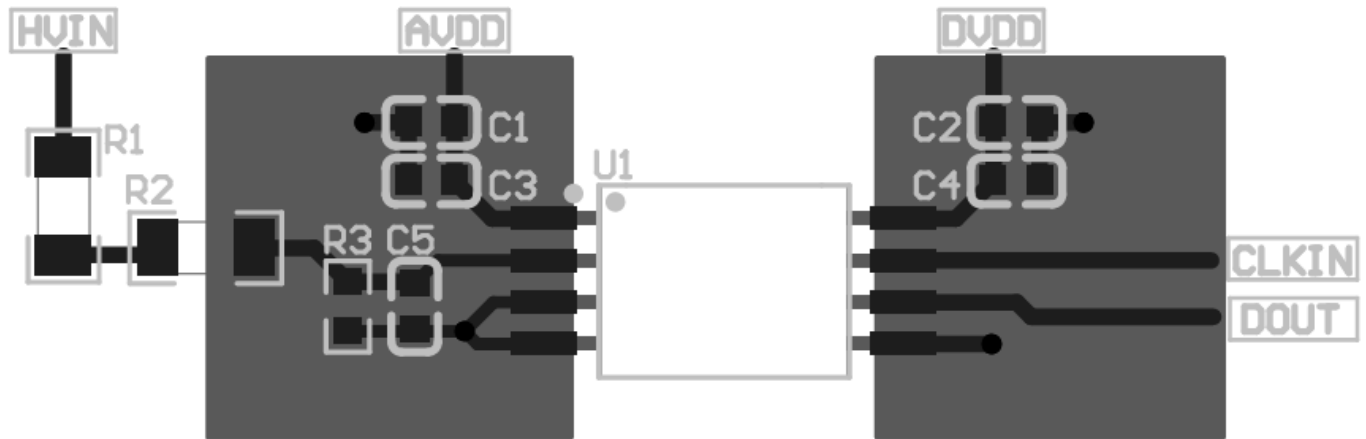
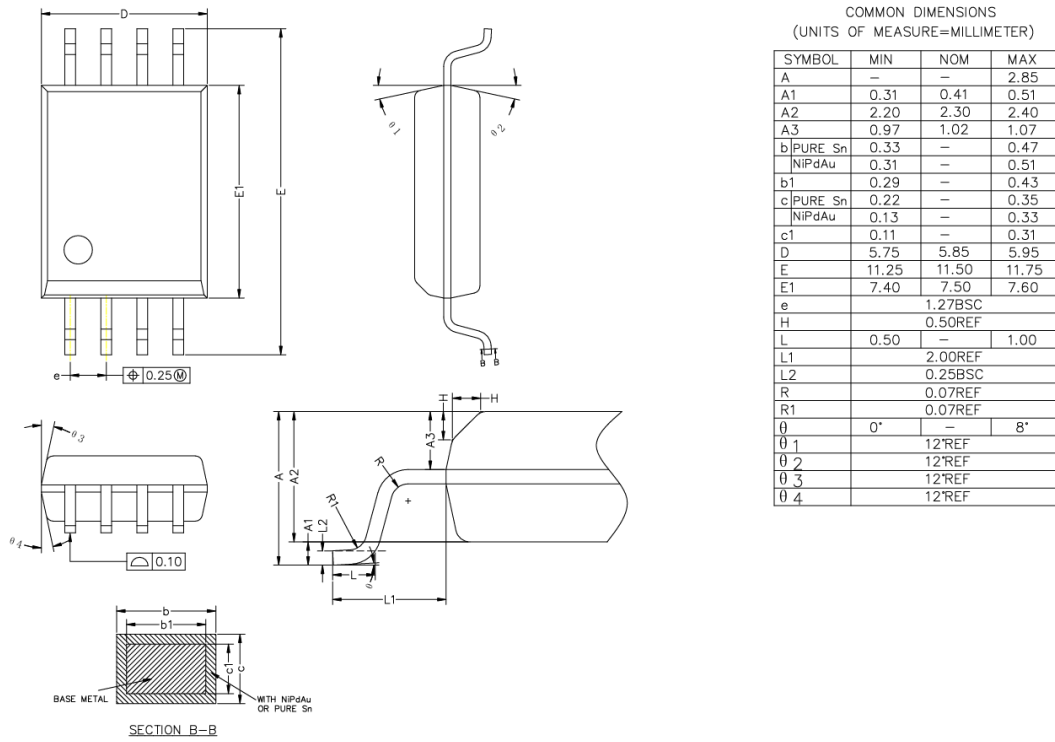


Figure 9.2 Layout Example of NSI1316

10. Package Information



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOW8 package shape and dimension in millimeters

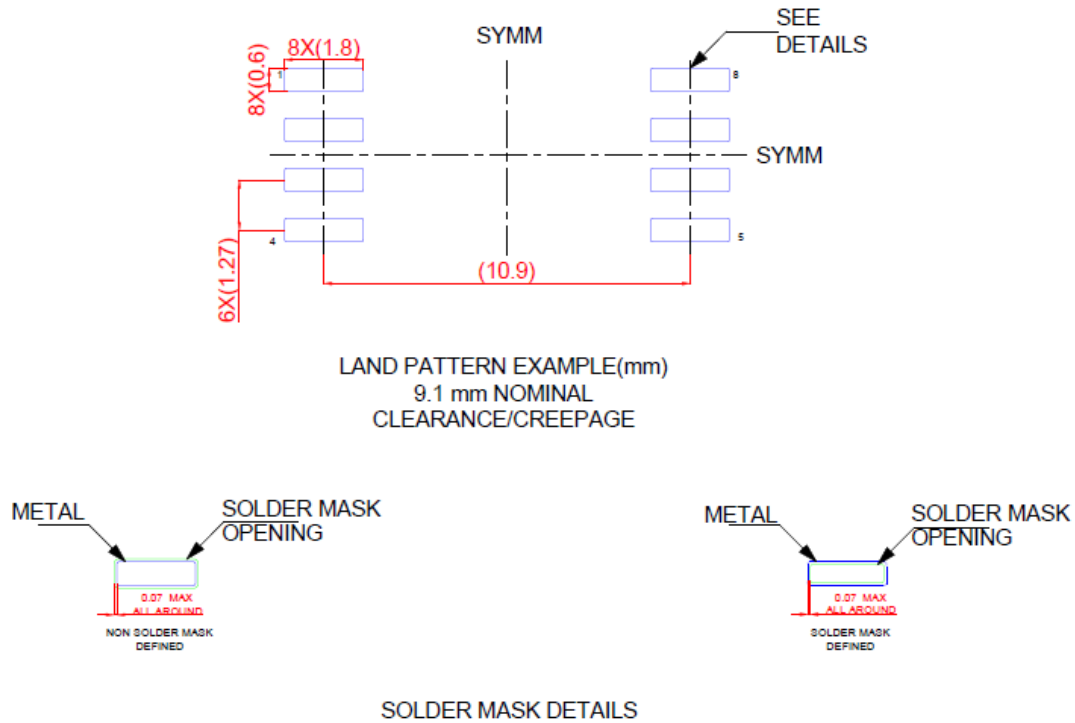


Figure 10.2 SOW8 Package Board Layout Example

11. Ordering Information

<i>Part No.</i>	<i>Isolation Rating (kV)</i>	<i>Temperature</i>	<i>MSL</i>	<i>Device Marking</i>	<i>Package Type</i>	<i>Package Drawing</i>	<i>SPQ</i>	<i>MPQ</i>
NSI1316-DSWVR	5	-40 to 125°C	3	NSi13 16D	SOP8(300mil)	SOW8	1000	1000

12. Documentation Support

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolator selection guide</i>
NSI1316	Click here	Click here	Click here	Click here

13. Tape and Reel Information

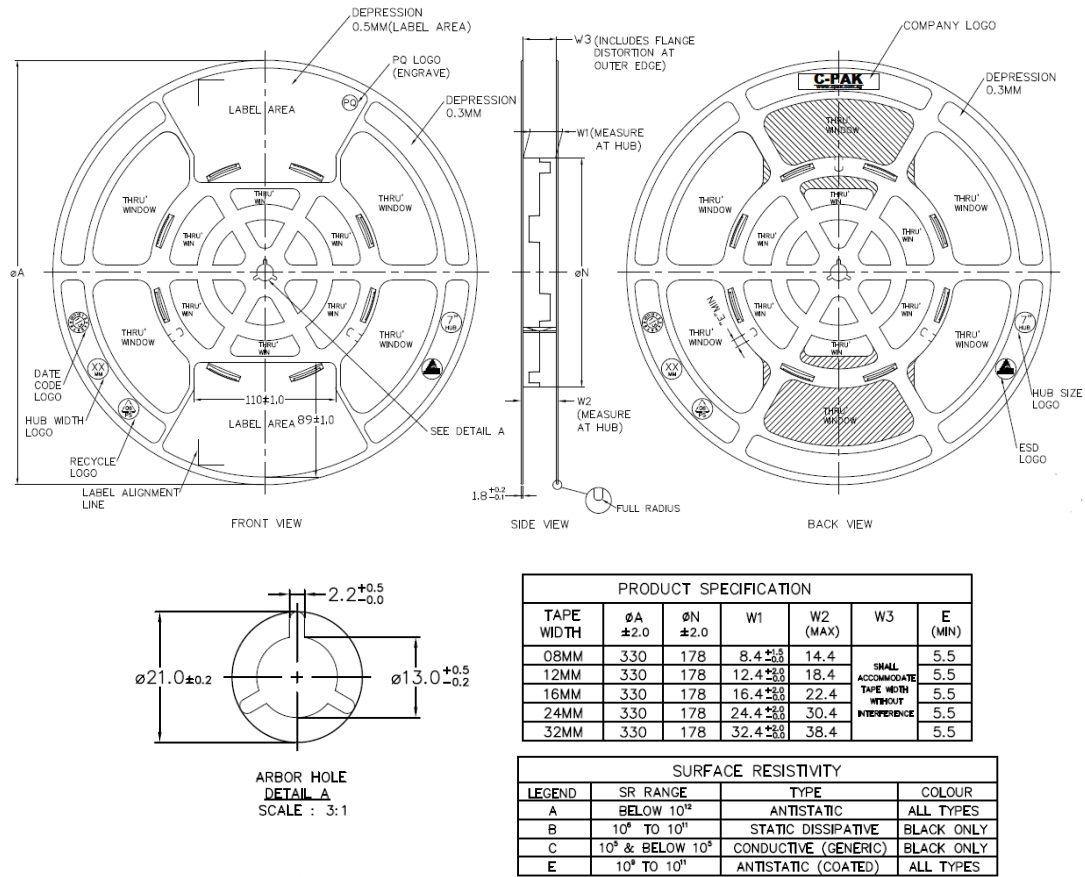


Figure 13.1 Tape Information

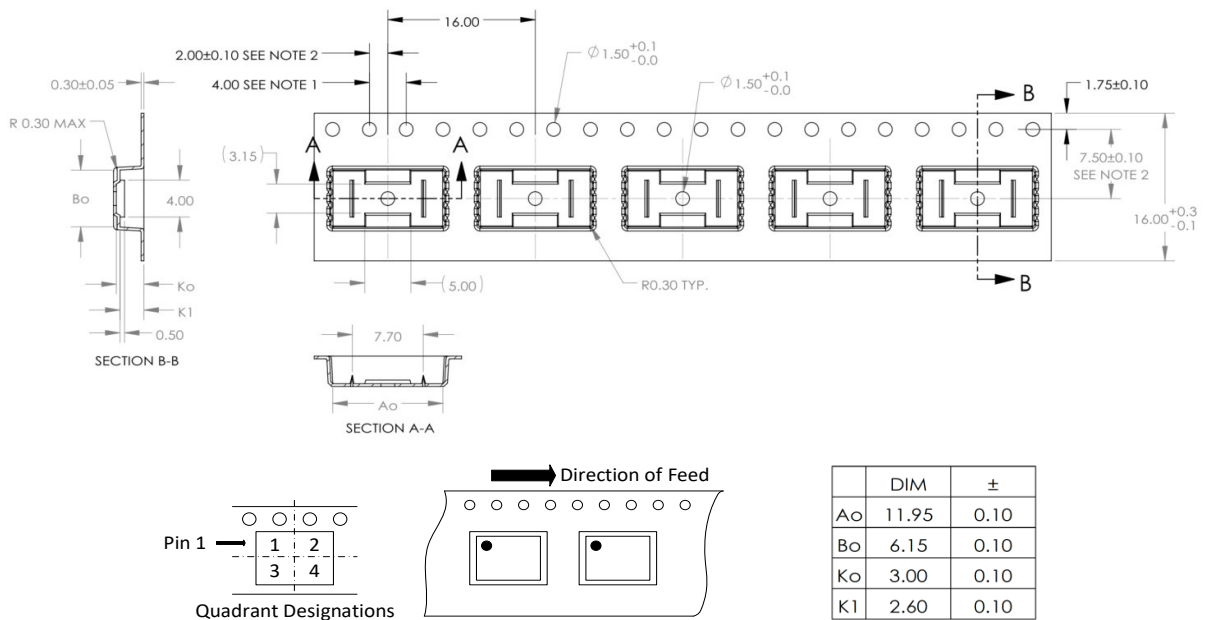


Figure 13.2 Reel Information of SOP8(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Release	2026/3/11

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