NOVOSENSE

NSI1311-DSWWAR

High Reliability Reinforced Isolated Amplifier

Datasheet (EN) 1.0

Product Overview

NSI1311-DSWWAR is a high-performance isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a single-ended input signal range from 0.02V to 2V. The high input impedance of NSI1311-DSWWAR makes it highly suitable for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

The device has a fixed gain of 1 and provides a differential analog output.

The low offset and gain drift ensure the accuracy over the entire temperature range. The high common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe function (missing VDD1 detection) simplifies system-level design and diagnostics.

Key Features

- Up to 7500V_{rms} Insulation voltage
- 0.02~2V, High-Impedance Input Voltage Range
- Fixed Gain: 1
- Low Offset Error and Drift:
  ±1.5mV (Max), 25μV/℃ (Max)
- Low Gain Error and Drift:
  ±0.3% (Max), ±45ppm/℃ (Max)
- Low Nonlinearity and Drift:
  ±0.05% (Max) for 0.02V~0.1V VIN
  ±0.04% (Max) for 0.1V~2V VIN
  ±1ppm/℃ (Typ)
- SNR: 82dB (Typ, BW=10kHz), 70dB (Typ, BW=100kHz)
- Wide bandwidth: 400kHz (Typ)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Feature:
  VDD1 monitoring
- Operation Temperature: -40℃~125℃
- AEC-Q100 qualified for automotive applications
- RoHS-Compliant Packages:
  SOP-8(600mil)

Safety Regulatory Approvals

- UL recognition: up to 7500V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A approval
- DIN VDE V 0884-17

Applications

- Bus voltage monitoring
- AC motor controls
- Power and solar inverters
- Uninterruptible Power Suppliers
- Automotive onboard chargers

Device Information

Part Number	Package	Body Size
NSI1311-DSWWAR	SOP8(600mil)	6.25 mm × 13.60mm

Functional Block Diagrams

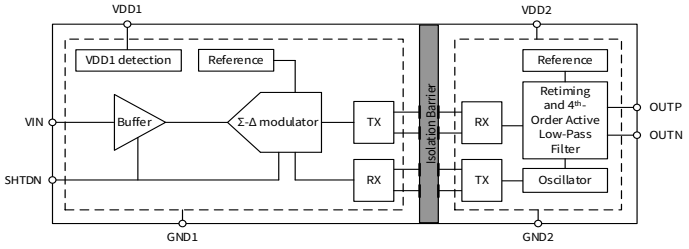

Figure 1. Block Diagram

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1. Pin Configuration and Functions

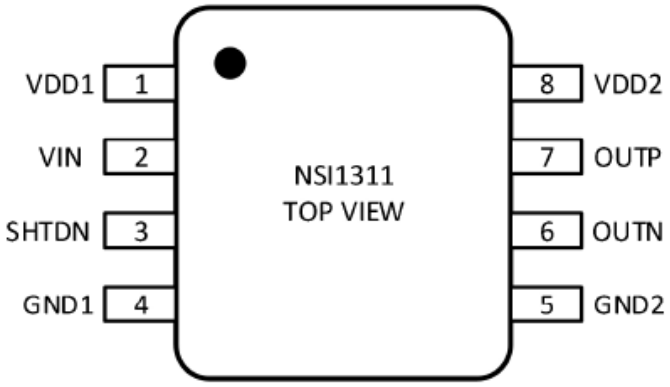


Figure 1.1 Package

Table 1.1 Pin Configuration and Description

NSI1311 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power supply for input side(3.0V to 5.5V)
2	VIN	Analog input
3	SHTDN	Shutdown input, active high, pulled up internally (typical resistor value: 100kΩ)
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for output side (3.0V to 5.5V)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	-0.3		6.5	V
Input Voltage	VIN	GND1-6		VDD1+0.5	V
	SHTDN	GND1-0.5		VDD1+0.5	
Output Voltage	OUTP, OUTN	GND2-0.5		VDD2+0.5	V
Output current per Output Pin	Io	-10		10	mA
Operating Temperature	T_{OPR}	-40		125	℃
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-55		150	℃
Electrostatic discharge	HBM (1)	±2000			V
	CDM (2)	±1000			V

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Side1 Power Supply	VDD1	3.0	5.0	5.5	V
Side2 Power Supply	VDD2	3.0	3.3	5.5	V
Differential input voltage before clipping output	$V_{Clipping}$		2.56		V
Linear differential input full scale voltage	V_{FSR}	0.02		2	V
Digital input voltage	SHTDN	GND1		VDD1	
Operating Ambient Temperature	T_A	-40		125	℃

4. Thermal Information

Parameters	Symbol	SOP8(600mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	78.9	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	41.6	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	43.6	℃/W

5. Specifications

5.1. Electrical Characteristics

(VDD1 = 3.0V~5.5V, VDD2 = 3.0V~5.5V, VIN = 0.02V to 2V, and SHTDN = GND1 = 0V, TA = -40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, TA = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1		11.4	15.1	mA	SHTDN = LOW
			0.001	1	mA	SHTDN = HIGH
Side2 Supply Current	IDD2		6.3	8.4	mA	
VDD1 undervoltage detection threshold voltage	$VDD1_{UV}$	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Input offset voltage	V_{OS}	-1.5	±0.4	1.5	mV	T_a=25℃ 4.5V≤VDD1≤5.5V VIN = 1V
Input offset drift	$\lvert dV_{OS}/dT_A \rvert$			25	μV/℃	
Input resistance	R_{IN}		1		GΩ	T_a=25℃
Input capacitance	C_{IN}		7		pF	f_{IN} = 275kHz
Input bias current	I_{IB}	-15	3.5	15	nA	T_a=25℃ VIN = GND1
Input bias current drift	TCI_{IB}		±10		pA/℃	
Analog Output						
Nominal Gain			1		V/V	
Gain error	E_G	-0.3%	±0.05%	0.3%		T_a=25℃
Gain error thermal drift	TCE_G	-45	±5	45	ppm/℃	
Nonlinearity		-0.05%	±0.01%	0.05%		T_a=25℃ 0.02V≤VIN≤0.1V
		-0.04%	±0.01%	0.04%		T_a=25℃ 0.1V≤VIN≤2V
Nonlinearity drift			±1		ppm/℃	
Total harmonic distortion	THD		-87		dB	VIN = 1.8V, f_{IN} = 10kHz, BW = 100kHz
Output noise			210		μV_{RMS}	VIN = 1V, BW = 100kHz
Signal to noise ratio	SNR	78	82		dB	VIN = 1.8V, f_{IN} = 1kHz, BW = 10kHz
			70		dB	VIN = 1.8V, f_{IN} = 10kHz, BW = 100kHz
Common-mode output voltage	V_{CMout}	1.35	1.4	1.46	V	
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.53	-2.44	V	SHTDN active, or VDD1 missing
Output Bandwidth	BW		400		kHz	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply rejection ratio (1)	$PSRR_{dc}$		-78		dB	PSRR vs VDD1, at DC
	$PSRR_{ac}$		-75		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	$PSRR_{dc}$		-82		dB	PSRR vs VDD2, at DC
	$PSRR_{ac}$		-74		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance	R_{OUT}		<0.2		Ω	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Digital Input (SHTDN)						
Input current	I_{IN}	-70		1	μA	$GND1 \le V_{SHTDN} \le VDD1$
Input capacitance	C_{IN}		5		pF	
High-level input voltage	V_{IH}	0.7*VDD1		VDD1+0.3	V	
Low-level input voltage	V_{IL}	-0.3		0.3*VDD1	V	
Timing						
Rising time of OUTP, OUTN	t_r		1.3		μs	
Falling time of OUTP, OUTN	t_f		1.3		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.6	2.1	μs	
Analog setting time	t_{AS}		0.5		ms	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling
Device enable time	t_{EN}		80	100	μs	SHTDN high to low
Shutdown time	t_{SHTDN}		1.2	5	μs	SHTDN low to high

(1) Input referred.

5.2. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5V, VDD2 = 3.3V, 0.02V to 2V, and SHTDN = GND1 = 0V, f_{IN} = 1kHz, BW = 10kHz.

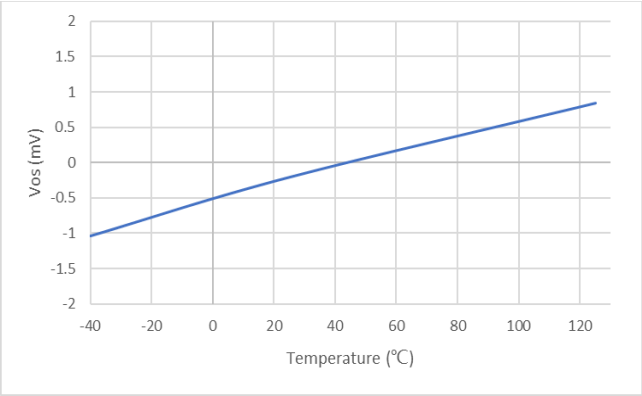


Figure 5.1 Input Offset Voltage vs Temperature

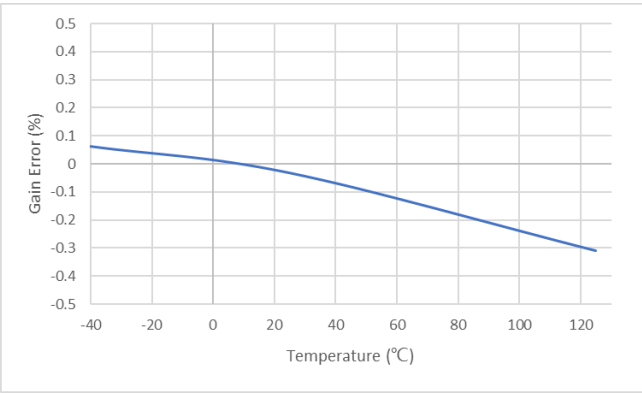


Figure 5.2 Gain Error vs Temperature

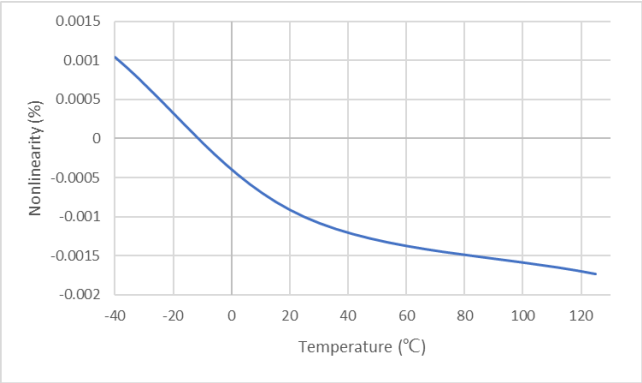


Figure 5.3 Nonlinearity vs Temperature

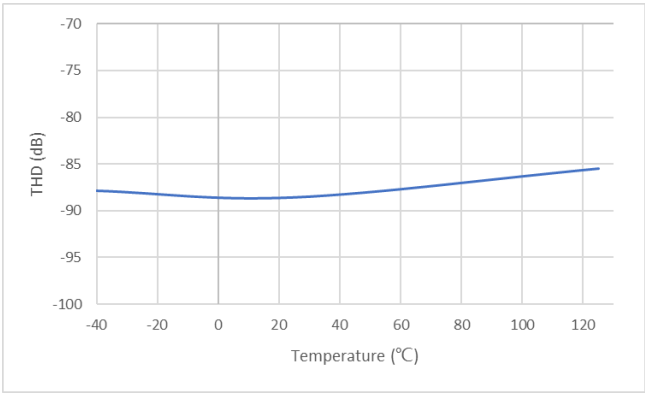


Figure 5.4 Total Harmonic Distortion vs Temperature

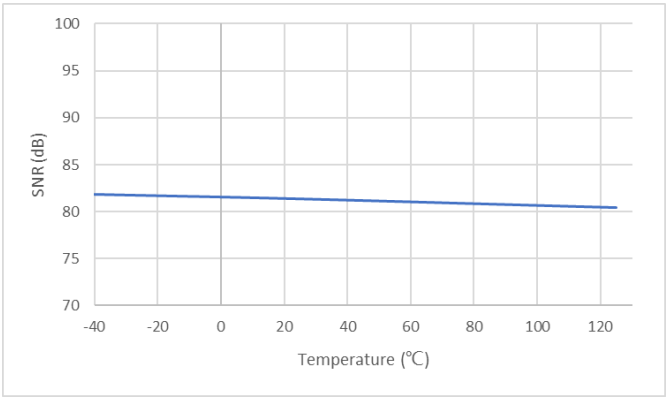


Figure 5.5 Signal-to-Noise Ratio vs Temperature

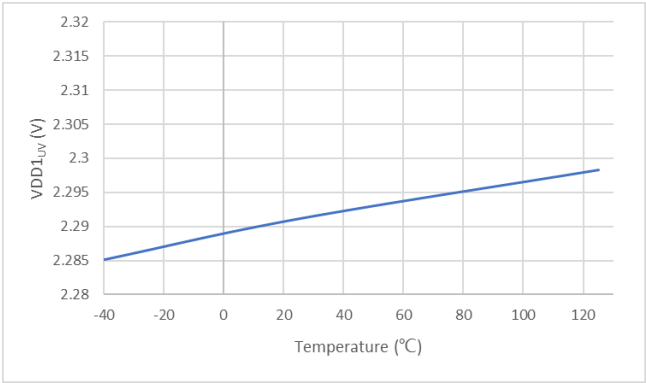


Figure 5.6 UVLO of VDD1 vs Temperature

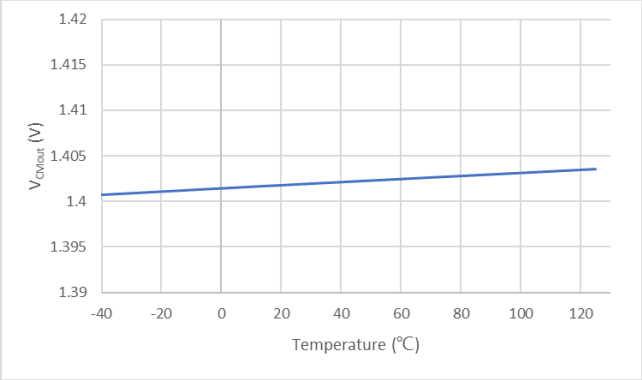


Figure 5.7 Output Common-Mode Voltage vs Temperature

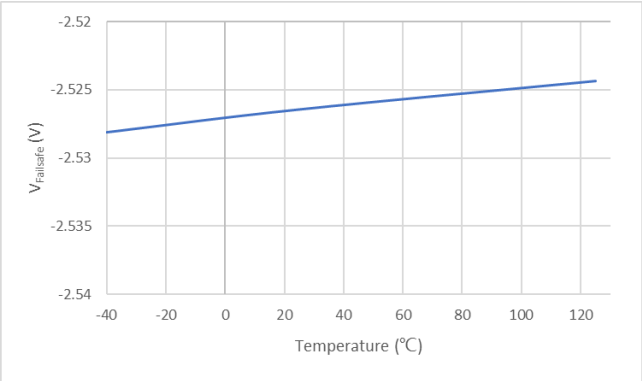


Figure 5.8 Fail-Safe Output Voltage vs Temperature

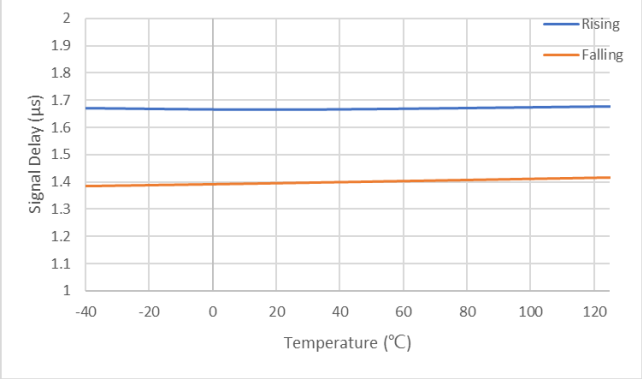


Figure 5.9 Vin to Vout Delay vs Temperature

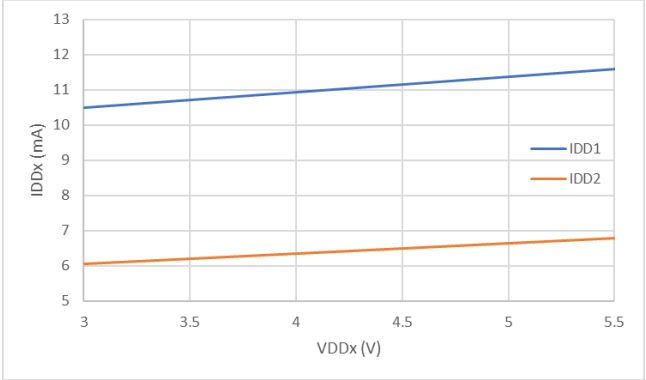


Figure 5.10 Supply Current vs Supply Voltage

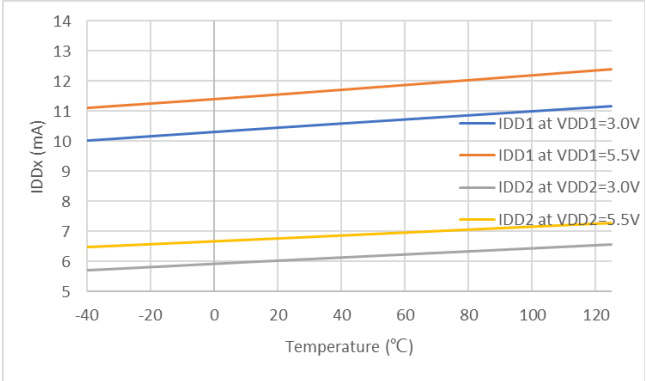


Figure 5.11 Supply Current vs Temperature

5.3. Parameter Measurement Information

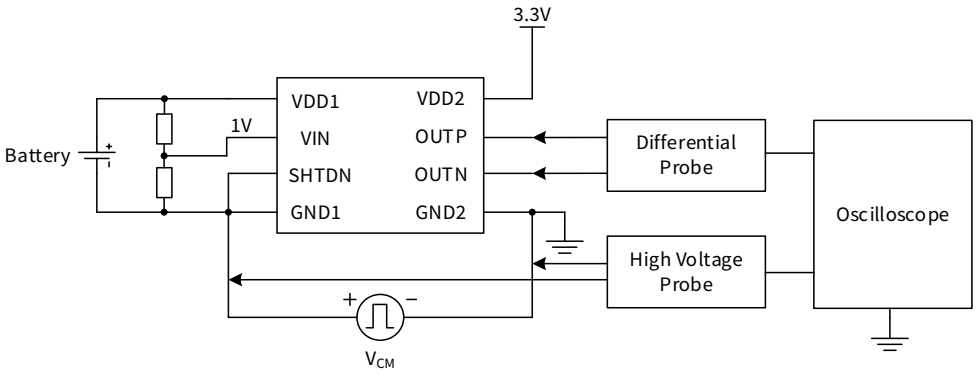


Figure 5.121 Common-Mode Transient Immunity Test Circui

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Clearance	CLR	15	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	15	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	32	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	*Test Condition*	*Value*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110,		2

6.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s			
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd(m)}$=1.875*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	10600	Vpeak
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geqslant V_{IMP} \times 1.3$	V_{IOSM}	12800	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^9	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	792	mW
Safety input, output, or supply current	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	158	mA
Maximum safety temperature		Ts	150	℃
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	7500	V_{RMS}

6.3. Regulatory Information

The NSI1311-DSWWAR are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*	*TUV*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 7500V_{rms} Isolation voltage	Single Protection, 7500V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121Vpeak VIOTM=10600Vpeak VIOSM=12800Vpeak	Reinforced insulation	7500Vrms for 1min
E500602	E500602	File (pending)	CQC24001426054	File (pending)

7. Function Description

7.1. Overview

The NSI1311-DSWWAR is a high performance isolated amplifier with a high input impedance that accept wide range single-ended input. The singled-ended input is suited to bus voltage monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ-Δ modulator in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated side1 and side2 voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the side2 and has a differential output.

SHTDN pin is used to disable the conversion. Since SHTDN is an active high signal and is pulled up by a 100kΩ (typical) internally, it should be connected to GND1 or logic LOW in normal operation.

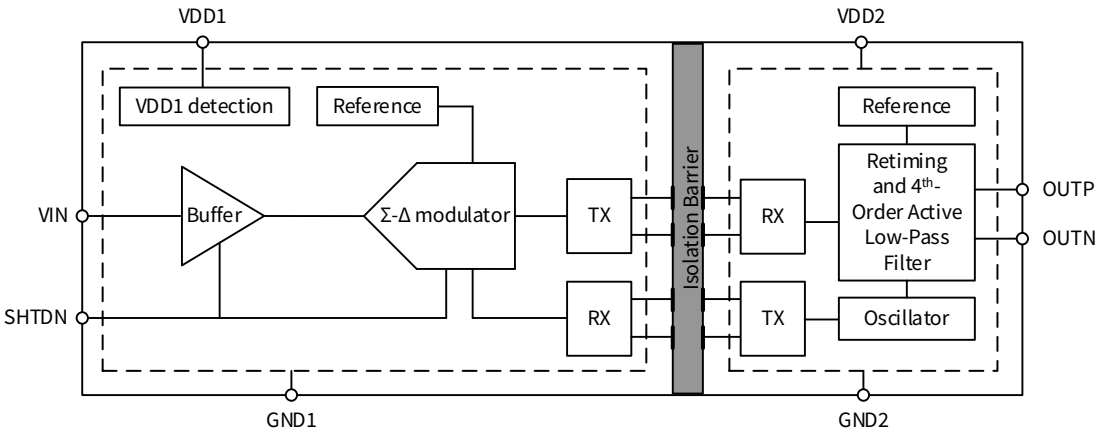


Figure 7.1 Function Block Diagram

7.2. Analog Input

There are two restrictions on the analog input signal (VIN).

- If the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR).

7.3. Analog Output

For linear input range, NSI1311-DSWWAR provides an analog differential output which has a fixed gain of 1. If a full-scale input signal is applied to the NSI1311-DSWWAR ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped, as is shown in Figure 7.2(a).

In addition, NSI1311-DSWWAR integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage shown in Figure 7.2(b), which does not occur under normal device operation and will only be activated in following conditions:

- When the undervoltage of VDD1 is detected (VDD1< $VDD1_{UV}$).
- When SHTDN signal is activated (pulled high).

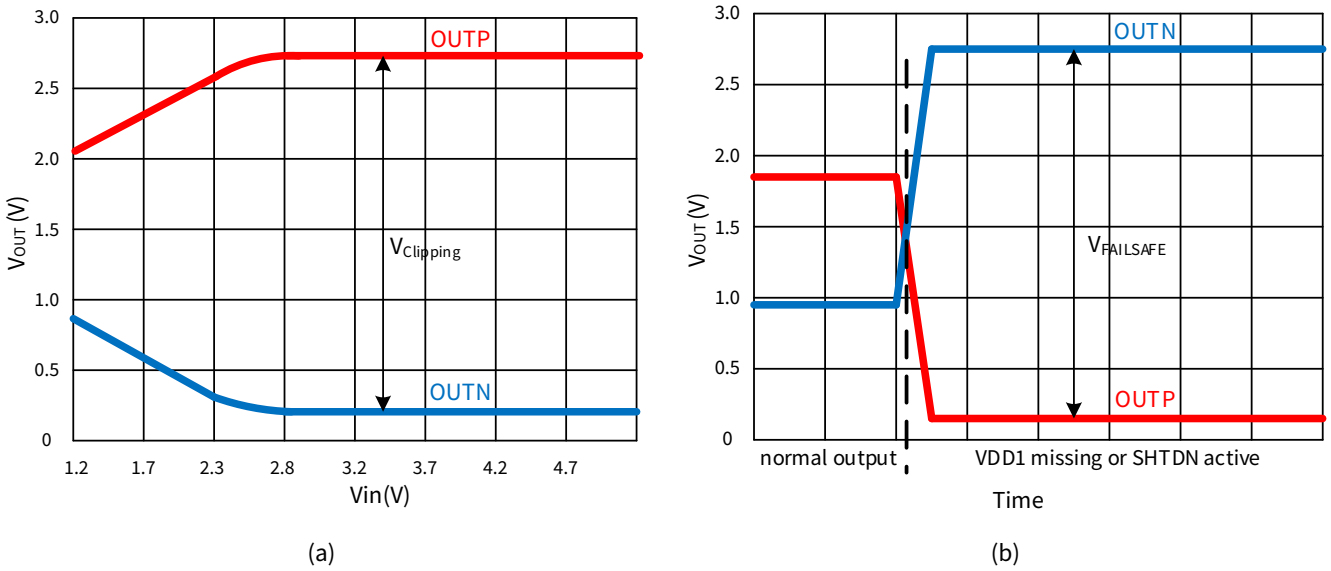


Figure 7.2 Typical Failsafe output and clipping output

8. Application Note

8.1. Typical Application Circuit

NSI1311-DSWWAR has an input impedance of up to 1GΩ, and has a wide input voltage range as well. These features make NSI1311-DSWWAR ideally suitable for isolated voltage sensing applications such as frequency inverters. The typical application circuit is shown in Figure 8.1.

The bus voltage of the frequency inverter is divided by a resistance network, and the divided voltage is applied to the input of NSI1311-DSWWAR through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

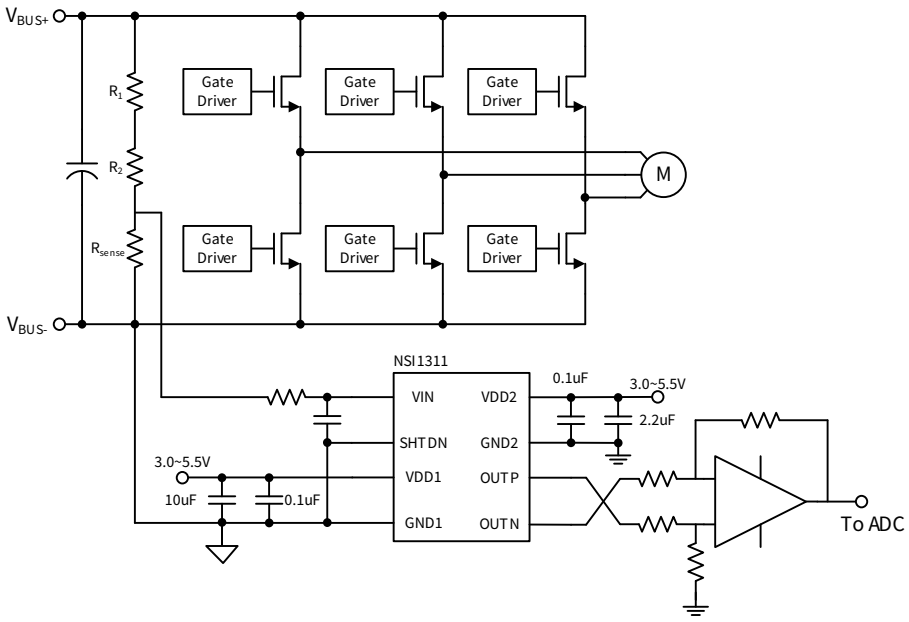


Figure 8.1 Typical application circuit in voltage sensing

8.2. Sense Resistor Selection

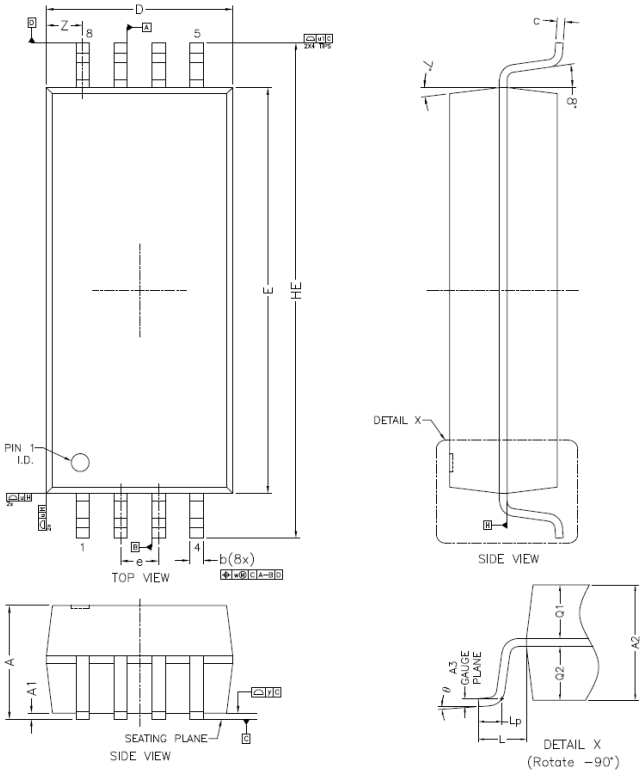
There are two other factors should be considered when selecting the sense resistor:

- The voltage-drop on R_{sense} divided by nominal V_{BUS} must not exceed the recommended linear input voltage range: $V_{IN} \leq FSR$.
- The voltage-drop on R_{sense} divided by V_{BUS} in maximum allowed overvoltage condition must not exceed the input voltage that causes a clipping output: $V_{IN} \leq V_{Clipping}$.

8.3. PCB Layout

- NSI1311-DSWWAR requires a 0.1μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.

9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	3.580	3.807	4.034
A1	0.100	0.200	0.300
A2	3.480	3.607	3.734
b	0.357	0.457	0.557
c	0.254 REF		
D	6.121	6.248	6.375
E	13.473	13.600	13.727
HE	16.360	16.610	16.860
Q1	1.6515	1.6765	1.7015
Q2	1.6515	1.6765	1.7015
e	1.27 BSC		
A3	0.25 BSC		
L	1.505 REF		
Lp	0.635	--	--
w	0.25		
y	0.10		
u	0.10		
u1	0.20		
Z	0.525		
θ	0°	--	8°

Figure 9.1 SOP8(600mil)/SOWW8 Package Shape and Dimension in millimeters

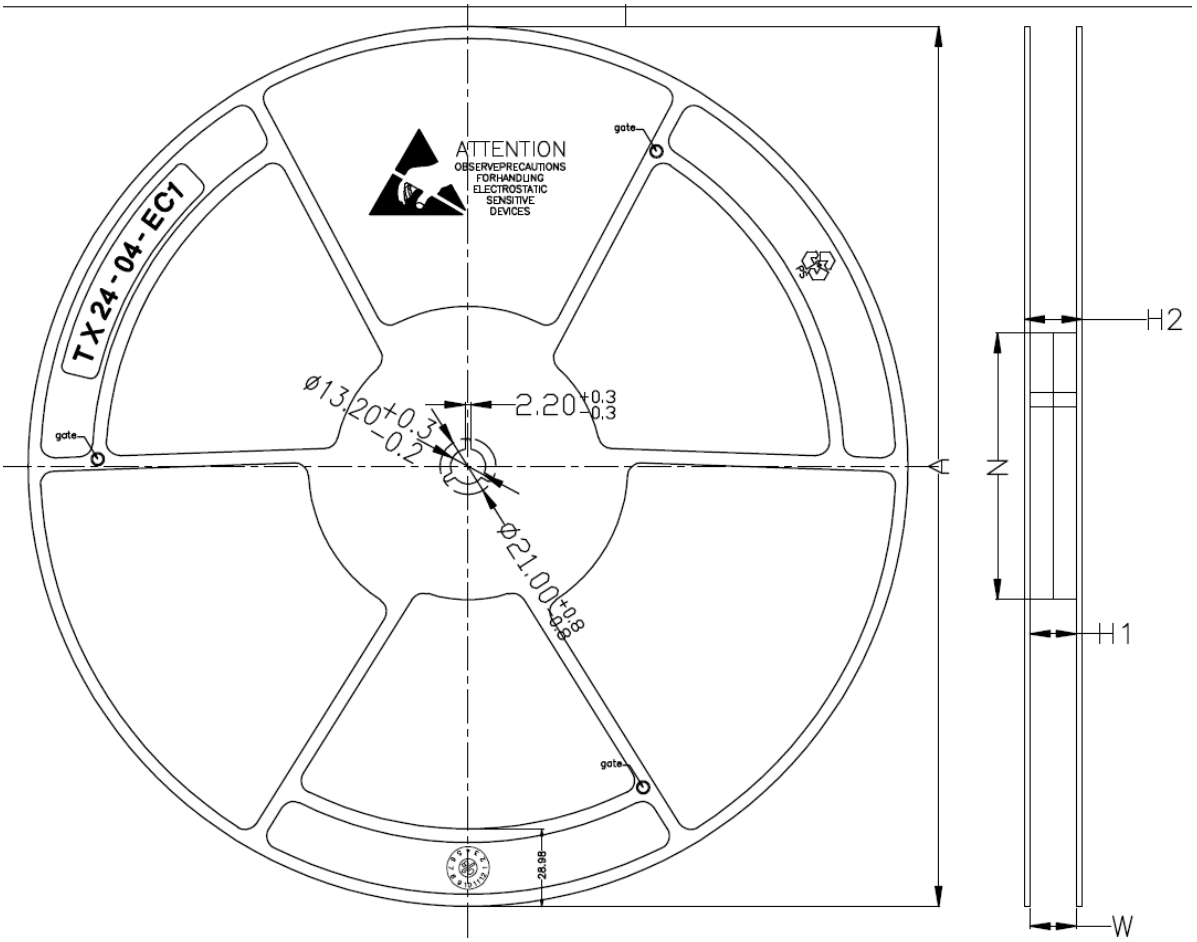
10. Ordering Information

Part No.	*Isolation Rating(kV)*	*Linear Input Range(V)*	*Moisture Sensitivity Level*	*Temperature*	*Automotive*	*Package Type*	*Package Drawing*	*SPQ*
NSI1311 - DSWWAR	7.5	0.02-2	Level-3	-40 to 125℃	NO	SOP8 (600mil)	SOWW8	1000

11. Documentation Support

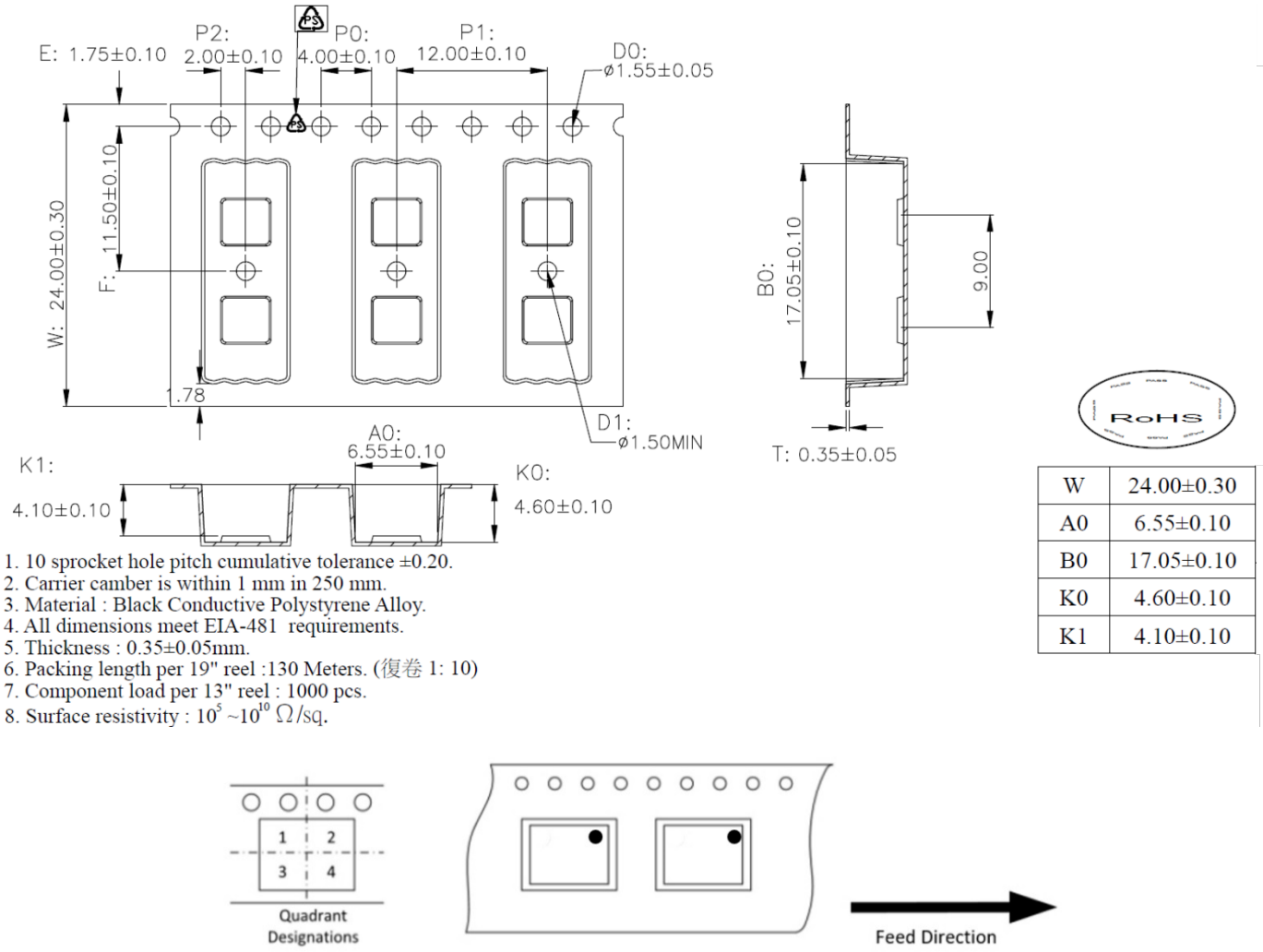
Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI1311-DSWWAR	Click here	Click here	Click here	Click here

12. Tape and Reel Information



PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA $^{+2}_{-2}$	øN $^{+2}_{-2}$	H1 $^{+2}_{-0}$	H2 $^{+1}_{-1}$	W $^{+3.5}_{-0.2}$
24MM	330	100	24.4	28.6	24.4

NOTES:
1.MATERIAL:DISSIPATIVE(BLACK)
2.FLANGE WARPAGE:3 MM MAXIMUM 5
3.ALL DIMENSIONS ARE IN MM
4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5.GENERAL TOLERANCE: ±0.25 MM



W	24.00±0.30
A0	6.55±0.10
B0	17.05±0.10
K0	4.60±0.10
K1	4.10±0.10

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.35±0.05mm.
6. Packing length per 19" reel :130 Meters. (復卷 1: 10)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : 10^5 ~10^{10} Ω/sq.

Figure 12.1 Tape and Reel Information of SOP8(600mil)

13. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/9/24

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