NOVOSENSE

NSI1305

High Reliability Reinforced Isolated Sigma-Delta Modulator

Datasheet (EN) 1.2

Product Overview

The NSI1305 is a high performance Σ-Δ modulator with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of ±50mV (±64mV full-scale) or ±250mV (±320mV full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The analog input is amplified and continuously sampled by a second-order Σ-Δ modulator and converted to a high speed, single bit data stream. The output data is synchronous to the external clock with a frequency range from 5MHz to 21MHz. By using an appropriate digital filter (such as sinc3 filter) to decimate the bitstream, the device can achieve 16 bits resolution and an 86dB/82.5dB signal to noise ratio (SNR) at 78.125kSPS with a 20MHz master clock.

The fail-safe functions including input common-mode overvoltage detection and missing AVDD detection simplify system-level design and diagnostics.

Key Features

- Up to 5700V_{RMS} Insulation Voltage
- Clock frequency: 5MHz to 21MHz
- ±50mV or ±250mV Linear Input Voltage Range
- Excellent DC Performance:
  - Offset Error: ±50μV or ±100μV (Max)
  - Offset Drift: -1~1μV/°C (Max)
  - Gain Error: ±0.2% (Max)
  - Gain Drift: ±40ppm/°C (Max)
- SNR: 82.5dB or 86dB (Typ)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Features:
  - AVDD monitoring
  - Input common-mode overvoltage detection
- Operation Temperature: -40°C~125°C
- RoHS-Compliant Packages:
  - SOW8 wide body (SOP8 300mil)
  - SOW16 wide body (SOP16 300mil)

Safety Regulatory Approvals

- UL recognition per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Shunt current monitoring
- AC motor controls
- Power and solar inverters
- Uninterruptible Power Suppliers
- Automotive onboard chargers

Device Information

Part Number	*Package*	*Body Size*
NSI1305x-DSWVR	SOP8(300mil)	5.85mm × 7.50mm
NSI1305x-DSWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

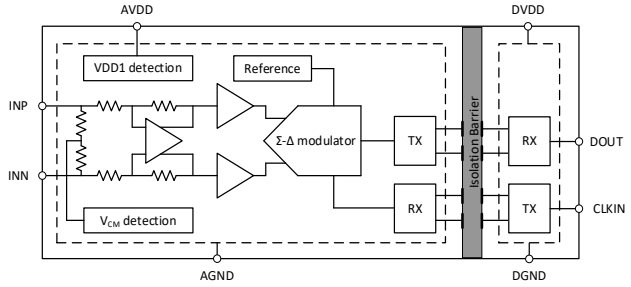

Figure 1. NSI1305 Block Diagram

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1. Pin Configuration and Functions

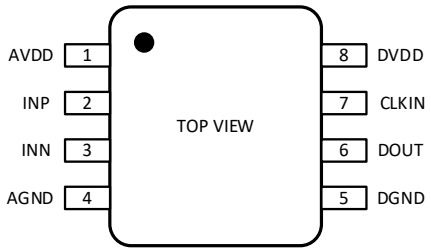


Figure 1.1 NSI1305 Package (SOP8(300mil))

Table 1.1 NSI1305 Pin Configuration and Description

NSI1305 PIN NO.	*SYMBOL*	*FUNCTION*
1	AVDD	Power supply for analog side (3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1305M25 and ±50mV recommended for NSI1305M05)
3	INN	Negative analog input
4	AGND	Analog ground reference
5	DGND	Digital ground reference
6	DOUT	Modulator data output
7	CLKIN	Modulator clock input: 5~21MHz
8	DVDD	Power supply for digital side (3.0V to 5.5V)

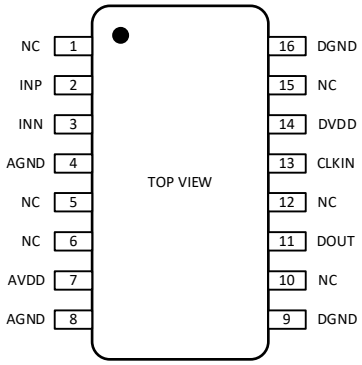


Figure 1.2 NSI1305 Package (SOP16(300mil))

Table 1.2 NSI1305 Pin Configuration and Description

NSI1305 PIN NO.	*SYMBOL*	*FUNCTION*
1	NC	Internally connected to AVDD, this pin can be left floating or tied to AVDD
2	INP	Positive analog input (±250mV recommended for NSI1305M25 and ±50mV recommended for NSI1305M05)
3	INN	Negative analog input
4	AGND/NC	Not internally connected. This pin can be tied to AGND, or leave floating.
5	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
6	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
7	AVDD	Power supply for analog side (3.0V to 5.5V)
8	AGND	Analog ground reference
9	DGND	Digital ground reference
10	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
11	DOUT	Modulator data output
12	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
13	CLKIN	Modulator clock input: 5~21MHz
14	DVDD	Power supply for digital side (3.0V to 5.5V)
15	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
16	DGND	Digital ground reference

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	AVDD, DVDD	-0.3		6.5	V
Analog Input Voltage	INP, INN	AGND-6		AVDD+0.5	V
Digital Input Voltage	CLKIN	DGND-0.5		DVDD+0.5	V
Digital Output Voltage	DOUT	DGND-0.5		DVDD+0.5	V
Output current per Output Pin	Io	-10		10	mA
Operating Temperature	T_{OPR}	-40		125	°C
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{STG}	-55		150	°C

3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Unit
Analog Side Power Supply		AVDD	3.0	5.0	5.5	V
Digital Side Power Supply		DVDD	3.0	3.3	5.5	V
NSI1305M05	Differential input voltage before clipping output	$V_{Clipping}$		±64		mV
	Linear differential input full scale voltage	V_{FSR}	-50		50	mV
	Operating common-mode input voltage	V_{CM}	-0.032		0.8	V
NSI1305M25	Differential input voltage before clipping output	$V_{Clipping}$		±320		mV
	Linear differential input full scale voltage	V_{FSR}	-250		250	mV
	Operating common-mode input voltage	V_{CM}	-0.16		0.8	V
Operating Ambient Temperature		T_A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP8(300mil)	SOP16(300mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	86	82	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	42	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	46	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	4	12	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	42	46	°C/W

6. Specifications

6.1. Electrical Characteristics: NSI1305M05

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -50mV to +50mV, and INN = AGND = 0V, T_A = -40°C to 125°C and $sinc^3$ filter with OSR=256. Unless otherwise noted, Typical values are at CLKIN=20MHz, AVDD = 5V, DVDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.5	15	mA	
Digital Side Supply Current	IDVDD		2	3	mA	
AVDD undervoltage detection threshold voltage	$AVDD_{UV}$	2	2.5	3	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	$CMRR_{dc}$		-95		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-99		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		4.75		kΩ	INN = AGND
Differential input resistance	R_{IND}		4.9		kΩ	
Input capacitance	C_I		2		pF	
Input bias current	I_{IB}	-24	-23	-20	μA	T_A = 25°C, INP = INN = AGND, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±2		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
DC Accuracy						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	E_O	-50	±2.5	50	μV	T_A = 25°C, INP = INN = AGND
Offset error thermal drift	TCE_O	-0.5	±0.15	0.5	μV/°C	
Gain error	E_G	-0.2%	±0.005%	0.2%		T_A = 25°C
Gain error thermal drift	TCE_G	-30	±10	30	ppm/°C	
Power supply rejection ratio	PSRR		-106		dB	PSRR vs AVDD, at DC
			-104		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR	78	82.5		dB	f_{IN} = 1kHz
Signal to noise and distortion	SINAD	77	82.5		dB	f_{IN} = 1kHz
Total harmonic distortion	THD		-96	-84	dB	f_{IN} = 1kHz
Spurious-free dynamic range	SFDR	86	100		dB	f_{IN} = 1kHz
Digital Input / Output						
Input current	I_{IN}	-9		1	μA	DGND ≤ V_{IN} ≤ DVDD
Input capacitance	C_{IN}		5		pF	
Output load capacitance	C_{LOAD}		30		pF	
High-level input voltage	V_{IH}	0.7×DVDD		DVDD+0.3	V	
Low-level input voltage	V_{IL}	-0.3		0.3×DVDD	V	
High-level output voltage	V_{OH}	DVDD-0.1			V	I_{OH} = -20μA
		DVDD-0.4			V	I_{OH} = -4mA
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 20μA
				0.4	V	I_{OL} = 4mA
Timing						
CLKIN clock frequency	f_{CLKIN}	5		21	MHz	
CLKIN clock duty ratio	Duty	40	50	60	%	
CLKIN clock high time	t_{HIGH}	20	25	120	ns	
CLKIN clock low time	t_{LOW}	20	25	120	ns	
DOUT rising time	t_r			5	ns	C_{LOAD} = 15pF
DOUT falling time	t_f			5	ns	C_{LOAD} = 15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
DOUT hold time after rising edge of CLKIN	t_H	3.5			ns	C_{LOAD} = 15pF
Rising edge of CLKIN to DOUT valid delay	t_D			15	ns	C_{LOAD} = 15pF
Analog setting time	t_{AS}		0.5		ms	AVDD step to 3.0 V with DVDD ≥ 3.0 V, to DOUT valid, 0.1% settling

6.2. Electrical Characteristics: NSI1305M25

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = AGND = 0V, T_A = -40°C to 125°C and $sinc^3$ filter with OSR=256. Unless otherwise noted, Typical values are at CLKIN=20MHz, AVDD = 5V, DVDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.4	15.1	mA	
Digital Side Supply Current	IDVDD		1.78	3	mA	
AVDD undervoltage detection threshold voltage	$AVDD_{UV}$	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	$CMRR_{dc}$		-106		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-104		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		19		kΩ	INN = AGND
Differential input resistance	R_{IND}		22		kΩ	
Input capacitance	C_I		2		pF	
Input bias current	I_{IB}	-24	-18	-12	μA	T_A = 25°C, INP = INN = AGND, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±2		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Offset error	E_O	-100	±4.5	100	μV	T_A = 25°C, INP = INN = AGND
Offset error thermal drift	TCE_O	-1	±0.15	1	μV/°C	
Gain error	E_G	-0.2%	±0.005 %	0.2%		T_A = 25°C
Gain error thermal drift	TCE_G	-40	±20	40	ppm/°C	
Power supply rejection ratio	PSRR		-100		dB	PSRR vs AVDD, at DC
			-90		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR	82	86		dB	f_{IN} = 1kHz
Signal to noise and distortion	SINAD	80	84		dB	f_{IN} = 1kHz
Total harmonic distortion	THD		-90	-80	dB	f_{IN} = 1kHz
Spurious-free dynamic range	SFDR	82	92		dB	f_{IN} = 1kHz
Digital Input / Output						
Input current	I_{IN}	-9		1	μA	DGND ≤ V_{IN} ≤ DVDD
Input capacitance	C_{IN}		5		pF	
Output load capacitance	C_{LOAD}		30		pF	
High-level input voltage	V_{IH}	0.7×DVDD		DVDD+0.3	V	
Low-level input voltage	V_{IL}	-0.3		0.3×DVDD	V	
High-level output voltage	V_{OH}	DVDD-0.1			V	I_{OH} = -20μA
		DVDD-0.4			V	I_{OH} = -4mA
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 20μA
				0.4	V	I_{OL} = 4mA
Timing						
CLKIN clock frequency	f_{CLKIN}	5		21	MHz	
CLKIN clock duty ratio	Duty	40	50	60	%	
CLKIN clock high time	t_{HIGH}	20	25	120	ns	
CLKIN clock low time	t_{LOW}	20	25	120	ns	
DOUT rising time	t_r			5	ns	C_{LOAD} = 15pF
DOUT falling time	t_f			5	ns	C_{LOAD} = 15pF
DOUT hold time after rising edge of CLKIN	t_H	3.5			ns	C_{LOAD} = 15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Rising edge of CLKIN to DOUT valid delay	t_D			15	ns	C_{LOAD} = 15pF
Analog setting time	t_{AS}		0.5		ms	AVDD step to 3.0 V with DVDD ≥ 3.0 V, to DOUT valid, 0.1% settling

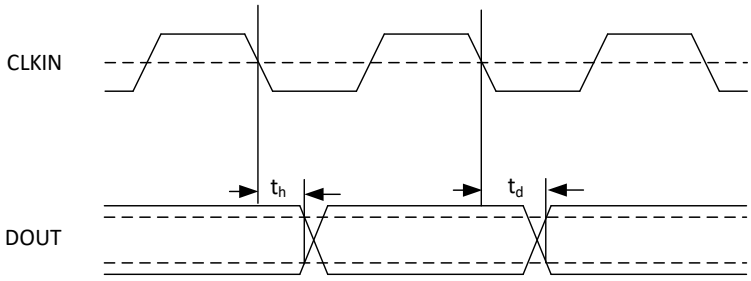


Figure 6.1 Digital Input and Output Timing

6.3. Typical Performance Characteristics

Unless otherwise noted, test at AVDD = 5V, DVDD = 3.3V, Vin = -250mV to 250mV (NSI1305M25) or -50mV to 50mV (NSI1305M05), CLKIN=20MHz, and sinc^3 filter with OSR=256.

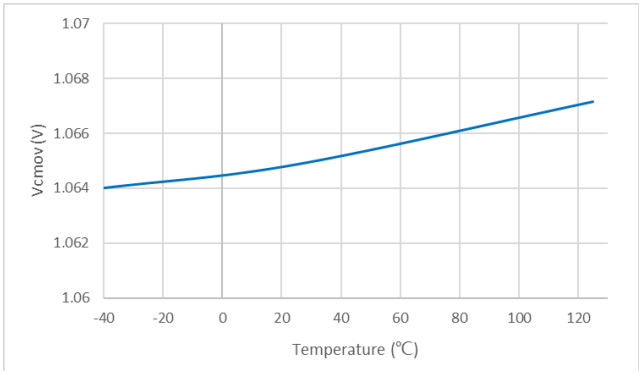


Figure 6.2 Common-Mode Overvoltage Detection Level vs Temperature

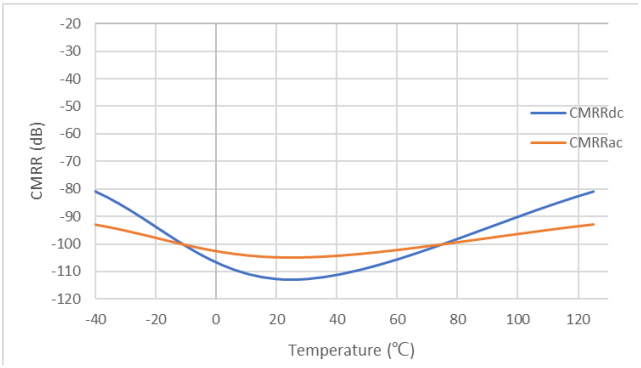


Figure 6.4 Common-Mode Rejection Ratio vs Temperature

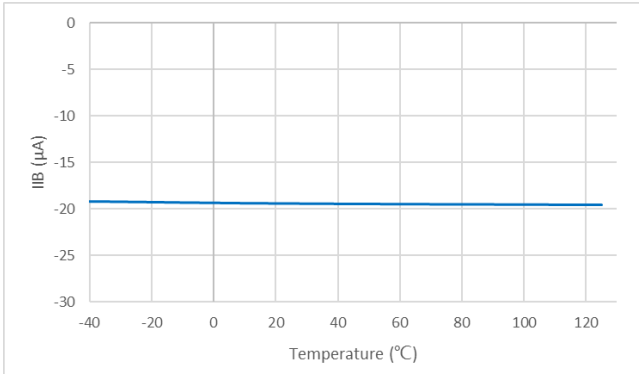


Figure 6.3 Input Bias Current vs Temperature

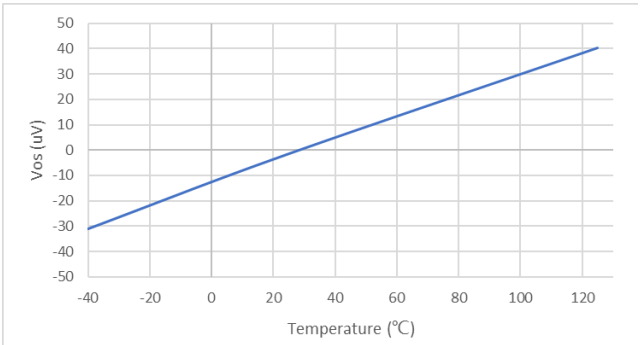


Figure 6.5 Input Offset Voltage vs Temperature

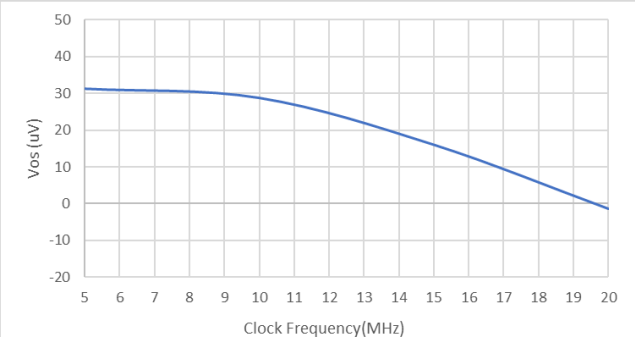


Figure 6.6 Input Offset Voltage vs Clock Frequency

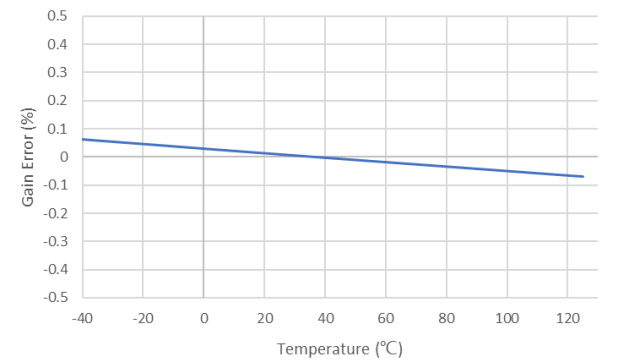


Figure 6.7 Gain Error vs Temperature

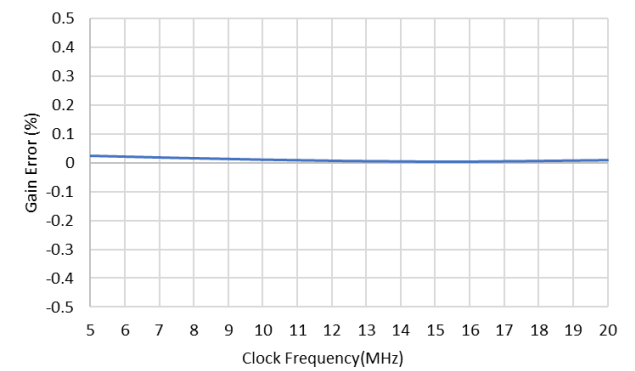


Figure 6.8 Gain Error vs Clock Frequency

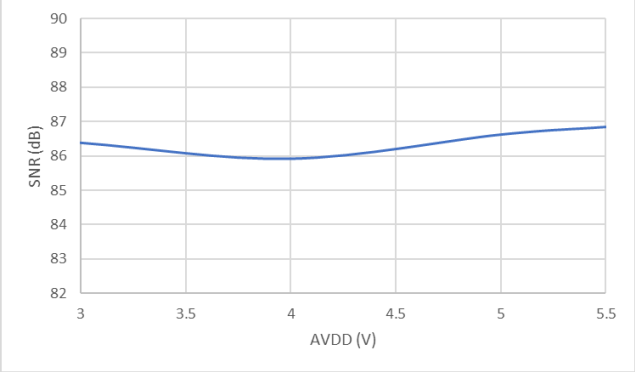


Figure 6.9 Signal-to-Noise Ratio vs Analog Side Supply Voltage

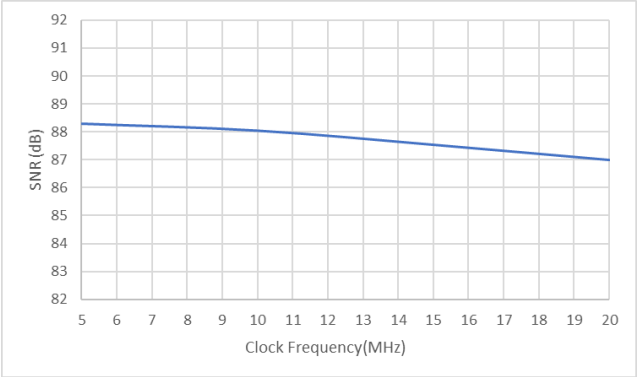


Figure 6.10 Signal-to-Noise Ratio vs Clock Frequency

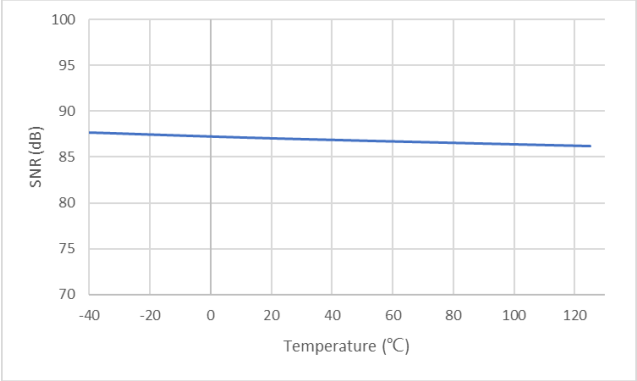


Figure 6.11 Signal-to-Noise Ratio vs Temperature

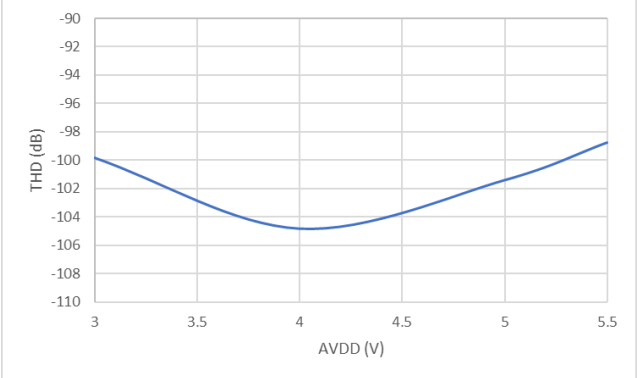


Figure 6.12 Total Harmonic Distortion vs Analog Side Supply Voltage

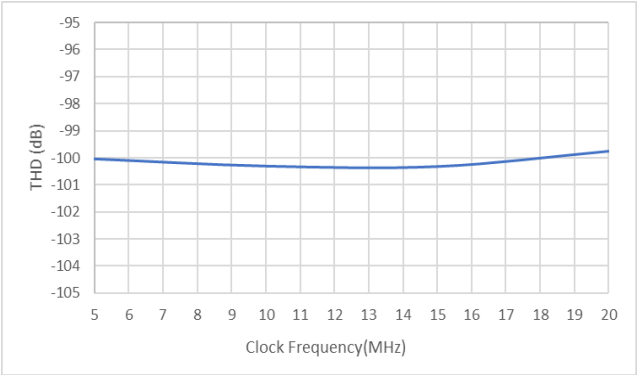


Figure 6.13 Total Harmonic Distortion vs Clock Frequency

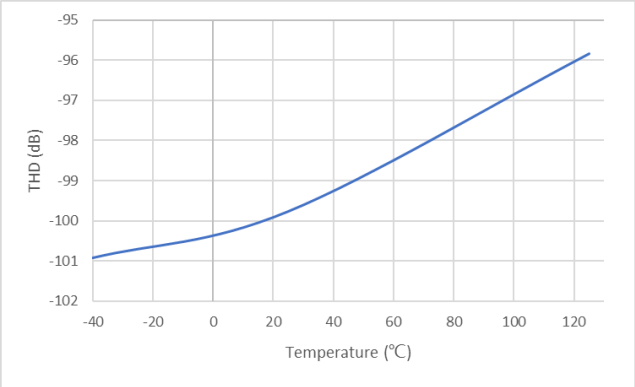


Figure 6.14 Total Harmonic Distortion vs Temperature

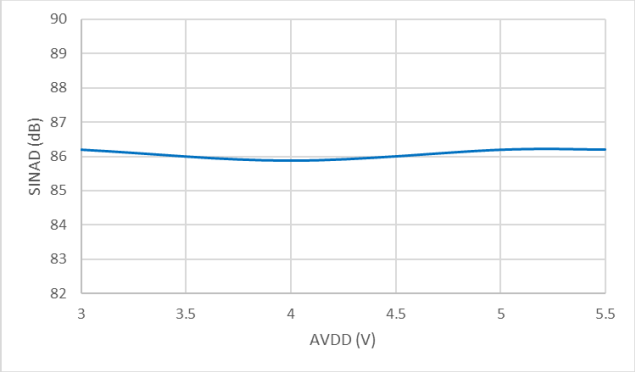


Figure 6.15 Signal-to-Noise + Distortion vs Analog Side Supply Voltage

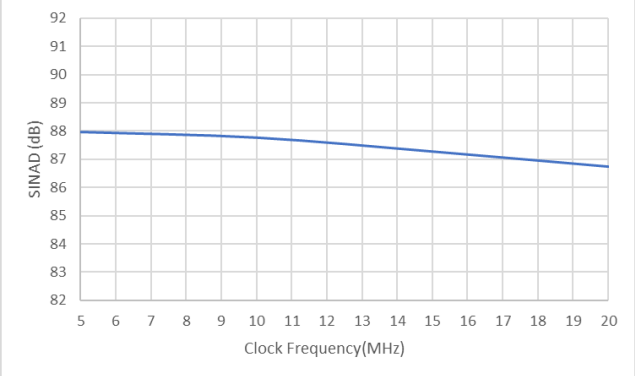


Figure 6.16 Signal-to-Noise + Distortion vs Clock Frequency

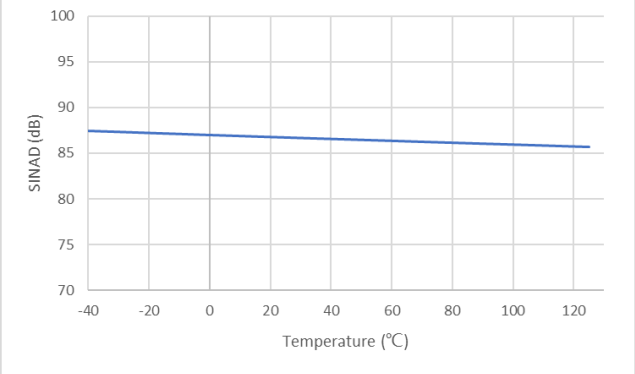


Figure 6.17 Signal-to-Noise + Distortion vs Temperature

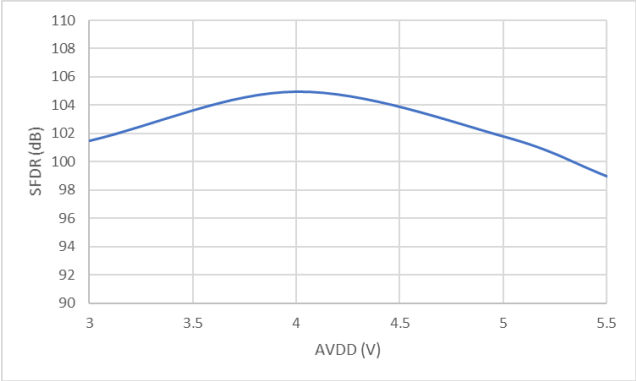


Figure 6.18 Spurious-Free Dynamic Range vs Analog Side Supply Voltage

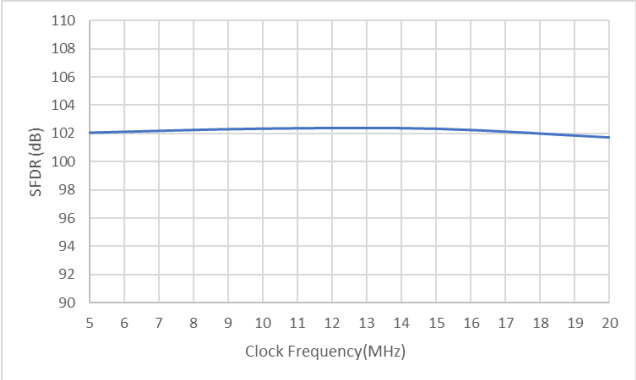


Figure 6.19 Spurious-Free Dynamic Range vs Clock Frequency

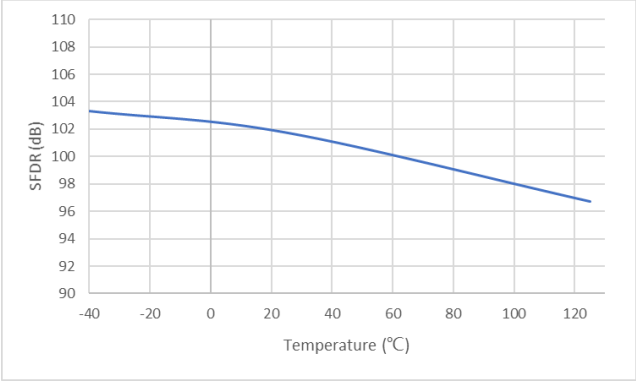


Figure 6.20 Spurious-Free Dynamic Range vs Temperature

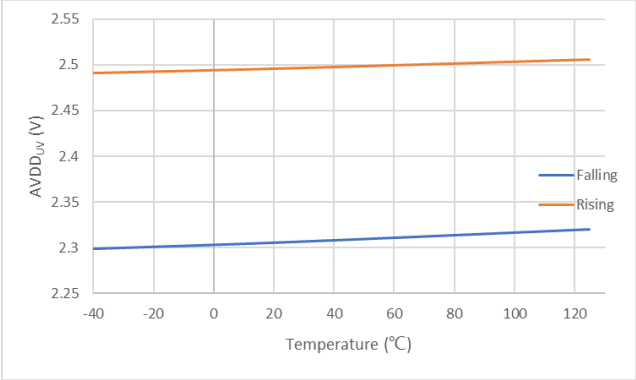


Figure 6.21 Analog Side Under-Voltage Detection Level vs Temperature

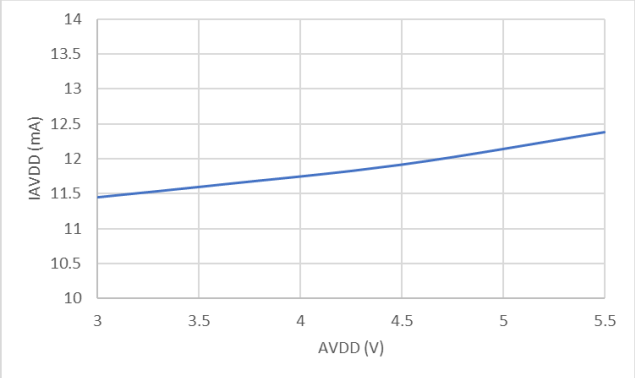


Figure 6.22 Analog Side Supply Current vs Supply Voltage

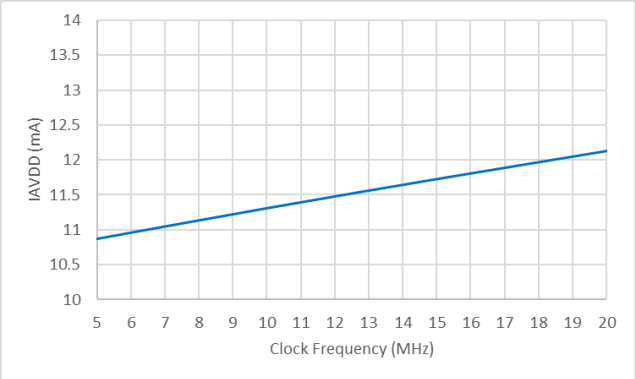


Figure 6.23 Analog Side Supply Current vs Clock Frequency

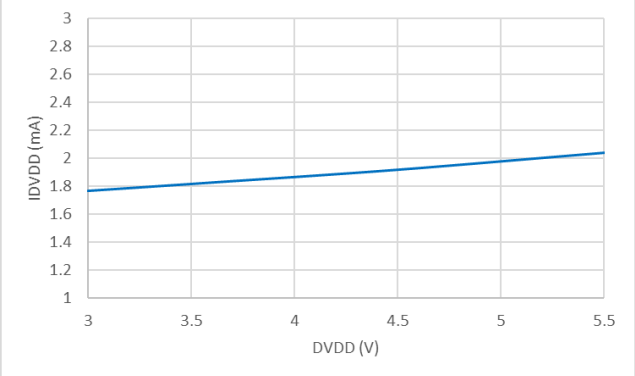


Figure 6.24 Digital Side Supply Current vs Supply Voltage

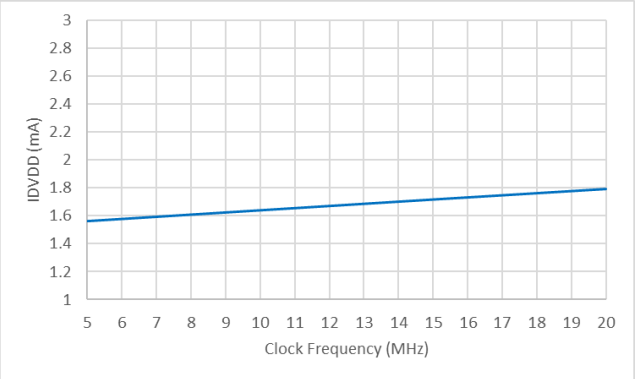


Figure 6.25 Digital Side Supply Current vs Clock Frequency

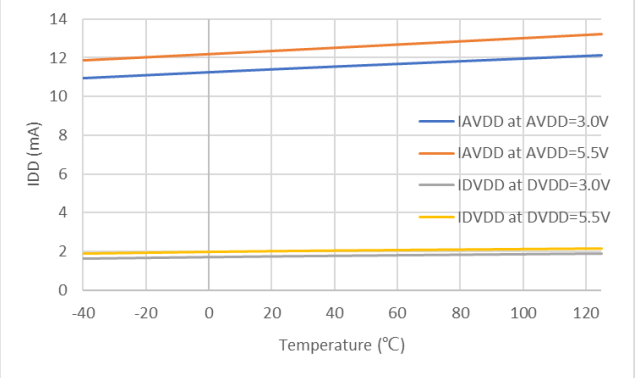


Figure 6.26 Supply Current vs Temperature

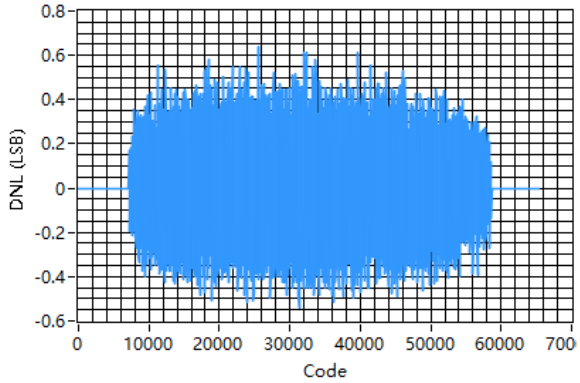


Figure 6.27 Typical Differential Nonlinearity

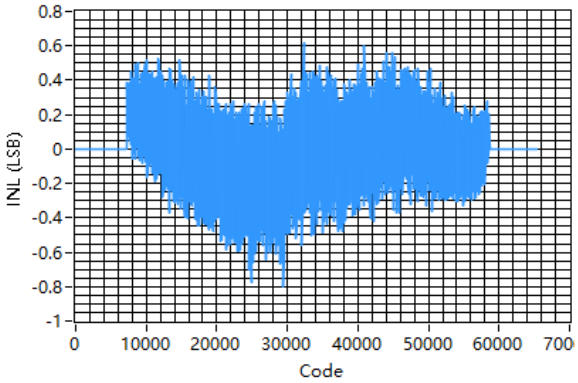


Figure 6.28 Typical Integral Nonlinearity

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value		Unit	Comments
		SOP8	SOP16		
Minimum External Clearance	CLR	8		mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8		mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28		μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I			IEC 60664-1

Description	Test Condition	Value	
		SOP8	SOP16
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III	I to III
Climatic Classification		40/125/21	
Pollution Degree per DIN VDE 0110		2	

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOP16	
DIN EN IEC 60747-17 (VDE 0884-17)					
Maximum repetitive isolation voltage		V_{IORM}	2121	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	1500	V_{RMS}
	DC Voltage		2121	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s , $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	<5	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s ,$V_{pd(m)}=1.6*V_{IORM}$, t_m=10s				
	Method b, routine test (100%				

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOP16	
	production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=V_{ini}, t_m=t_{ini}(method b2)				
Maximum transient isolation voltage	t = 60sec	V_{IOTM}	8000	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_A=25°C	R_{IO}	>10^{12}	>10^{12}	Ω
	V_{IO} =500V, 100°C ≤ T_A ≤ 125°C	R_{IO}	>10^{11}	>10^{11}	Ω
	V_{IO} =500V, T_A=T_s	R_{IO}	>10^{9}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150°C, T_A = 25°C	Ps	1430	1524	mW
Safety input, output, or supply current	θ_{JA} = 86°C /W for SOP8, V_I = 5.5V, T_J = 150°C, T_A = 25°C	Is	264	/	mA
	θ_{JA} = 82°C/W for SOP16, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C		/	277	mA
Maximum safety temperature		Ts	150	150	°C
UL1577					
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	5700	5700	V_{RMS}

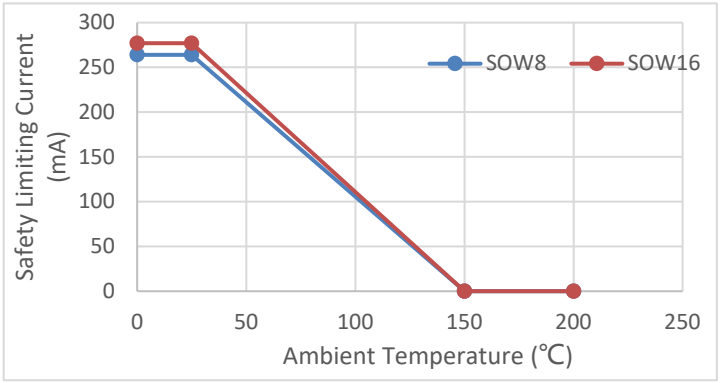


Figure 7.1 NSI1305 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI1305x-DSWVR are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5700V_{rms} Isolation voltage	Single Protection, 5700V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation	5000Vrms for 1min
E500602	E500602	Certificate No.40052820	CQC20001264938	R50574061

The NSI1305x-DSWR are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5700V_{rms} Isolation voltage	Single Protection, 5700V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation	5000Vrms for 1min
E500602	E500602	Certificate No.40052820	CQC20001264939	R50574061

8. Function Description

8.1. Overview

The NSI1305 is a high performance isolated modulator that accept fully-differential input. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ-Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream. The drivers (called TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier that separate external clock, as shown in the Functional Block Diagram.

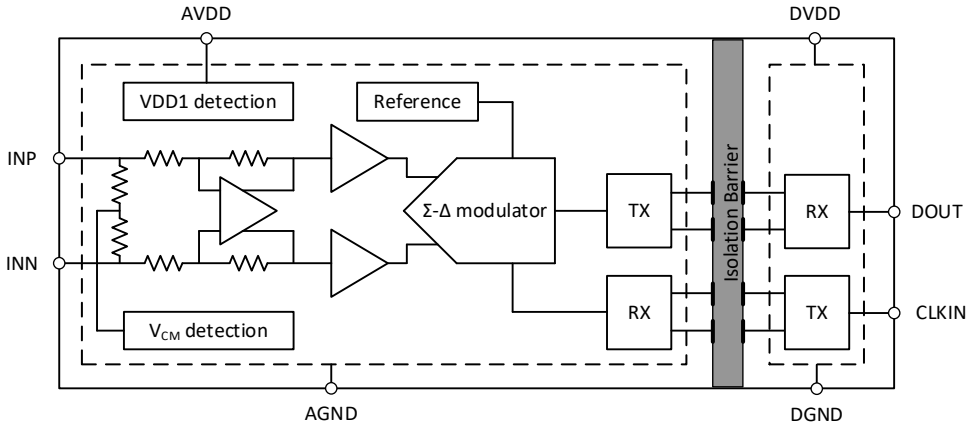


Figure 8.1 Function Block Diagram

8.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Digital Input

The digital input refers to clock signal which provides the clock for modulator conversion and output data frame clock. The clock signal should be supplied by an external source with a frequency range from 5MHz to 21MHz.

8.4. Digital Output

The digital output provides a stream of ones and zeros that can accurately represents the analog input voltage. Within the linear input range, the density of ones in the bitstream is proportional to the input voltage.

Ideally for a 0V input signal, the modulator outputs a bitstream with 50% high time. For a 250mV input signal (for the NSI1305M25), the modulator outputs a bitstream with 89.06% high time. For a -250mV input signal (for the NSI1305M25), the modulator outputs a bitstream with 10.94% high time.

If the input signal is greater than or equal to 320mV (64 mV for the NSI1305x05), the modulator clips with a steam of all ones. If the input signal is less than or equal to -320mV (–64 mV for the NSI1305x05), the output of the modulator clips with a stream of all zeros. In this case, however, the NSI1305 generates a single 0 (if the input is at positive full-scale) or 1 every 128 clock cycles to indicate proper device function (see section 7.5 for more details).

Due to quantization noise of internal Σ-Δ modulator, the digital output frequency is not fixed, but the density of high time is fixed based on input voltage. Typical modulator digital output characteristics are as below.

Table 8.1 Input voltage with ideal corresponding density of high time at modulator data output, and ADC code

Analog input	*Input voltage*	*Density of high time*	*Digital output code(16-bit unsigned decimation)*
+Differential input voltage before clipping output	+320mV (+64mV for NSI1305x05)	99.22%	65024
+Linear differential input full scale voltage	+250mV (+50mV for NSI1305x05)	89.06%	58366
Zero	0mV	50%	32768

Ideal density of 1s in the output bitstream for any input voltage(except for full-scale input, as described in section 7.5) at modulator data output can be calculated with:

$$\frac{V_{IN} + V_{CLIPPING}}{2 \times V_{CLIPPING}}$$

Similarly, the ADC code can be calculated, assuming a 16-bit unsigned decimation filter.

8.5. Fail-safe Output

NSI1305 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe function will be activated in following conditions:

- When the undervoltage of AVDD is detected (AVDD< $AVDD_{UV}$), DOUT pin output a bitstream of all logic zeros, as shown in Figure 8.2.
- When the overvoltage of common-mode input voltage is detected (V_{CM}>V_{CMov}), DOUT pin output a bitstream of all logic ones, as shown in Figure 8.2.

NOTE: If both of the faults above occur at the same time, DOUT pin output a bitstream of all logic zeros. (AVDD missing has a higher priority).

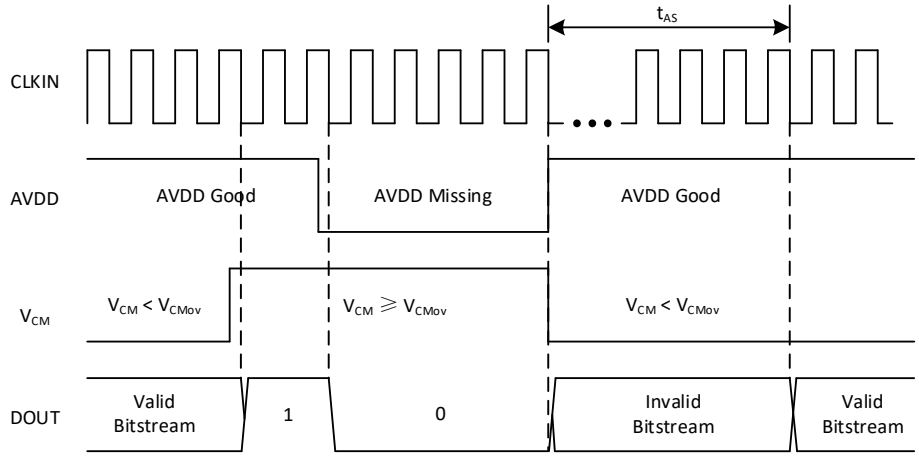


Figure 8.2 Fail-safe output

If an overrange input signal is applied to the NSI1305 ($V_{IN} \geq V_{Clipping}$), the output generates a single 0 or 1 every 128 clock cycles, as shown in Figure 7.3.

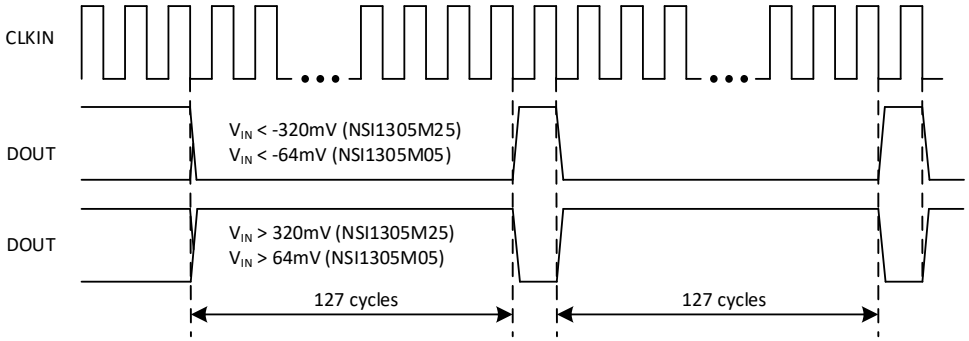


Figure 8.3 Overrange output

9. Application Note

9.1. Typical Application Circuit

NSI1305 is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 8.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1305 through a RC filter. The internal second-order sigma-delta modulator converts the analog input to a single-bit output stream. The external digital system provides a clock source for the modulator and a digital filter for decimation and quantization noise filtering.

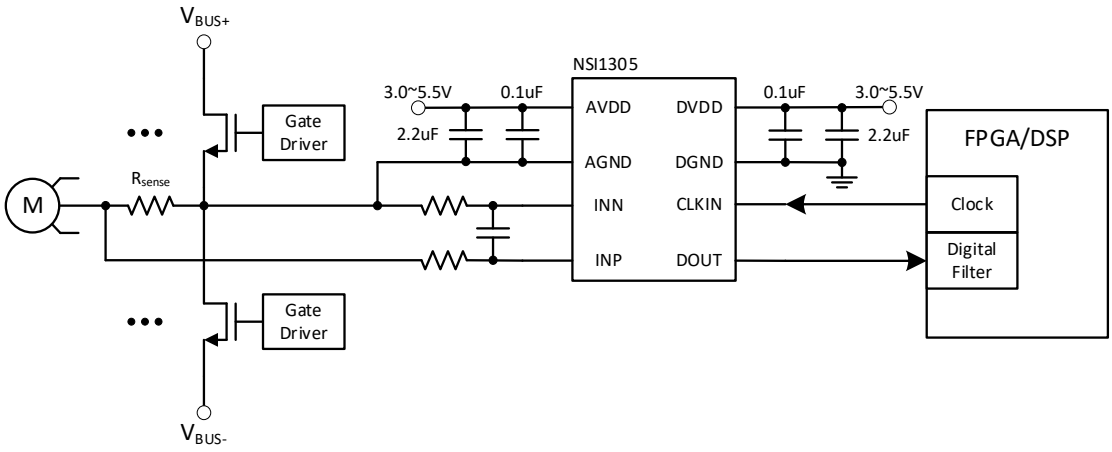


Figure 9.1 Typical application circuit in phase current sensing

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. Digital Filter

The Σ-Δ modulator a characteristics of noise shaping. Most of the quantization noise is pushed from a low frequency to a higher frequency.

In order to reduce higher-frequency quantization noise, the modulator output is fed to the digital low-pass filter. Subsequently, the signal of interest passes through to the output of the digital filter, while much of the higher-frequency quantization noise is filtered out.

The digital filter serves another function – decimation. It creates a digital output code from the bitstream that the modulator outputs. The ratio of the modulator rate (f_{MOD}) of the delta-sigma modulator to its output data rate (f_{DR}) is the oversampling ratio (OSR). The relationship between f_{DR} and f_{MOD} is:

$$f_{DR} = f_{MOD} / OSR \qquad \text{Equation 9.1}$$

A sinc3 filter is recommended since it's simple and requires less hardware resources. Equation 9.2 describes the transfer function of a sinc filter.

$$H(Z) = \left(\frac{1}{DR}\frac{(1-Z^{-DR})}{(1-Z^{-1})}\right)^{N} \qquad \text{Equation 9.2}$$

where:

DR is the decimation rate;

N is the sinc filter order.

The filter can be implemented in an FPGA or DSP. The sinc filter creates a digital output code by taking a multi-order moving average of the modulator output over a certain number of modulator clock periods.

The higher the decimation rate, the higher the conversion accuracy, and the lower the output data rate. So, there is a trade-off between accuracy and data rate. All the characterization in this datasheet is tested with a sinc3 filter with an oversampling ratio (OSR) of 256.

The output data size is expressed in Equation 9.3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ Size = N \times \log_2 DR \quad \text{（Equation 9.3）}$$

The filter characteristics for a third-order sinc filter are summarized in Table 8.2.

Table 9.2 Sinc3 Filter Characteristics for 20 MHz CLKIN

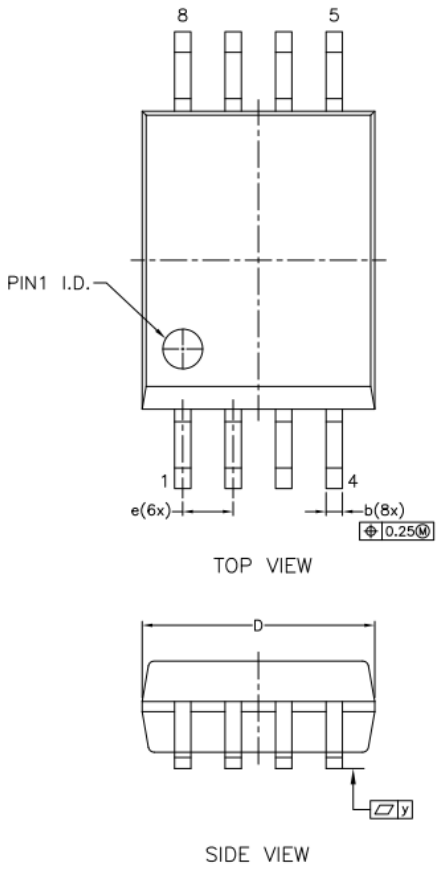
Decimation Rate (DR)	*Data Output Rate (kHz)*	*Data Size (bits)*	*Filter Response (kHz)*
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

9.4. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1305 requires a 0.1μF bypass capacitor between AVDD and AGND, DVDD and DGND. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1305. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1305. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

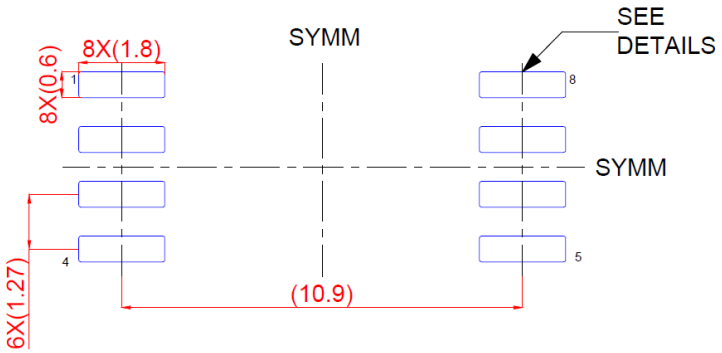
10. Package Information



* CONTROLLING DIMENSION : MM

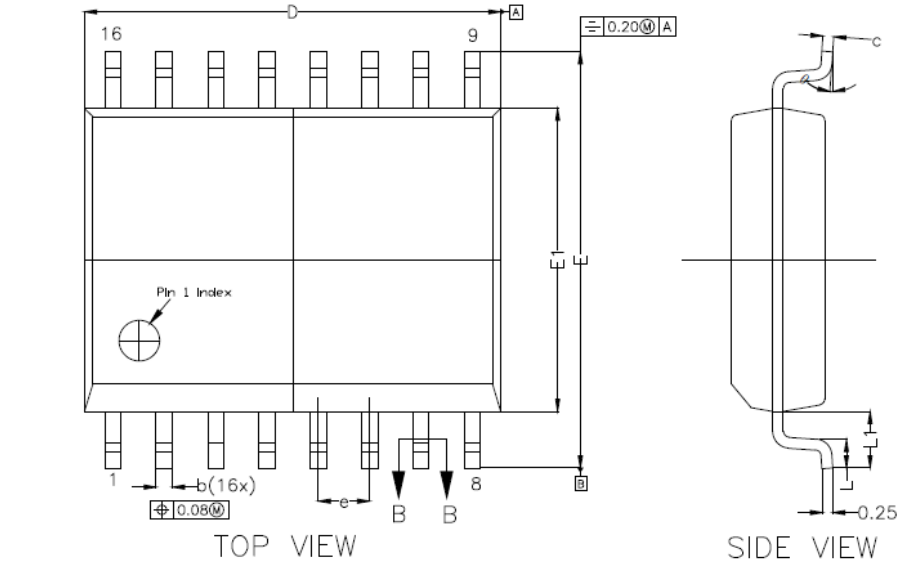
SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

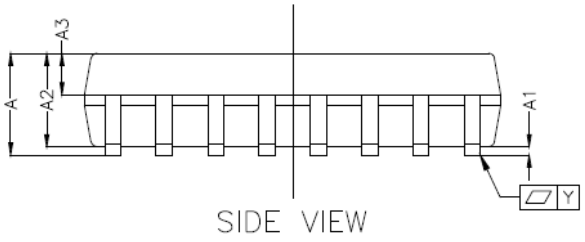
Figure 10.1 SOW8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE

Figure 10.2 SOW8 Package Board Layout Example





* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 10.3 SOW16 package shape and dimension in millimeters

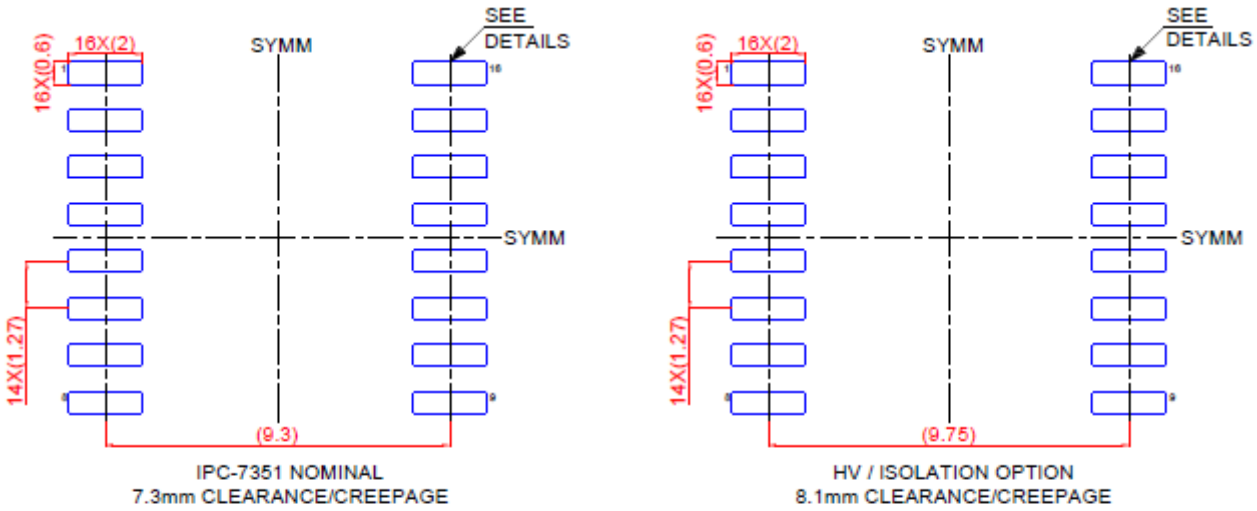


Figure 10.4 SOW16 Package Board Layout Example

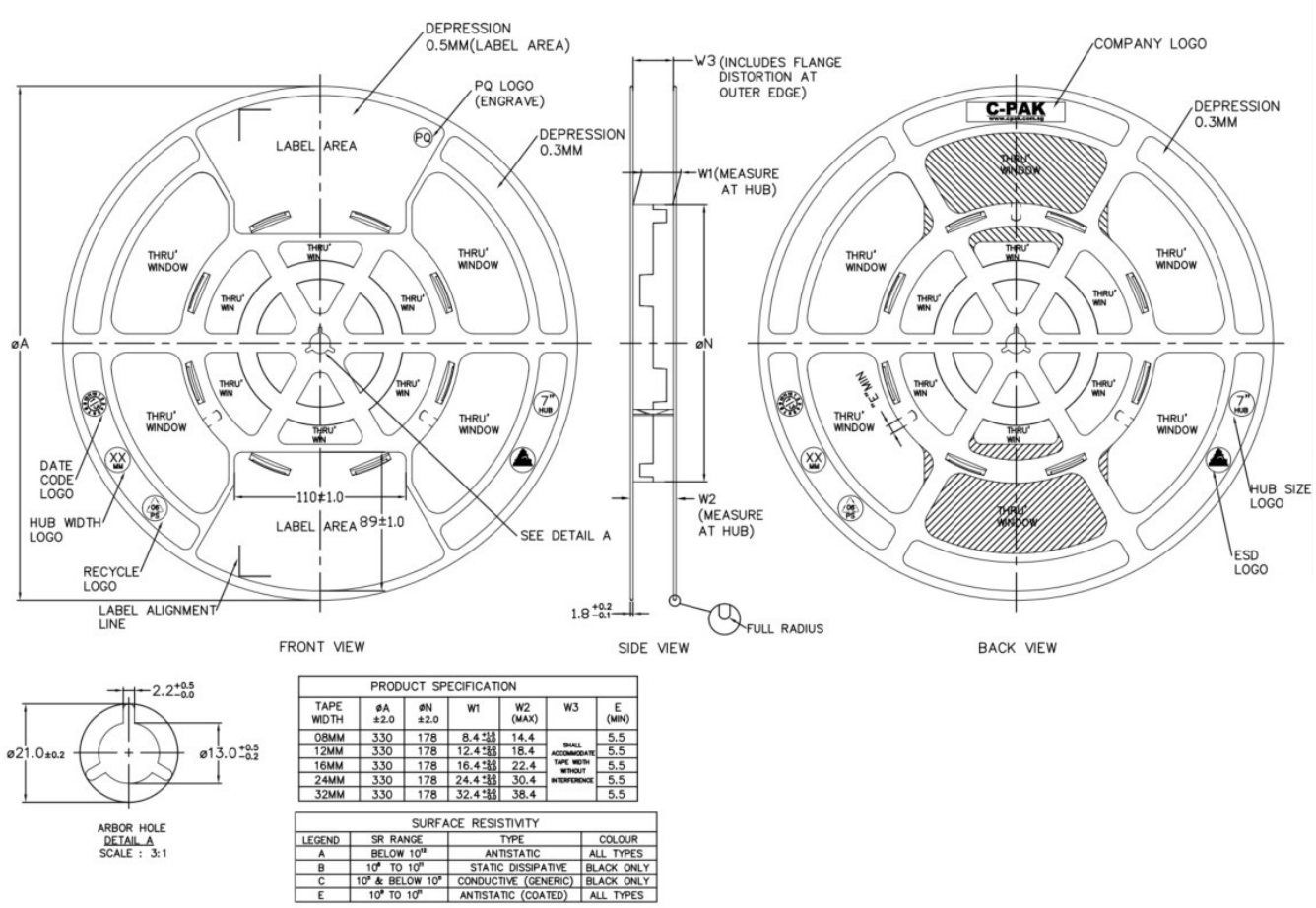
11. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Package Type	Package Drawing	SPQ	Release to Market
NSI1305M05-DSWVR	5	-50 ~ 50	Level-3	-40 to 125°C	SOP8 (300mil)	SOW8	1000	NO
NSI1305M25-DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	SOP8 (300mil)	SOW8	1000	NO
NSI1305M05-DSWR	5	-50 ~ 50	Level-2	-40 to 125°C	SOP16 (300mil)	SOW16	1000	NO
NSI1305M25-DSWR	5	-250 ~ 250	Level-2	-40 to 125°C	SOP16 (300mil)	SOW16	1000	YES

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1305	Click here	Click here	Click here	Click here

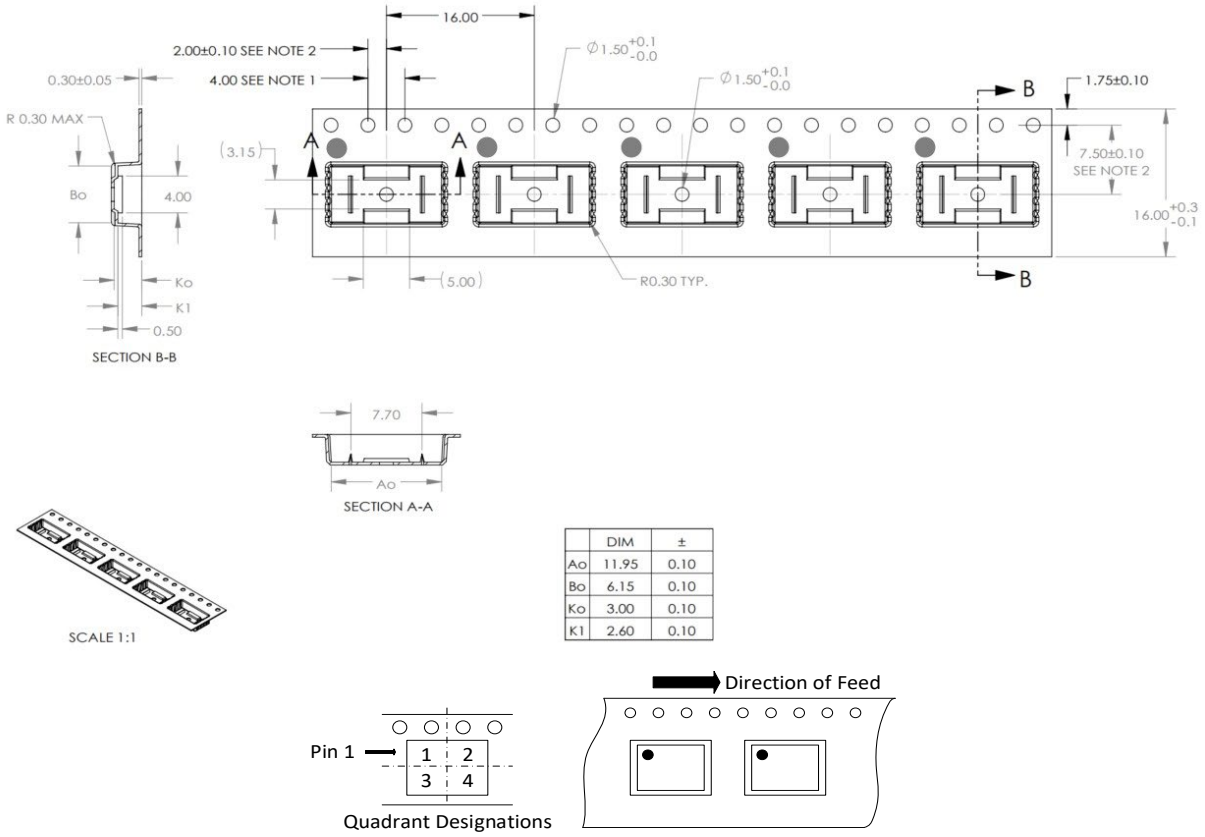
13. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

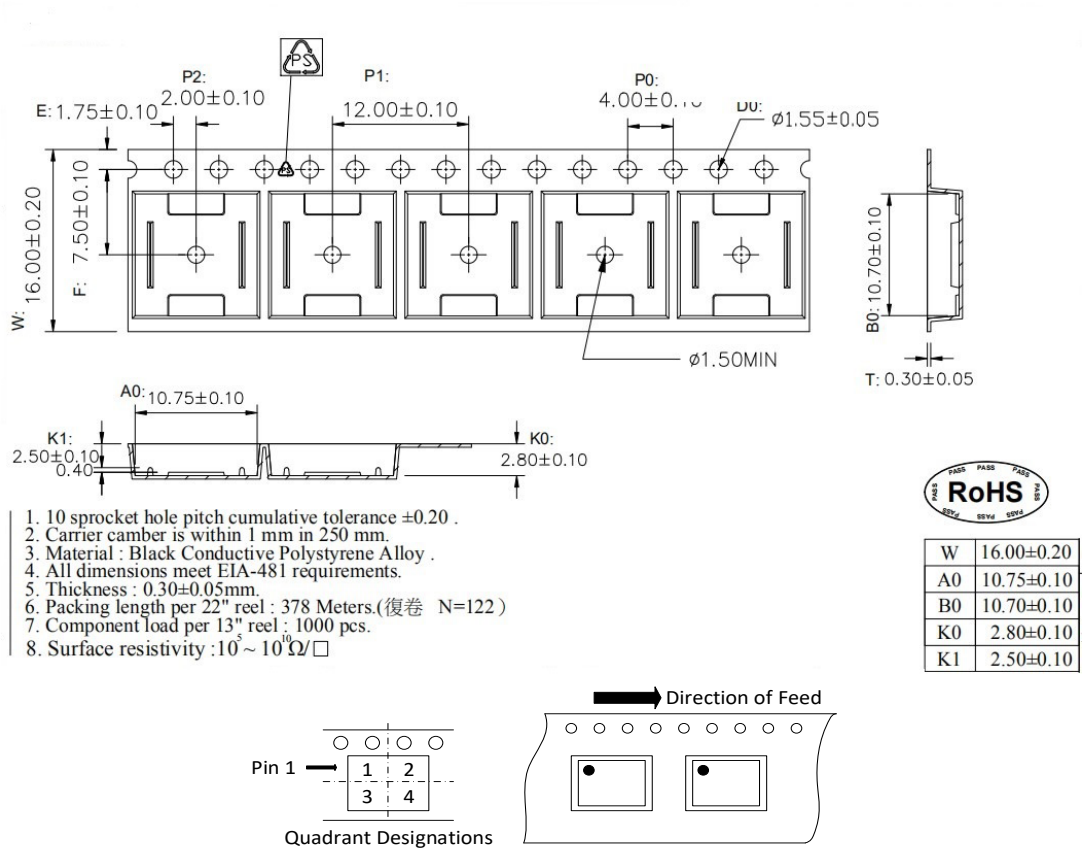
SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{9} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{8}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 13.1 Tape Information



	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

Figure 13.2 Reel Information of SOP8(300mil)



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : $10^{5} \sim 10^{10}\Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

Figure 13.3 Reel Information of SOP16(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Release	2020/8/29
1.1	Update offset drift in Key Features in page 1, description form of Vpd (m) and the standard on which VIOSM test method is based in 6.2. Update typeface to Source Sans Pro.	2023/3/30
1.2	1. Update safety regulatory info 2. Update all NSI to NSI. 3. Update test temperature condition of I_{IB}, E_O and E_G	2024/11/29

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