NOVOSENSE

NSI1303Ex

High Reliability Reinforced Isolated Sigma-Delta Modulator with Manchester Output

Datasheet (EN) 1.1

Product Overview

The NSI1303 is a high performance Σ-Δ modulator with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of ±50mV (±64mV full-scale) or ±250mV (±320mV full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The analog input is amplified and continuously sensed by a second-order Σ-Δ modulator and converted to a high speed, single bit data stream. The output bit-stream of the NSI1303 is synchronized to the internally generated clock and is Manchester coded. NSI1303 can achieve 16 bits resolution by using an appropriate digital filter (such as sinc3 filter) to decimate the bitstream from internal clock. The Manchester coded output supports single-wire data and clock transfer without the setup and hold time limitations of the receiving device.

The fail-safe functions including input common-mode overvoltage detection and missing AVDD detection simplify system-level design and diagnostics.

Key Features

- Up to 5700V_{RMS} Insulation Voltage
- 10MHz and 20MHz internal clock frequency options
- ±50mV or ±250mV Linear Input Voltage Range
- Excellent DC Performance:
  - Offset Error: ±50μV or ±100μV (Max)
  - Offset Drift: ±1μV/°C (Max)
  - Gain Error: ±0.2% (Max)
  - Gain Drift: ±40ppm/°C (Max)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Features:
  - AVDD monitoring
  - Input common-mode overvoltage detection
- Operation Temperature: -40°C~125°C
- RoHS-Compliant Packages:
  - SOP8(300mil)

Safety Regulatory Approvals

- UL recognition per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Shunt Current Monitoring
- AC Motor Controls
- Uninterruptible Power Suppliers
- Automotive Onboard Chargers

Device Information

Part Number	*Package*	*Body Size*
NSI1303Ex-DSWVR	SOP8(300mil)	5.85mm × 7.50mm

Functional Block Diagrams

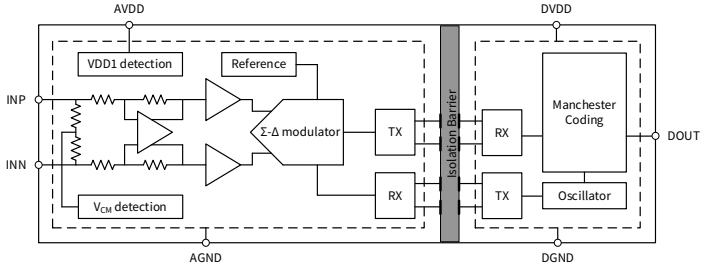

Figure 1. NSI1303Ex Block Diagram

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1. Pin Configuration and Functions

PART NUMBER	LINEAR INPUT VOLTAGE RANGE	DIFFERENTIAL INPUT RESISTANCE	INTERNAL CLOCK FREQUENCY	DIGITAL OUTPUT INTERFACE
NSI1303E01	±50mV	4.9kΩ	10MHz	Manchester coded CMOS
NSI1303E21	±250mV	22kΩ		
NSI1303E02	±50mV	4.9kΩ	20MHz	
NSI1303E22	±250mV	22kΩ		

Figure 1.2 NSI1303Ex Package (SOP8(300mil))

Table 1.1 NSI1303Ex Pin Configuration and Description (SOP8(300mil))

NSI1303Ex PIN NO.	SYMBOL	FUNCTION
1	AVDD	Power supply for analog side (3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1303E2x and ±50mV recommended for NSI1303E0x)
3	INN	Negative analog input
4	AGND	Analog ground reference
5	DGND	Digital ground reference
6	DOUT	Modulator data output
7	DGND	Connect this pin to the controller-side ground for NSI1303Ex
8	DVDD	Power supply for digital side (3.0V to 5.5V)

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2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	AVDD, DVDD	-0.3		6.5	V
Analog Input Voltage	INP, INN	AGND-6		AVDD+0.5	V
Digital Input Voltage	CLKIN	DGND-0.5		DVDD+0.5	V
Digital Output Voltage	DOUT	DGND-0.5		DVDD+0.5	V
Output current per Output Pin	Io	-10		10	mA
Operating Temperature	T_{OPR}	-40		125	°C
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{STG}	-55		150	°C

3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Unit
Analog Side Power Supply		AVDD	3.0	5.0	5.5	V
Digital Side Power Supply		DVDD	3.0	3.3	5.5	V
NSI1303E01/2	Differential input voltage before clipping output	$V_{Clipping}$		±64		mV
	Linear differential input full scale voltage	V_{FSR}	-50		50	mV
	Operating common-mode input voltage	V_{CM}	-0.032		0.8	V
NSI1303E21/2	Differential input voltage before clipping output	$V_{Clipping}$		±320		mV
	Linear differential input full scale voltage	V_{FSR}	-250		250	mV
	Operating common-mode input voltage	V_{CM}	-0.16		0.8	V
Operating Ambient Temperature		T_A	-40		125	°C

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5. Thermal Information

Parameters	Symbol	SOP8(300mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	86	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	4	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	42	°C/W

6. Specifications

6.1. Electrical Characteristics: NSI1303E0x

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -50mV to +50mV, and INN = AGND = 0V, T_A = -40°C to 125°C and sinc^3 filter with OSR=256. Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.8	14.1	mA	for E01
			12	14.3	mA	for E02
Digital Side Supply Current	IDVDD		2.8		mA	for E01, C_{LOAD}=15pF
			3.2	5.5	mA	for E02, C_{LOAD}=15pF
AVDD undervoltage detection threshold voltage	$AVDD_{UV}$	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	$CMRR_{dc}$		-100		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-100		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Input capacitance	C_{IN}		2		pF	INN=AGND
Single-ended input resistance	R_{IN}		4.75		kΩ	INN = AGND
Differential input resistance	R_{IND}		4.9		kΩ	
Input bias current	I_{IB}	-26	-23	-20	μA	T_A = 25°C, INP = INN = AGND, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±2		nA/°C	

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Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Input bandwidth	BW		800		kHz	
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	V_{OS}	-50	±2.5	50	μV	T_A = 25°C, INP = INN = AGND
Offset error thermal drift	TCV_{OS}	-0.5	±0.15	0.5	μV/°C	
Gain error	E_G	-0.2%	±0.005 %	0.2%		T_A = 25°C
Gain error thermal drift	TCE_G	-30	±10	30	ppm/°C	
Power supply rejection ratio	PSRR		-106		dB	PSRR vs AVDD, at DC
			-104		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR		84		dB	f_{IN} = 1kHz for x01
		77	83		dB	f_{IN} = 1kHz for x02
Signal to noise and distortion	SINAD	77	82.5		dB	f_{IN} = 1kHz
Total harmonic distortion	THD		-97	-86	dB	f_{IN} = 1kHz
Spurious-free dynamic range	SFDR		96		dB	f_{IN} = 1kHz for x01
			97		dB	f_{IN} = 1kHz for x02
Digital Input / Output						
Output load capacitance	C_{LOAD}		30		pF	
High-level output voltage	V_{OH}	DVDD-0.1			V	I_{OH} = -20μA
		DVDD-0.4			V	I_{OH} = -4mA
		DVDD-0.8				I_{OH} = -8mA
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 20μA
				0.4	V	I_{OL} = 4mA
				0.8	V	I_{OL} = 8mA

6.2. Electrical Characteristics: NSI1303E2x

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = AGND = 0V, T_A = -40°C to 125°C and $sinc^3$ filter with OSR=256. Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						

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Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.2	13.8	mA	for x21
			11.7	14.2	mA	for x22
Digital Side Supply Current	IDVDD		2.8		mA	for E21, CLOAD=15pF
			3.2	5.5	mA	for E22, CLOAD=15pF
AVDD undervoltage detection threshold voltage	$AVDD_{UV}$	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	$CMRR_{dc}$		-106		dB	INP = INN, fIN = 0 Hz, VCM min ≤ VIN ≤ VCM max
	$CMRR_{ac}$		-95		dB	INP = INN, fIN = 10 kHz, VCM min ≤ VIN ≤ VCM max
Input capacitance	C_{IN}		2		pF	INN=AGND
Single-ended input resistance	R_{IN}		19		kΩ	INN = AGND
Differential input resistance	R_{IND}		22		kΩ	
Input bias current	I_{IB}	-24	-18	-12	μA	T_A = 25°C, INP = INN = AGND, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±1		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Input bandwidth	BW		800		kHz	
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	V_{OS}	-100	±2.5	100	μV	T_A = 25°C, INP = INN = AGND
Offset error thermal drift	TCV_{OS}	-1	±0.15	1	μV/°C	
Gain error	E_G	-0.2%	±0.005%	0.2%		T_A = 25°C
Gain error thermal drift	TCE_G	-40	±20	40	ppm/°C	
Power supply rejection ratio	PSRR		-100		dB	PSRR vs AVDD, at DC
			-95		dB	PSRR vs AVDD, 100mV and 10kHz ripple

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AC Accuracy						
Signal to noise ratio	SNR		87		dB	fIN = 1kHz for E21
		84	86.5		dB	fIN = 1kHz for E22
Signal to noise and distortion	SINAD	82	86		dB	fIN = 1kHz
Total harmonic distortion	THD		-90	-82	dB	fIN = 1kHz for E21
			-95	-82	dB	fIN = 1kHz for E22
Spurious-free dynamic range	SFDR		96		dB	fIN = 1kHz for E21
			98		dB	fIN = 1kHz for E22
Digital Input / Output						
Output load capacitance	C_{LOAD}		30		pF	
High-level output voltage	V_{OH}	DVDD-0.1			V	IOH = -20μA
		DVDD-0.4			V	IOH = -4mA
		DVDD-0.8				IOH = -8mA
Low-level output voltage	V_{OL}			0.1	V	IOL = 20μA
				0.4	V	IOL = 4mA
				0.8	V	IOL = 8mA

6.3. Timing Characteristics

Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25°C.Over operating ambient temperature range (unless otherwise noted)

PARAMETERS	*Symbol*	*MIN*	*TYP*	*MAX*	*Unit*	*Comments*
clock frequency	f_{CLK}	9.6	10	10.4	MHz	For NSI1303Ex1
		19.2	20	20.8	MHz	For NSI1303Ex2
DOUT rising time	t_R		1.8	3.5	ns	C_{LOAD} = 15pF
DOUT falling time	t_F		1.8	3.5	ns	C_{LOAD} = 15pF
Analog setting time	t_{AS}		0.5		ms	AVDD step to 3.0 V with DVDD ≥ 3.0 V, to DOUT valid, 0.1% settling

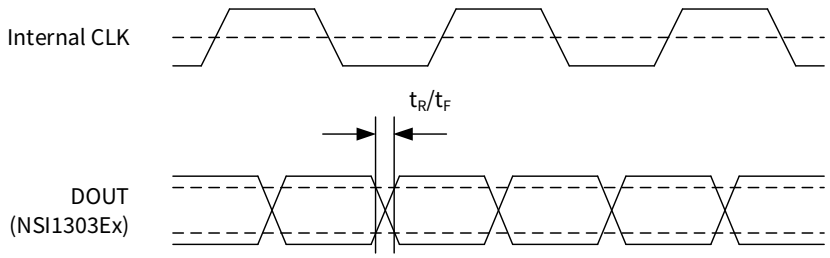

Figure 6.1 NSI1303Ex digital interface timing

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6.4. Typical Performance Characteristics

Unless otherwise noted, test at AVDD = 5V, DVDD = 3.3V, Vin = -250mV to 250mV (NSI1303E2x) or -50mV to 50mV (NSI1303E0x), and sinc^3 filter with OSR=256.

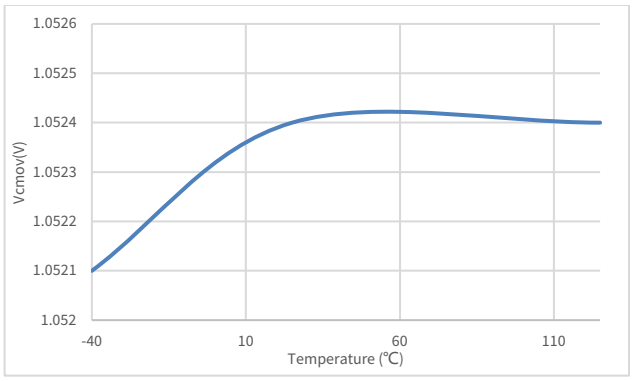

Figure 6.2 Common-Mode Overvoltage Detection Level vs Temperature

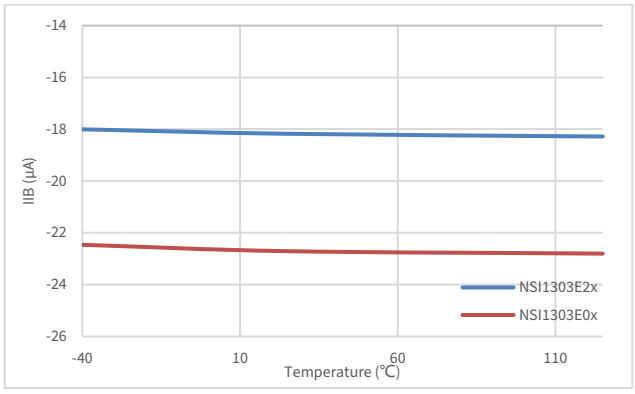

Figure 6.3 Input Bias Current vs Temperature

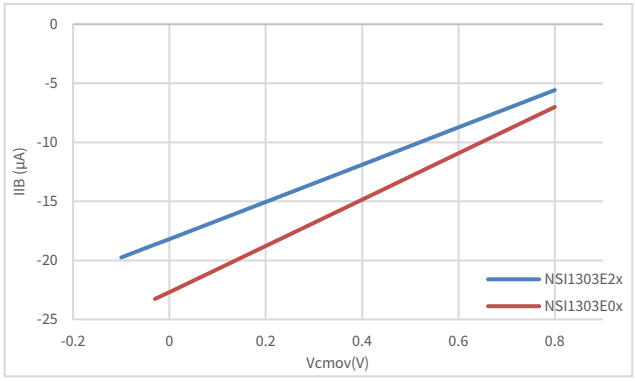

Figure 6.4 Input Bias Current vs Common-Mode voltage

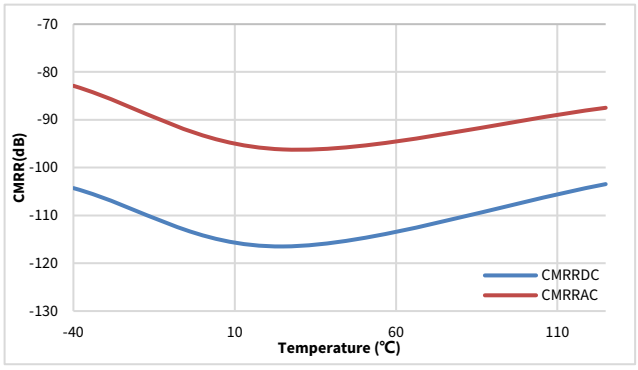

Figure 6.5 Common-Mode Rejection Ratio vs Temperature (NSI1303E02)

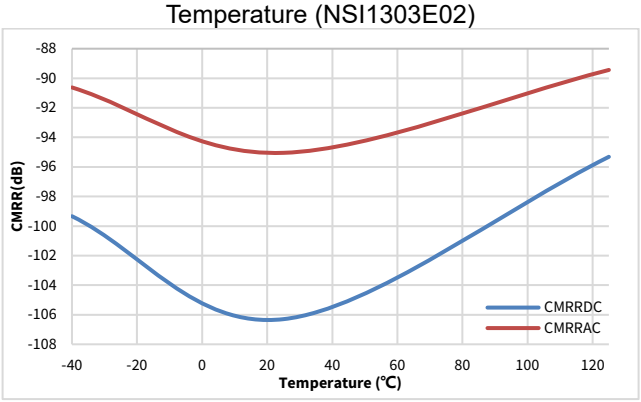

Figure 6.6 Common-Mode Rejection Ratio vs Temperature (NSI1303E22)

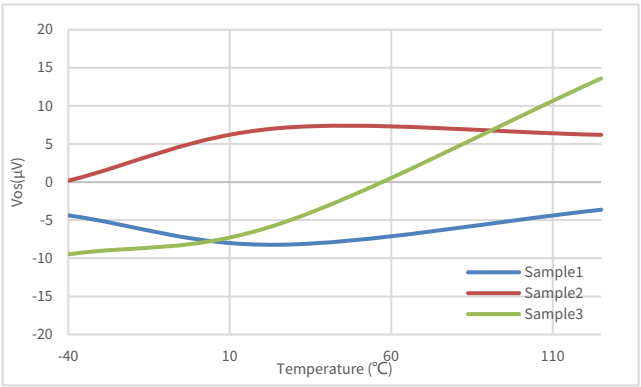

Figure 6.7 Input Offset Voltage vs Temperature (NSI1303E02)

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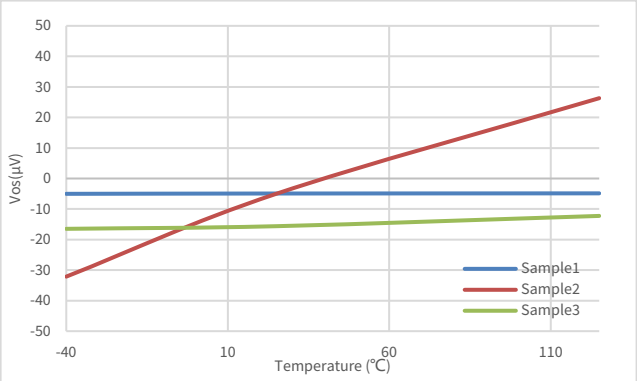

Figure 6.8 Input Offset Voltage vs Temperature (NSI1303E22)

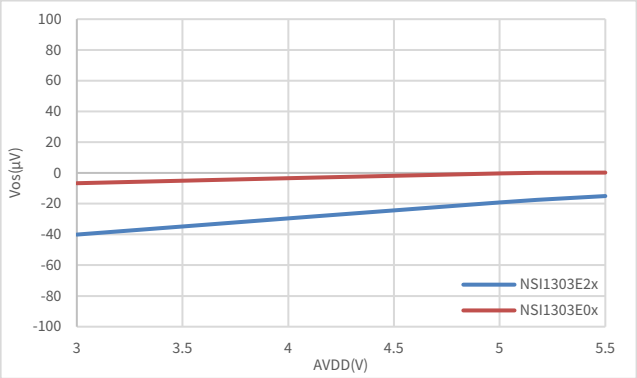

Figure 6.9 Input Offset Voltage vs Analog Side Supply Voltage

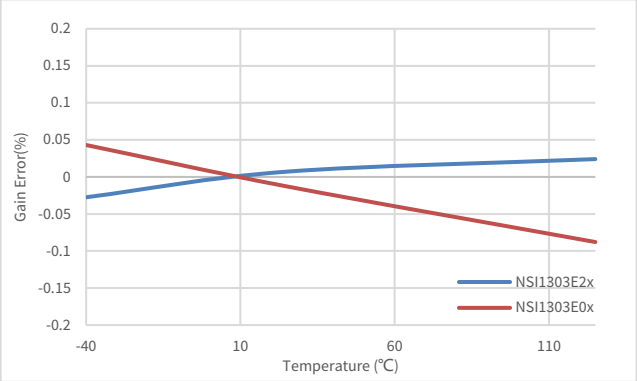

Figure 6.10 Gain Error vs Temperature

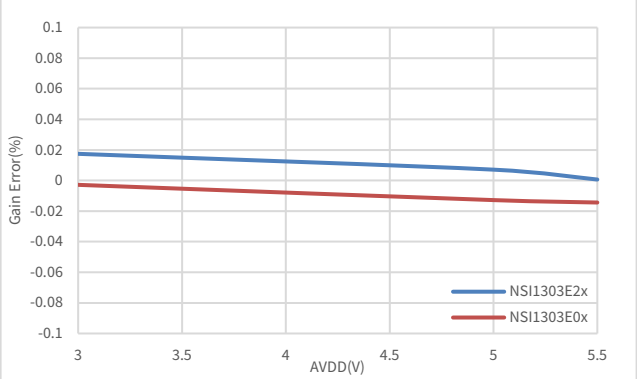

Figure 6.11 Gain Error vs Analog Side Supply Voltage

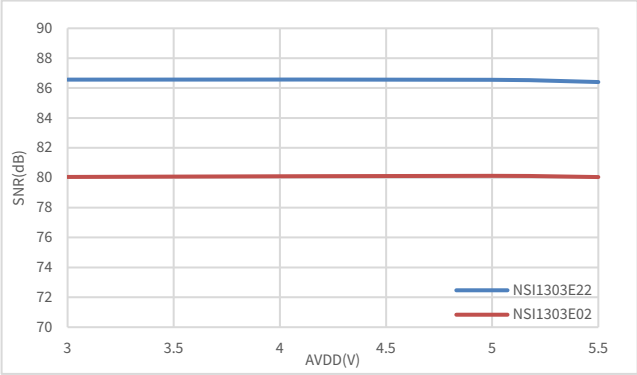

Figure 6.12 Signal-to-Noise Ratio vs Analog Side Supply Voltage

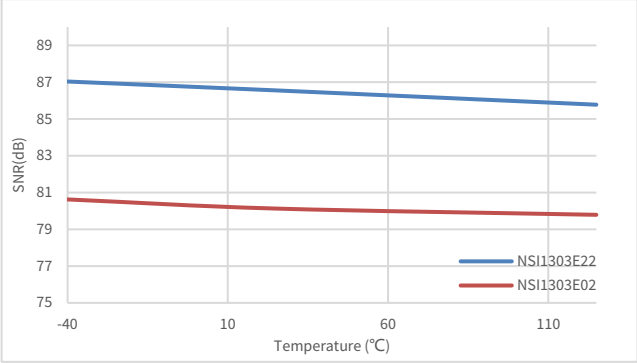

Figure 6.13 Signal-to-Noise Ratio vs Temperature

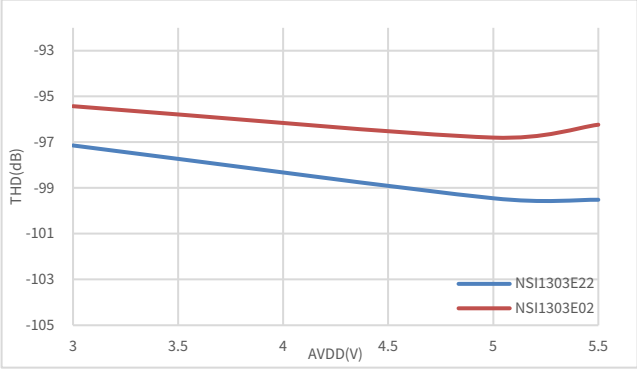

Figure 6.14 Total Harmonic Distortion vs Analog Side Supply Voltage

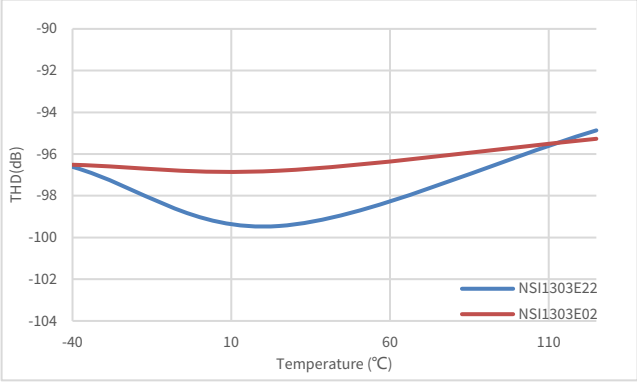

Figure 6.15 Total Harmonic Distortion vs Temperature

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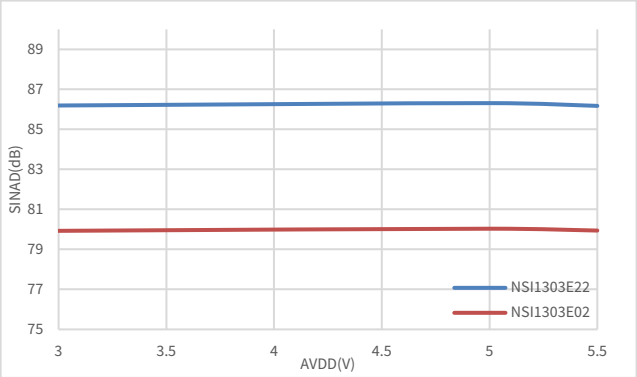

Figure 6.16 Signal-to-Noise + Distortion vs Analog Side Supply Voltage

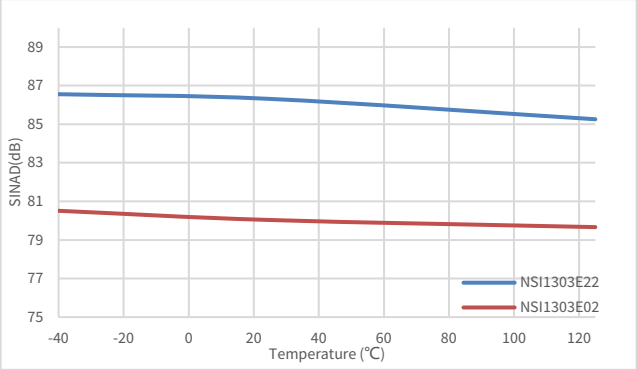

Figure 6.17 Signal-to-Noise + Distortion vs Temperature

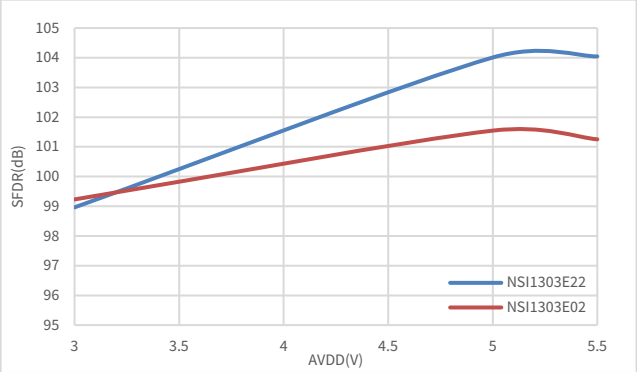

Figure 6.18 Spurious-Free Dynamic Range vs Analog Side Supply Voltage

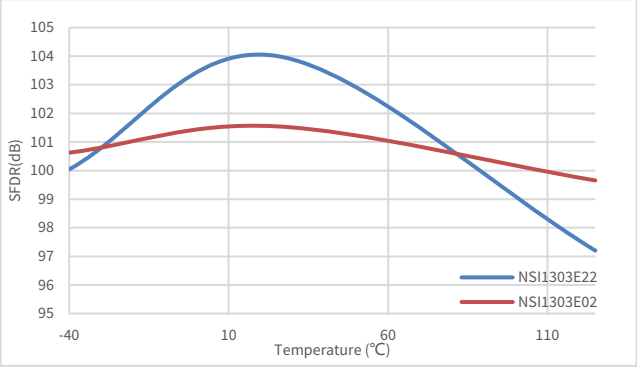

Figure 6.19 Spurious-Free Dynamic Range vs Temperature

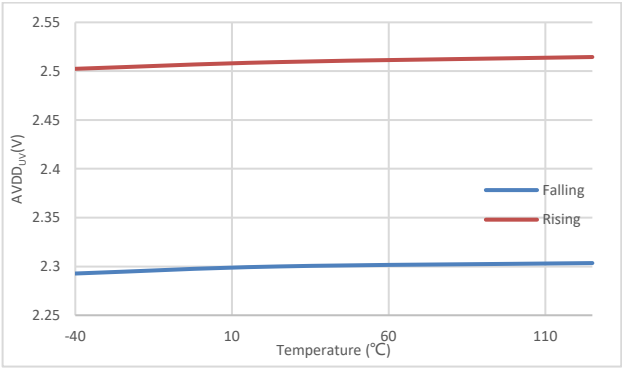

Figure 6.20 Analog Side Under-Voltage Detection Level vs Temperature

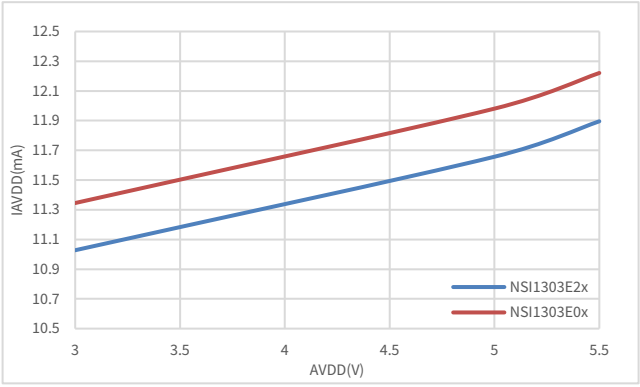

Figure 6.21 Analog Side Supply Current vs Supply Voltage

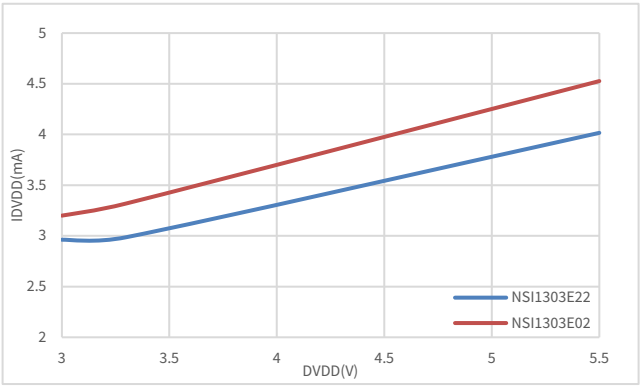

Figure 6.22 Digital Side Supply Current vs Supply Voltage

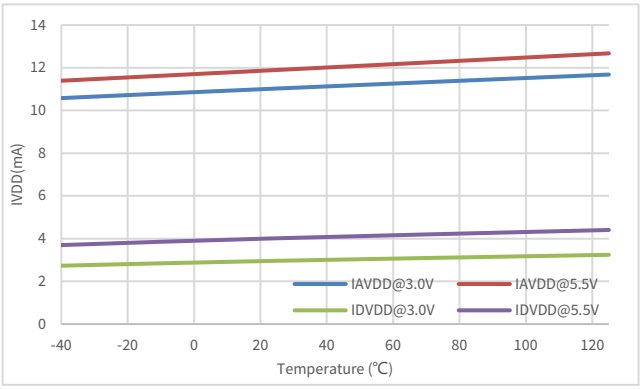

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Figure 6.23 Supply Current vs Temperature (NSI1303E22)

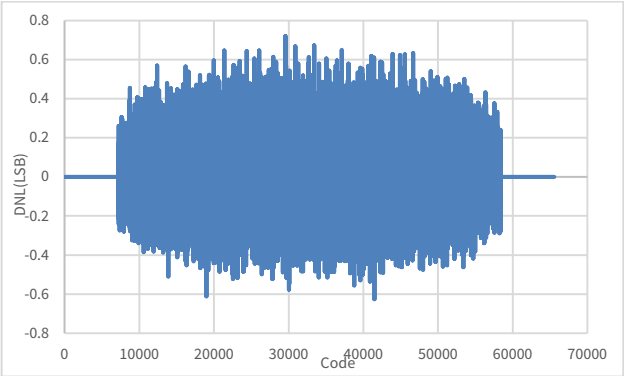

Figure 6.24 Typical Differential Nonlinearity

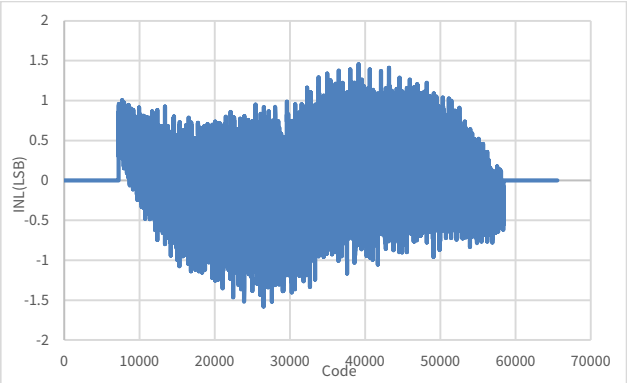

Figure 6.25 Typical Integral Nonlinearity

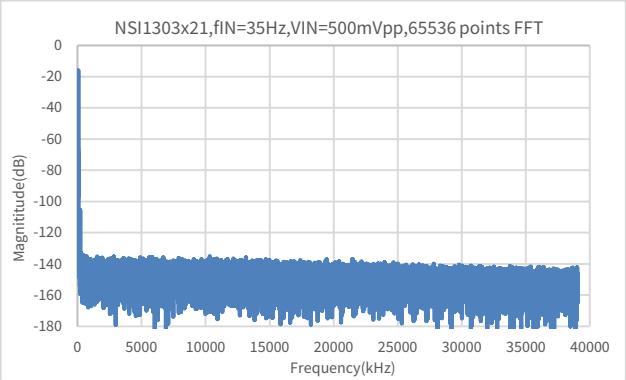

Figure 6.26 Frequency Spectrum

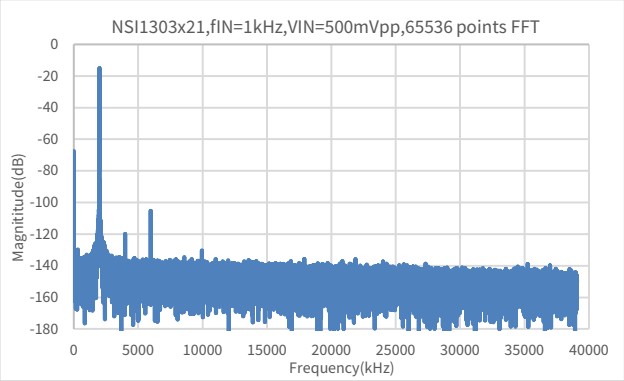

Figure 6.27 Frequency Spectrum

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	*Test Condition*	*Value*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III
Climatic Classification		40/125/21

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Description	Test Condition	Value
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s , $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s ,$V_{pd(m)}=1.6*V_{IORM}$, t_m=10s			
	Method b, routine test (100% production) and preconditioning (type test);$V_{ini}=1.2*V_{IOTM}$, t_{ini}=1s $V_{pd\ (m)}=1.875*V_{IORM}$, t_m=1s（method b1）or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$(method b2)			
Maximum transient isolation voltage	t = 60sec	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_A=25°C	R_{IO}	$>10^{12}$	Ω
	V_{IO} =500V, 100°C ≤ T_A ≤ 125°C	R_{IO}	$>10^{11}$	Ω
	V_{IO} =500V, $T_A=T_s$	R_{IO}	$>10^{9}$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150°C, T_A = 25°C	Ps	1430	mW
Safety input, output, or supply current	θ_{JA} = 86°C /W for SOP8, V_I = 5.5V, T_J = 150°C, T_A = 25°C	Is	264	mA
Maximum safety temperature		Ts	150	°C
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	V_{ISO}	5700	V_{RMS}

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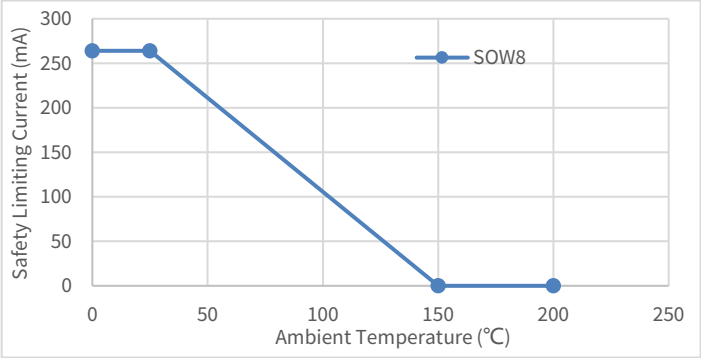

Figure 7.1 NSI1303 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI1303 are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*	*TUV*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011	Certified by IEC 62368-1
Single Protection, 5700V_{rms} Isolation voltage	Single Protection, 5700V_{rms} Isolation voltage	Reinforce Insulation 2121Vpeak, V_{IOSM}=6250Vpeak	Reinforced insulation	5000Vrms reinforced Isolation Working insulation voltage at 1500Vrms a.c. and 2121V d.c.
E500602	E500602	Certificate No.40052820	CQC20001264938	R50574061

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8. Function Description

8.1. Overview

The NSI1303Ex is a high performance isolated modulator that accepts fully-differential input with internal clock. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sensed by a second-order Σ-Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream that is synchronous to the internally-generated clock. The drivers (called TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier, as shown in the Functional Block Diagram. The extended clock frequency of 20 MHz on the NSI1303Ex2 supports faster control loops and higher performance levels compared to the other solutions available on the market. The digital output is Manchester coded and supports single-wire data and clock transfer without the setup and hold time limitations of the receiving device.

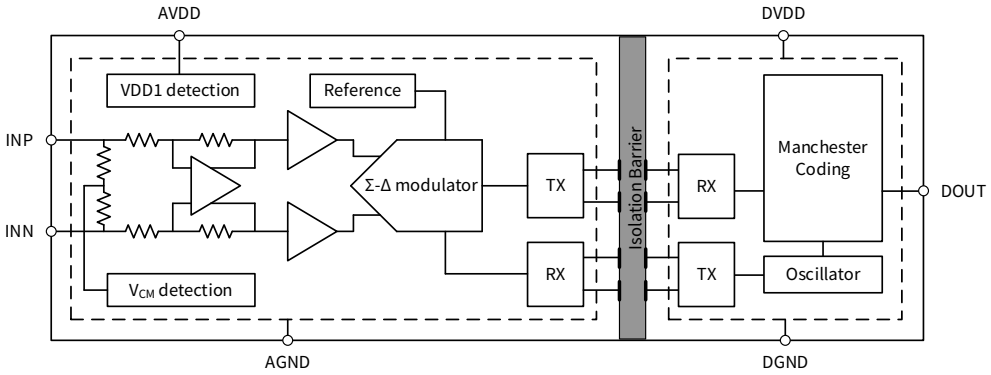

Figure 8.1 Function Block Diagram of NSI1303Ex

8.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Digital Output

The DOUT pin of the NSI1303Ex provides the Manchester coded (IEEE 802.3-compliant) output. The Manchester coding combines the clock and data information using exclusive or (XOR) logical operation. Figure 8.2 shows the resulting bitstream.

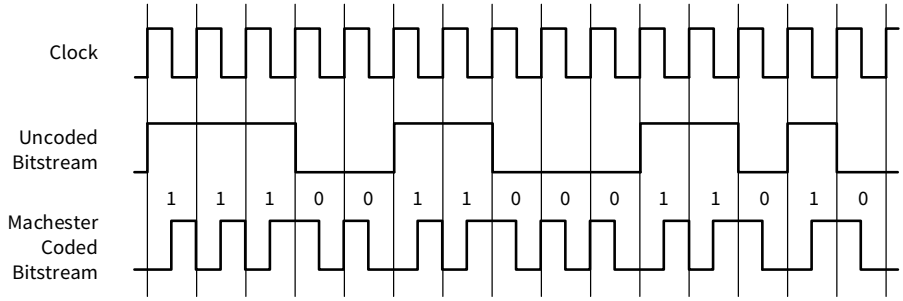

Figure 8.2 Manchester Coded Output of NSI1303Ex

The uncoded bitstream provides a stream of ones and zeros that can accurately represents the analog input voltage. Within the linear input range, the density of ones in the bitstream is proportional to the input voltage.

Ideally for a 0V input signal, the modulator outputs a bitstream with 50% high time. For a 250mV input signal (for the NSI1303E2x), the modulator outputs a bitstream with 89.06% high time. For a -250mV input signal (for the NSI1303E2x), the modulator outputs a bitstream with 10.94% high time.

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If the input signal is greater than or equal to 320mV (64 mV for the NSI1303E0x), the modulator clips with a steam of all ones. If the input signal is less than or equal to -320mV (–64 mV for the NSI1303E0x), the output of the modulator clips with a stream of all zeros. In this case, however, the NSI1303 generates a single 0 (if the input is at positive full-scale) or 1 every 128 clock cycles to indicate proper device function (see section8.4 for more details).

Figure 8.3 shows the uncoded data vs isolated modulator input voltage.

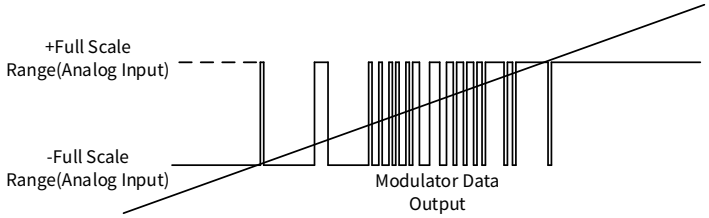

Figure 8.3 Uncoded data vs input voltage

Within full-scale input range, Equation 8.1 calculates the ones and zeros density of uncoded data for input voltage:

$$Density = (V_{IN}+V_{CLIPPING})/(2*V_{CLIPPING}) \quad \text{Equation 8.1}$$

8.4. Fail-safe Output

NSI1303 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe function will be activated in following conditions:

- When the undervoltage of AVDD is detected (AVDD< $AVDD_{UV}$), DOUT pin output a Manchester coded bitstream of all logic zeros, as shown in Figure 8.4.
- When the overvoltage of common-mode input voltage is detected (V_{CM}>V_{CMov}), DOUT pin output a Manchester coded bitstream of all logic ones, as shown in Figure 8.4.

NOTE: If both of the faults above occur at the same time, DOUT pin output a Manchester coded bitstream of all logic zeros. (AVDD missing has a higher priority).

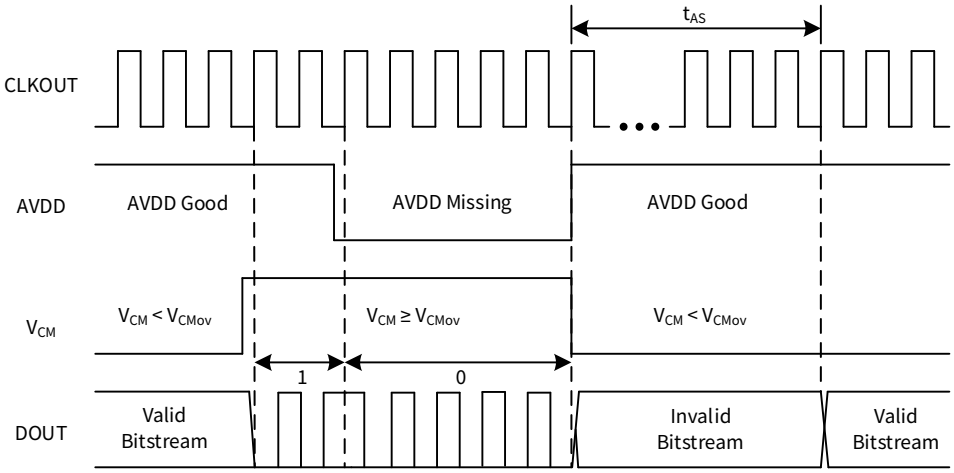

Figure 8.4 Fail-safe Bitstream Output of NSI1303Ex

If an overrange input signal is applied to the NSI1303 (V_{IN} ≥ $V_{Clipping}$), the output generates a single Manchester code of logic 0 or 1 every 128 bits at DOUT, as shown in Figure 8.5.

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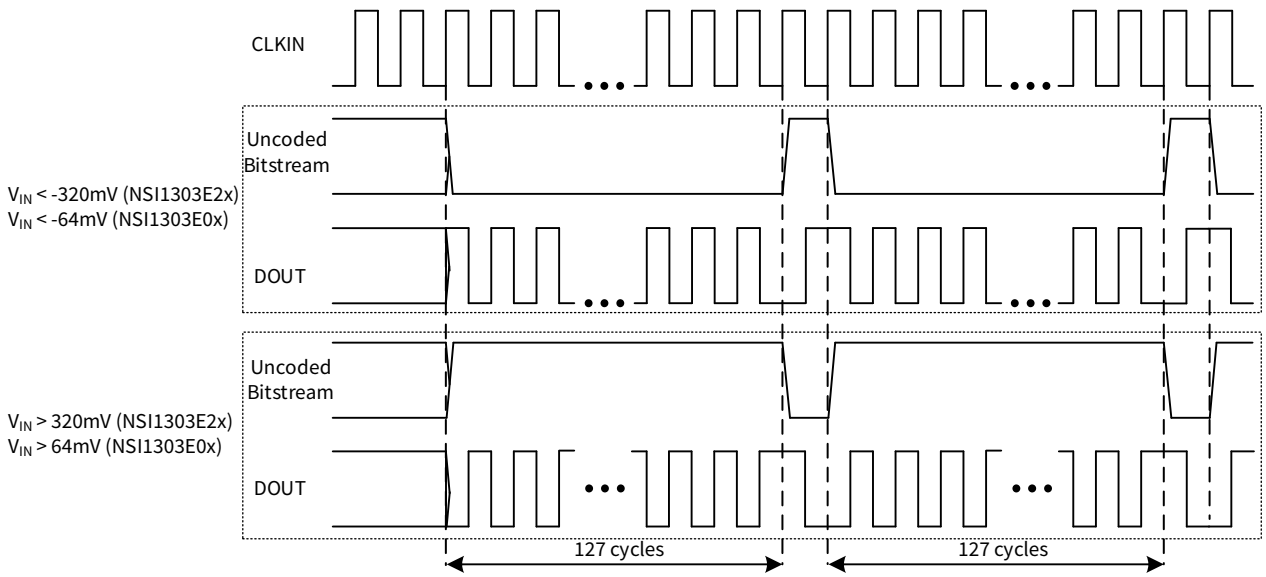

Figure 8.5 Overrange Bitstream Output

9. Application Note

9.1. Typical Application Circuit

The NSI1303Ex is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 9.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of the NSI1303Ex through a RC filter. The internal second-order sigma-delta modulator converts the analog input to a single-bit output stream. The DOUT pin outputs the Manchester coded bitstream, which is synchronized with the internally generated clock. The external digital system receives and decodes the Manchester coded bitstream and provides a digital filter for decimation and quantization noise filtering.

With the clock signal embedded in, the Manchester coded output supports single-wire data and clock transfer. This greatly simplifies PCB layout of the signal lines without consideration of propagation delay mismatch caused by different line lengths. Design of setup and hold times is correspondingly simplified in users' systems.

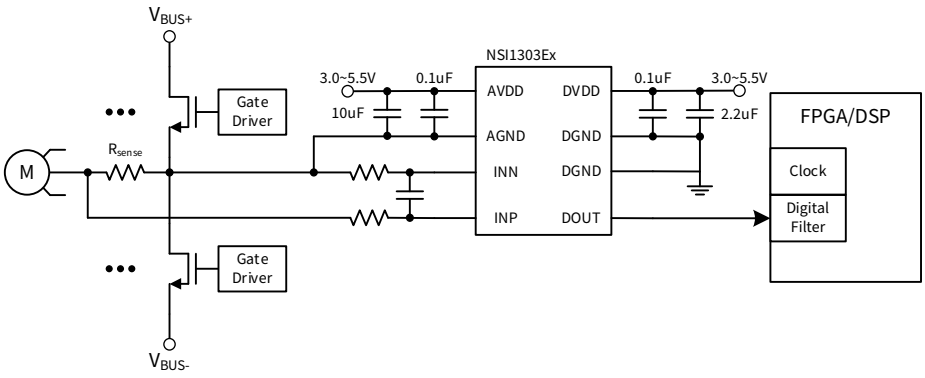

Figure 9.1 Typical application circuit of NSI1303Ex in phase current sensing

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

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- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. Digital Filter

The Σ-Δ modulator has characteristics of noise shaping. Most of the quantization noise is pushed from a low frequency to a higher frequency.

In order to reduce higher-frequency quantization noise, the modulator output is fed to the digital low-pass filter. Subsequently, the signal of interest passes through to the output of the digital filter, while much of the higher-frequency quantization noise is filtered out.

The digital filter serves another function – decimation. It creates a digital output code from the bitstream that the modulator outputs. The ratio of the modulator rate (f_{MOD}) of the delta-sigma modulator to its output data rate (f_{DR}) is the oversampling ratio (OSR). The relationship between f_{DR} and f_{MOD} is:

$$f_{DR} = f_{MOD} / OSR \quad \text{Equation 9.1}$$

A sinc3 filter is recommended since it's simple and requires less hardware resources. Equation 9.2 describes the transfer function of a sinc filter.

$$H(Z) = \left(\frac{1}{DR}\frac{(1-Z^{-DR})}{(1-Z^{-1})}\right)^{N} \quad \text{Equation 9.2}$$

where:

DR is the decimation rate;

N is the sinc filter order.

The filter can be implemented in an FPGA or DSP. The sinc filter creates a digital output code by taking a multi-order moving average of the modulator output over a certain number of modulator clock periods.

The higher the decimation rate, the higher the conversion accuracy, and the lower the output data rate. So, there is a trade-off between accuracy and data rate. All the characterization in this datasheet is tested with a sinc3 filter with an oversampling ratio (OSR) of 256.

The output data size is expressed in Equation 9.3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ Size = N \times \log_2 DR \quad \text{Equation 9.3}$$

The filter characteristics for a third-order sinc filter are summarized in Table 9.1.

Table 9.1 Sinc3 Filter Characteristics for 20 MHz CLKIN

Decimation Rate (DR)	*Data Output Rate (kHz)*	*Data Size (bits)*	*Filter Response (kHz)*
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

9.4. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1303 requires a 0.1μF bypass capacitor between AVDD and AGND, DVDD and DGND. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1303. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1303. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

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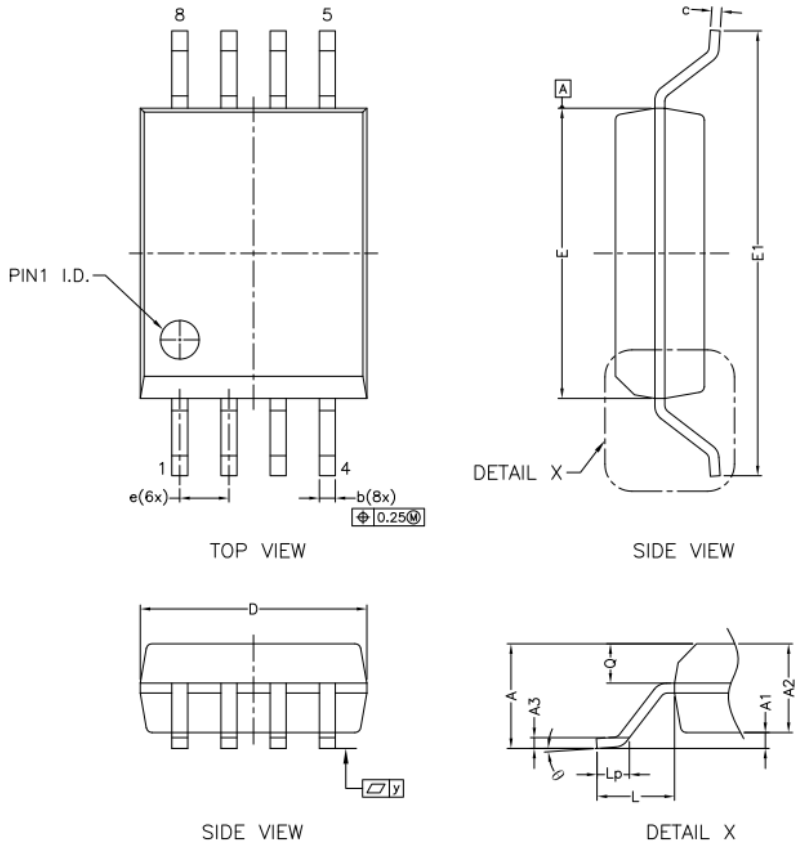
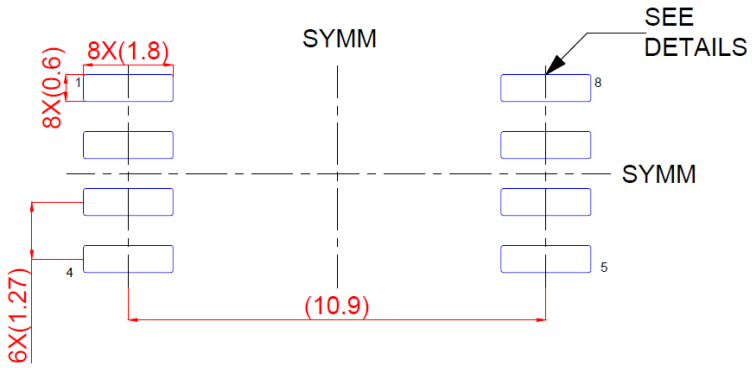
10. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

Figure 10.1 SOW8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE

Figure 10.2 SOW8 Package Board Layout Example

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11. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Internal clock frequency	Package Type	Package Drawing	SPQ	Release to Market
NSI1303E01-DSWVR	5	-50 ~ 50	Level-3	-40 to 125°C	10MHz	SOP8 (300mil)	SOW8	1000	NO
NSI1303E21-DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	10MHz	SOP8 (300mil)	SOW8	1000	NO
NSI1303E02-DSWVR	5	-50 ~ 50	Level-3	-40 to 125°C	20MHz	SOP8 (300mil)	SOW8	1000	YES
NSI1303E22-DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	20MHz	SOP8 (300mil)	SOW8	1000	YES

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1303	Click here	Click here	Click here	Click here

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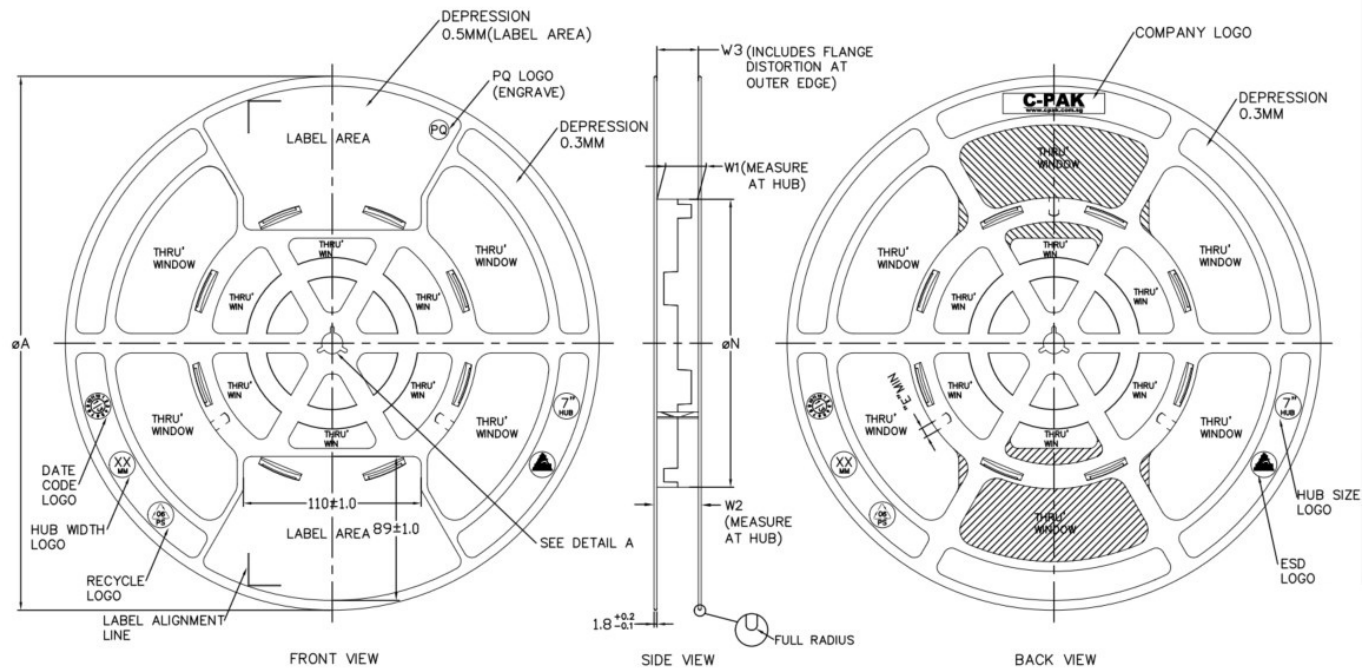
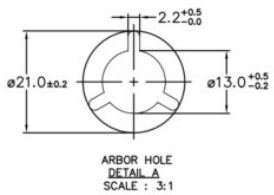
13. Tape and Reel Information





PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +3.0 -0.0	30.4		5.5
32MM	330	178	32.4 +3.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{5} TO 10^{9}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{6}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{6} TO 10^{9}	ANTISTATIC (COATED)	ALL TYPES

Figure 13.1 Tape Information

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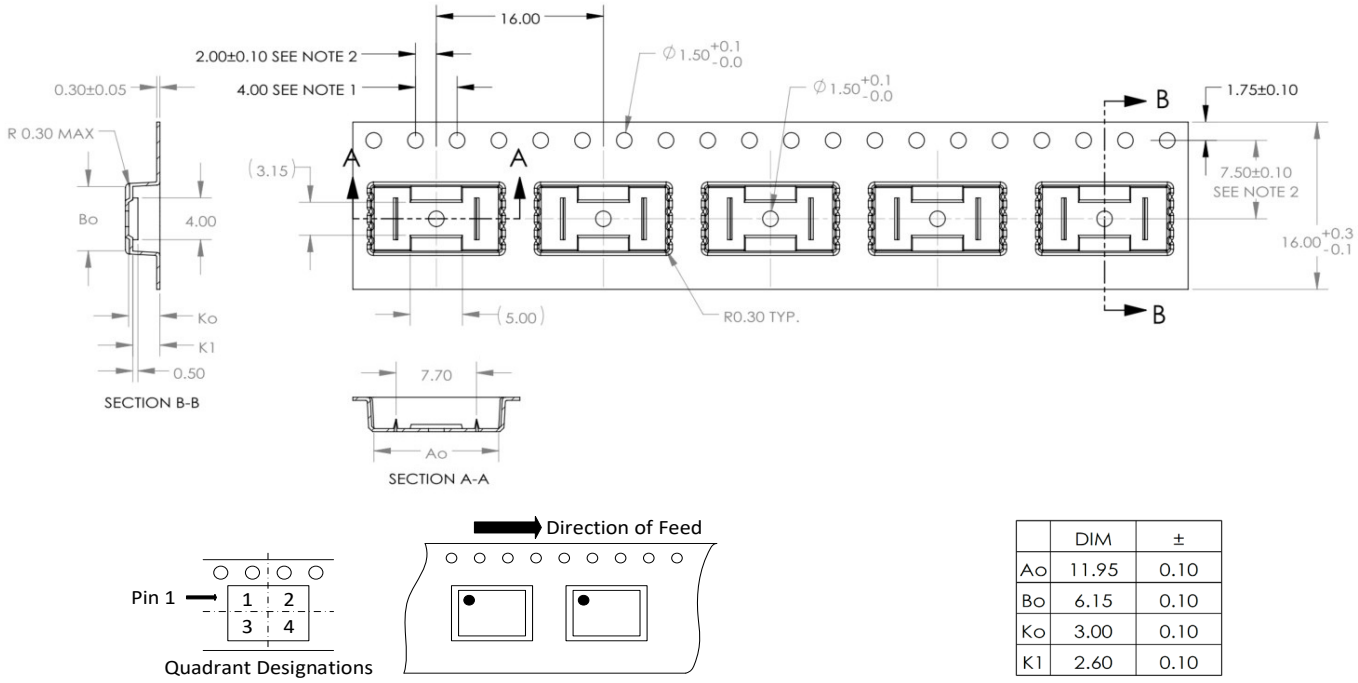

	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

Figure 13.2 Reel Information of SOP8(300mil)

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14. Revision History

Revision	Description	Date
1.0	Initial Release	2022/12/26
1.1	1. Update safety regulatory info 2. Update all NSI to NSI. 3. Update test temperature condition of I_{IB}, E_O and E_G 4. Update Viso from 5000Vrms to 5700Vrms	2024/11/29

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