

Product Overview

NSI1300D25-DSWWAR is a high-performance isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of $\pm 250\text{mV}$ ($\pm 320\text{mV}$ full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The device has a fixed gain of 8.2 and provides a differential analog output.

The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe functions including input common-mode overvoltage detection and missing VDD1 detection simplify system-level design and diagnostics.

Key Features

- Up to $7500\text{V}_{\text{rms}}$ Insulation voltage
- $\pm 250\text{mV}$ linear Input Voltage Range
- Fixed Gain: 8.2
- Low Offset Error and Drift:
NSI1300D25: $\pm 0.2\text{mV}$ (Max), $4\mu\text{V}/^\circ\text{C}$ (Max)
- Low Gain Error and Drift:
 $\pm 0.3\%$ (Max), $\pm 50\text{ppm}/^\circ\text{C}$ (Max)
- Low Nonlinearity and Drift:
 $\pm 0.03\%$ (Max), $\pm 1\text{ppm}/^\circ\text{C}$ (Typ)
- SNR: 86dB (Typ, BW=10kHz), 72dB (Typ, BW=100kHz)
- Wide bandwidth: 310kHz (Typ)
- High CMTI: $150\text{kV}/\mu\text{s}$ (Typ)

- System-Level Diagnostic Features:
 - VDD1 monitoring
 - Input common-mode overvoltage detection
- Operation Temperature: $-40^\circ\text{C} \sim 125^\circ\text{C}$
- RoHS-Compliant Packages: SOP8(600mil)

Safety Regulatory Approvals

- UL recognition: SOP8(600mil) $7500\text{V}_{\text{RMS}}$ for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA componen1t notice 5A approval
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Shunt current monitoring
- Motor Drives
- Uninterruptible Power Suppliers
- Solar Inverters

Device Information

Part Number	Package	Body Size
NSI1300D25-DSWWAR	SOP8(600mil)	6.25 mm × 13.60mm

Functional Block Diagrams

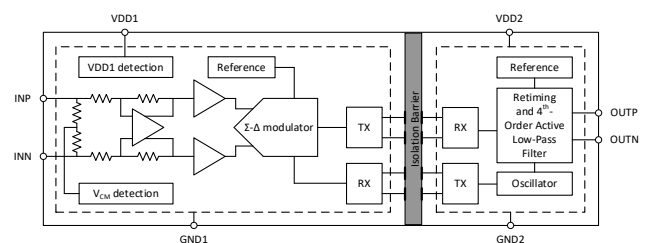


Figure 1. NSI1300 Block Diagram

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1. Pin Configuration and Functions

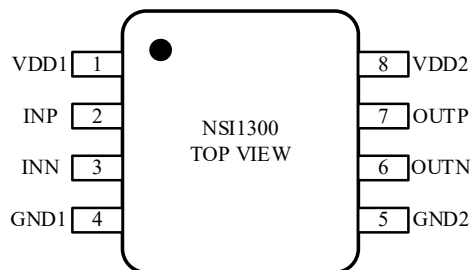


Figure 1.1 NSI1300 Package

Table 1.1 NSI1300 Pin Configuration and Description

NSI1300 PIN NO.	SYMBOL	FUNCTION
1	VDD1	Power supply for input side(3.0V to 5.5V)
2	INP	Positive analog input ($\pm 250\text{mV}$ recommended for NSI1300D25 and $\pm 50\text{mV}$ recommended for NSI1300D05)
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for output side(3.0V to 5.5V)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
Output Voltage	OUTP, OUTN	GND2-0.5		VDD2+0.5	V
Output current per Output Pin	I _o	-10		10	mA
Operating Temperature	T _{OPR}	-40		125	°C
Junction Temperature	T _J	-40		150	°C
Storage Temperature	T _{STG}	-55		150	°C

3. ESD Ratings ⁽¹⁾

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±1000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation or damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Side1 Power Supply	VDD1	3.0	5.0	5.5	V
Side2 Power Supply	VDD2	3.0	3.3	5.5	V
NSI1300D25	Differential input voltage before clipping output	V _{Clipping}	±320		mV
	Linear differential input full scale voltage	V _{FSR}	-250	250	mV
	Operating common-mode input voltage	V _{CM}	-0.16	0.8	V
Operating Ambient Temperature	T _A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP8(600mil)	Unit
Junction-to-ambient thermal resistance	R _{θJA}	78.9	°C/W

Parameters	Symbol	SOP8(600mil)	Unit
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	41.6	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	43.6	°C/W

6. Specifications

6.1. Electrical Characteristics: NSI1300D25-DSWWAR

(VDD1 = 3.0V ~ 5.5V, VDD2 = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = GND1 = 0V, T_A = -40°C to 125°C.

Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1		11.4	15.1	mA	
Side2 Supply Current	IDD2		6.3	8.4	mA	
VDD1 undervoltage detection threshold voltage	VDD1 _{UV}	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Common-mode overvoltage detection level	V _{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Input offset voltage	V _{OS}	-0.2	±0.01	0.2	mV	T _A =25°C 4.5V ≤ VDD1 ≤ 5.5V INP = INN = GND1
Input offset drift ⁽¹⁾	dV _{OS} /dT _A			4	μV/°C	
Common-mode rejection ratio	CMRR _{dc}		-106		dB	INP = INN, f _{IN} = 0 Hz, V _{CM min} ≤ V _{IN} ≤ V _{CM max}
	CMRR _{ac}		-106		dB	INP = INN, f _{IN} = 10 kHz, V _{CM min} ≤ V _{IN} ≤ V _{CM max}
Single-ended input resistance	R _{IN}		19		kΩ	T _A =25°C INN = GND1
Differential input resistance	R _{IND}		22		kΩ	
Input capacitance	C _I		2		pF	
Input bias current	I _{IB}	-24	-18	-12	μA	T _A =25°C INP = INN = GND1, I _{IB} = (I _{IBP} + I _{IBN}) / 2
Input bias current drift ⁽¹⁾	TCI _{IB}		±1		nA/°C	
Analog Output						
Nominal Gain			8.2		V/V	
Gain error	E _G	-0.3%	±0.05%	0.3%		T _A =25°C

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Gain error thermal drift ⁽¹⁾	TCE _G	-50	±15	50	ppm/°C	
Nonlinearity		-0.03%	±0.01%	0.03%		T _A =25°C
Nonlinearity drift ⁽¹⁾			±1		ppm/°C	
Total harmonic distortion ⁽³⁾	THD		-85		dB	V _{IN} = 500mVpp, f _{IN} = 10kHz, BW = 100kHz
Output noise			195		μV _{RMS}	INP = INN = GND1, BW = 100kHz
Signal to noise ratio	SNR	80	86		dB	V _{IN} = 500mVpp, f _{IN} = 1kHz, BW = 10kHz
			72		dB	V _{IN} = 500mVpp, f _{IN} = 10kHz, BW = 100kHz
Common-mode output voltage	V _{CMout}	1.39	1.44	1.49	V	
Failsafe differential output voltage	V _{FAILSAFE}		-2.6	-2.5	V	V _{CM} > V _{CMov} , or VDD1 missing
Output bandwidth	BW	250	310		kHz	
Power supply rejection ratio ⁽²⁾	PSRR _{dc}		-104		dB	PSRR vs VDD1, at DC
	PSRR _{ac}		-102		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	PSRR _{dc}		-90		dB	PSRR vs VDD2, at DC
	PSRR _{ac}		-85		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance	R _{OUT}		< 0.2		Ω	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t _r		1.3		μs	
Falling time of OUTP, OUTN	t _f		1.3		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t _{PD}		1.6	2.1	μs	
Analog setting time	t _{AS}		0.5		ms	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) The temperature drift is calculated within the whole temperature range (-40°C to 125°C).

(2) Input referred.

(3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).

6.2. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5V, VDD2 = 3.3V, Vin = -250mV to 250mV.

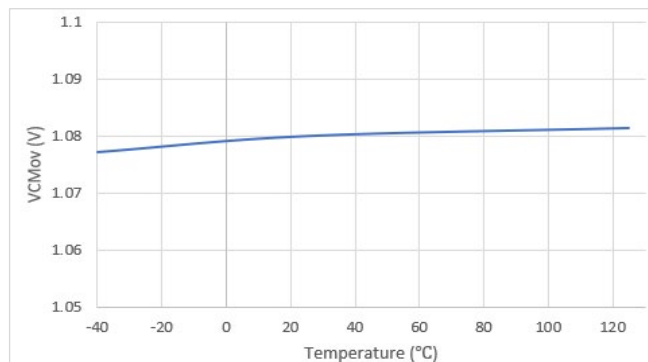


Figure 6.1 Common-Mode Overvoltage Detection Level vs Temperature

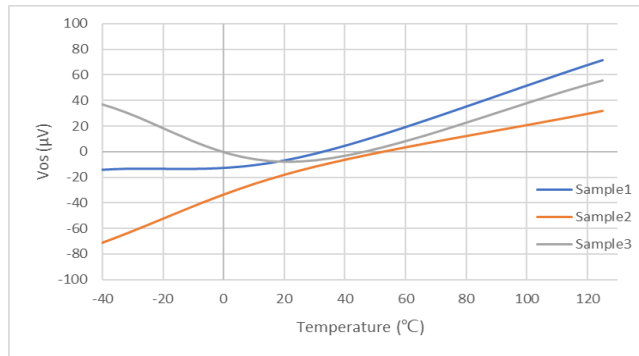


Figure 6.2 Input Offset Voltage vs Temperature

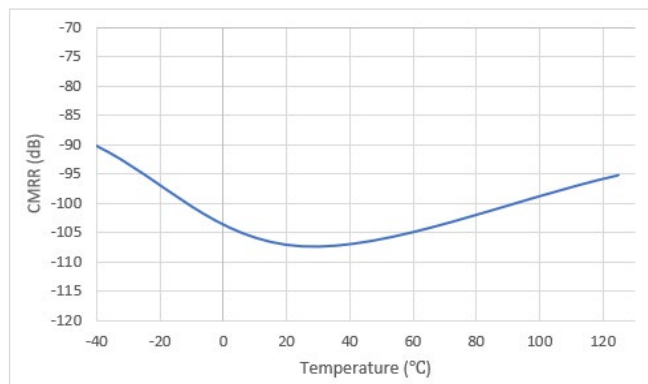


Figure 6.3 Common-Mode Rejection Ratio vs Temperature

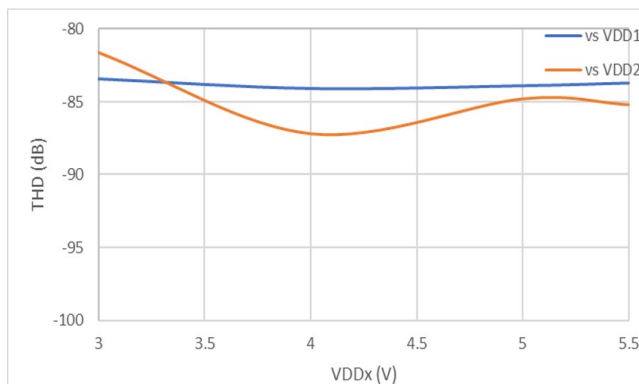


Figure 6.4 THD vs Supply Voltage

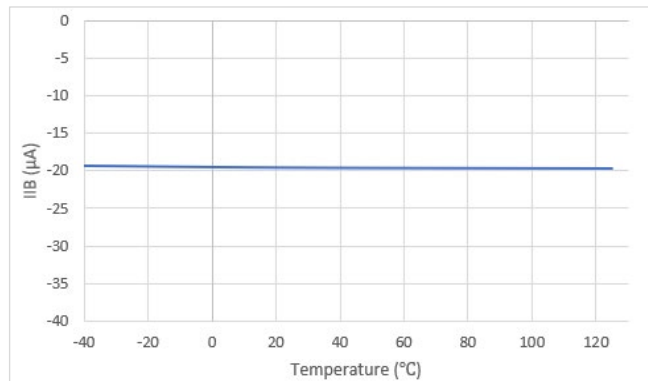


Figure 6.5 Input Bias Current vs Temperature

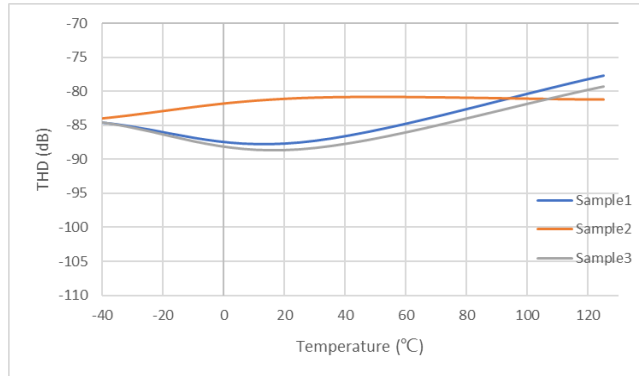


Figure 6.6 THD vs Temperature

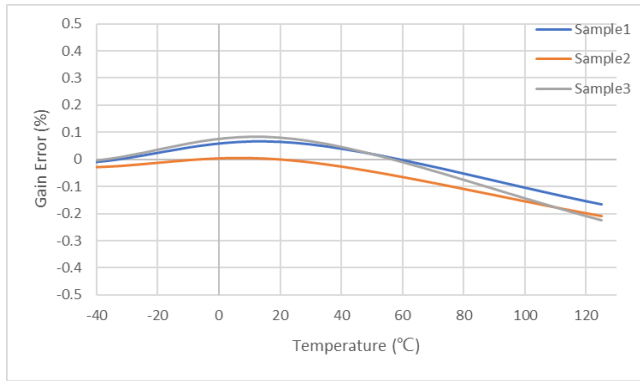


Figure 6.7 Gain Error vs Temperature

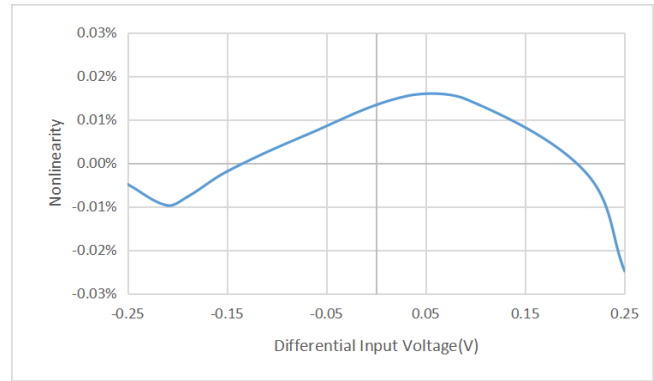


Figure 6.8 Nonlinearity vs Input Voltage

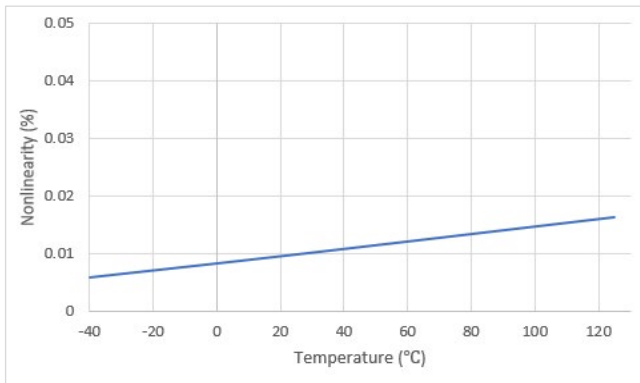


Figure 6.9 Nonlinearity vs Temperature

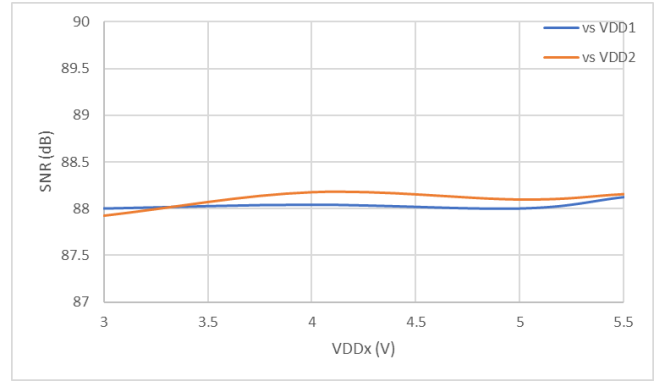


Figure 6.10 SNR vs Supply Voltage

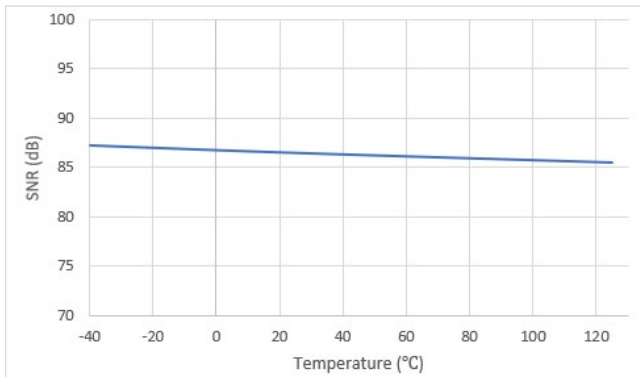


Figure 6.11 SNR vs Temperature

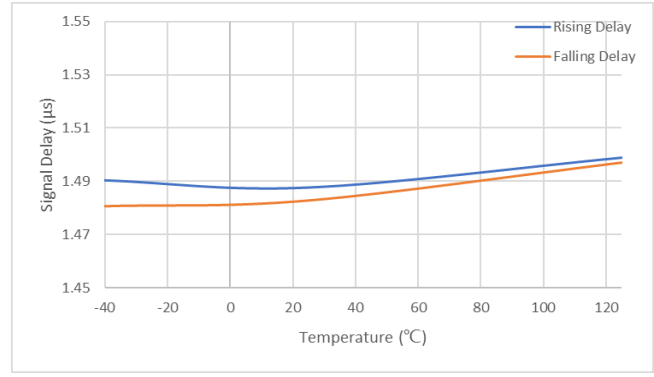


Figure 6.12 Vin to Vout Delay vs Temperature

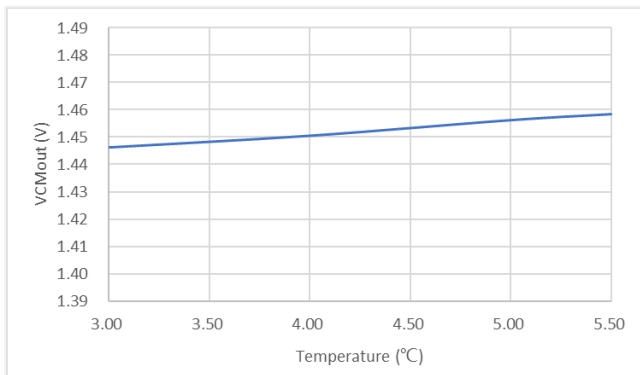


Figure 6.13 Output Common-Mode Voltage vs Side2 Supply Voltage

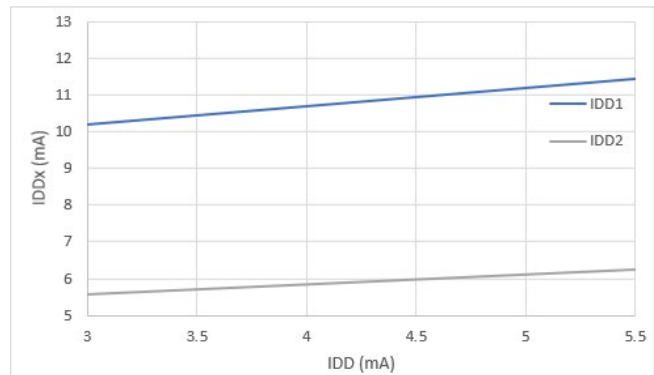


Figure 6.14 Supply Current vs Supply Voltage

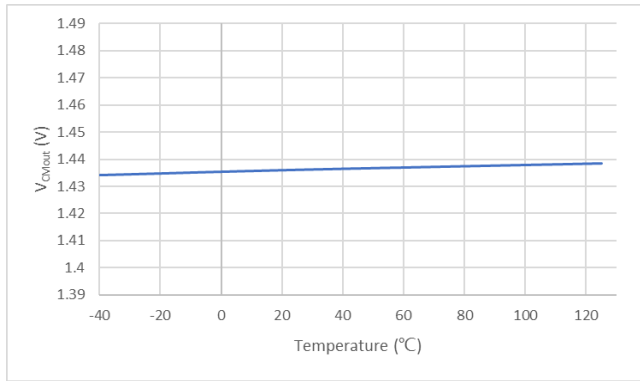


Figure 6.15 Output Common-Mode Voltage vs Temperature

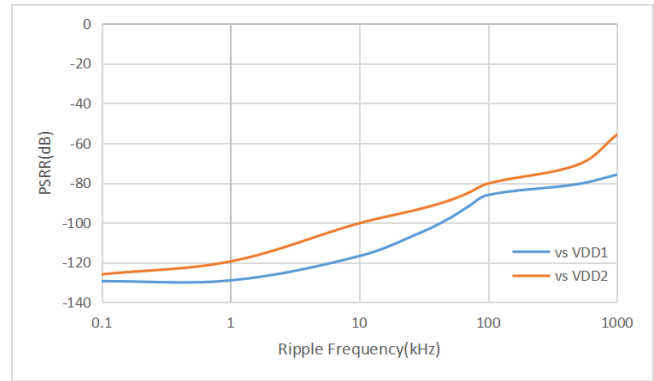


Figure 6.16 Power-Supply Rejection Ratio vs Ripple Frequency

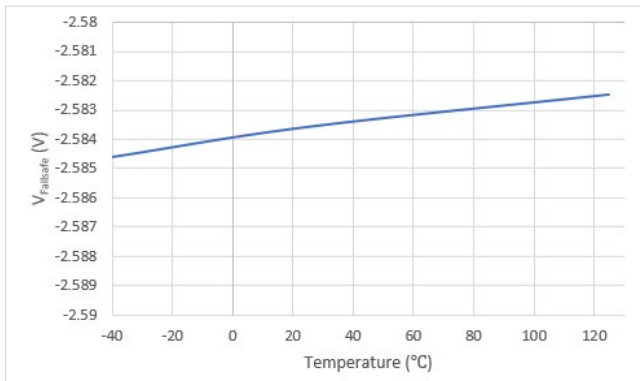


Figure 6.17 Fail-Safe Output Voltage vs Temperature

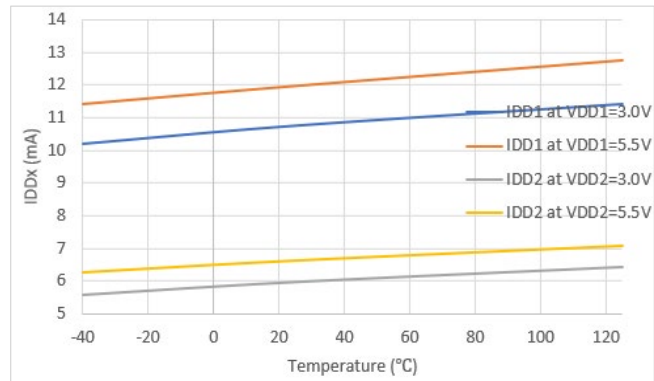


Figure 6.18 Supply Current vs Temperature

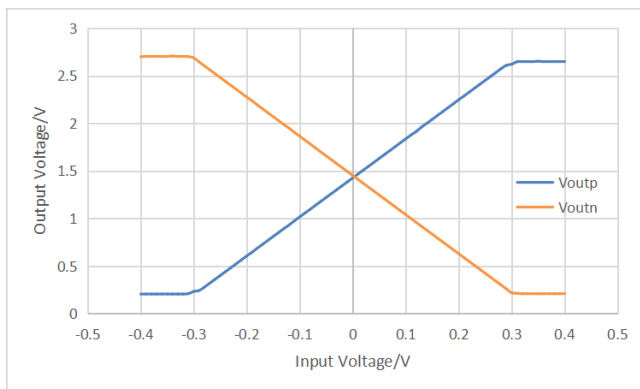


Figure 6.19 Output Voltage vs Input Voltage

6.3. Parameter Measurement Information

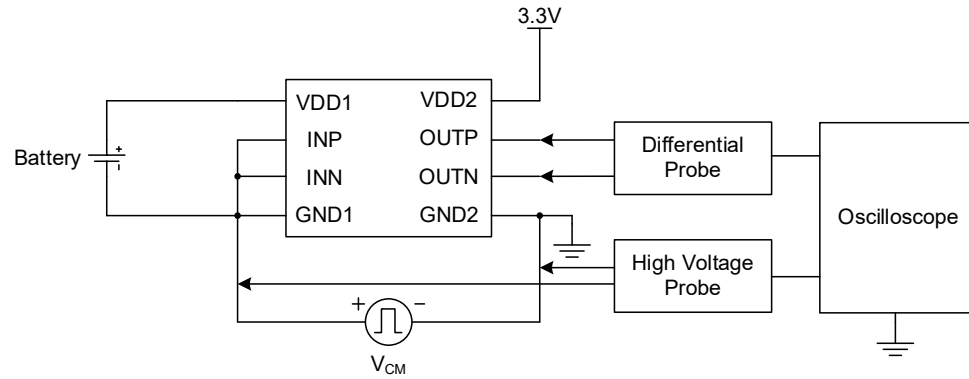


Figure 6.1 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Clearance	CLR	15	mm	IEC 60664-1
Minimum External Creepage	CPG	15	mm	IEC 60664-1
Distance Through Insulation	DTI	32	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 150 V_{\text{RMS}}$	I to IV
	For Rated Mains Voltage $\leq 300 V_{\text{RMS}}$	I to IV
	For Rated Mains Voltage $\leq 600 V_{\text{RMS}}$	I to IV
	For Rated Mains Voltage $\leq 1000 V_{\text{RMS}}$	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110,		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{\text{ini}}=V_{\text{IOTM}}$, $t_{\text{ini}} = 60 \text{ s}$, $V_{\text{pd(m)}}=1.2*V_{\text{IORM}}$, $t_{\text{m}}=10\text{s}$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{\text{ini}}=V_{\text{IOTM}}$, $t_{\text{ini}}=60\text{s}$, $V_{\text{pd(m)}}=1.6*V_{\text{IORM}}$, $t_{\text{m}}=10\text{s}$			
	Method b, routine test (100% production) and preconditioning (type test); $V_{\text{ini}}=1.2*V_{\text{IOTM}}$, $t_{\text{ini}}=1\text{s}$			

Description	Test Condition	Symbol	Value	Unit
	$V_{pd(m)}=1.875 \cdot V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			
Maximum transient isolation voltage	$t = 60 \text{ sec}$	V_{IOTM}	12000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	8000	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	12800	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$, $T_{amb}=25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500V$, $100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500V$, $T_{amb}=T_s$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	pF
Safety total power dissipation	$V_I = 5.5V$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	P_s	792	mW
Safety input, output, or supply current	$V_I = 5.5V$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	P_s	158	mA
Maximum safety temperature		T_s	150	$^{\circ}C$
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60 \text{ s}$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1 \text{ s}$ (100% production test)	V_{ISO}	7500	V_{RMS}

7.3. Regulatory Information

The NSI1300D25-DSWWAR are approved by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 7500 V _{RMS} Isolation voltage	Single Protection, 7500V _{RMS} Isolation voltage	Reinforce Insulation V _{IORM} =2121 V _{PEAK} V _{IOTM} =10600 V _{PEAK} V _{IOSM} =12800 V _{PEAK}	Reinforced Insulation	7500 V _{RMS} for 1min
E500602	E500602	40052820	CQC24001426054	R50574061

8. Function Description

8.1. Overview

The NSI1300D25-DSWWAR is a high performance isolated amplifier that accept fully-differential input. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ - Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator convert the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated side1 and side2 voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the side2 and has a differential output.

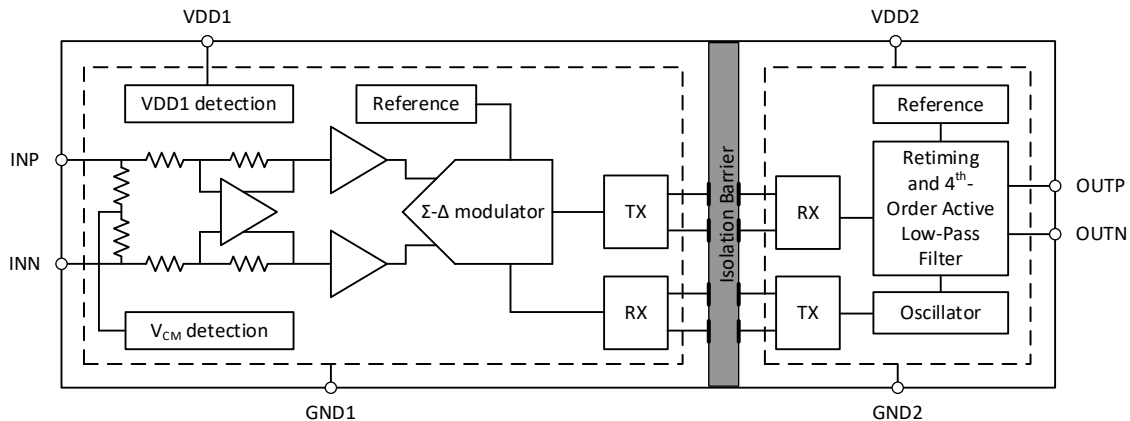


Figure 8.1 Function Block Diagram

8.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Analog Output

For linear input range, the analog output of NSI1300D25-DSWWAR has a fixed gain of 8.2. If a full-scale input signal is applied between VINP & VINN ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically, 2.45V for positive clipping and -2.45V for negative clipping).

In addition, NSI1300D25-DSWWAR integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated in following conditions:

- When the undervoltage of VDD1 is detected ($V_{DD1} < V_{DD1_{UV}}$).
- When the overvoltage of common-mode input voltage is detected ($V_{CM} > V_{CMov}$).

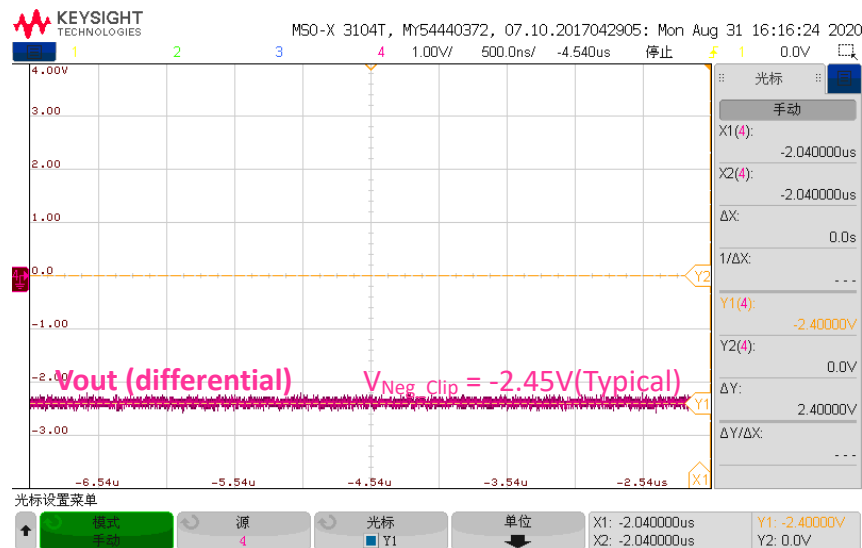


Figure 8.2 Typical negative clipping output

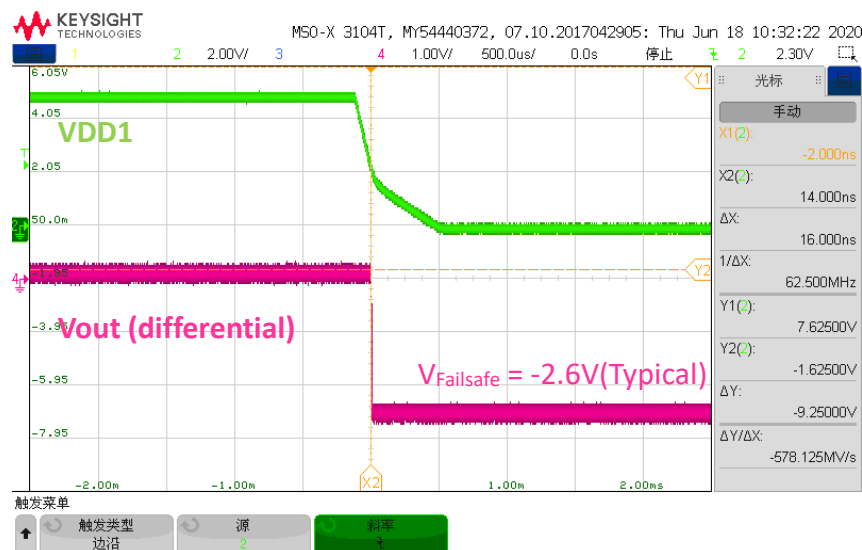


Figure 8.3 Typical Failsafe output when VDD1 undervoltage

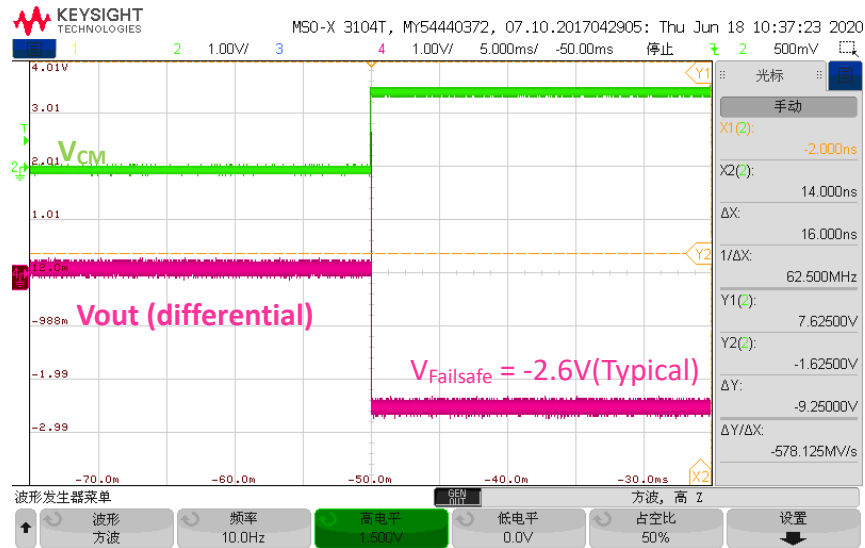


Figure 8.4 Typical Failsafe output when input common mode signal overvoltage

9. Application Note

9.1. Typical Application Circuit

NSI1300D25-DSWWAR is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 9.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1300D25-DSWWAR through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add $>1k\Omega$ resistor on the OUTP and OUTN pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

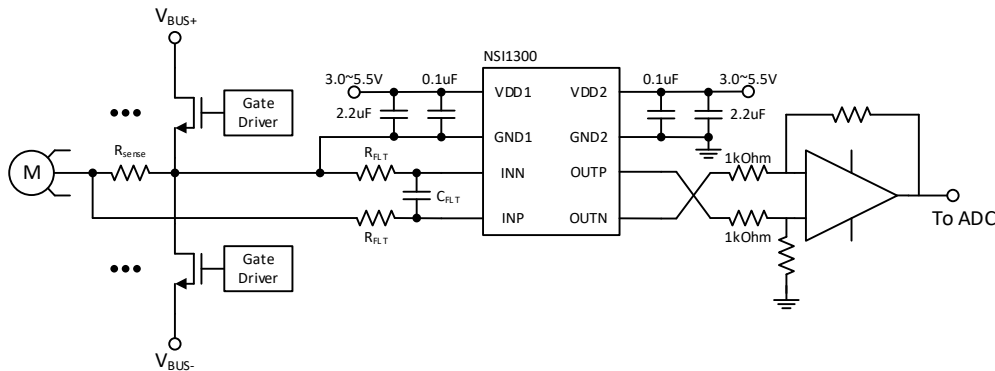


Figure 9.1 Typical application circuit in phase current sensing

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

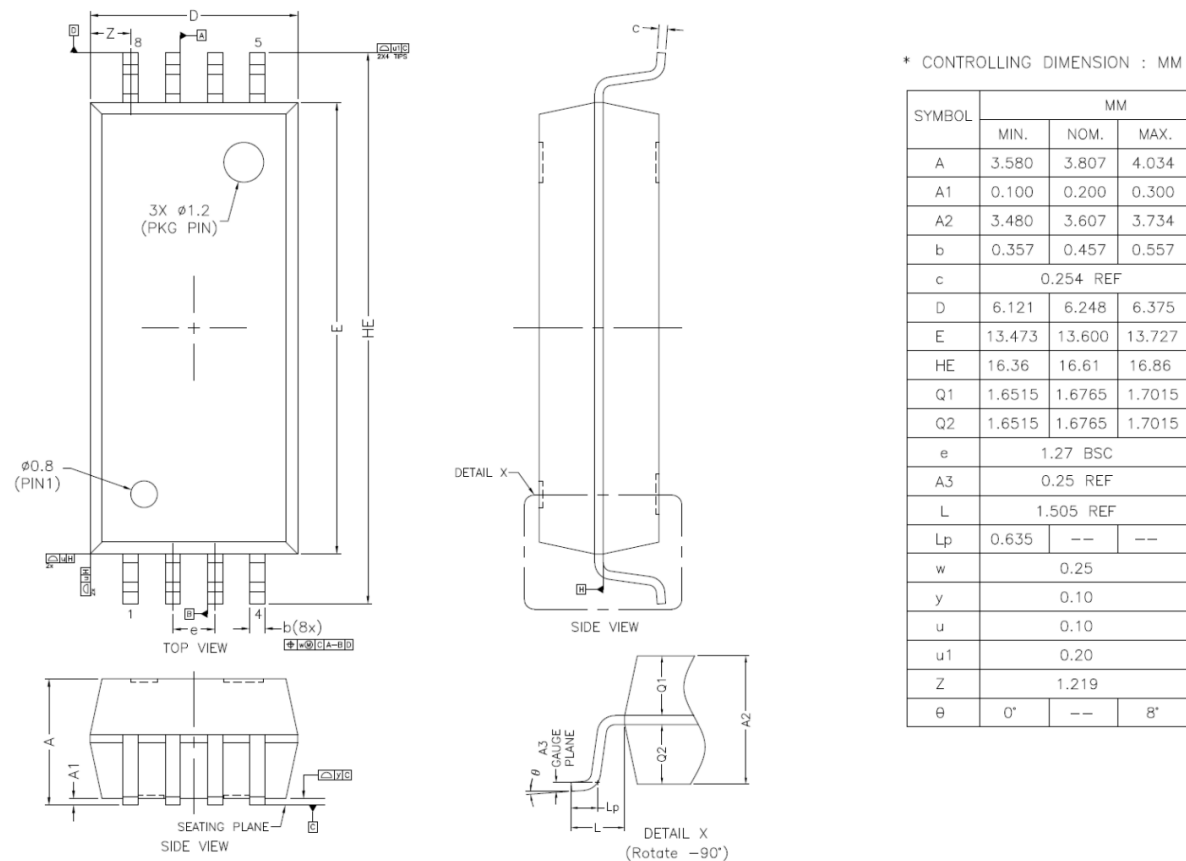
- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1300 requires a 0.1 μ F bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10 μ F capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1300. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1300. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

10. Package Information



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOP8(600mil)/SOWW8 Package Shape and Dimension in millimeters

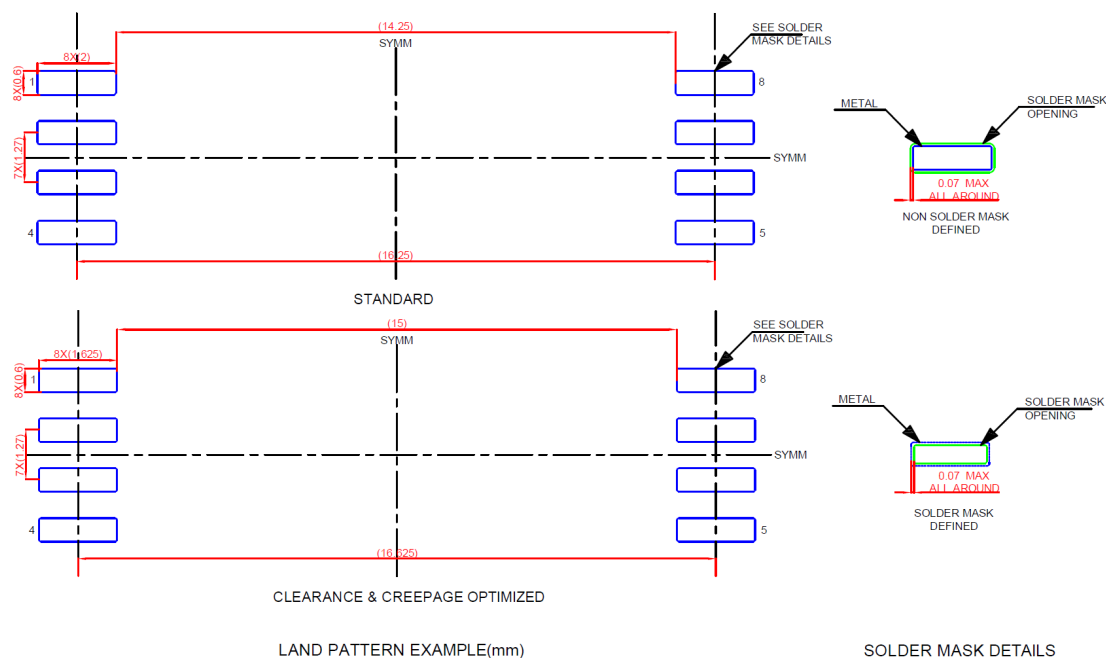


Figure 10.2 SOP8(600mil) Package Board Layout Example

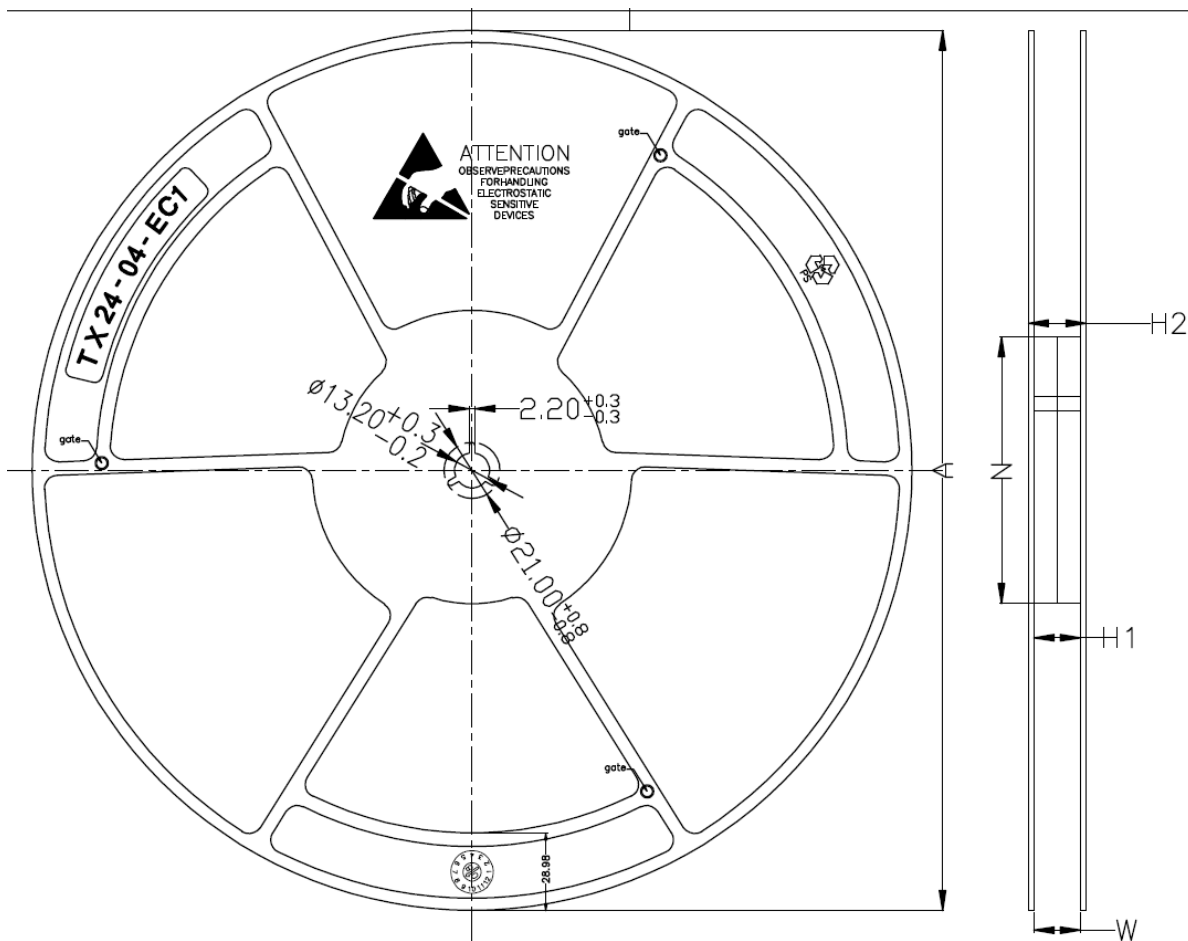
11. Ordering Information

Part No.	Isolation Rating	Linear Input Range	MSL	Device Marking	Temperature	Auto-motive	Package Type	Package Drawing	SPQ	MPQ
NSI1300D25 - DSWWAR	7.5kV	-250 ~ 250mV	Level-3	NSi13 00D25D	-40 to 125°C	NO	SOP8 (600mil)	SOWW8	1000	1000

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1300D25-DSWWAR	Click here	Click here	Click here	Click here

13. Tape and Reel Information



PRODUCT SPECIFICATIONS					
TAPE WIDTH	ϕA^{+2}_{-2}	ϕN^{+2}_{-2}	$H1^{+2}_{-0}$	$H2^{+1}_{-1}$	$W^{+3.5}_{-0.2}$
24MM	330	100	24.4	28.6	24.4

NOTES:

- 1.MATERIAL:DISSIPATIVE(BLACK)
- 2.FLANGE WARPAGE:3 MM MAXIMUM
- 3.ALL DIMENSIONS ARE IN MM
- 4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
- 5.GENERAL TOLERANCE: ± 0.25 MM

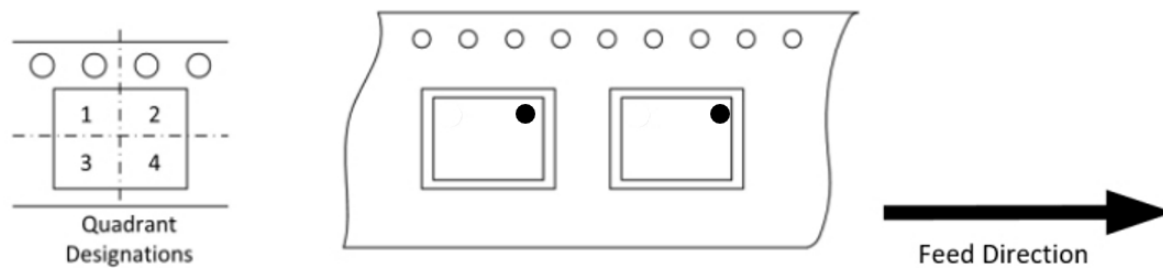
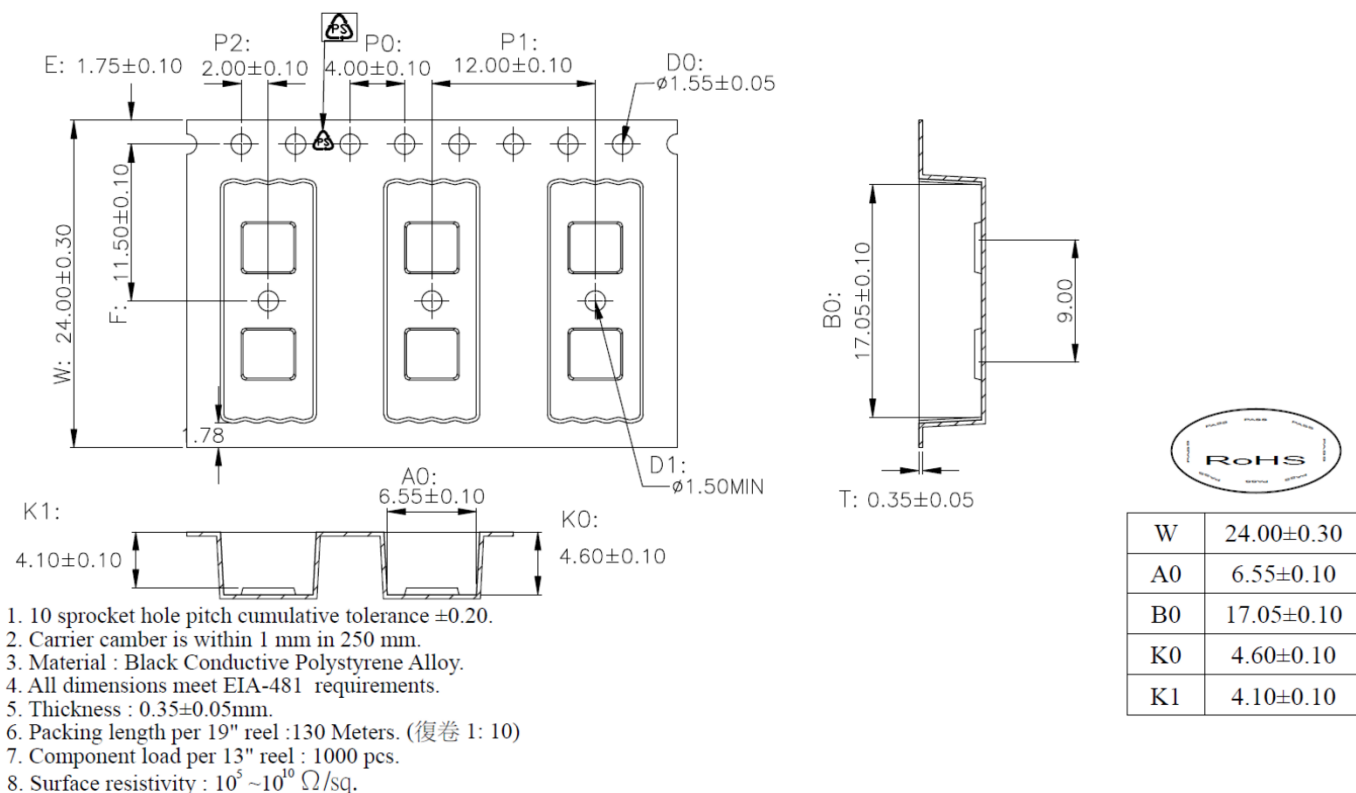


Figure 13.1 Tape and Reel Information of SOP8(600mil)

14. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/8/15
1.1	• Update Insulation Characteristics in 7.2 and Regulatory Information in 7.3. • Update Package Related Information and Pad Diagram in Part 10. • Update Template of Datasheet.	2026/7/27

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