

Product Overview

NSI1200C is a high-performance isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of ± 250 mV (± 320 mV full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The device has a fixed gain of 8.0 and provides a differential analog output.

The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe functions including input common-mode overvoltage detection and missing VDD1 detection simplify system-level design and diagnostics.

Key Features

- Up to 5000 V_{rms} Insulation voltage
- ± 250 mV linear Input Voltage Range
- Fixed Gain: 8.0
- Low Offset Error and Drift:
 ± 0.5 mV (Max), ± 5 μ V/ $^{\circ}$ C (Max)
- Low Gain Error and Drift:
 $\pm 0.3\%$ (Max), ± 30 ppm/ $^{\circ}$ C (Max)
- Low Nonlinearity and Drift:
 $\pm 0.05\%$ (Max), ± 1 ppm/ $^{\circ}$ C (Typ)
- SNR: 72 dB (Typ, BW=100 kHz)
- Wide bandwidth: 220 kHz (Typ)
- High CMTI: 125 kV/ μ s (Typ)
- System-Level Diagnostic Features:

- VDD1 monitoring
 - Input common-mode overvoltage detection
- Operation Temperature: -40° C \sim 125° C
- AEC-Q100 qualified for automotive applications: Grade 1
- RoHS-Compliant Packages:
 - SOW8 wide body (SOP8 300mil)

Safety Regulatory Approvals

- UL recognition:
 - SOW8: 5000 V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- On Board Chargers
- DC/DC Converters
- Charging Piles
- Traction Inverters

Device Information

Part Number	Package	Body Size
NSI1200C-Q1SWVR	SOP8(300mil)	5.85mm × 7.50mm

Functional Block Diagrams

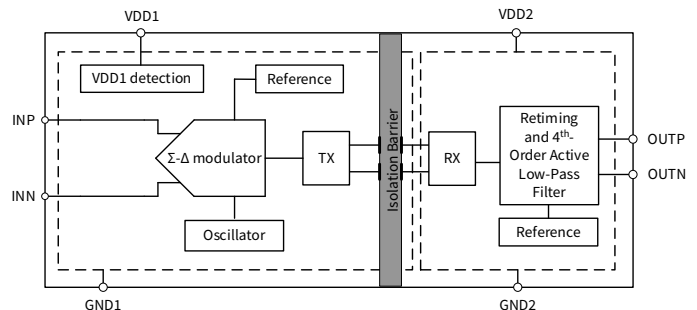


Figure 1. NSI1200C Block Diagram

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1. Pin Configuration and Functions

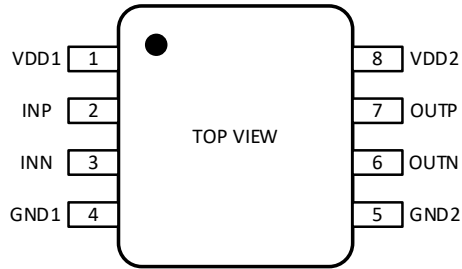


Figure 1.1 NSI1200C Package

Table 1.1 NSI1200C Pin Configuration and Description

NSI1200C PIN NO.	SYMBOL	FUNCTION
1	VDD1	Power supply for input side (3.0 V to 5.5 V)
2	INP	Positive analog input (±250 mV recommended for NSI1200C)
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for output side (3.0 V to 5.5 V)

2. Absolute Maximum Ratings⁽¹⁾

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage ⁽²⁾	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
Output Voltage	OUTP, OUTN	GND2-0.5		VDD2+0.5	V
Input current per IO Pin	I _{in}	-10		10	mA
Junction Temperature	T _J	-40		150	°C
Storage Temperature	T _{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

(2) VDD1 to GND1, VDD2 to GND2

3. ESD Ratings⁽¹⁾

Parameters	Test condition	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per AEC-Q100-002-RevD	±4000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	±1000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation or damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Side1 Power Supply	VDD1	3.0	5.0	5.5	V
Side2 Power Supply	VDD2	3.0	3.3	5.5	V
Differential input voltage before clipping output	V _{Clipping}		±320		mV
Linear differential input full scale voltage	V _{FSR}	-250		250	mV
Operating common-mode input voltage	V _{CM}	-0.16		2.6	V
Operating Ambient Temperature	T _A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP8(300mil)	Unit
Junction-to-ambient thermal resistance	R _{θJA}	86	°C/W
Junction-to-case (top) thermal resistance	R _{θJC(top)}	28	°C/W
Junction-to-board thermal resistance	R _{θJB}	42	°C/W

Parameters	Symbol	SOP8(300mil)	Unit
Junction-to-top characterization parameter	Ψ_{JT}	4	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	42	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD1 = 3.0 V ~ 5.5 V, VDD2 = 3.0 V ~ 5.5 V, INP = -250 mV to +250 mV, and INN = GND1 = 0 V, T_A = -40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5 V, VDD2 = 3.3 V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1	3.4	5.8	8.0	mA	
Side2 Supply Current	IDD2	3.4	5.1	6.8	mA	
VDD1 undervoltage detection threshold voltage	VDD1 _{UV}	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Common-mode overvoltage detection level	V _{CMov}		2.8		V	Detection level has a typical hysteresis of 96 mV
Input offset voltage ⁽¹⁾	V _{OS}	-0.5	±0.1	0.5	mV	INP = INN = GND1, at T _A = 25°C
Input offset drift ⁽²⁾	TCV _{OS}	-5	±1.5	5	µV/°C	
Common-mode rejection ratio	CMRR _{dc}		-98		dB	INP = INN, f _{IN} = 0 Hz, V _{CM min} ≤ VIN ≤ V _{CM max}
	CMRR _{ac}		-95		dB	INP = INN, f _{IN} = 10 kHz, V _{CM min} ≤ VIN ≤ V _{CM max}
Single-ended input resistance	R _{IN}		29		kΩ	INN = GND1
Differential input resistance	R _{IND}		29.5		kΩ	
Input capacitance	C _i		12		pF	
Input bias current	I _{IB}		-0.1		µA	INP = INN = GND1, I _{IB} = (I _{IBP} + I _{IBN}) / 2, at T _A = 25°C
Input bias current drift ⁽²⁾	TCI _{IB}		±1		nA/°C	
Analog Output						
Nominal Gain			8.0		V/V	
Gain error ⁽¹⁾	E _G	-0.3%	±0.05%	0.3%		at T _A = 25°C
Gain error thermal drift ⁽¹⁾⁽²⁾	TCE _G	-30	±5	30	ppm/°C	
Nonlinearity ⁽¹⁾⁽³⁾		-0.05%	±0.01%	0.05%		at T _A = 25°C

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Nonlinearity drift ^{(1) (2)}			±1		ppm/°C	
Total harmonic distortion ⁽⁴⁾	THD		-90	-70	dB	V _{IN} =500 mV _{pp} , f _{IN} = 1 kHz, BW = 10 kHz
			-75		dB	V _{IN} =500 mV _{pp} , f _{IN} = 10 kHz, BW = 100 kHz
Output noise			360		μV _{RMS}	INP = INN = GND1, BW = 100 kHz
Signal to noise ratio	SNR		85		dB	V _{IN} = 500 mV _{pp} , f _{IN} = 1kHz, BW = 10 kHz
			72		dB	V _{IN} = 500 mV _{pp} , f _{IN} = 10 kHz, BW = 100 kHz
Common-mode output voltage	V _{CMout}	1.37	1.45	1.50	V	
Failsafe differential output voltage	V _{FAILSAFE}		-2.6	-2.5	V	V _{CM} >V _{CMov} , or VDD1 missing
Output bandwidth	BW	175	220		kHz	
Power supply rejection ratio ⁽⁵⁾	PSRR _{dc}		-110		dB	PSRR vs VDD1, at DC
	PSRR _{ac}		-100		dB	PSRR vs VDD1, 100 mV and 10 kHz ripple
	PSRR _{dc}		-110		dB	PSRR vs VDD2, at DC
	PSRR _{ac}		-90		dB	PSRR vs VDD2, 100 mV and 10 kHz ripple
Output resistance	R _{OUT}		< 0.2		Ω	
Output current limit	I _{OUT}		±13		mA	
Common-mode transient immunity	CMTI	100	125		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t _r		1.7		μs	
Falling time of OUTP, OUTN	t _f		1.7		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t _{PD}		1.6	2.3	μs	C _{LOAD} =15 pF
Analog setting time	t _{AS}		0.5		ms	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) The typical value includes one standard deviation (sigma) range under typical operating conditions.

(2) The temperature drift is calculated with the whole temperature range (-40°C to 125°C).

(3) Nonlinearity is defined as half of the peak-peak value of the deviation between the measuring point and the fitting curve divided by the full-scale range of the output voltage.

(4) THD is defined as the ratio of the sum of the rms value of first nine higher harmonics to the amplitude of the fundamental.

(5) Input referred.

6.2. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5 V, VDD2 = 3.3 V, INN=GND1=0 V, INP = -250 mV to 250 mV, $f_{IN} = 1$ kHz, BW = 10 kHz.

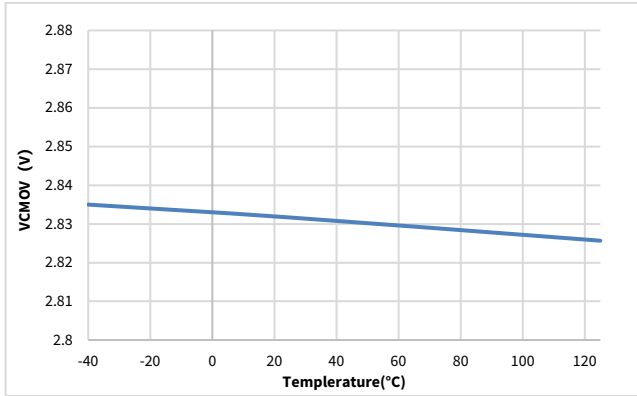


Figure 6.1 Common-Mode Overvoltage Detection Level vs Temperature

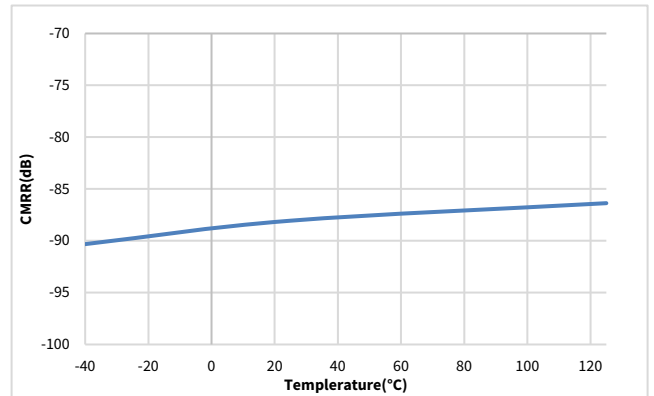


Figure 6.4 Common-Mode Rejection Ratio vs Temperature

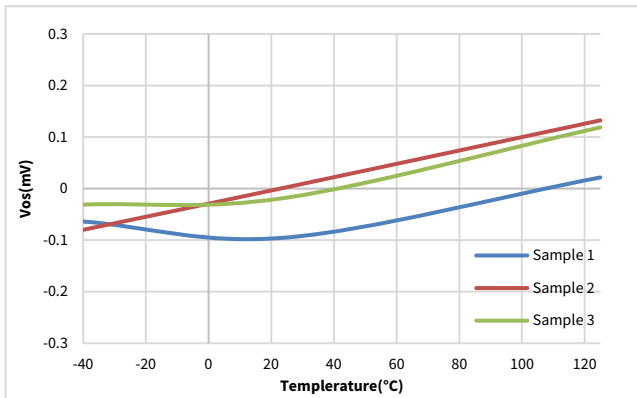


Figure 6.2 Input Offset Voltage vs Temperature

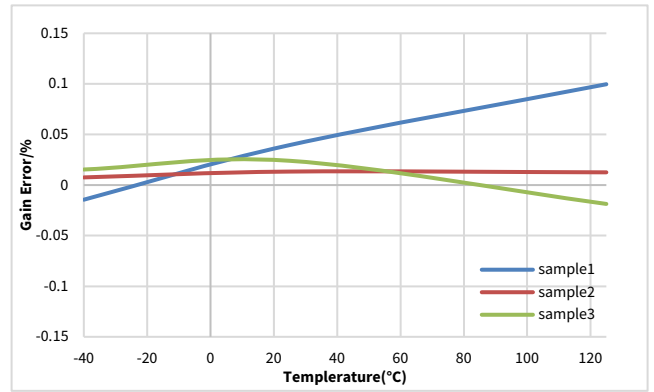


Figure 6.5 Gain Error vs Temperature

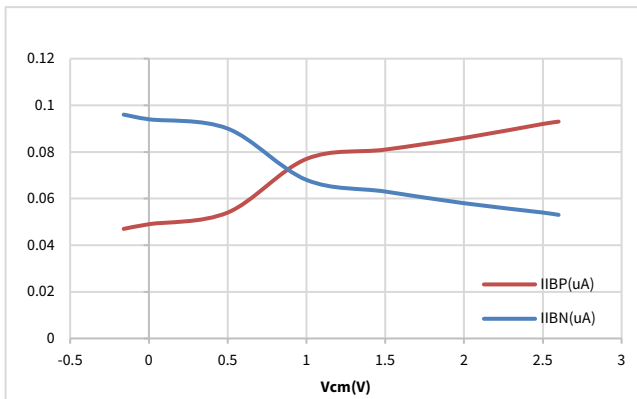


Figure 6.3 Input Bias Current vs Common-Mode Voltage

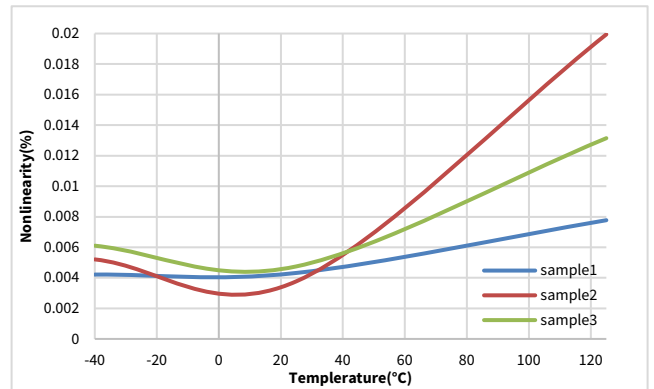


Figure 6.6 Nonlinearity vs Temperature

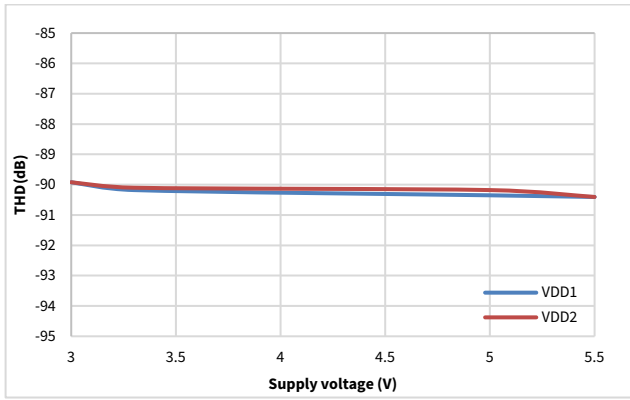


Figure 6.7 THD vs Supply Voltage

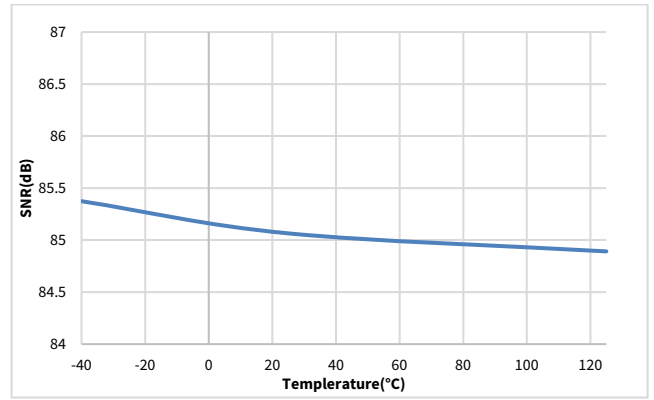


Figure 6.11 SNR vs Temperature

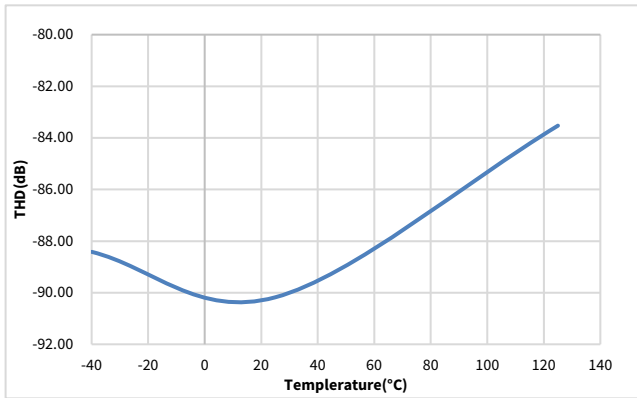


Figure 6.8 THD vs Temperature

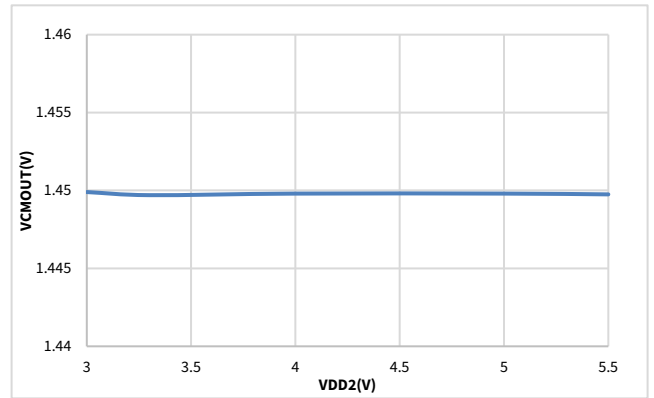


Figure 6.12 Output Common-Mode Voltage vs Side2 Supply Voltage

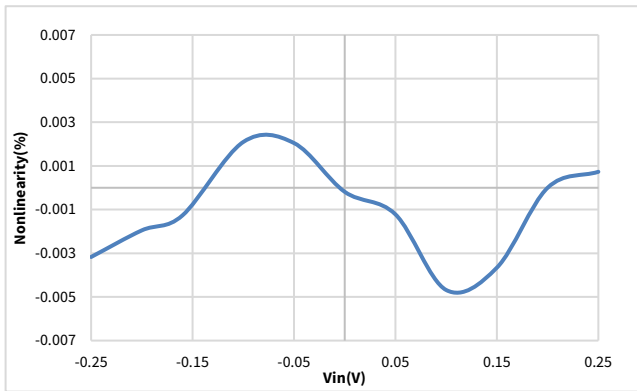


Figure 6.9 Nonlinearity vs Input Voltage

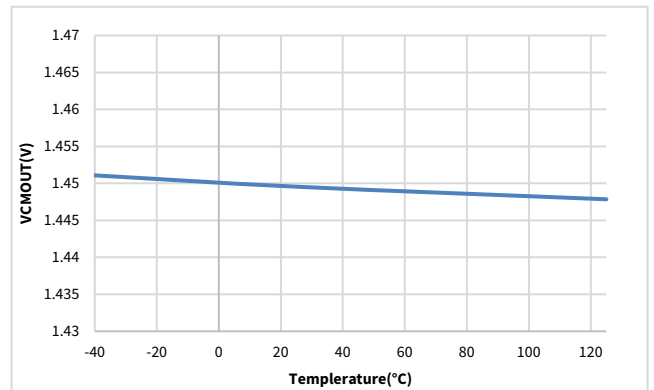


Figure 6.13 Output Common-Mode Voltage vs Temperature

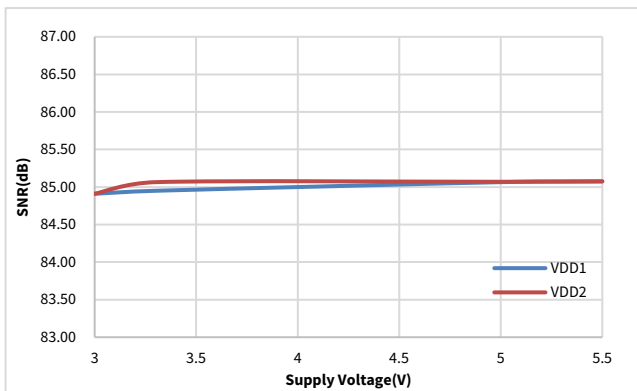


Figure 6.10 SNR vs Supply Voltage

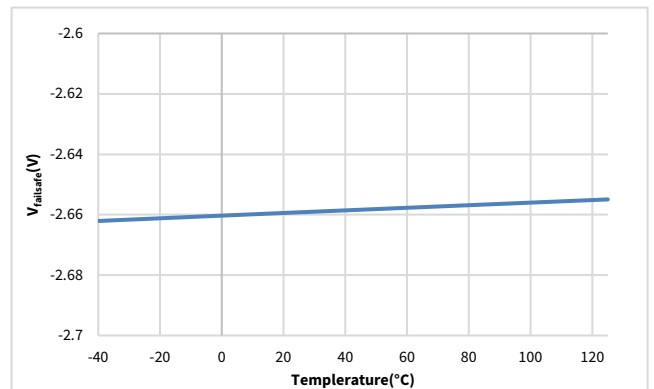


Figure 6.14 Fail-Safe Output Voltage vs Temperature

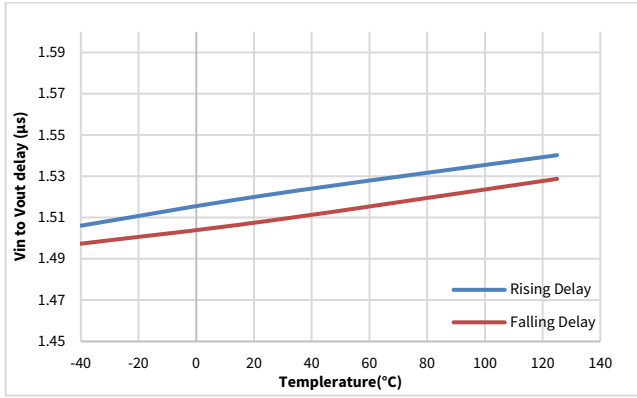


Figure 6.15 Vin to Vout Delay vs Temperature

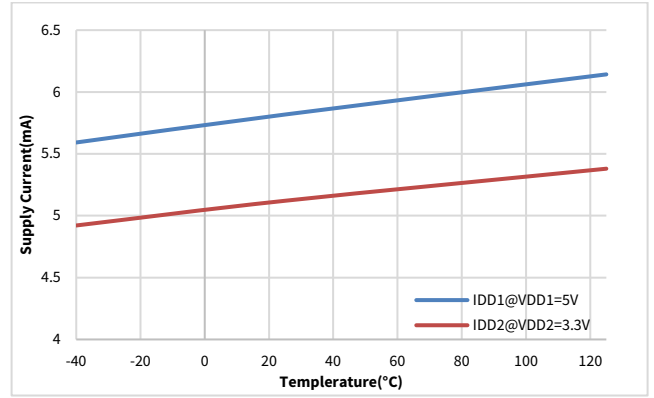


Figure 6.18 Supply Current vs Temperature

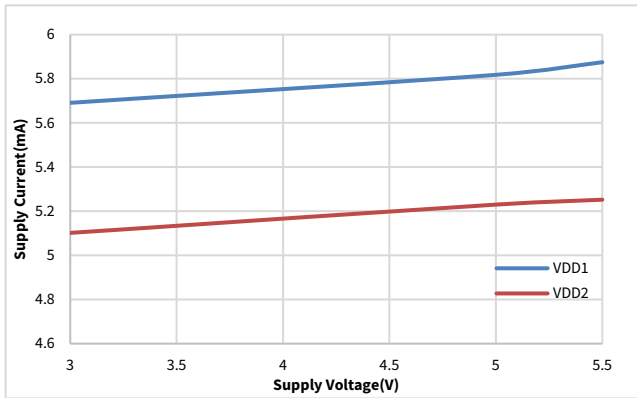


Figure 6.16 Supply Current vs Supply Voltage

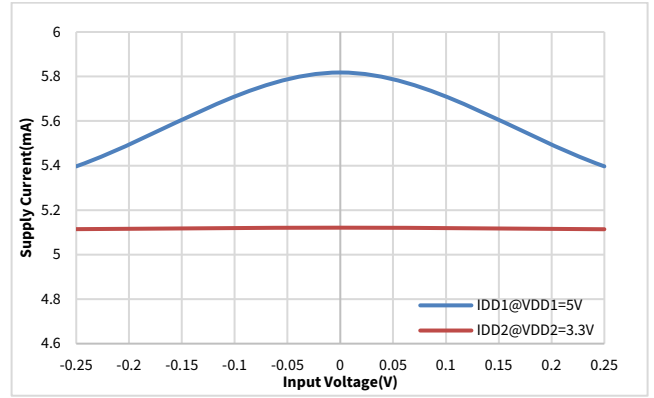


Figure 6.19 Supply Current vs Input Voltage

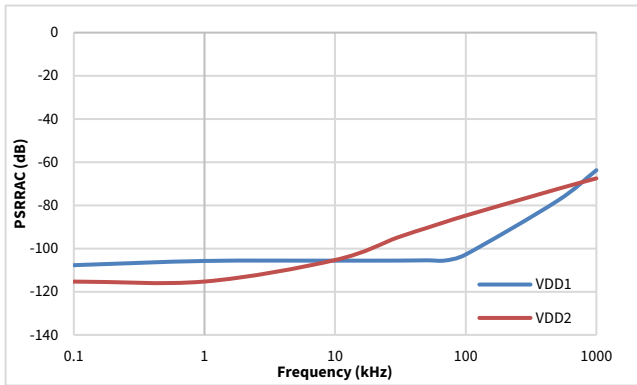


Figure 6.17 Power-Supply Rejection Ratio vs Ripple Frequency

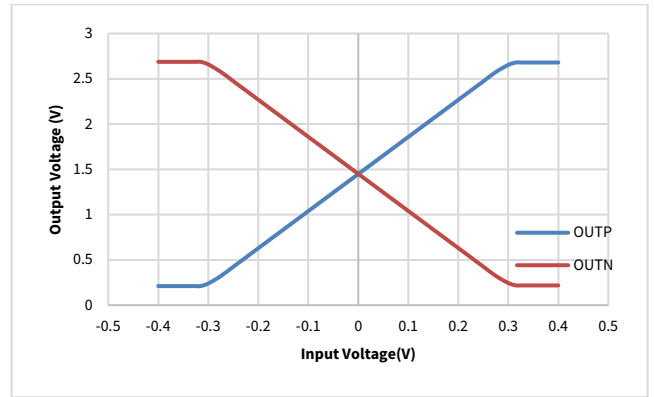


Figure 6.20 Output Voltage vs Input Voltage

6.3. Parameter Measurement Information

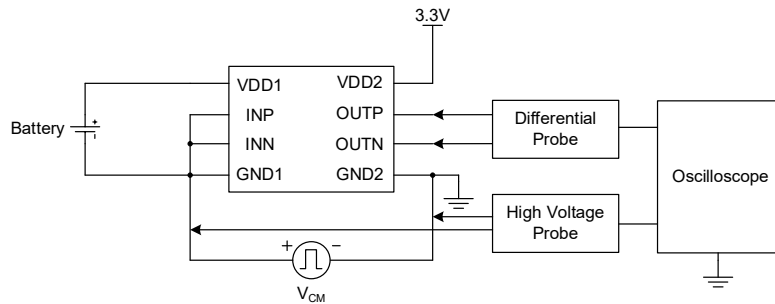


Figure 6.21 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28	µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage \leq 150 Vrms	I to IV
	For Rated Mains Voltage \leq 300 Vrms	I to IV
	For Rated Mains Voltage \leq 600 Vrms	I to IV
	For Rated Mains Voltage \leq 1000 Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60$ s, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10$ s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60$ s, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10$ s			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1$ s			pC

Description	Test Condition	Symbol	Value	Unit
	$V_{pd(m)}=1.875 \cdot V_{IORM}$, $t_m=1$ s (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			
Maximum transient isolation voltage	$t = 60$ sec	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50 us waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50 us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500$ V, $T_{amb}=25^\circ\text{C}$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500$ V, $100^\circ\text{C} \leq T_{amb} \leq 125^\circ\text{C}$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500$ V, $T_{amb}=T_s$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1$ MHz	C_{IO}	0.8	pF
Safety total power dissipation	$V_I = 5.5$ V, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$	P_s	1453	mW
Safety input, output, or supply current	$\theta_{JA} = 86^\circ\text{C/W}$ for SOW8, $V_I = 5.5$ V, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$	I_s	264	mA
Maximum safety temperature		T_s	150	$^\circ\text{C}$
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60$ s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1$ s (100% production test)	V_{ISO}	5000	V_{RMS}

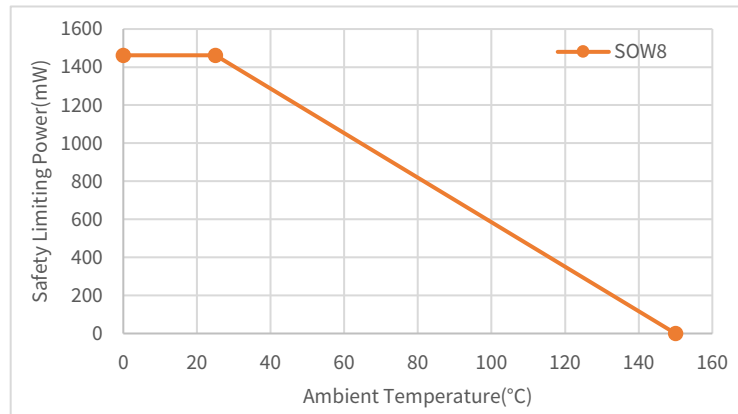


Figure 7.1 NSI1200C Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE 0884-17

7.3. Regulatory Information

The NSI1200C-Q1SWVR is approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000 V _{rms} Isolation voltage	Single Protection, 5000 V _{rms} Isolation voltage	Reinforce Insulation V _{IORM} =2121 V _{PEAK} V _{IOTM} =8000 V _{PEAK} V _{IOSM} =10000 V _{PEAK}	Reinforced insulation	5000 Vrms for 1 min
E500602	E500602	File (pending)	File (pending)	R50574061

8. Function Description

8.1. Overview

The NSI1200C is a high-performance isolated amplifier that accepts fully-differential input. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ - Δ modulator in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated input side and output side voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order filter on the output side and has a differential output.

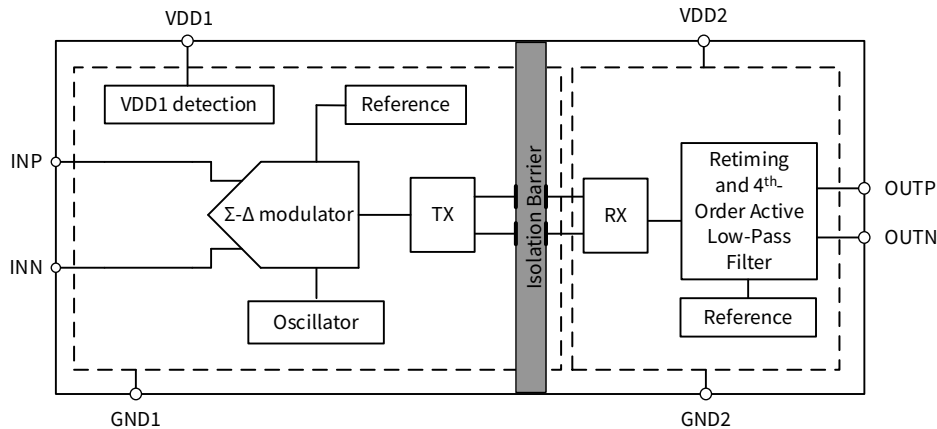


Figure 8.1 Function Block Diagram

8.2. Analog Input

The analog input of the NSI1200C is a switched-capacitor circuit based on the second-order Σ - Δ modulator. The Equivalent circuit of analog input is shown in Figure 8.2. The internal capacitance C_{IND} is continuously charged and discharged through periodical switching action with the internal clock frequency f_{CLK} for input signal digitization. In the charging phase, the external input source must provide enough transient charge for the internal capacitance. To prevent transient voltage drop of C_{IND} , an external capacitor (C_{FLT} in Figure 8.1, also acting as filter capacitance) of more than 330 pF should be placed as close as possible to the device as charge buffering, which ensures sensing accuracy.

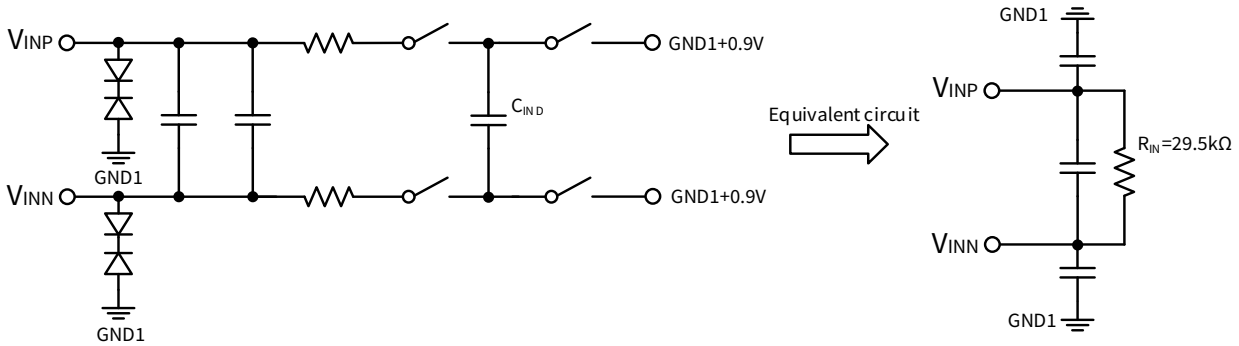


Figure 8.2 Equivalent Circuit of Analog Input

According to the equivalent circuit, the input resistance R_{IN} can be calculated as

$$R_{IND} = 1 / (f_{CLK} * C_{IND})$$

There are two restrictions on the analog input signals (V_{INP} and V_{INN}).

- If the input voltage exceeds the range $GND1 - 6\text{ V}$ to $VDD1 + 0.5\text{ V}$, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Analog Output

For linear input range, the analog output of NSI1200C has a fixed gain 8.0. If a full-scale input signal is applied to the NSI1200C ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically, 2.45 V for positive clipping and -2.45 V for negative clipping). The typical negative clipping output of NSI1200C is shown in Figure 8.3.

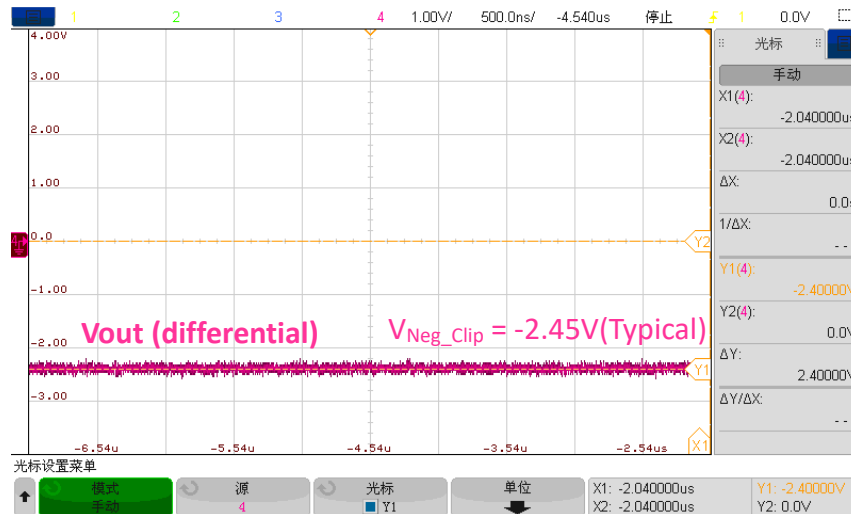


Figure 8.3 Typical negative clipping output

In addition, NSI1200C integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated in following conditions:

- When the undervoltage of $VDD1$ is detected ($VDD1 < VDD1_{UV}$).
- When the overvoltage of common-mode input voltage is detected ($V_{CM} > V_{CMov}$).

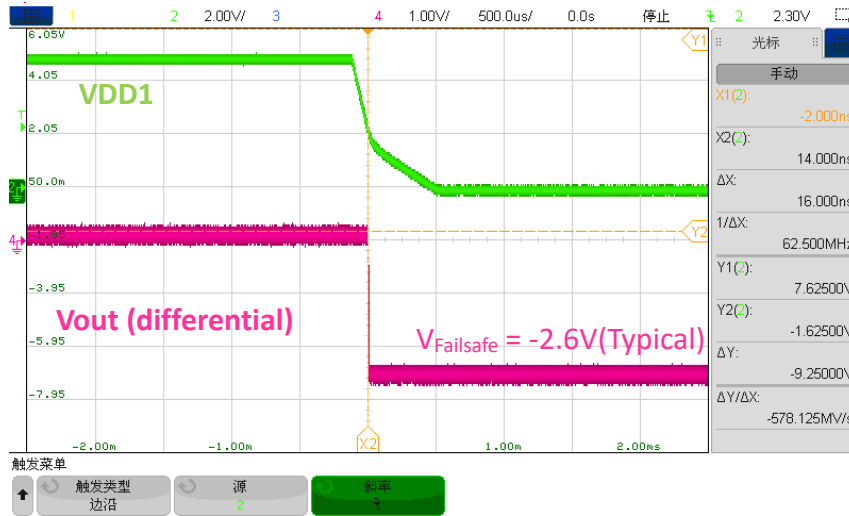


Figure 8.4 Typical Failsafe output when VDD1 undervoltage

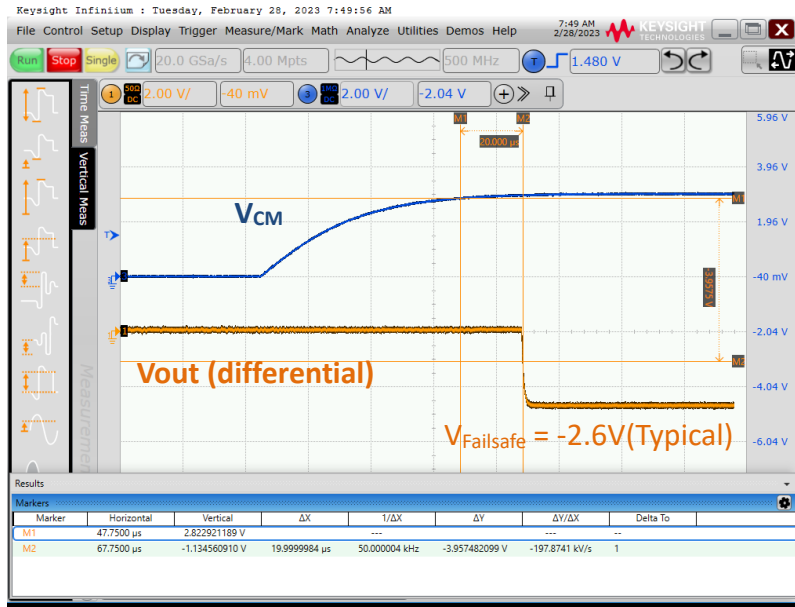


Figure 8.5 Typical Failsafe output when input common mode signal overvoltage

9. Application Note

9.1. Typical Application Circuit

NSI1200C is ideally suited to shunt resistor-based current sensing in high voltage applications such as motor drives. The typical application circuit is shown in Figure 9.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1200C through a RC filter (R_{FLT} and C_{FLT}). The filter capacitance of more than 330 pF placing as close as possible to the device must be added for charge buffering of the input switched-capacitor circuit (further details in 8.2 Analog Input) and better performance in high-noise applications.

The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add >1 kΩ resistor on the OUPN and OUPP pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

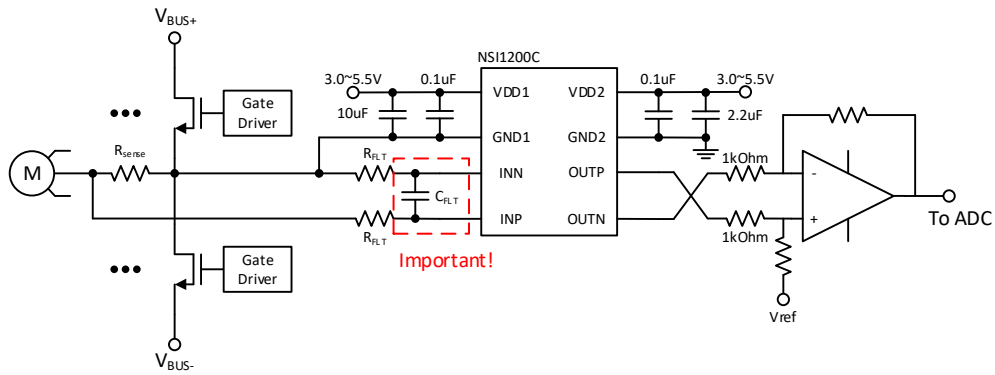


Figure 9.1 Typical application circuit in phase current sensing

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- Place the input filter capacitors as close as possible to the INP and INN pins for best performance.
- NSI1200C requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10 μF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1200C. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1200C. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

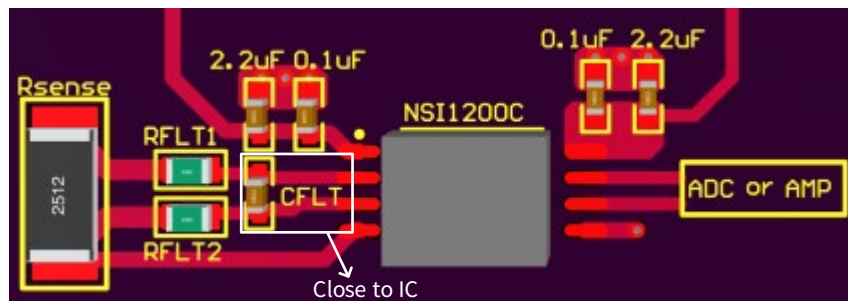
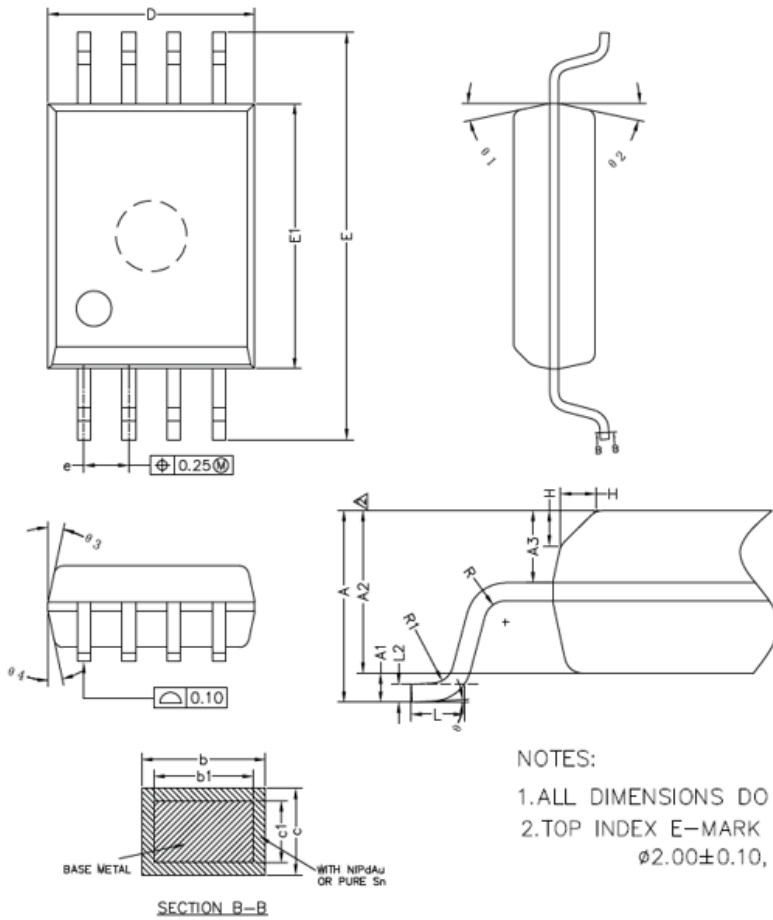


Figure 9.2 Typical application circuit in phase current sensing

10. Package Information



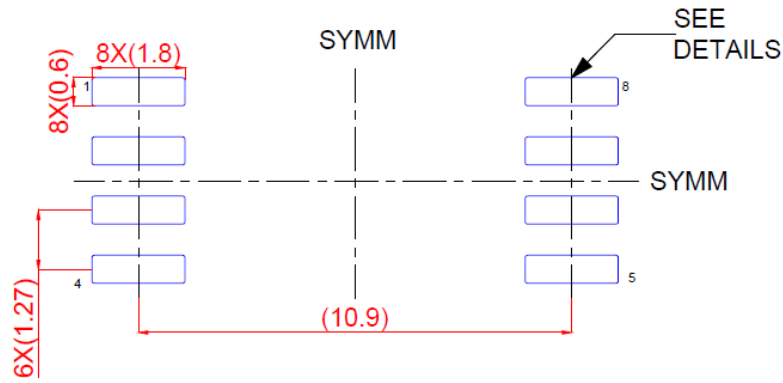
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	2.85
A1	0.31	0.41	0.51
A2	2.20	2.30	2.40
A3	0.97	1.02	1.07
b PURE Sn	0.33	—	0.47
NiPdAu	0.33	—	0.44
b1	0.33	0.38	0.43
c PURE Sn	0.22	—	0.32
NiPdAu	0.22	—	0.29
c1	0.22	0.25	0.28
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.17	1.27	1.37
H	0.40	0.50	0.60
L	0.55	0.75	0.90
L1	2.00REF		
L2	0.25BSC		
R	0.07	—	—
R1	0.07	—	—
θ	0°	—	8°
θ 1	10°	12°	14°
θ 2	10°	12°	14°
θ 3	10°	12°	14°
θ 4	10°	12°	14°

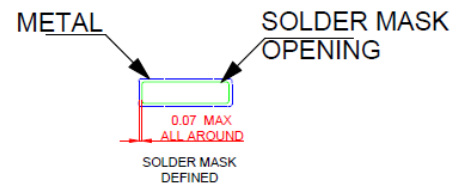
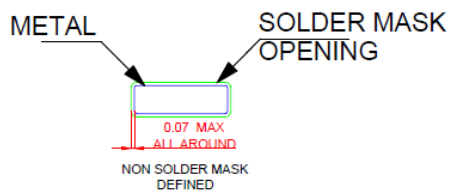
NOTES:

1. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. TOP INDEX E-MARK $\varnothing 1.00 \pm 0.10$, DEPTH $0.10^{+0.15}_{-0.08}$, BOTTOM E-MARK $\varnothing 2.00 \pm 0.10$, DEPTH $0.15^{+0.15}_{-0.13}$.

Figure 10.1 SOW8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE



SOLDER MASK DETAILS

Figure 10.2 SOW8 Package Board Layout Example

11. Ordering Information

Part No.	Isolation Rating (kV)	Linear Input Range (mV)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SP Q
NSI1200C-Q1SWVR	5	-250 ~ 250	Level-3	-40 to 125°C	YES	SOP8 (300mil)	SOW8	1000

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1200C	Click here	Click here	Click here	Click here

13. Tape and Reel Information

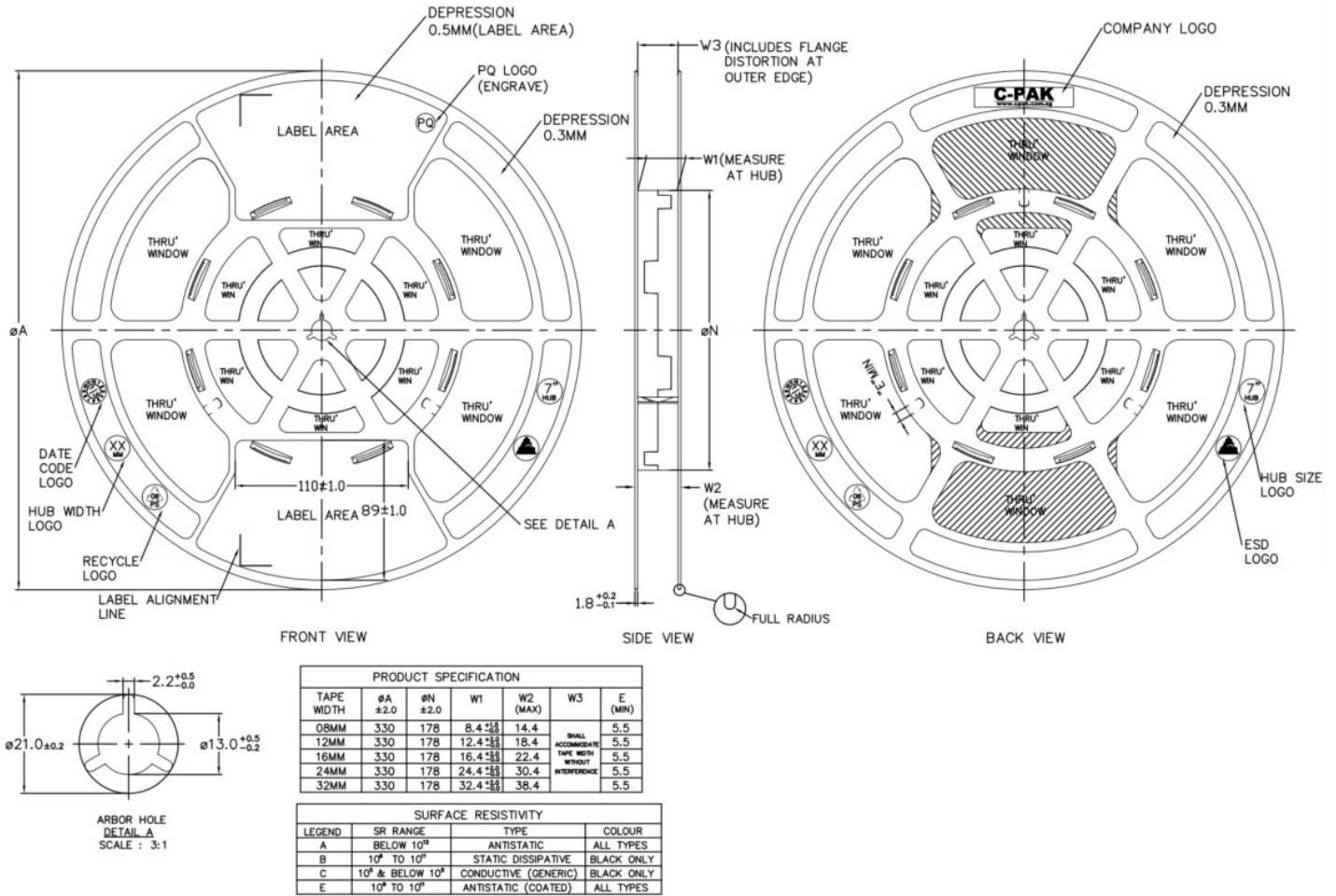


Figure 13.1 Reel Information

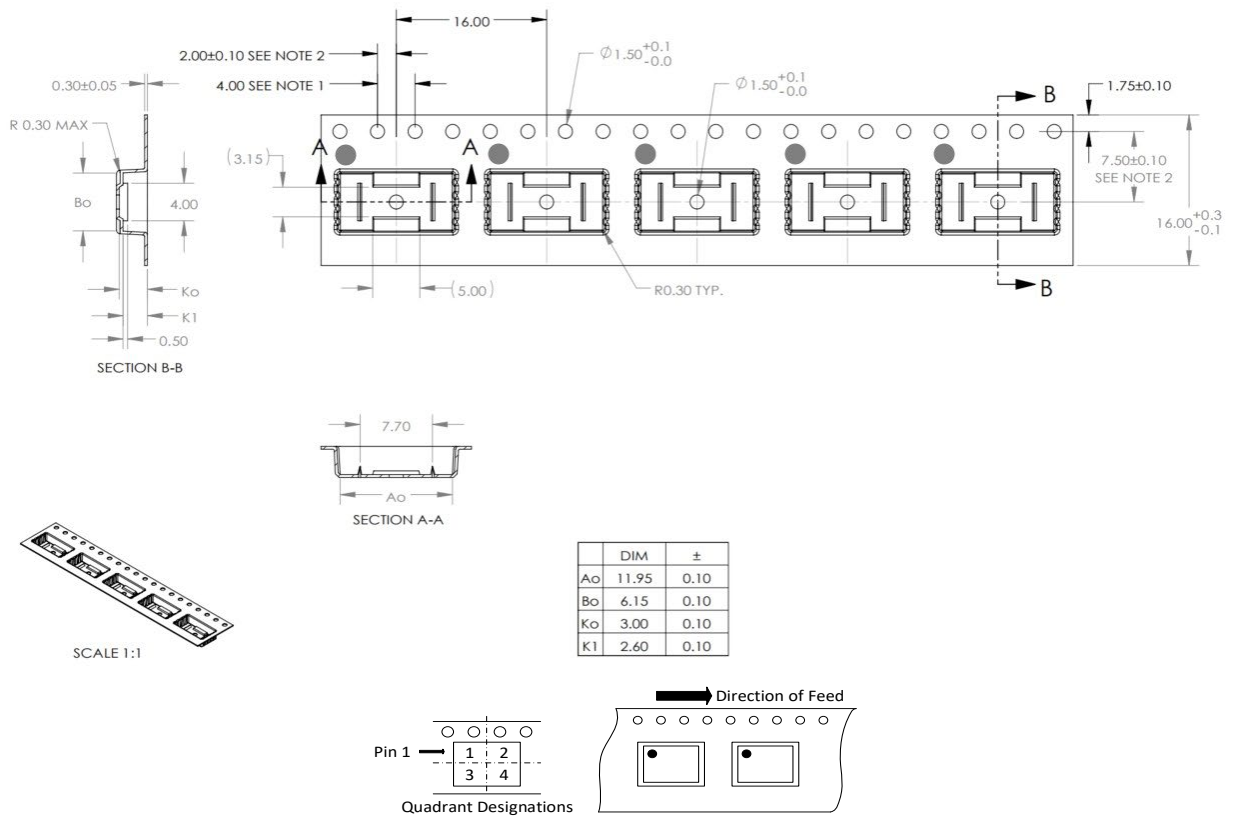


Figure 13.2 Tape Information of SOP8(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial release	2025/6/18

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