

### Product Overview

NSI1200-Q1 is a high-performance isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of  $\pm 250\text{mV}$  ( $\pm 320\text{mV}$  full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The device has a fixed gain of 8 and provides a differential analog output.

The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe functions including input common-mode overvoltage detection and missing VDD1 detection simplify system-level design and diagnostics.

### Key Features

- Up to  $5000V_{\text{rms}}$  Insulation voltage
- $\pm 250\text{mV}$  linear Input Voltage Range
- Fixed Gain: 8
- Low Offset Error and Drift:  
 $\pm 0.5\text{mV}$  (Max),  $-5\sim 5\mu\text{V}/^\circ\text{C}$  (Max)
- Low Gain Error and Drift:  
 $\pm 0.35\%$  (Max),  $\pm 50\text{ppm}/^\circ\text{C}$  (Max)
- Low Nonlinearity and Drift:  
 $\pm 0.05\%$  (Max),  $\pm 1\text{ppm}/^\circ\text{C}$  (Typ)
- SNR: 86dB (Typ, BW=10kHz), 72dB (Typ, BW=100kHz)
- Bandwidth: 100kHz (Typ)
- High CMTI:  $150\text{kV}/\mu\text{s}$  (Typ)
- System-Level Diagnostic Features:

- VDD1 monitoring
- Input common-mode overvoltage detection

- Operation Temperature:  $-40^\circ\text{C} \sim 125^\circ\text{C}$
- AEC-Q100 qualified for automotive applications
- RoHS-Compliant Packages:  
SOP8(300mil)

### Safety Regulatory Approvals

- UL recognition: up to  $5000V_{\text{rms}}$  for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-11:2017-01

### Applications

- Shunt current monitoring
- AC motor controls
- Power and solar inverters
- Uninterruptible Power Suppliers
- Automotive onboard chargers

### Device Information

Part Number	Package	Body Size
NSI1200-Q1SWVR	SOP8(300mil)	5.85mm × 7.50mm

### Functional Block Diagrams

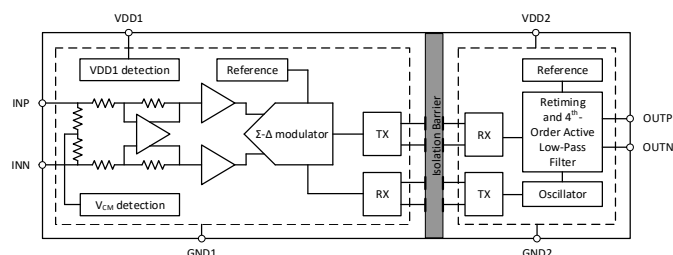


Figure 1. NSI1200-Q1 Block Diagram

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## 1. Pin Configuration and Functions

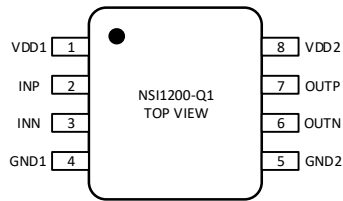


Figure 1.1 NSI1200-Q1 Package

Table 1.1 NSI1200-Q1 Pin Configuration and Description

<b>NSI1200-Q1 PIN NO.</b>	<b>SYMBOL</b>	<b>FUNCTION</b>
1	VDD1	Power supply for isolator side 1(3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1200-Q1)
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for isolator side 2 (3.0V to 5.5V)

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
Output Voltage	OUTP, OUTN	GND2-0.5		VDD2+0.5	V
Output current per Output Pin	I <sub>o</sub>	-10		10	mA
Operating Temperature	T <sub>OPR</sub>	-40		125	°C
Junction Temperature	T <sub>J</sub>	-40		150	°C
Storage Temperature	T <sub>STG</sub>	-55		150	°C
Electrostatic discharge	HBM <sup>(1)</sup>	±2000			V
	CDM <sup>(2)</sup>	±1000			V

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

## 3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Side1 Power Supply	VDD1	3.0	5.0	5.5	V
Side2 Power Supply	VDD2	3.0	3.3	5.5	V
Differential input voltage before clipping output	V <sub>Clipping</sub>		±320		mV
Linear differential input full scale voltage	V <sub>F<sub>SR</sub></sub>	-250		250	mV
Operating common-mode input voltage	V <sub>CM</sub>	-0.16		0.8	V
Operating Ambient Temperature	T <sub>A</sub>	-40		125	°C

## 4. Thermal Information

Parameters	Symbol	DUB8	SOP8(300mil)	Unit
Junction-to-ambient thermal resistance	R <sub>θJA</sub>	76	86	°C/W
Junction-to-case (top) thermal resistance	R <sub>θJC(top)</sub>	58	28	°C/W
Junction-to-board thermal resistance	R <sub>θJB</sub>	40	42	°C/W
Junction-to-top characterization parameter	Ψ <sub>JT</sub>	27	4	°C/W
Junction-to-board characterization parameter	Ψ <sub>JB</sub>	38	42	°C/W

## 5. Specifications

### 5.1. Electrical Characteristics

(VDD1 = 3.0V ~ 5.5V, VDD2 = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = GND1 = 0V, T<sub>A</sub> = -40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T<sub>A</sub> = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
<b>Power Supply</b>						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1		11.4	15	mA	
Side2 Supply Current	IDD2		6.3	8	mA	
VDD1 undervoltage detection threshold voltage	VDD1 <sub>UV</sub>	1.8	2.3	2.7	V	VDD1 falling
<b>Analog Input</b>						
Common-mode overvoltage detection level	V <sub>CMov</sub>	0.9			V	Detection level has a typical hysteresis of 96 mV
Input offset voltage	V <sub>OS</sub>	-0.5	±0.05	0.5	mV	INP = INN = GND1
Input offset drift	TCV <sub>OS</sub>	-5	1	5	µV/°C	
Common-mode rejection ratio	CMRR <sub>dc</sub>		-85		dB	INP = INN, f <sub>IN</sub> = 0 Hz, V <sub>CM min</sub> ≤ VIN ≤ V <sub>CM max</sub>
	CMRR <sub>ac</sub>		-106		dB	INP = INN, f <sub>IN</sub> = 10 kHz, V <sub>CM min</sub> ≤ VIN ≤ V <sub>CM max</sub>
Single-ended input resistance	R <sub>IN</sub>		19		kΩ	INN = GND1
Differential input resistance	R <sub>IND</sub>		22		kΩ	
Input bias current	I <sub>IB</sub>	-24	-18	-12	µA	INP = INN = GND1, I <sub>IB</sub> = (I <sub>IBP</sub> + I <sub>IBN</sub> ) / 2
Input bias current drift	TCI <sub>IB</sub>		±1.8		nA/°C	
<b>Analog Output</b>						
Nominal Gain			8		V/V	
Gain error	E <sub>G</sub>	-0.35%	±0.05%	0.35%		
Gain error thermal drift	TCE <sub>G</sub>	-50	±15	50	ppm/°C	
Nonlinearity		-0.05%	±0.01%	0.05%		
Nonlinearity drift			±1		ppm/°C	
Total harmonic distortion	THD		-78		dB	V <sub>IN</sub> = 0.5V, f <sub>IN</sub> = 10kHz, BW = 100kHz
Output noise			180		µV <sub>RMS</sub>	INP = INN = GND1, BW = 100kHz
Signal to noise ratio	SNR		86		dB	V <sub>IN</sub> = 0.5V, f <sub>IN</sub> = 1kHz, BW = 10kHz

Parameters	Symbol	Min	Typ	Max	Unit	Comments
			72		dB	$V_{IN} = 0.5V, f_{IN} = 10kHz, BW = 100kHz$
Common-mode output voltage	$V_{CMout}$	1.36	1.4	1.49	V	
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.53	-2.44	V	$V_{CM} > V_{CMov}$ , or VDD1 missing
Output bandwidth	BW	60	100		kHz	
Power supply rejection ratio <sup>(1)</sup>	$PSRR_{dc}$		-104		dB	PSRR vs VDD1, at DC
	$PSRR_{ac}$		-102		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	$PSRR_{dc}$		-90		dB	PSRR vs VDD2, at DC
	$PSRR_{ac}$		-85		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance	$R_{OUT}$		< 0.2		$\Omega$	
Common-mode transient immunity	CMTI	100	150		kV/ $\mu$ s	Common-mode transient immunity
<b>Timing</b>						
Rising time of OUTP, OUTN	$t_r$		3.6		$\mu$ s	
Falling time of OUTP, OUTN	$t_f$		3.6		$\mu$ s	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	$t_{PD}$		3.5	4.2	$\mu$ s	
Analog setting time	$t_{AS}$		0.5		ms	VDD1 step to 3.0 V with VDD2 $\geq$ 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) Input referred.

### 5.2. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5V, VDD2 = 3.3V, Vin = -250mV to 250mV.

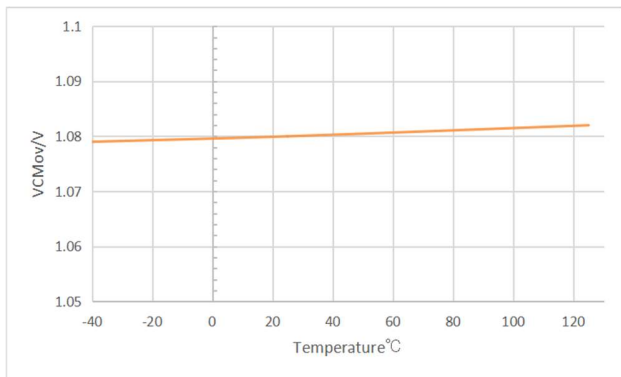


Figure 5.1 Common-Mode Overvoltage Detection Level vs Temperature

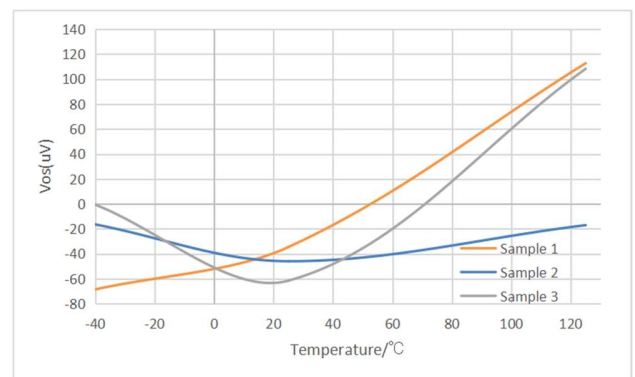


Figure 5.2 Input Offset Voltage vs Temperature

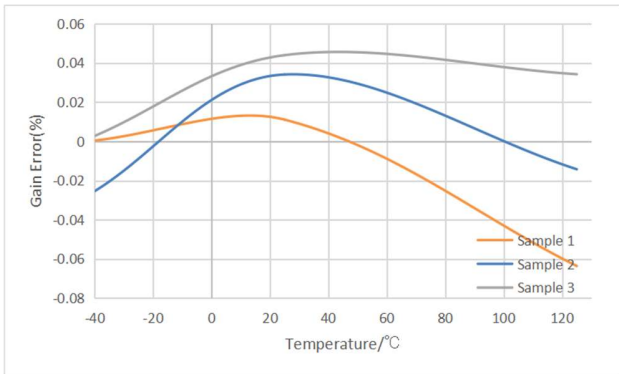


Figure 5.3 Gain Error vs Temperature

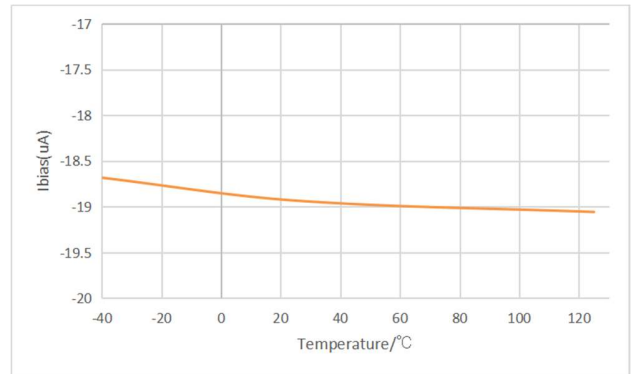


Figure 5.7 Input Bias Current vs Temperature

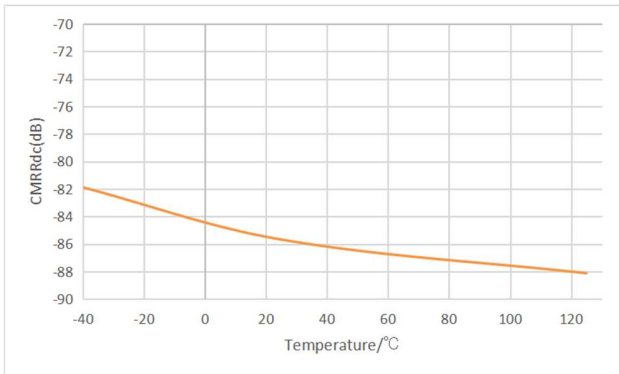


Figure 5.4 Common-Mode Rejection Ratio vs Temperature

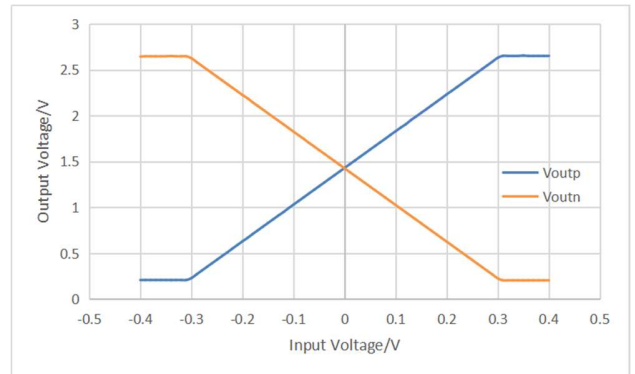


Figure 5.8 Output Voltage vs Input Voltage

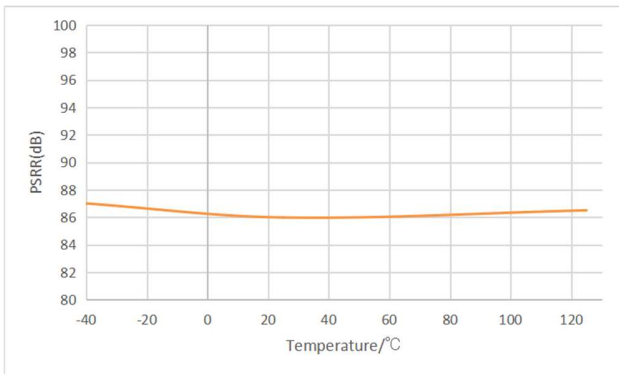


Figure 5.5 SNR vs Temperature

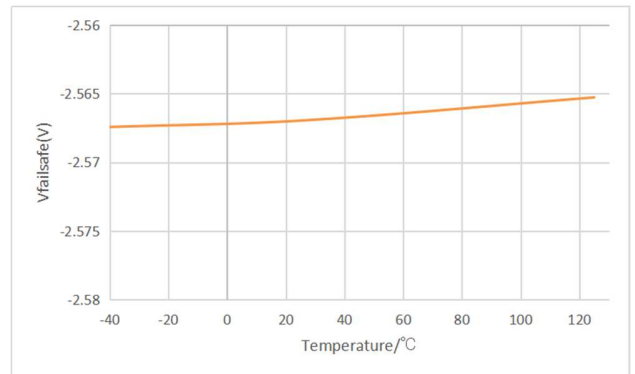


Figure 5.9 Fail-Safe Output Voltage vs Temperature

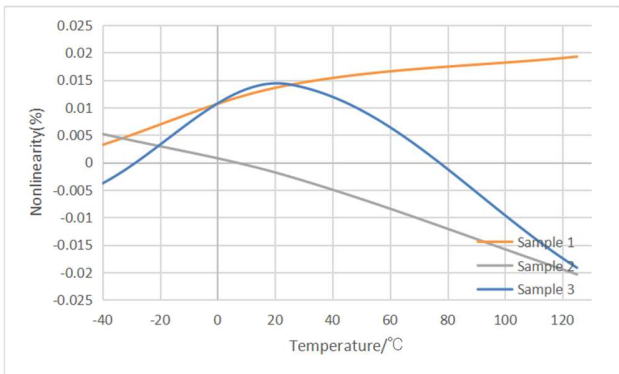


Figure 5.6 Nonlinearity vs Temperature

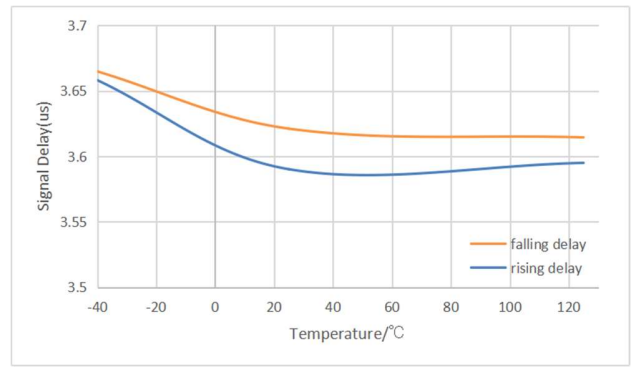


Figure 5.10 Vin to Vout Delay vs Temperature

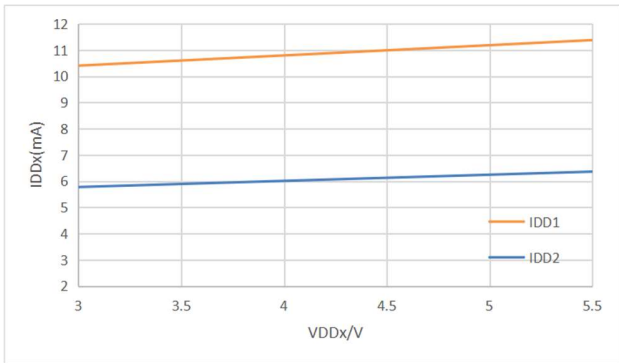


Figure 5.11 Supply Current vs Supply Voltage

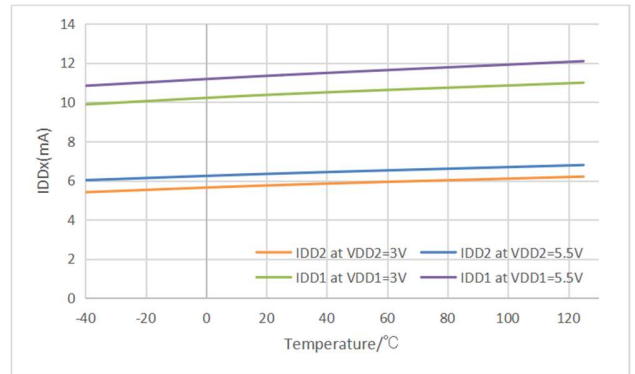


Figure 5.12 Supply Current vs Temperature

### 5.3. Parameter Measurement Information

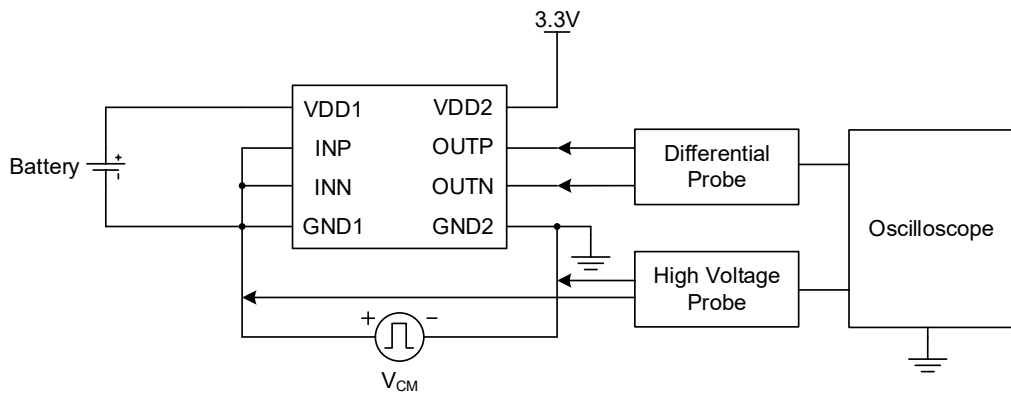


Figure 5.13 Common-Mode Transient Immunity Test Circuit

## 6. High Voltage Feature Description

### 6.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	28	µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

### 6.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
<b>DIN VDE 0110</b>				
For Rated Mains Voltage ≤ 150Vrms			I to IV	

Description	Test Condition	Symbol	Value	Unit
For Rated Mains Voltage ≤ 300Vrms			I to IV	
For Rated Mains Voltage ≤ 400Vrms			I to IV	
Climatic Classification			10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage		$V_{IORM}$	2121	$V_{PEAK}$
Maximum working isolation voltage	AC Voltage	$V_{IOWM}$	1500	$V_{RMS}$
	DC Voltage		2121	$V_{PEAK}$
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	3977	$V_{PEAK}$
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	3394	$V_{PEAK}$
Input to Output Test Voltage, Method A. After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	2545	$V_{PEAK}$
Maximum transient isolation voltage	$t = 60$ sec	$V_{IOTM}$	7000	$V_{PEAK}$
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = V_{IOSM} / 1.6$	$V_{IOSM}$	6250	$V_{PEAK}$
Isolation resistance	$V_{IO} = 500V$ , $T_{amb} = T_s$	$R_{IO}$	$>10^9$	$\Omega$
	$V_{IO} = 500V$ , $100^\circ C \leq T_{amb} \leq 125^\circ C$	$R_{IO}$	$>10^{11}$	$\Omega$
Isolation capacitance	$f = 1MHz$	$C_{IO}$	0.8	pF
Input capacitance		$C_i$	2	pF
Safety input, output, or total power		$P_s$	1453	mW
Safety input, output, or supply current	$\theta_{JA} = 86^\circ C/W$ , $V_i = 5.5V$ , $T_J = 150^\circ C$ , $T_A = 25^\circ C$	$I_s$	260	mA
Maximum safety temperature		$T_s$	150	$^\circ C$
<b>UL1577</b>				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$ , $t = 60$ s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1$ s (100% production test)	$V_{ISO}$	5000	$V_{RMS}$

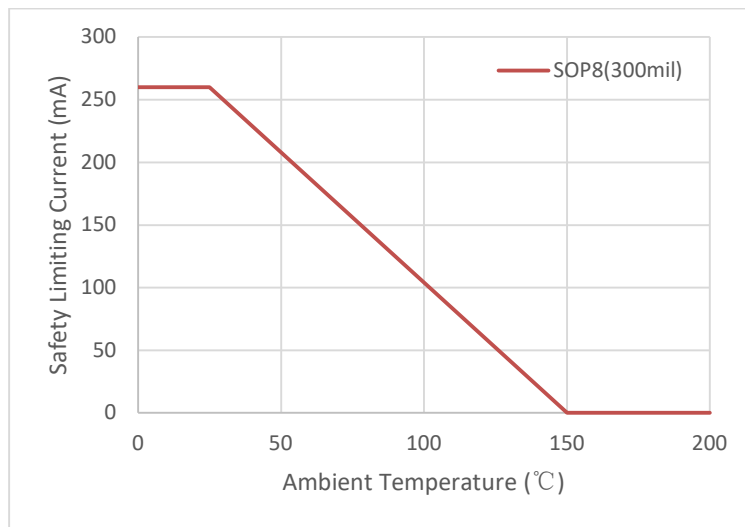


Figure 6.1 NSI1200-Q1 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

### 6.3. Regulatory Information

The NSI1200-Q1 are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V <sub>rms</sub> Isolation voltage	Single Protection, 5000V <sub>rms</sub> Isolation voltage	Reinforce Insulation 1414V <sub>peak</sub> , V <sub>IOSM</sub> =6250V <sub>peak</sub>	Reinforced insulation
Certificate No.E500602	Certificate No.E500602	Certificate No.40052820	CQC20001264938

## 7. Function Description

### 7.1. Overview

The NSI1200-Q1 is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, sigma-delta ( $\Sigma\Delta$ ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier that separates the side1 and side2 voltage domains. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the side2 and presented as a differential output of the device.

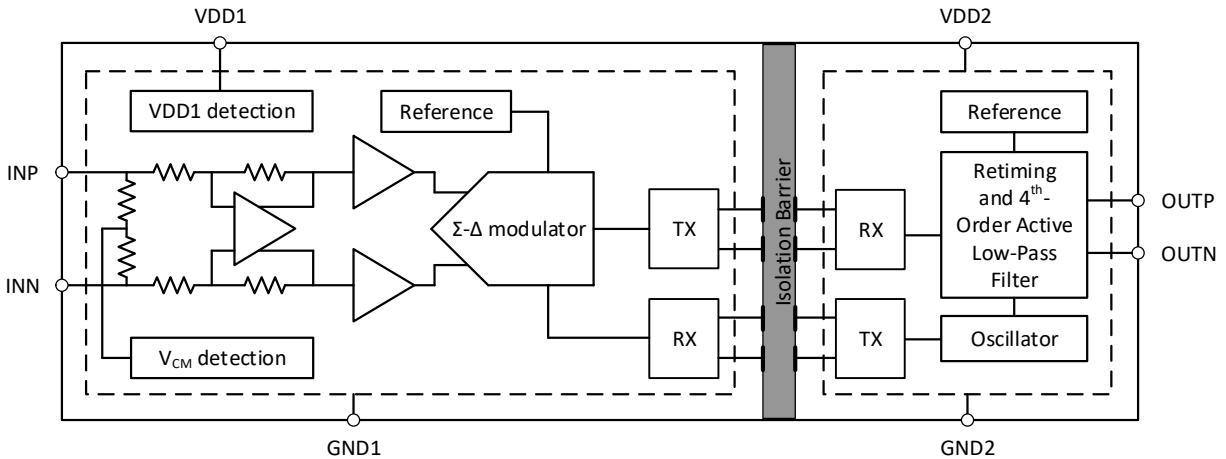


Figure 7.1 Function Block Diagram

### 7.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

### 7.3. Analog Output

For linear input range, the analog output of NSI1200-Q1 has a fixed gain of 8. If a full-scale input signal is applied to the NSI1200-Q1 ( $V_{IN} \geq V_{Clipping}$ ), the analog output will be clipped (typically, 2.4V for positive clipping and -2.4V for negative clipping).

In addition, NSI1200-Q1 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated in following conditions:

- When the undervoltage of VDD1 is detected ( $VDD1 < VDD1_{UV}$ ).
- When the overvoltage of common-mode input voltage is detected ( $V_{CM} > V_{CMOV}$ ).

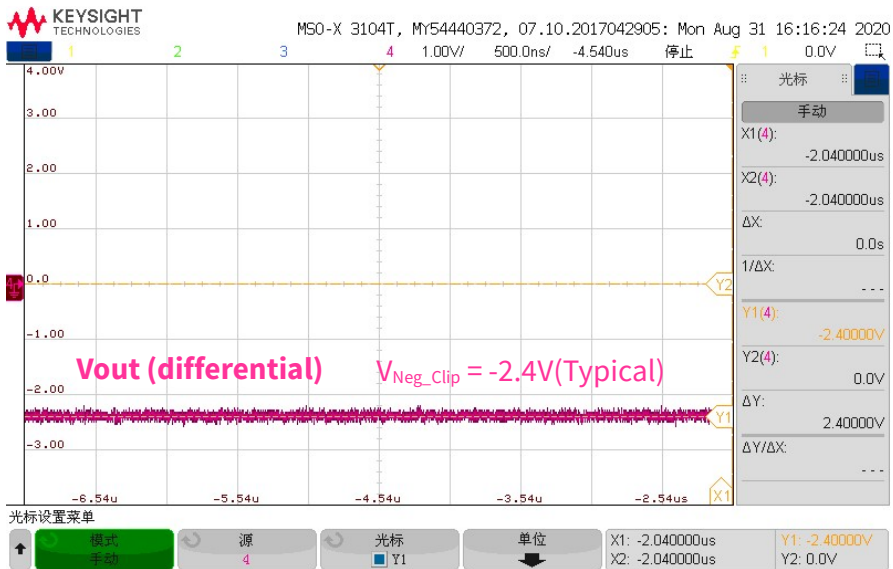


Figure 7.2 Typical negative clipping output

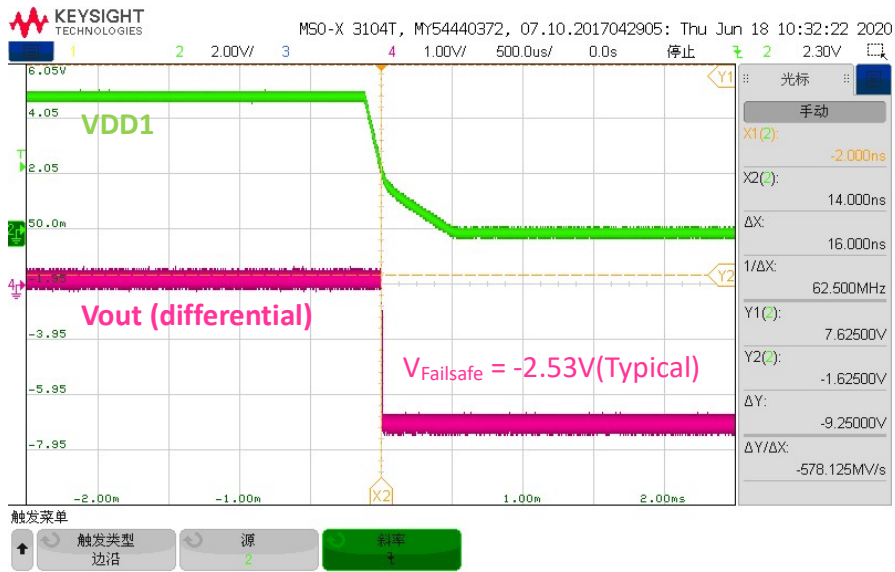


Figure 7.3 Typical Failsafe output when VDD1 undervoltage

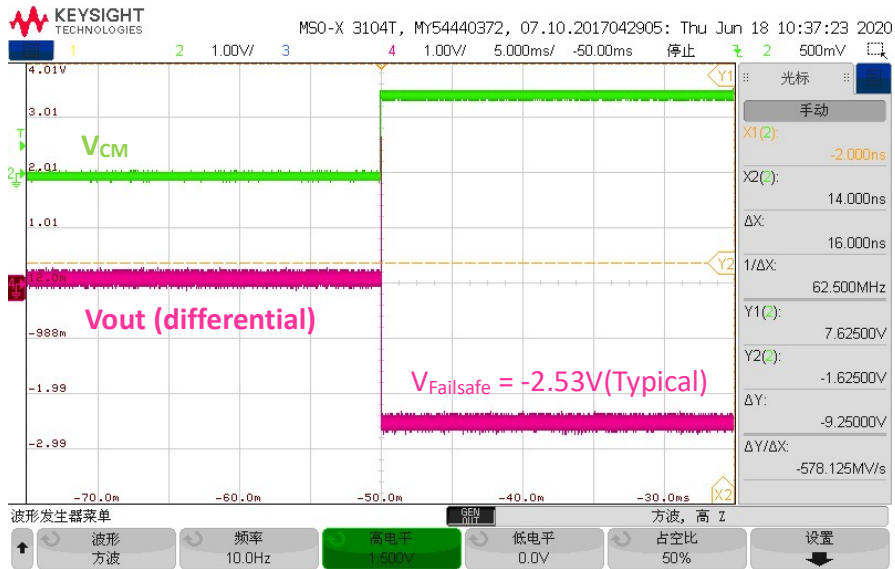


Figure 7.4 Typical Failsafe output when input common mode signal overvoltage

## 8. Application Note

### 8.1. Typical Application Circuit

NSI1200-Q1 is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 8.1.

The voltage across the shunt resistor  $R_{sense}$  is applied to the differential input of NSI1200-Q1 through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add  $>1k\Omega$  resistor on the OUPN and OUPM pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

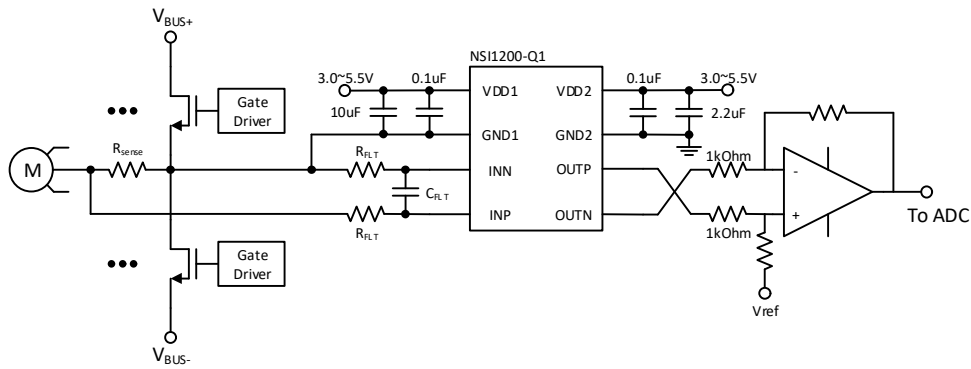


Figure 8.1 Typical application circuit in phase current sensing

### 8.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

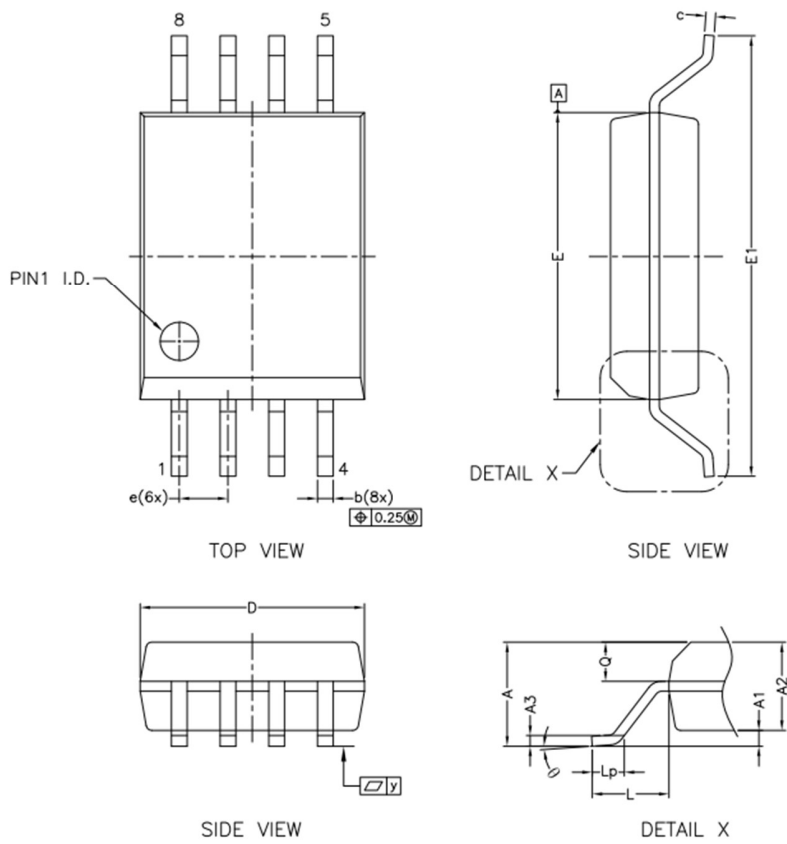
- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range:  $V_{SHUNT} \leq FSR$ .
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output:  $V_{SHUNT} \leq V_{Clipping}$ .

### 8.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1200-Q1 requires a 0.1µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10µF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1200-Q1. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1200-Q1. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

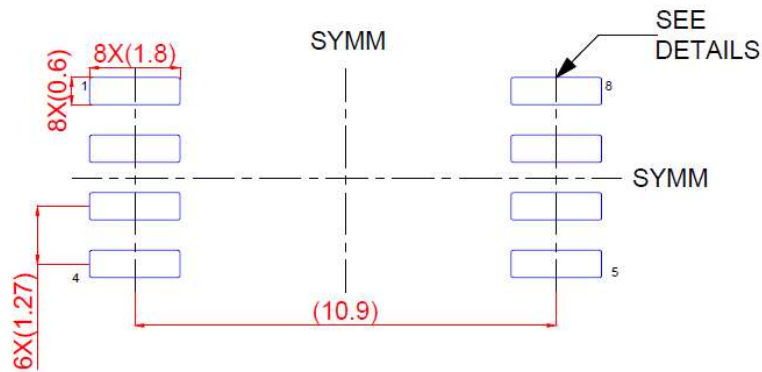
### 9. Package Information



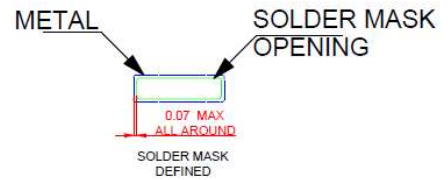
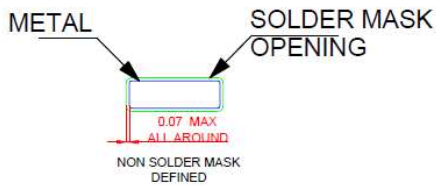
\* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
$\theta$	0°	--	8°

Figure 9.1 SOW8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)  
9.1 mm NOMINAL  
CLEARANCE/CREEPAGE



SOLDER MASK DETAILS

Figure 9.2 SOW8 Package Board Layout Example

### 10. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SPQ
NSI1200-Q1SWVR	5	-250 ~ 250	Level-3	-40 to 125 °C	YES	SOP8 (300mil)	SOW8	1000

### 11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1200-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12. Tape and Reel Information

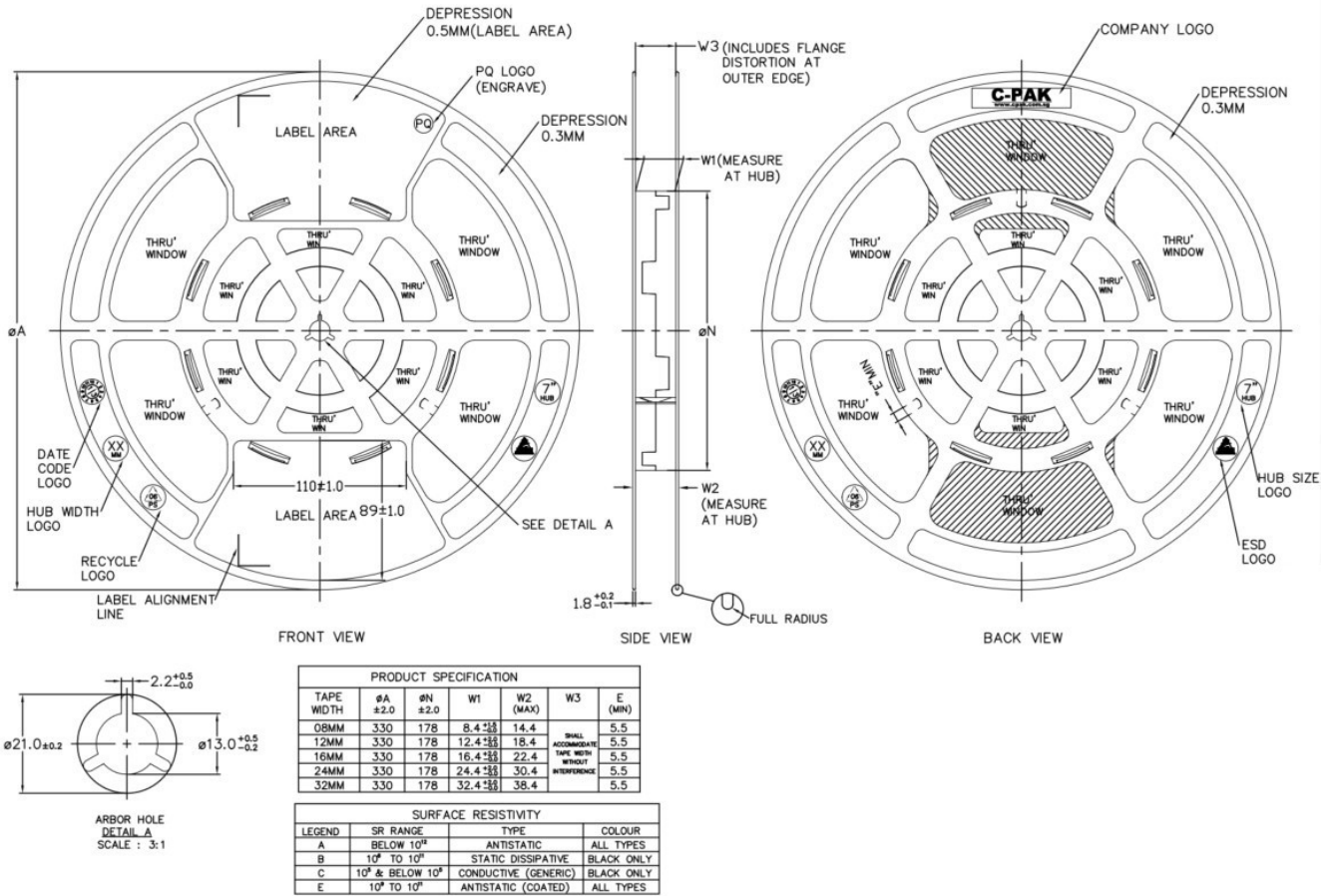


Figure 12.1 Tape Information

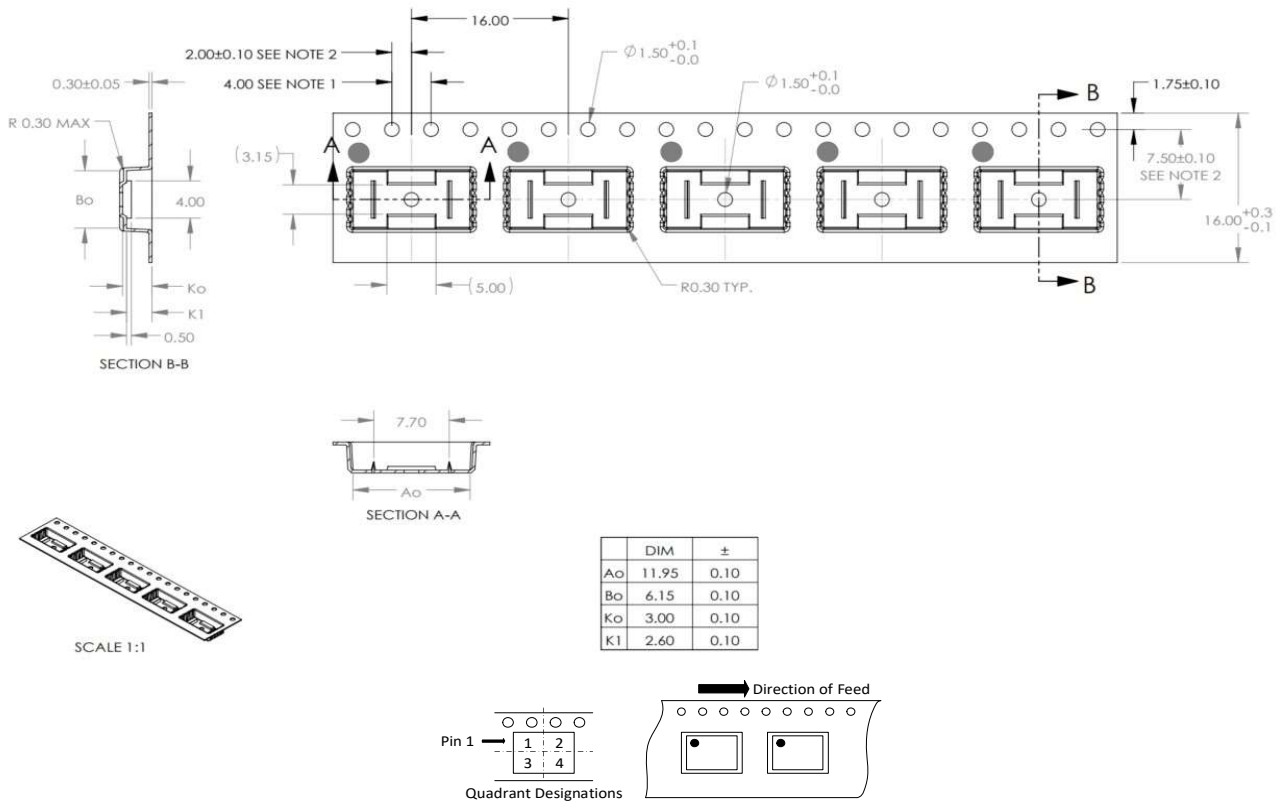


Figure 12.2 Reel Information of SOP8(300mil)

### 13. Revision History

Revision	Description	Date
1.0	Initial Release	2021/1/11
1.1	Add $V_{ISO}$ specification in 6.2 Insulation Characteristics and AEC-Q100 qualification	2021/4/12
1.2	Update Electrical Characteristics in 5.1	2022/10/1
1.3	Update the standard on which VIOSM test method is based in 6.2, description form of $V_{pd}$ (m) in 6.2, Isolation resistance in 6.2 and CQC certificate description in 6.3. Update typeface to Source Sans Pro. Add SOW8 Package Board Layout Example in part 9.	2023/4/13

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