

Product Overview

NSI1200 is a high-performance isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of $\pm 250\text{mV}$ ($\pm 320\text{mV}$ full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The device has a fixed gain of 8 and provides a differential analog output.

The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe functions including input common-mode overvoltage detection and missing VDD1 detection simplify system-level design and diagnostics.

Key Features

- Up to $5000V_{\text{rms}}$ Insulation voltage
- $\pm 250\text{mV}$ linear Input Voltage Range
- Fixed Gain: 8
- Low Offset Error and Drift:
 $\pm 0.5\text{mV}$ (Max), $-4 \sim 4\mu\text{V}/^\circ\text{C}$ (Max)
- Low Gain Error and Drift:
 $\pm 0.3\%$ (Max), $\pm 50\text{ppm}/^\circ\text{C}$ (Max)
- Low Nonlinearity and Drift:
 $\pm 0.03\%$ (Max), $\pm 1\text{ppm}/^\circ\text{C}$ (Typ)
- SNR: 86dB (Typ, BW=10kHz), 72dB (Typ, BW=100kHz)
- Bandwidth: 100kHz (Typ)
- High CMTI: $150\text{kV}/\mu\text{s}$ (Typ)
- System-Level Diagnostic Features:
 - VDD1 monitoring

- Input common-mode overvoltage detection

- Operation Temperature: $-40^\circ\text{C} \sim 125^\circ\text{C}$
- RoHS-Compliant Packages:
 SOP8(300mil)
 DUB8

Safety Regulatory Approvals

- UL recognition: up to $5000V_{\text{rms}}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-11:2017-01

Applications

- Shunt current monitoring
- AC motor controls
- Power and solar inverters
- Uninterruptible Power Suppliers
- Automotive onboard chargers

Device Information

Part Number	Package	Body Size
NSI1200-DSWVR	SOP8(300mil)	5.85mm × 7.50mm
NSI1200-DDBR	DUB8	9.27mm × 6.20mm

Functional Block Diagrams

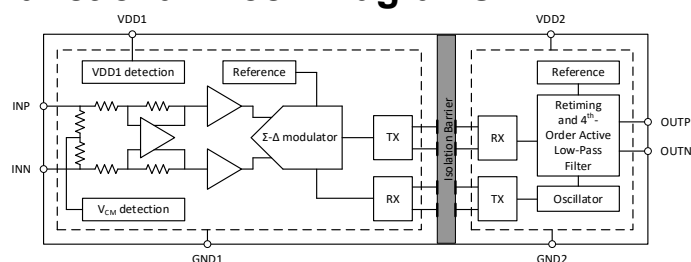


Figure 1. NSI1200 Block Diagram

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1. Pin Configuration and Functions

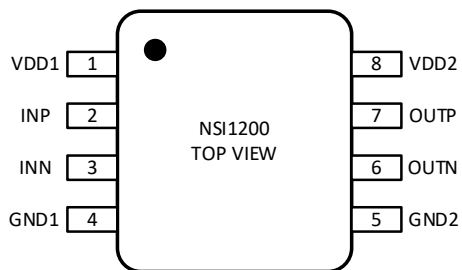


Figure 1.1 NSI1200 Package

Table 1.1 NSI1200 Pin Configuration and Description

NSI1200 PIN NO.	SYMBOL	FUNCTION
1	VDD1	Power supply for isolator side 1(3.0V to 5.5V)
2	INP	Positive analog input ($\pm 250\text{mV}$ recommended for NSI1200)
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for isolator side 2 (3.0V to 5.5V)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
Output Voltage	OUTP, OUTN	GND2-0.5		VDD2+0.5	V
Output current per Output Pin	I _o	-10		10	mA
Junction Temperature	T _J	-40		150	°C
Storage Temperature	T _{STG}	-55		150	°C
Electrostatic discharge	HBM ⁽¹⁾	±2000			V
	CDM ⁽²⁾	±1000			V

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Side1 Power Supply	VDD1	3.0	5.0	5.5	V
Side2 Power Supply	VDD2	3.0	3.3	5.5	V
Differential input voltage before clipping output	V _{Clipping}		±320		mV
Linear differential input full scale voltage	V _{FSR}	-250		250	mV
Operating common-mode input voltage	V _{CM}	-0.16		0.8	V
Operating Ambient Temperature	T _A	-40		125	°C

4. Thermal Information

Parameters	Symbol	DUB8	SOP8(300mil)	Unit
Junction-to-ambient thermal resistance	R _{θJA}	76	86	°C/W
Junction-to-case (top) thermal resistance	R _{θJC(top)}	58	28	°C/W
Junction-to-board thermal resistance	R _{θJB}	40	42	°C/W
Junction-to-top characterization parameter	Ψ _{JT}	27	4	°C/W
Junction-to-board characterization parameter	Ψ _{JB}	38	42	°C/W

5. Specifications

5.1. Electrical Characteristics

(VDD1 = 3.0V ~ 5.5V, VDD2 = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = GND1 = 0V, T_A = -40°C to 125°C.

Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1		11.4	15	mA	
Side2 Supply Current	IDD2		6.3	8	mA	
VDD1 undervoltage detection threshold voltage	VDD1 _{UV}	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Common-mode overvoltage detection level	V _{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Input offset voltage	V _{OS}	-0.5	±0.01	0.5	mV	T _A =25°C, INP = INN = GND1
Input offset drift	TCV _{OS}	-4	1	4	μV/°C	
Common-mode rejection ratio	CMRR _{dc}		-80		dB	INP = INN, f _{IN} = 0 Hz, V _{CM min} ≤ V _{IN} ≤ V _{CM max}
	CMRR _{ac}		-106		dB	INP = INN, f _{IN} = 10 kHz, V _{CM min} ≤ V _{IN} ≤ V _{CM max}
Single-ended input resistance	R _{IN}		19		kΩ	INN = GND1
Differential input resistance	R _{IND}		22		kΩ	
Input capacitance	C _I		2		pF	
Input bias current	I _{IB}	-20	-18	-15	μA	T _A =25°C, INP = INN = GND1, I _{IB} = (I _{IBP} + I _{IBN}) / 2
Input bias current drift	TCI _{IB}		±1.8		nA/°C	
Analog Output						
Nominal Gain			8		V/V	
Gain error	E _G	-0.3%	±0.05%	0.3%		T _A =25°C
Gain error thermal drift	TCE _G	-50	±15	50	ppm/°C	
Nonlinearity		-0.03%	±0.01%	0.03%		T _A =25°C
Nonlinearity drift			±1		ppm/°C	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Total harmonic distortion	THD		-80		dB	$V_{IN} = 0.5V$, $f_{IN} = 10kHz$, $BW = 100kHz$
Output noise			180		μV_{RMS}	$INP = INN = GND1$, $BW = 100kHz$
Signal to noise ratio	SNR	79	86		dB	$V_{IN} = 0.5V$, $f_{IN} = 1kHz$, $BW = 10kHz$
			72		dB	$V_{IN} = 0.5V$, $f_{IN} = 10kHz$, $BW = 100kHz$
Common-mode output voltage	V_{CMout}	1.36	1.4	1.46	V	
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.53	-2.44	V	$V_{CM} > V_{CMov}$, or $VDD1$ missing
Output bandwidth	BW	60	100		kHz	
Power supply rejection ratio (1)	$PSRR_{dc}$		-104		dB	PSRR vs $VDD1$, at DC
	$PSRR_{ac}$		-102		dB	PSRR vs $VDD1$, 100mV and 10kHz ripple
	$PSRR_{dc}$		-90		dB	PSRR vs $VDD2$, at DC
	$PSRR_{ac}$		-85		dB	PSRR vs $VDD2$, 100mV and 10kHz ripple
Output resistance	R_{OUT}		< 0.2		Ω	
Common-mode transient immunity	CMTI	100	150		kV/ μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t_r		3.6		μs	
Falling time of OUTP, OUTN	t_f		3.6		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		3.5	4	μs	
Analog setting time	t_{AS}		0.5		ms	$VDD1$ step to 3.0 V with $VDD2 \geq 3.0 V$, to OUTP, OUTN valid, 0.1% settling

(1) Input referred.

5.2. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5V, VDD2 = 3.3V, Vin = -250mV to 250mV.

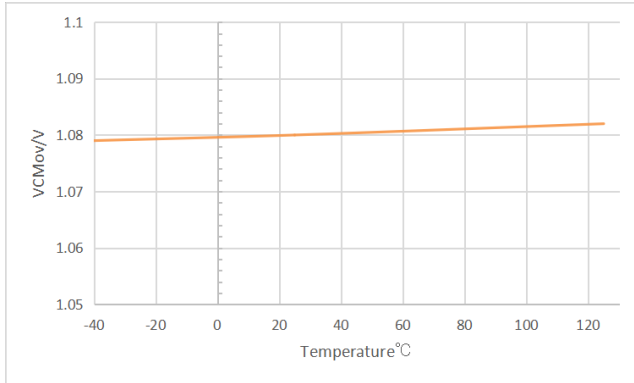


Figure 5.1 Common-Mode Overvoltage Detection Level vs Temperature

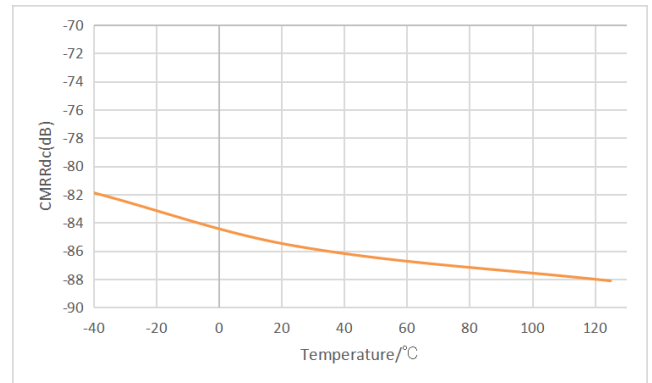


Figure 5.4 Common-Mode Rejection Ratio vs Temperature

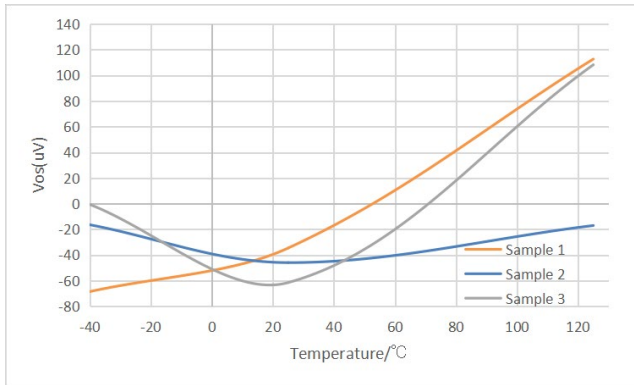


Figure 5.2 Input Offset Voltage vs Temperature (NSI1200)

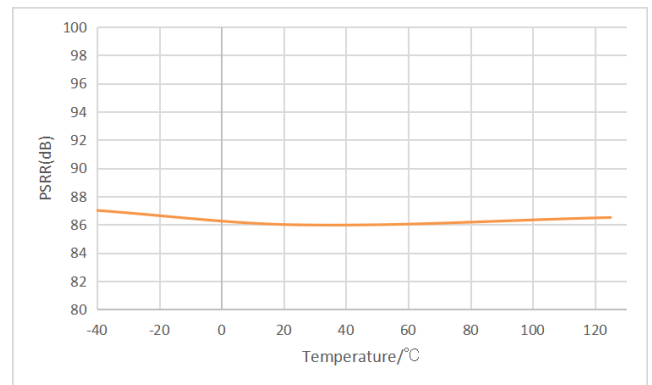


Figure 5.5 SNR vs Temperature

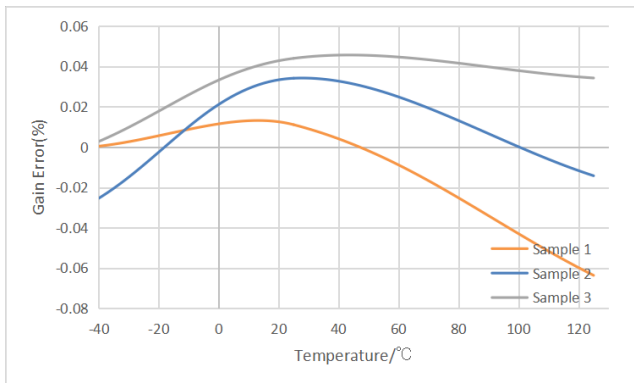


Figure 5.3 Gain Error vs Temperature

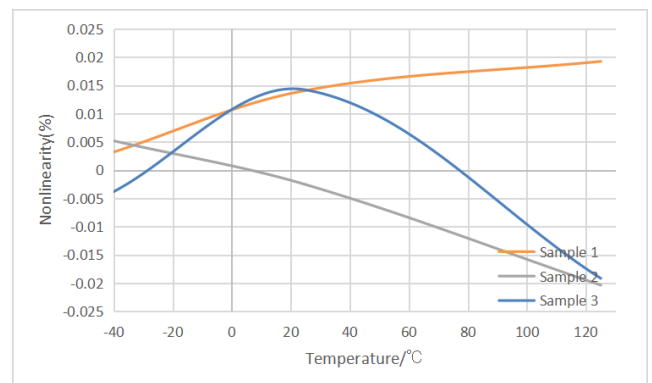


Figure 5.6 Nonlinearity vs Temperature

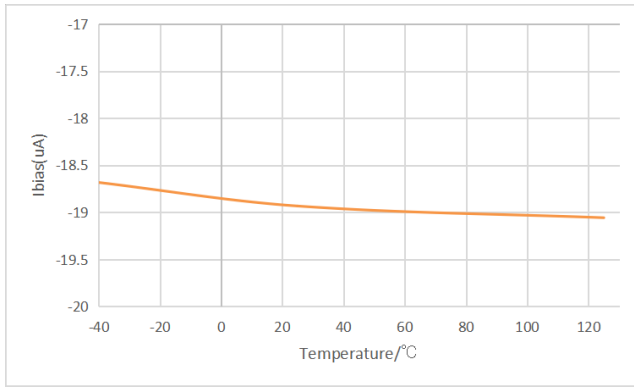


Figure 5.7 Input Bias Current vs Temperature

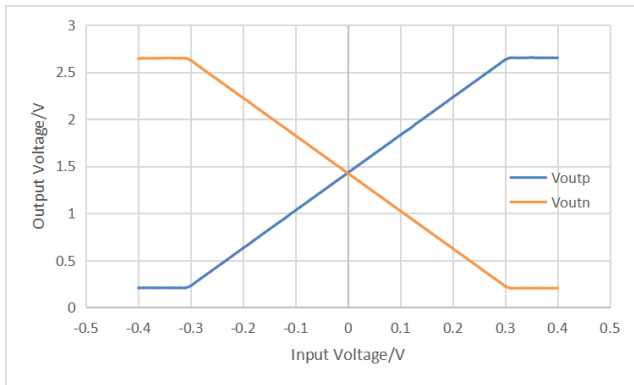


Figure 5.8 Output Voltage vs Input Voltage

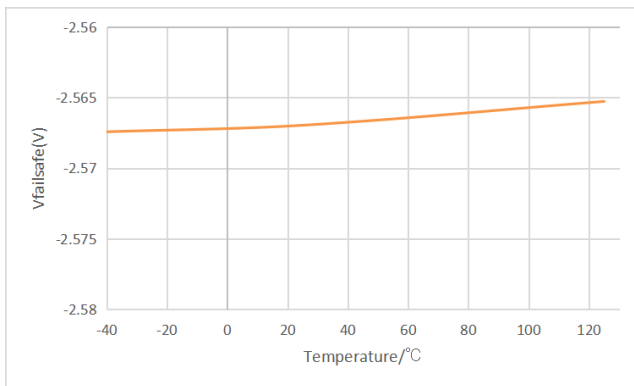


Figure 5.9 Fail-Safe Output Voltage vs Temperature

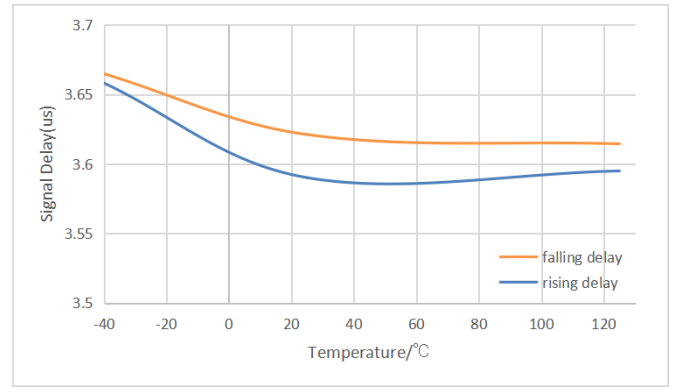


Figure 5.10 Vin to Vout Delay vs Temperature

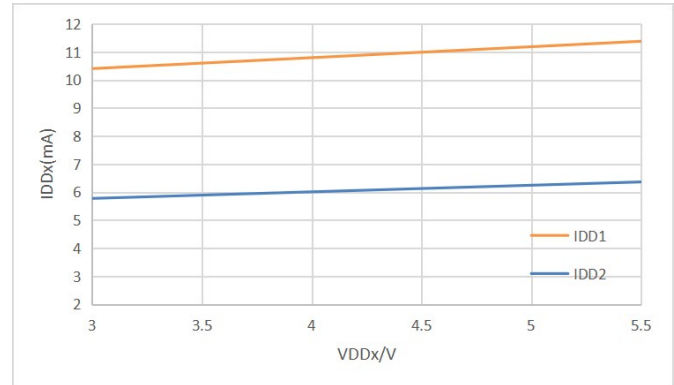


Figure 5.11 Supply Current vs Supply Voltage

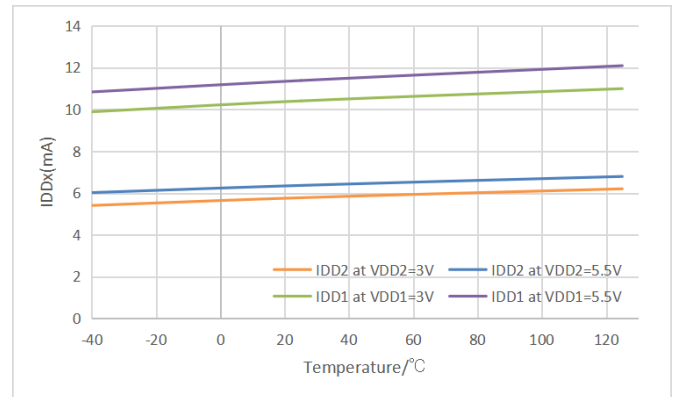


Figure 5.12 Supply Current vs Temperature

5.3. Parameter Measurement Information

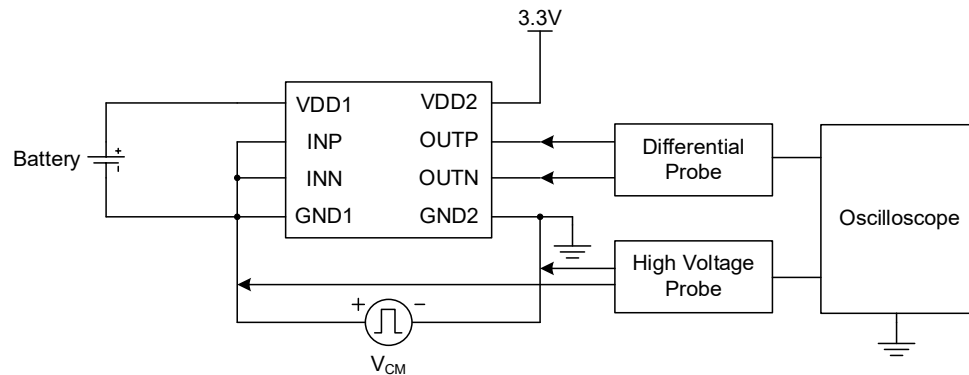


Figure 5.1 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value		Unit	Comments
		DUB8	SOP8(300mil)		
Minimum External Air Gap (Clearance)	CLR	6.5	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	6.5	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	32	32	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I	I		IEC 60664-1

Description	Test Condition	Value	
		DUB8	SOP8(300mil)
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 150\text{Vrms}$	I to IV	I to IV
	For Rated Mains Voltage $\leq 300\text{Vrms}$	I to IV	I to IV
	For Rated Mains Voltage $\leq 600\text{Vrms}$	I to IV	I to IV
	For Rated Mains Voltage $\leq 1000\text{Vrms}$	I to III	I to III
Climatic Classification		40/125/21	40/125/21
Pollution Degree per DIN VDE 0110, Table 1		2	2

6.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			DUB8	SOW8	
Maximum repetitive isolation voltage		V_{IORM}	2121	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	1500	V_{RMS}
	DC Voltage		2121	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{ s}$.	q_{pd}	<5	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$,				

Description	Test Condition	Symbol	Value		Unit
			DUB8	SOW8	
	$t_{ini}=60s$, $V_{pd(m)}=1.6 \cdot V_{IORM}$, $t_m=10s$ Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2 \cdot V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.875 \cdot V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)				
Maximum transient isolation voltage	$t = 60 \text{ sec}$	V_{IOTM}	8000	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$, $T_{amb}=25^{\circ}C$	R_{IO}	$>10^{12}$	$>10^9$	Ω
	$V_{IO} = 500V$, $100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	$V_{IO} = 500V$, $T_{amb}=T_s$	R_{IO}	$>10^9$	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	0.8	pF
Total Power Dissipation at 25°C	$V_I = 5.5V$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	P_s	1650	1430	mW
Safety input, output, or supply current	$\theta_{JA} = 75^{\circ}C/W$, $V_I = 5.5V$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	I_s	300	/	mA
Safety input, output, or supply current	$\theta_{JA} = 86^{\circ}C/W$, $V_I = 5.5V$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	I_s	/	260	mA
Maximum safety temperature		T_s	150	150	$^{\circ}C$
UL1577					
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60 \text{ s}$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1 \text{ s}$ (100% production test)	V_{ISO}	5000	5000	V_{RMS}

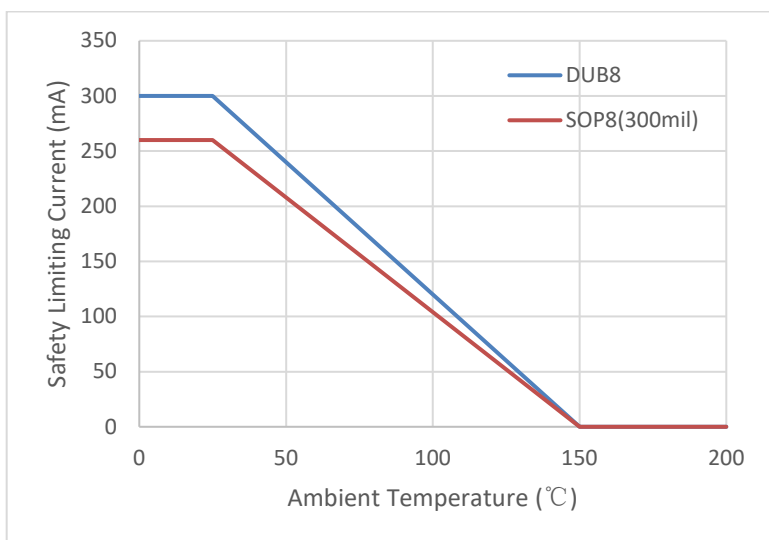


Figure 6.1 NSI1200 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

6.3. Regulatory Information

The NSI1200 are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforce Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	Reinforced insulation	5000V _{rms} for 1min
E500602	E500602	40052820	CQC20001264938 for SOW8 CQC20001263786 for DUB8	R50574061

7. Function Description

7.1. Overview

The NSI1200 is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, sigma-delta ($\Sigma\Delta$) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier that separates the side1 and side2 voltage domains. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the side2 and presented as a differential output of the device.

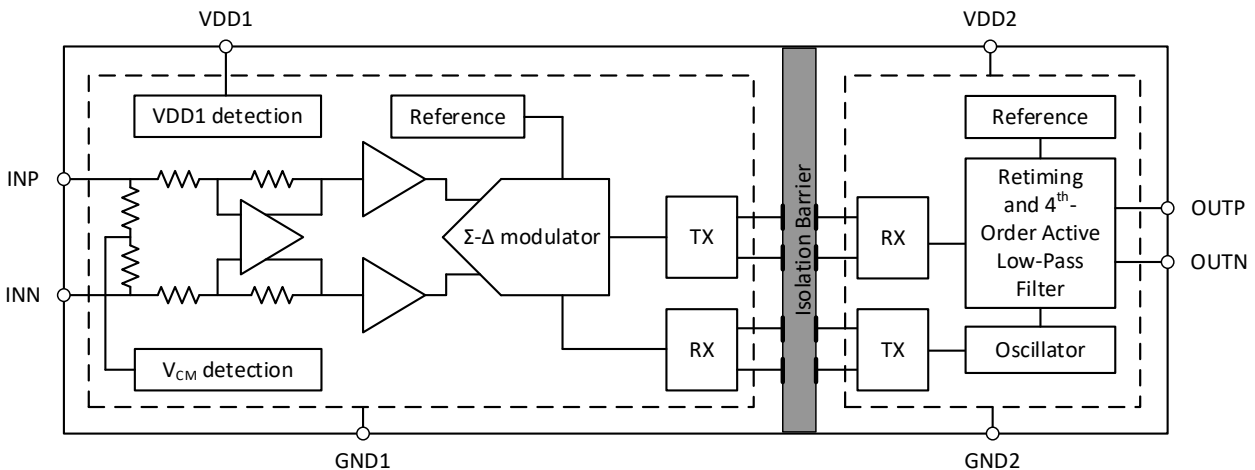


Figure 7.1 Function Block Diagram

7.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range $GND1 - 6\text{ V}$ to $VDD1 + 0.5\text{ V}$, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

7.3. Analog Output

For linear input range, the analog output of NSI1200 has a fixed gain of 8. If a full-scale input signal is applied to the NSI1200 ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically, 2.4V for positive clipping and -2.4V for negative clipping).

In addition, NSI1200 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated in following conditions:

- When the undervoltage of VDD1 is detected ($VDD1 < VDD1_{UV}$).
- When the overvoltage of common-mode input voltage is detected ($V_{CM} > V_{CMov}$).

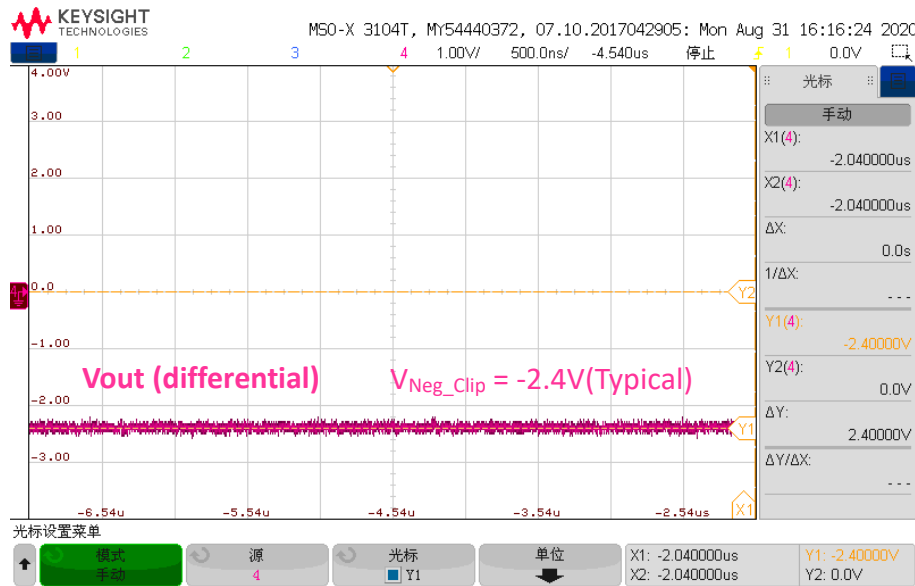


Figure 7.2 Typical negative clipping output

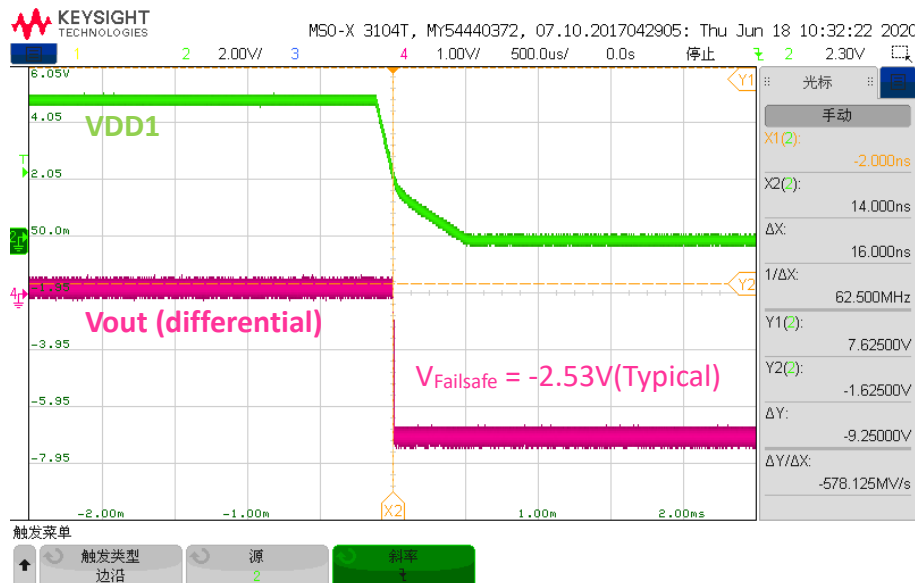


Figure 7.3 Typical Failsafe output when VDD1 undervoltage

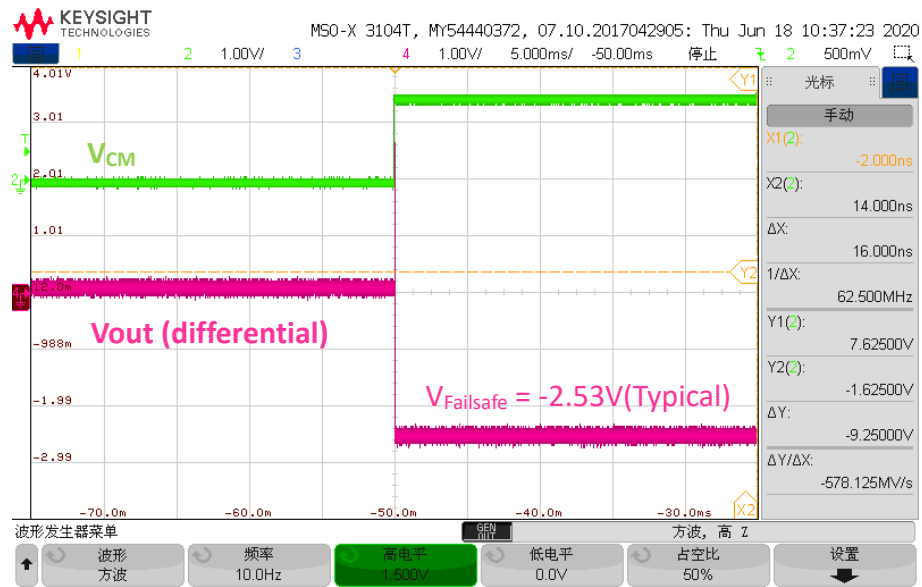


Figure 7.4 Typical Failsafe output when input common mode signal overvoltage

8. Application Note

8.1. Typical Application Circuit

NSI1200 is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 8.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1200 through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add $>1k\Omega$ resistor on the OUTP and OUTN pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

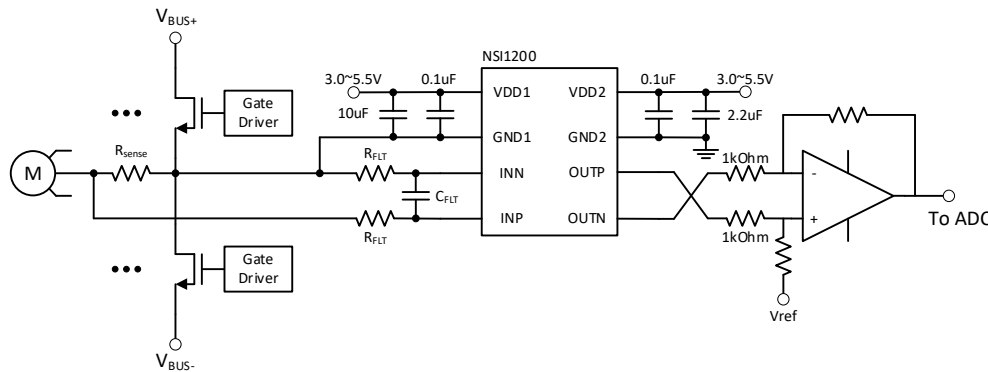


Figure 8.1 Typical application circuit in phase current sensing

8.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

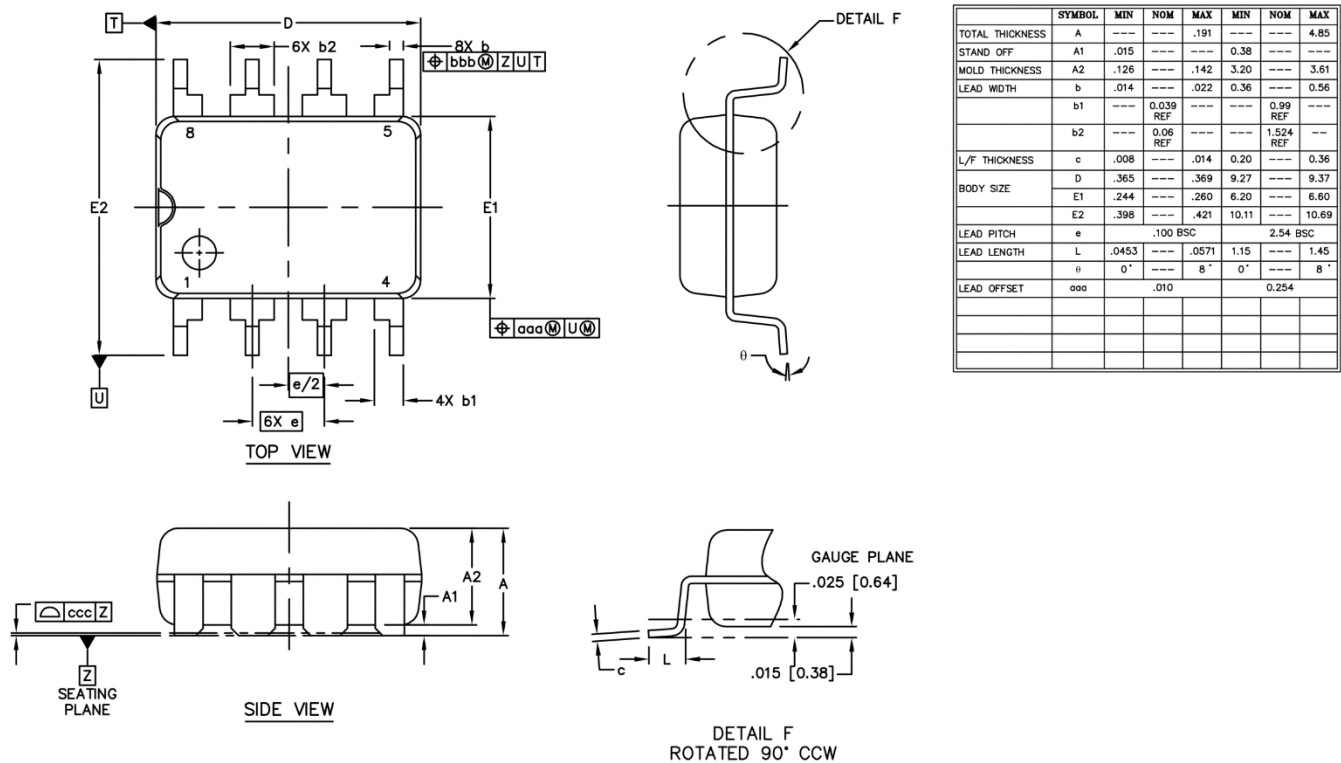
- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

8.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

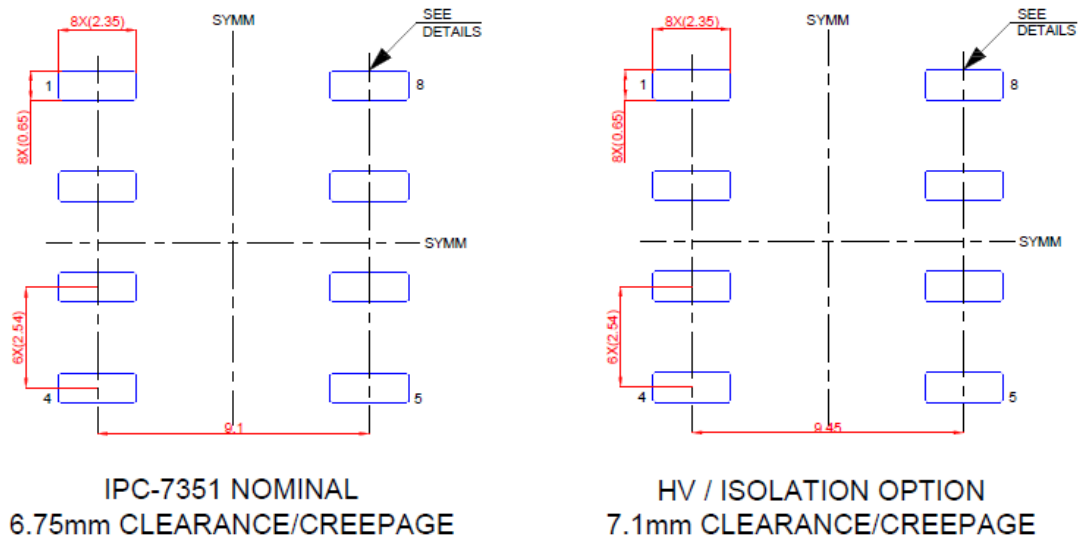
- NSI1200 requires a $0.1\mu F$ bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional $1\sim 10\mu F$ capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1200. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1200. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

9. Package Information

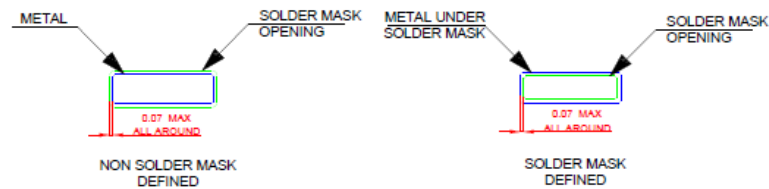


NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.1 DUB8 Package Shape and Dimension in millimeters

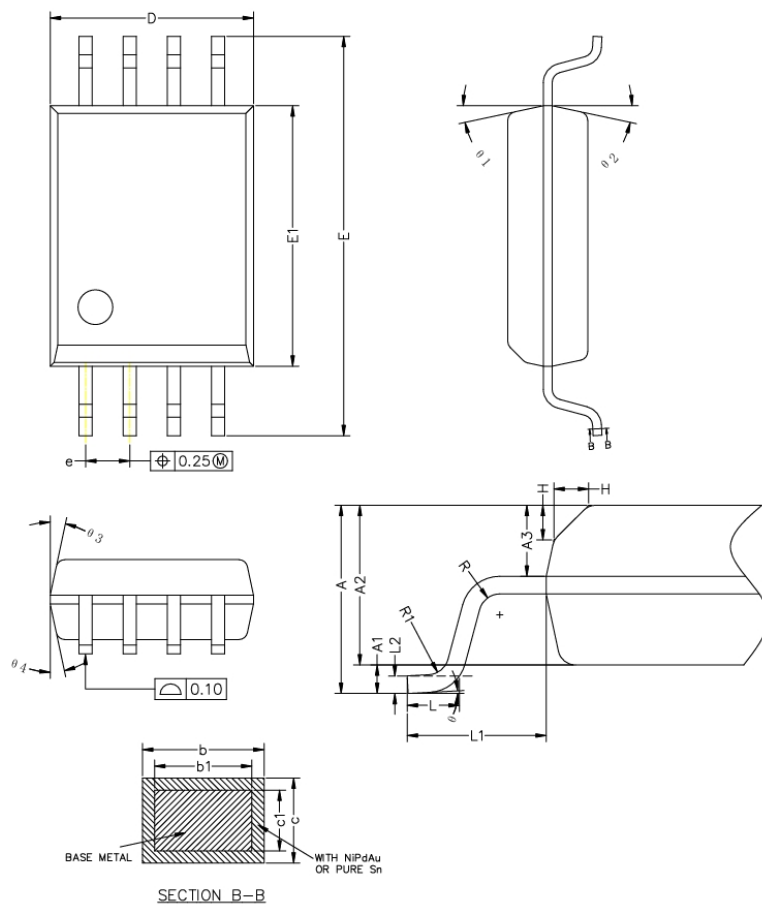


LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 9.2 DUB8 Package Board Layout Example



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.3 SOW8 Package Shape and Dimension in millimeters

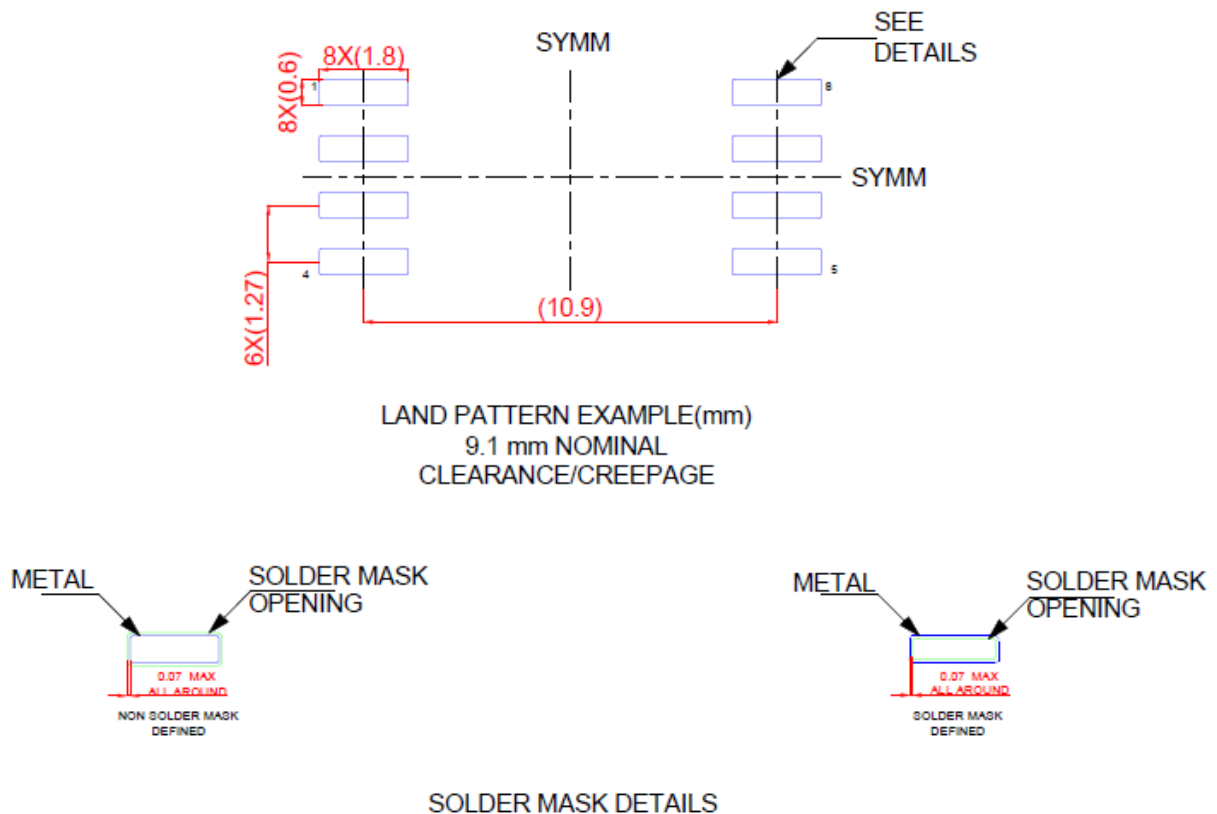


Figure 9.4 SOW8 Package Board Layout Example

10. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SPQ
NSI1200 - DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	NO	SOP8 (300mil)	SOW8	1000
NSI1200- DDBR	5	-250 ~ 250	Level-3	-40 to 125°C	NO	DUB8	DUB8	800

11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1200	Click here	Click here	Click here	Click here

12. Tape and Reel Information

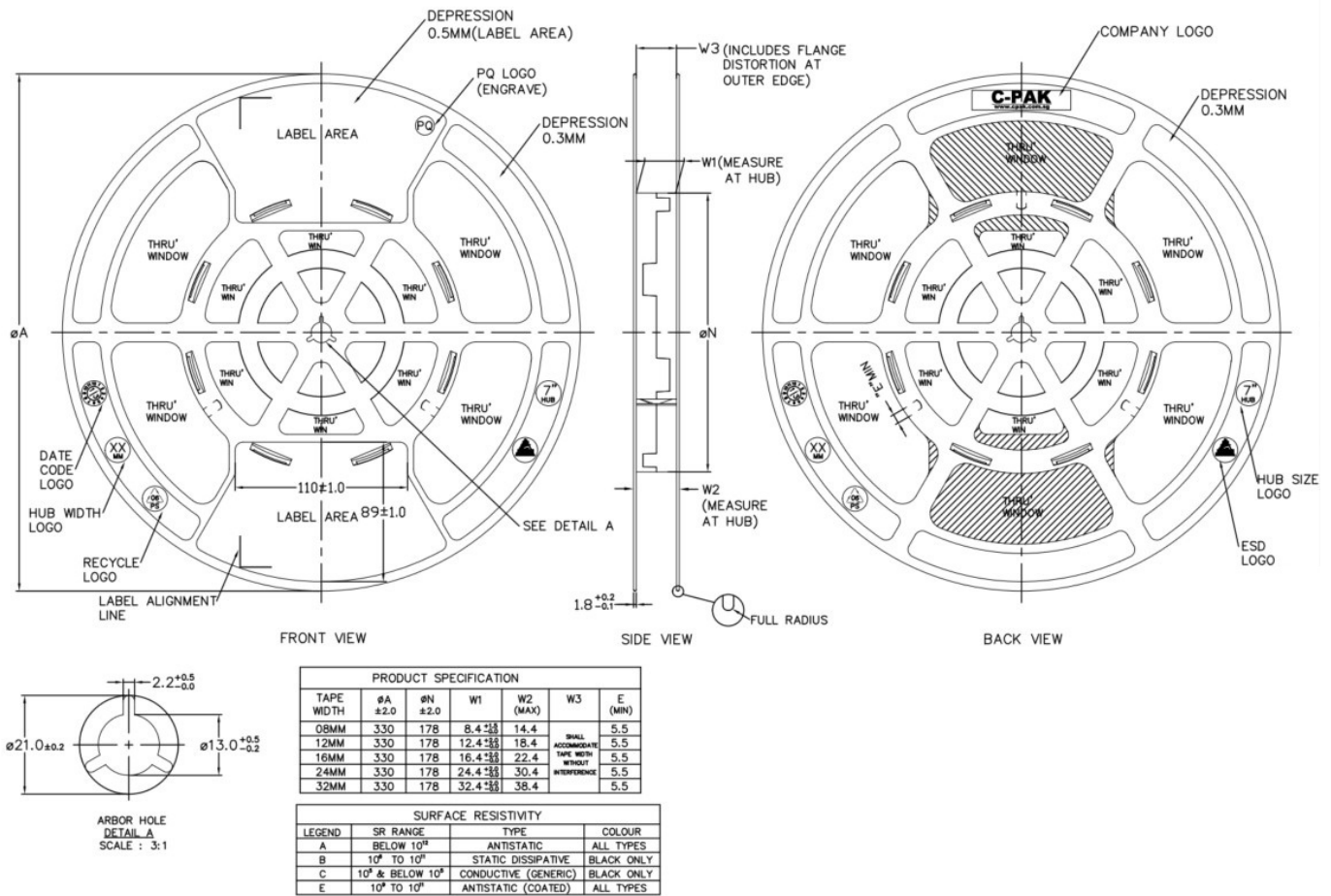
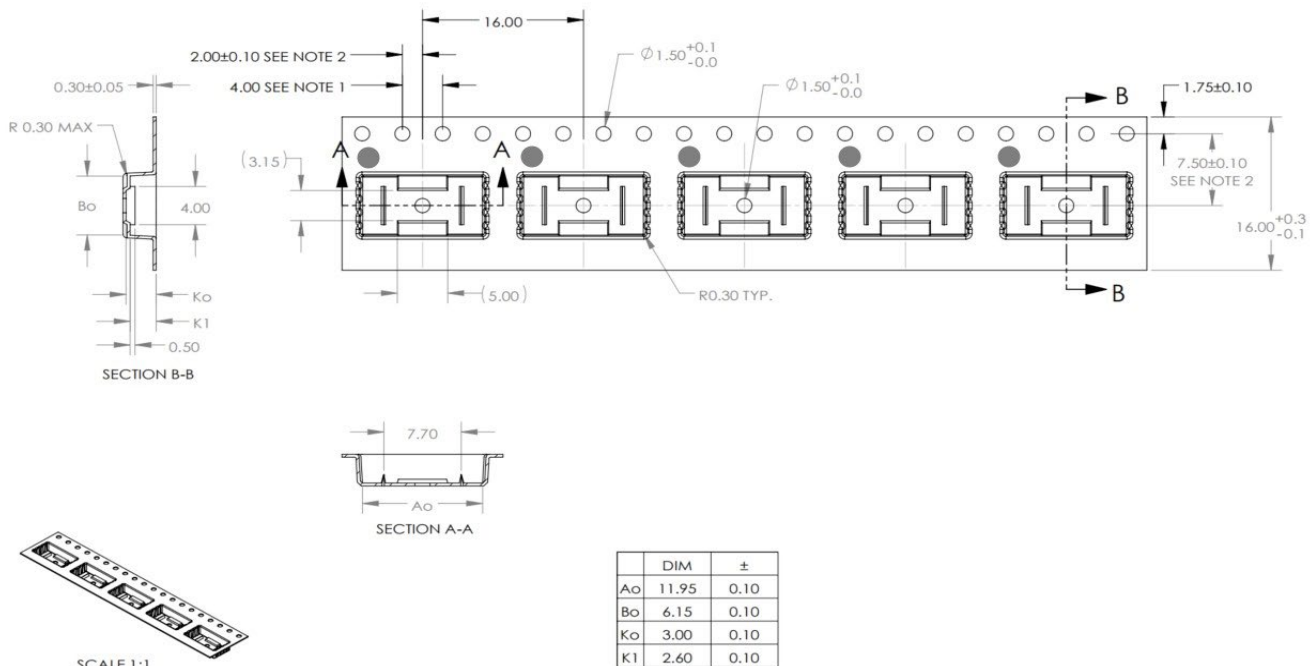


Figure 12.1 Tape Information



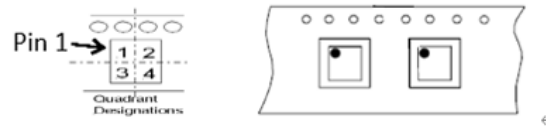


Figure 12.2 Reel Information of SOP8(300mil)

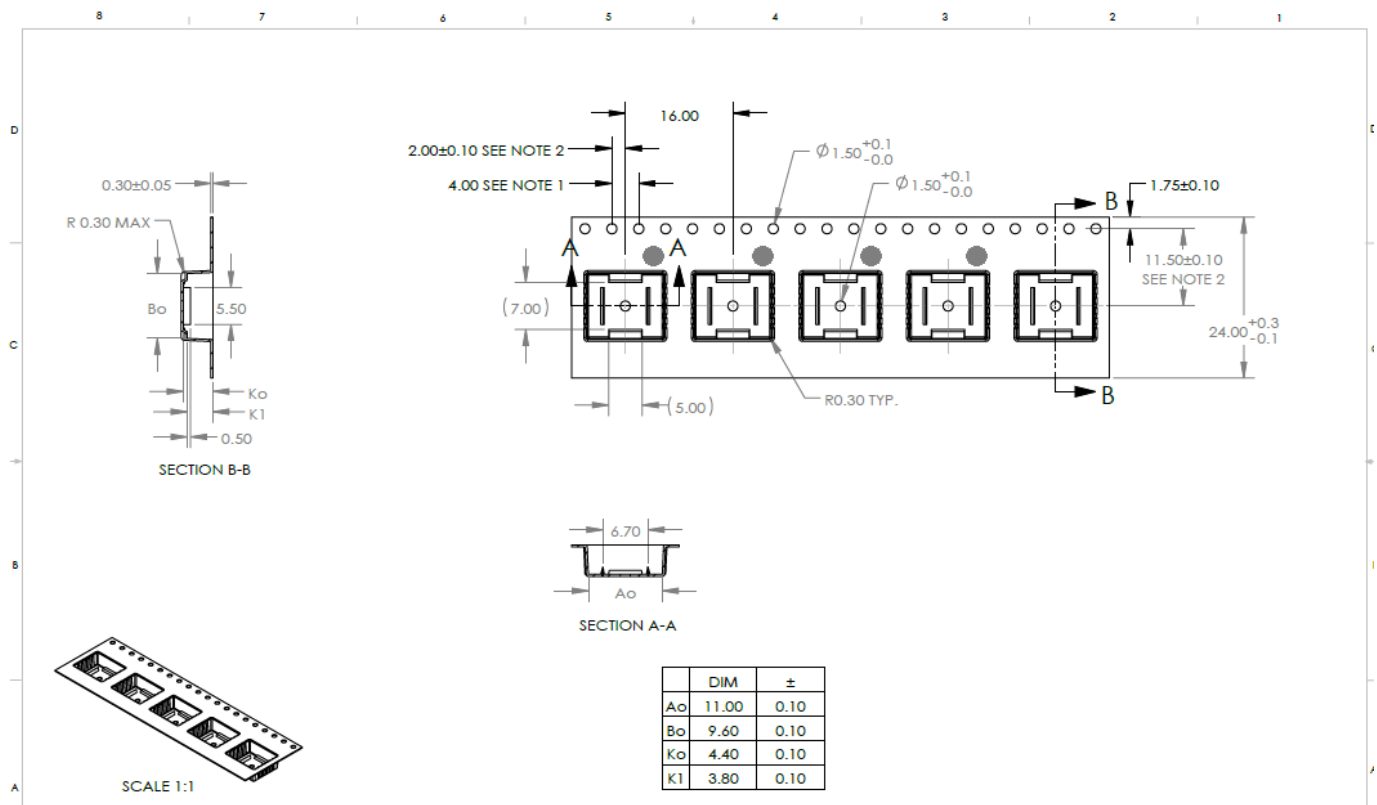


Figure 12.3 Reel Information of DUB8

13. Revision History

Revision	Description	Date
1.0	Initial Release	2021/1/11
1.1	Add V_{ISO} specification in 6.2 Insulation Characteristics and AEC-Q100 qualification	2121/4/12
1.2	Update insulation characteristics in 6.2	2021/7/17
1.3	Update the standard on which V_{IOSM} test method is based in 6.2, description form of V_{pd} (m) in 6.2, Isolation resistance and Isolation capacitance specification in 6.2, certificate number in 6.3 and important notice at the end of the datasheet. Delete NSI1200-Q1SWVR in part 10. Update typeface to Source Sans Pro.	2023/2/24
1.4	● Update all NSi to NSI. ● Update test temperature condition of V_{os}, I_{IB}, E_G and Nonlinearity in 5.1 ● Update safety regulatory info in 6.1~6.3 ● Update Package Information in Figure 9.1~9.4	2025/11/3

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