NSI1150
Isolated CAN Transceiver
Datasheet (EN) 1.2

Product Overview

The NSI1150 is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSI1150 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSI1150 device is safety certified by UL1577 support 3 kV_{rms},5kV_{rms} and 7.5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSI1150 is up to 5Mbps. The NSI1150 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 3000Vrms/5000Vrms Insulation voltage
- Power supply voltage
  VDD_1: 2.5V to 5.5V
  VDD_2: 4.5V to 5.5V
- Bus fault protection of -70V to +70V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Data rate: up to 5Mbps
- High CMTI: 150kV/μs
- Low loop delay: <220ns
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40°C ~125°C
- RoHS-compliant packages: SOP16(300mil), DUB8, SOP8(300mil), SOP8(600mil)

Safety Regulatory Approvals

- UL recognition:
  - SOP16(300mil): 5000V_{rms} for 1 minute per UL1577
  - DUB8: 3000V_{rms} for 1 minute per UL1577
  - SOP8(300mil): 5000Vrms for 1 minute per UL1577
  - SOP8(600mil): 7500Vrms for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

Device Information

Part Number	Package	Body Size
NSI1150-DDBR	DUB8	9.32mm ×6.35mm
NSI1150-DSWR	SOP16(300mil)	10.30mm × 7.50mm
NSI1150-DSWVR	SOP8(300mil)	5.85mm × 7.50mm
NSI1150-DSWWAR	SOP8(600mil)	6.25mm×13.6mm

Functional Block Diagrams

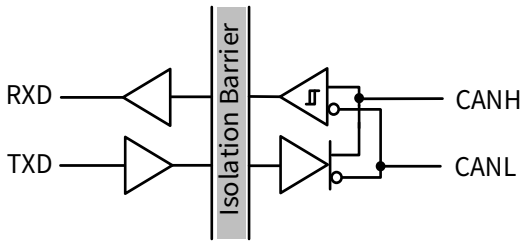

Figure 1. NSI1150 Simplified Schematic

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1. Pin Configuration and Functions

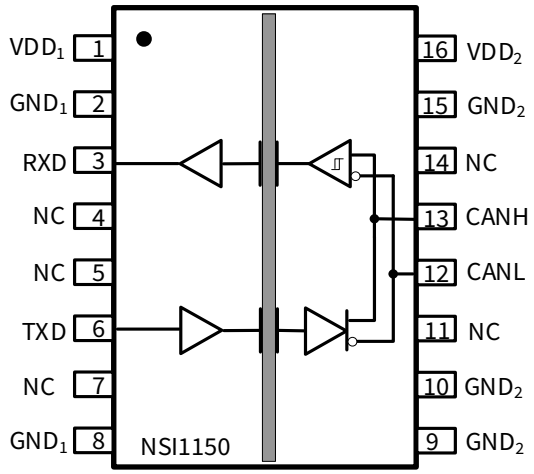


Figure 1.1 SOP16(300mil) Package Top View

Table1.1 SOP16(300mil) Pin Configuration and Description

SOP16(300mil) PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD_1	Power Supply for Side 1
2, 8	GND_1	Ground 1, the ground reference for Isolator Side 1
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4, 5, 7, 11, 14	NC	No Connection
6	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
9, 10, 15	GND_2	Ground 2, the ground reference for Isolator Bus Side
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
16	VDD_2	Power supply for Bus Side

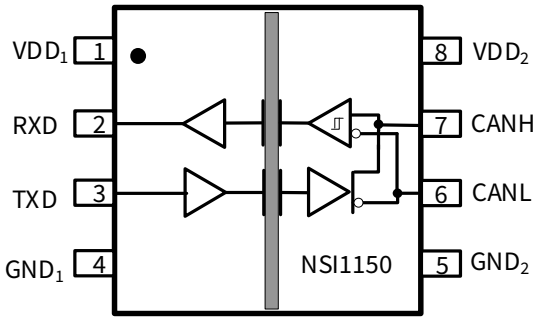


Figure 1.2 DUB8 Package Top View

Table1.2 DUB8 Pin Configuration and Description

DUB8 PIN NO.	SYMBOL	FUNCTION
1	VDD_1	Power Supply for Side 1
2	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
3	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
4	GND_1	Ground 1, the ground reference for Isolator Side 1
5	GND_2	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD_2	Power supply for Bus Side

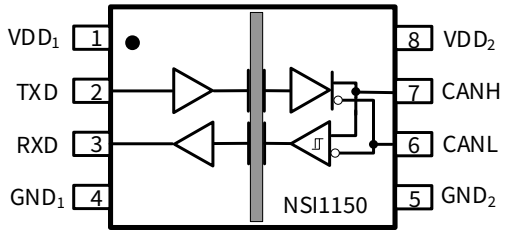


Figure 1.3 SOP8(300mil)/ SOP8(600mil) Package Top View

Table1.3 SOP8(300mil) / SOP8(600mil) Package Pin Configuration and Description

SOP8(300mil) SOP8(600mil) PIN NO.	SYMBOL	FUNCTION
1	VDD_1	Power Supply for Side 1
2	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	GND_1	Ground 1, the ground reference for Isolator Side 1
5	GND_2	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD_2	Power supply for Bus Side

2. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1) (2)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD_1, VDD_2	-0.5		6.5	V	VDD_1 to GND_1 VDD_2 to GND_2
Maximum Input/ Output Voltage	V_{TXD}, V_{RXD}	-0.5		VDD_1+0.5(3)	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-70		+70	V	CANH, CANL with respect to GND_2
Voltage between pin CANH and pin CANL	V_{CANH}-V_{CANL}	-70		+70	V	
Output current	I_o	-15		15	mA	RXD pin
Junction Temperature	T_J	-40		150	°C	
Storage Temperature	T_{stg}	-65		150	°C	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND_1 or GND_2) and are peak voltage values.

(3) Maximum voltage must not exceed 6.5 V.

3. ESD Ratings (1)

Parameters	Ratings		Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	All pins	±6000	V
		CANH and CANL to GND_2	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(3)	All pins	±2000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply voltage, controller side	V_{DD1}	2.5		5.5	V	VDD_1 to GND_1
Supply voltage, bus side	V_{DD2}	4.5	5	5.5	V	VDD_2 to GND_2
Voltage at bus pins (separately or common mode)	V_I or V_{IC}	-30		30	V	CANH or CANL with respect to GND_2
High-level input voltage	V_{IH}	0.7*VDD_1		VDD_1	V	TXD pin
Low-level input voltage	V_{IL}	0		0.3*VDD_1	V	TXD pin
Differential input voltage	V_{ID}	-7		7	V	CANH with respect to CANL
High-level output current	I_{OH}	-70			mA	CANH or CANL pin
		-4			mA	RXD pin

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Low-level output current	I_{OL}			70	mA	CANH or CANL pin
				4	mA	RXD pin
Operating ambient temperature	T_A	-40		125	°C	
Data Rate	DR			5	Mbps	

5. Thermal Information

Parameters	Symbol	DUB8	SOP8 (300mil)	SOP16 (300mil)	SOP8 (600mil)	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	73.3	84.3	76.0	77.3	°C/W
Junction-to-case(top) thermal resistance	$R_{\theta JC(top)}$	63.2	36.3	41	42.7	
Junction-to-board thermal resistance	$R_{\theta JB}$	43.0	47.0	47.7	26.4	
Junction-to-top characterization parameter	Ψ_{JT}	17.4	9.6	7	15.3	
Junction-to-board characterization parameter	Ψ_{JB}	41.8	29.2	23	25.7	

6. Specifications

6.1. Electrical Characteristics

(VDD_1=2.5V~5.5V, VDD_2=4.5V~5.5V, T_A=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD_1= 3.3V, VDD_2= 5V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply characteristics						
Supply Voltage	VDD_1	2.5		5.5	V	VDD_1 to GND_1
	VDD_2	4.5	5	5.5	V	VDD_2 to GND_2
Power on Reset	VDD_{1POR}	2	2.2	2.4	V	POR threshold as during VDD_1 power-up
	VDD_{1HYS}		0.1		V	VDD_1 POR threshold Hysteresis
	VDD_{2POR}	4.0	4.2	4.4	V	POR threshold as during VDD_2 power-up
	VDD_{2HYS}		0.2		V	VDD_2 POR threshold Hysteresis
Logic side supply current	IDD_1		2.65	4.5	mA	VDD_1=3.3V, V_{TXD}= 0V
			1.43	2.5	mA	VDD_1=3.3V, V_{TXD}=VDD_1
			2.72	4.5	mA	VDD_1=5V, V_{TXD}=0V
			1.48	2.5	mA	VDD_1=5V, V_{TXD}= VDD_1

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Bus side supply current	IDD_2		47.62	70	mA	V_{TXD}= 0V, R_{Load} =60Ω
			5.50	8	mA	V_{TXD}= VDD_1
Device characteristics						
Thermal-Shutdown Threshold	T_{TS}		170		°C	
Common Mode Transient Immunity	CMTI	±100	±150		kV/μs	See Figure 6.13
CAN transmit data input; pin TXD						
Rising input switching threshold	$V_{IT+(TXD)}$		0.6*VDD_1	0.7*VDD_1	V	
Falling input switching threshold	$V_{IT-(TXD)}$	0.3*VDD_1	0.4*VDD_1		V	
Input switching threshold hysteresis voltage	$V_{I\_HYS(TXD)}$		0.2*VDD_1		V	
High level input current	I_{IH}			10	μA	
Low level input current	I_{IL}	-10			μA	
Input Capacitance	C_{IN}		2		pF	
CAN receive data output; pin RXD						
Output Voltage High	V_{OH}	VDD_1-0.4	VDD_1-0.2		V	I_{OH} = -4mA
Output Voltage Low	V_{OL}		0.2	0.4	V	I_{OL} = 4mA
Driver electrical characteristics; pins CANH and CANL						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.60	4.5	V	V_{TXD}=0V, R_{Load} =60Ω, see Figure 6.1
CANL output voltage (Dominant)	$V_{OL(D)}$	0.8	1.43	2	V	V_{TXD}=0V, R_{Load} =60Ω, see Figure 6.1
Bus output voltage (Recessive)	$V_{O(R)}$	2	2.5	3	V	V_{TXD}=VDD_1, R_{Load} =60Ω
Differential output voltage (Dominant)	$V_{OD(D)}$	1.4		3	V	V_{TXD}=0V, R_{Load} =45Ω, see Figure 6.1
		1.5		3	V	V_{TXD}=0V, R_{Load} =60Ω, see Figure 6.1
		1.5		5	V	V_{TXD}=0V, R_{Load} =2240Ω, see Figure 6.1
Differential output voltage (Recessive)	$V_{OD(R)}$	-120	-30	12	mV	V_{TXD}=VDD_1, R_{Load} =60Ω, see Figure 6.1
		-500	-100	50	mV	V_{TXD}=VDD_1, No Load, see Figure 6.1

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Driver symmetry (dominant or recessive)	V_{SYM}	0.9		1.1	V/V	V_{SYM}= ($V_{O(CANH)}$ + $V_{O(CANL)}$) / VDD_2, See Figure 6.3
Common-mode output voltage	V_{OC}	2	2.48	3	V	See Figure 6.7
Peak-to-peak Common-mode output voltage	$V_{OC(PP)}$		360		mV	See Figure 6.7
Short- circuit output current (Dominant)	$I_{OS(D)}$	-105			mA	V_{CANH}= -30V, CANL open, see Figure 6.10
				105	mA	V_{CANL}= 30V, CANH open, see Figure 6.10
Short-circuit output current (Recessive)	$I_{OS(R)}$	-5		5	mA	V_{CANH}= V_{CANL}= -30V to 30V, CANL open, see Figure 6.10
Receiver electrical characteristics; pins CANH and CANL						
Differential input threshold voltage	$V_{IT(Diff)}$	500		900	mV	$\|V_{CM}\|$≤20V
		400		1000	mV	20V≤$\|V_{CM}\|$≤30V
Hysteresis voltage for differential input threshold	$V_{I\_HYS(Diff)}$		100		mV	
Common-mode voltage range	V_{COM}	-30		+30	V	
Input capacitance to ground	C_I		20		pF	
Differential input capacitance	C_{ID}		10		pF	
Power-off (unpowered) bus input leakage current	$I_{LKG(OFF)}$	-10		10	μA	
Differential input resistance	R_{ID}	50		100	kΩ	-2V ≤ V_{CANH} ≤ 7V, -2V ≤V_{CANL} ≤ 7V, R_{ID}=R_{CANH}+R_{CANL}
Input resistance	R_{IN}	25		50	kΩ	-2V ≤ V_{CANH} ≤ 7V, -2V ≤V_{CANL} ≤ 7V,
Input resistance matching	RI_{match}	-3		+3	%	CANH=CANL

6.2. Switching Electrical Characteristics

(VDD_1=2.5V~5.5V, VDD_2=4.5V~5.5V, T_A=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD_1 = 3.3V, VDD_2 = 5V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Device Switching Characteristics						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	t_{Loop1}		149	210	ns	Driver input to receiver output, Recessive to Dominant, see Figure 6.8
Loop delay2	t_{Loop2}		148	210	ns	Driver input to receiver output, Dominant to Recessive, see Figure 6.8
Fail-Safe output delay time from bus-side power loss	t_{fs}		5.5		μs	See Figure 6.11
Driver Switching Characteristics						
Propagation delay time, dominant -to- recessive output	t_{PLH}		68	110	ns	See Figure 6.4
Propagation delay time, recessive -to- dominant output	t_{PHL}		56	110	ns	See Figure 6.4
Differential output signal rise time	t_r		36		ns	See Figure 6.4
Differential output signal fall time	t_f		34		ns	See Figure 6.4
Transmit dominant time-out	t_{TXD_DTO}	1.2	2.5	4	ms	See Figure 6.9
Receiver Switching Characteristics						
Propagation delay time, low-to-high-level output	t_{PLH}		88	130	ns	See Figure 6.6
Propagation delay time, high-to-low-level output	t_{PHL}		86	130	ns	See Figure 6.6
RXD signal rise time	t_r		3		ns	See Figure 6.6
RXD signal fall time	t_f		3		ns	See Figure 6.6
CAN FD timing Characteristics						
Bit time on CAN bus output pins with $t_{bit(TXD)}$ = 500ns	$t_{bit(BUS)}$	435		530	ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See Figure 6.12
Bit time on CAN bus output pins with $t_{bit(TXD)}$ = 200ns		155		210	ns	
Bit time on RXD output pins with $t_{bit(TXD)}$ = 500ns	$t_{bit(RXD)}$	400		550	ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See Figure 6.12
Bit time on RXD output pins with $t_{bit(TXD)}$ = 200ns		120		220	ns	
Receiver timing symmetry with $t_{bit(TXD)}$ = 500ns	Δt_{rec}	-65		40	ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; $\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$ See Figure 6.12
Receiver timing symmetry with $t_{bit(TXD)}$ = 200ns		-45		15	ns	

6.3. Parameter Measurement Information

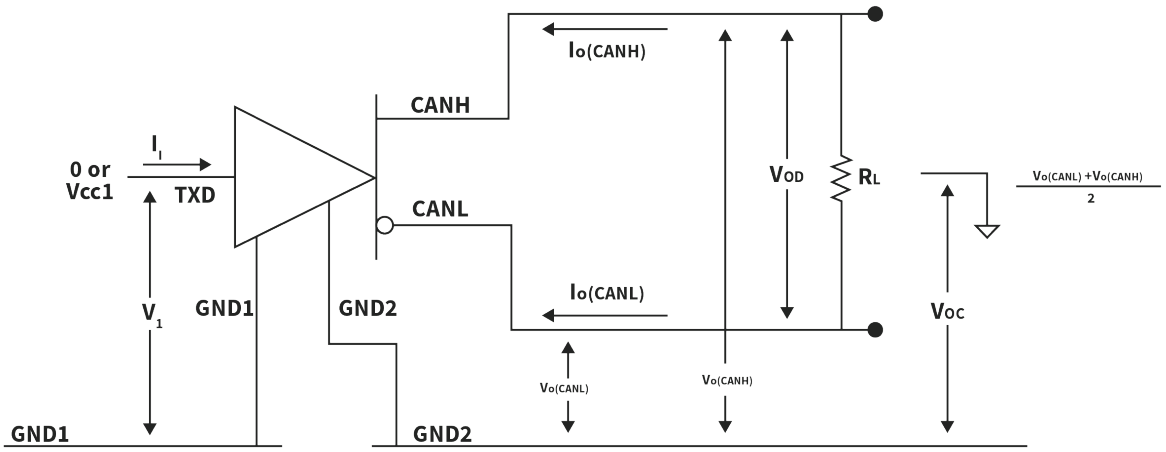


Figure 6.1. Driver Voltage, Current and Test Definitions

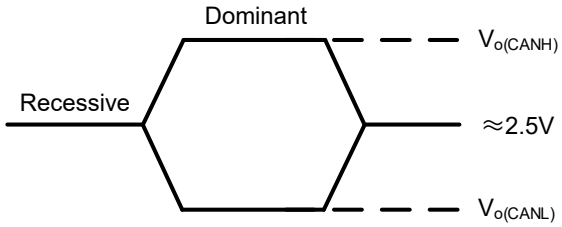


Figure 6.2. Bus Logic State Voltage Definitions

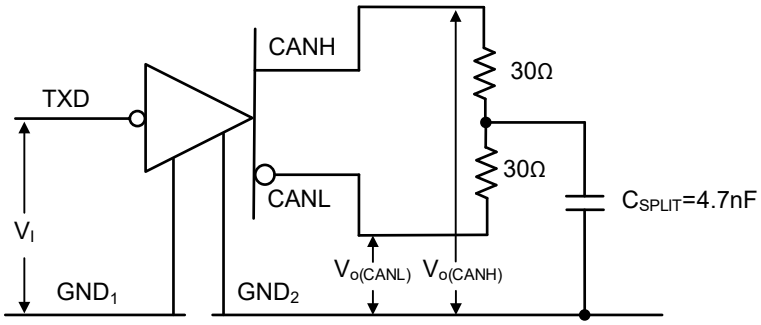
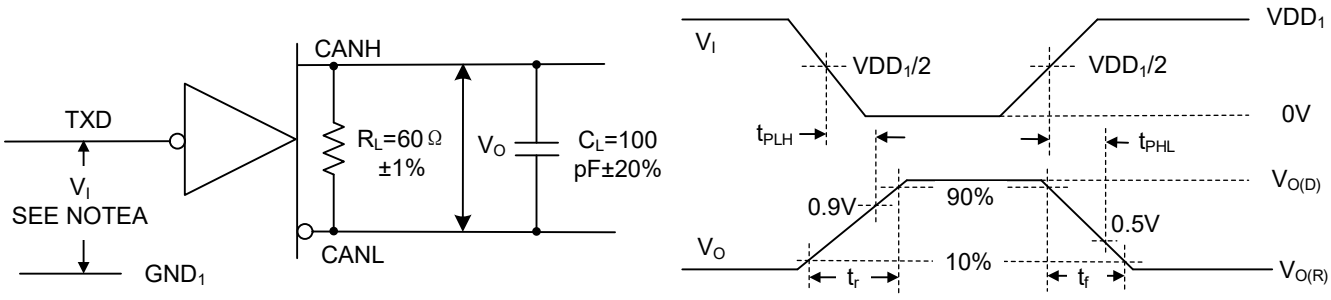


Figure 6.3. Transceiver Driver Symmetry Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle,

t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 6.4. Driver Test Circuit and Voltage Waveforms

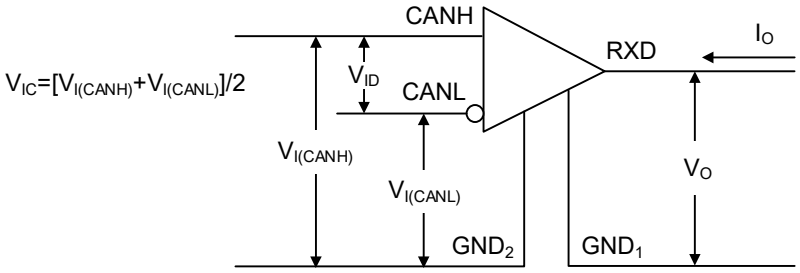
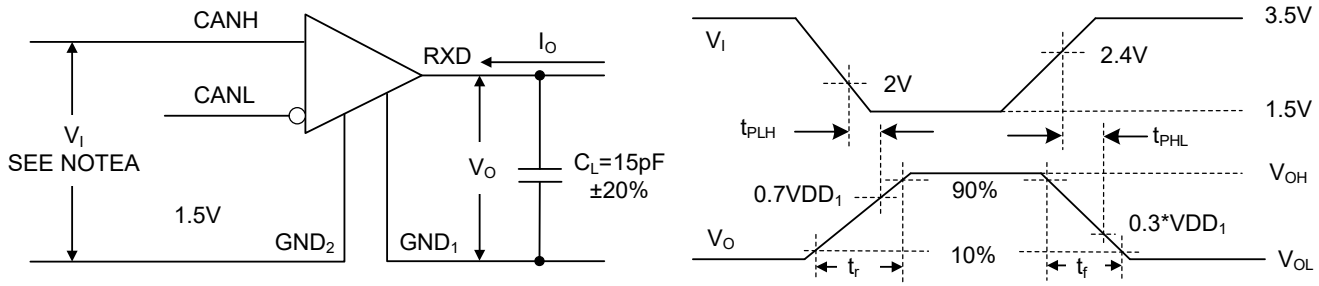


Figure 6.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 6.6. Receiver Test Circuit and Voltage Waveforms

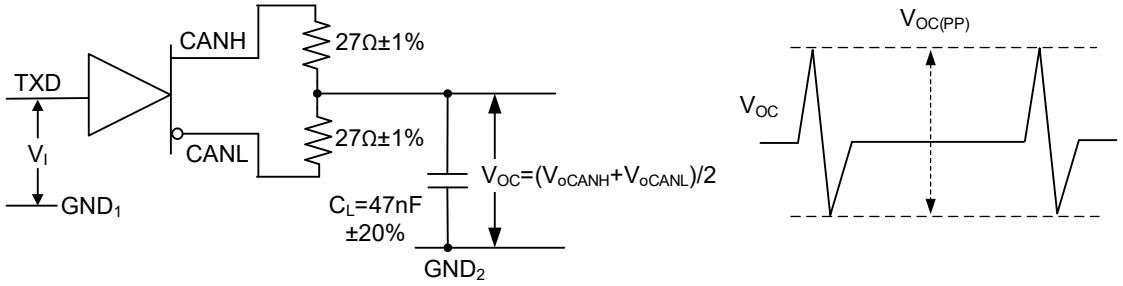


Figure 6.7. Peak-to-Peak Output Voltage Test Circuit and Waveforms

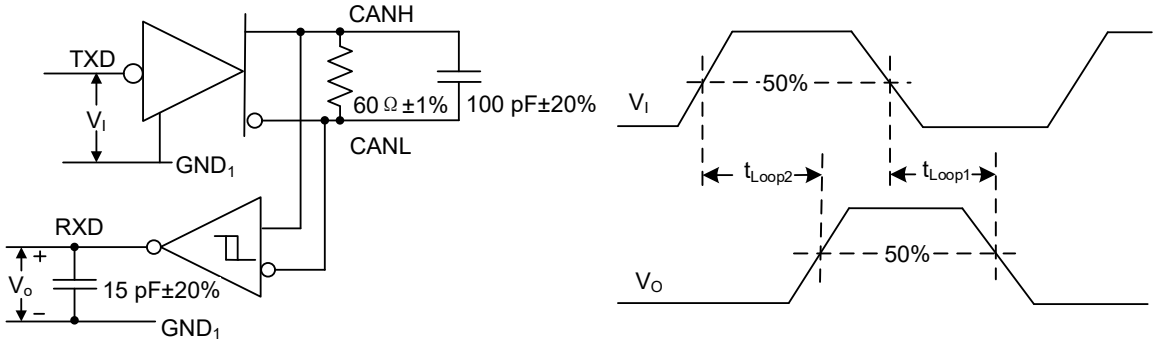
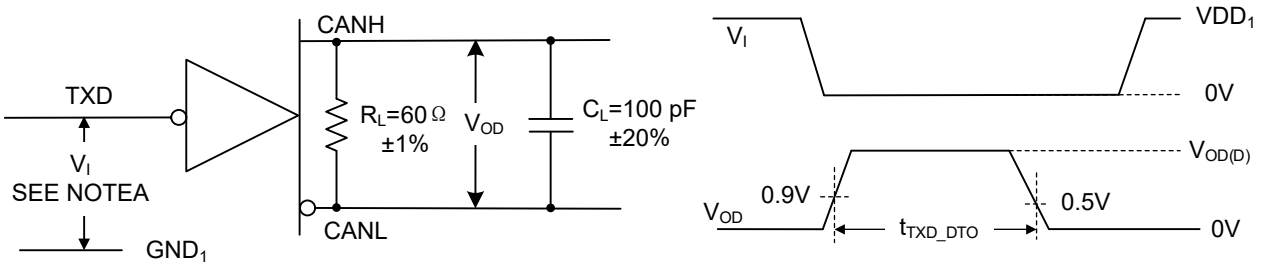


Figure 6.8. t_{LOOP} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 6.9. Dominant Time-out Test Circuit and Voltage Waveforms

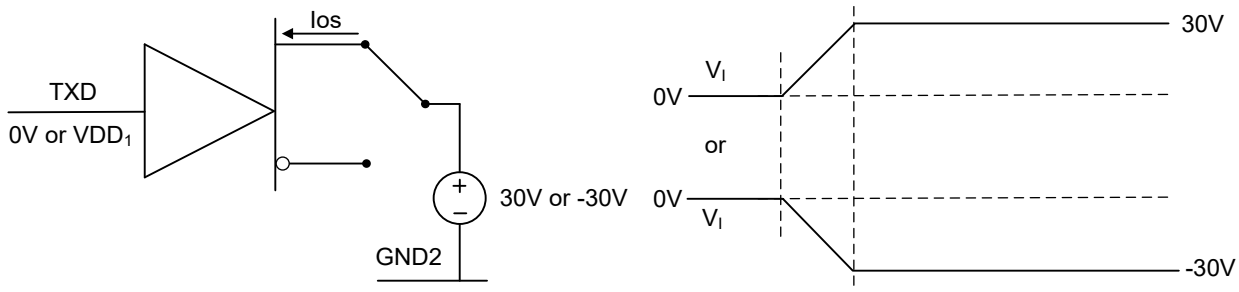


Figure 6.10. Driver Short-Circuit Current Test Circuit and Waveforms

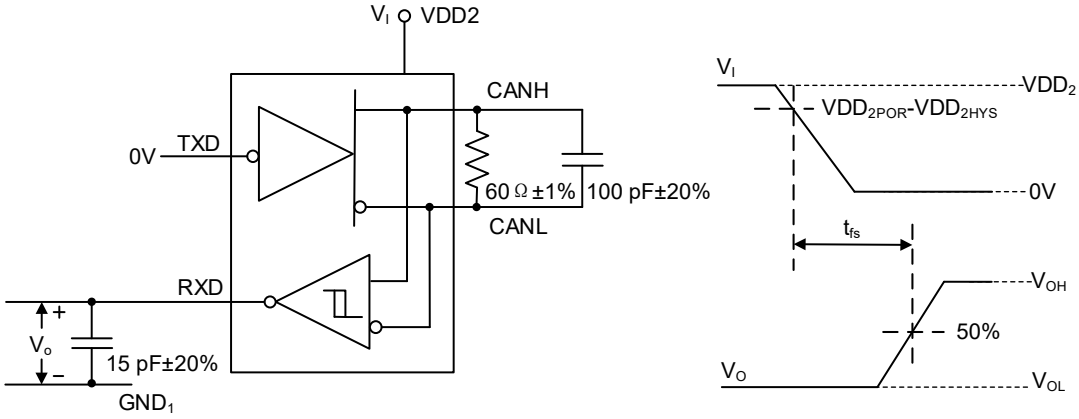


Figure 6.11. Fail-Safe Delay Time Test Circuit and Voltage Waveforms

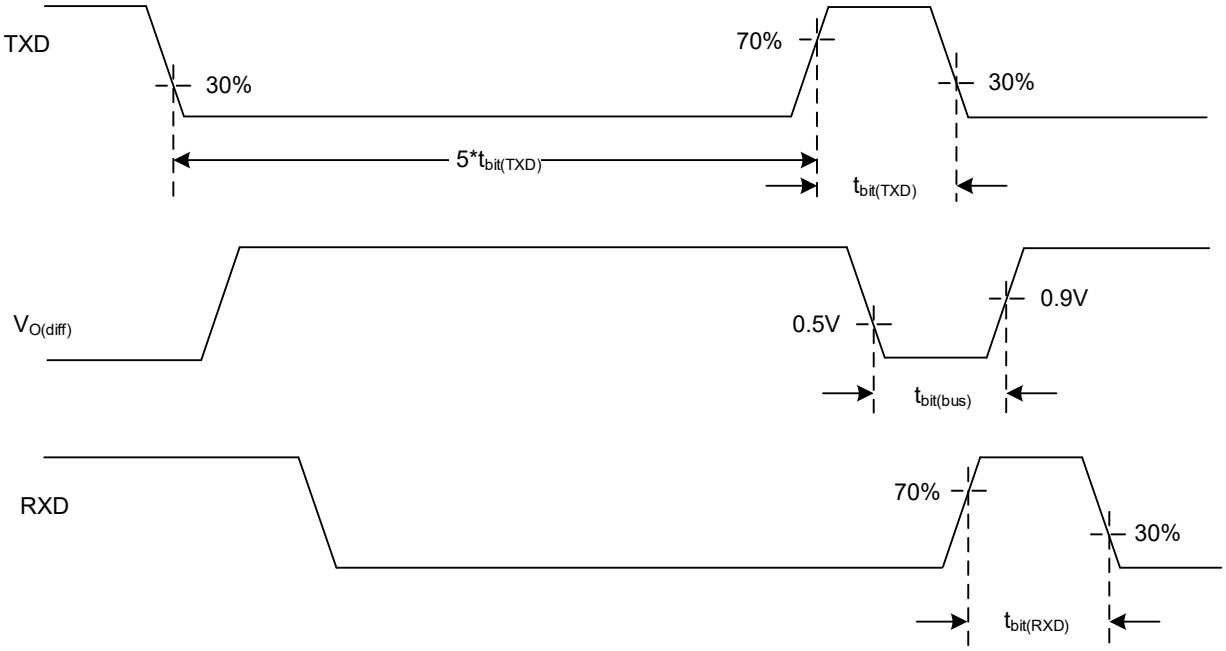


Figure 6.12. CAN FD Timing Parameter Test Circuit and Voltage Waveforms

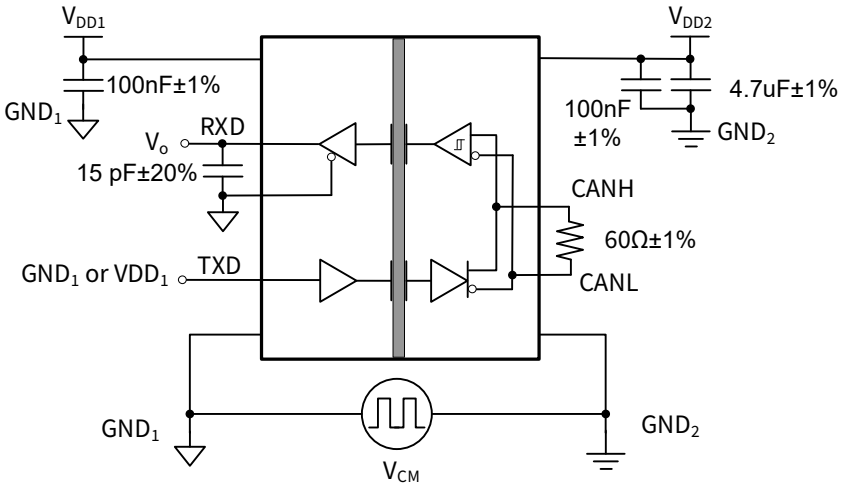
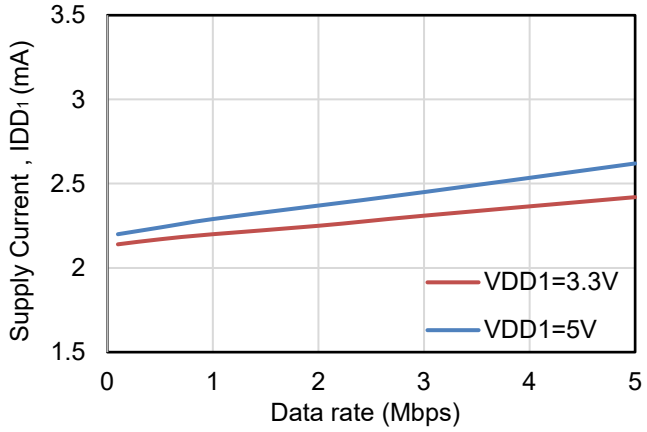


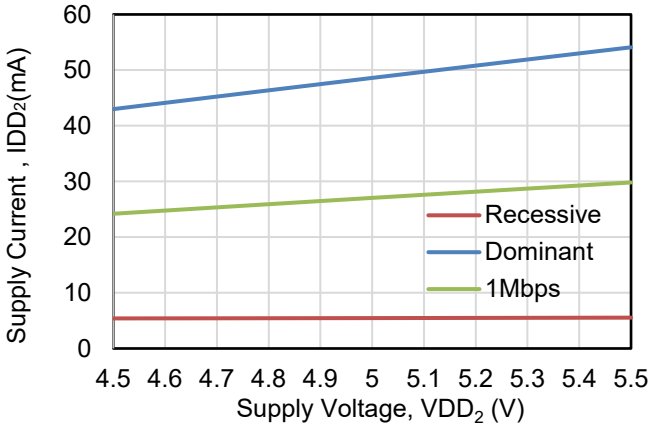
Figure 6.13. Common-Mode Transient Immunity Test Circuit

6.4. Typical Performance Characteristics



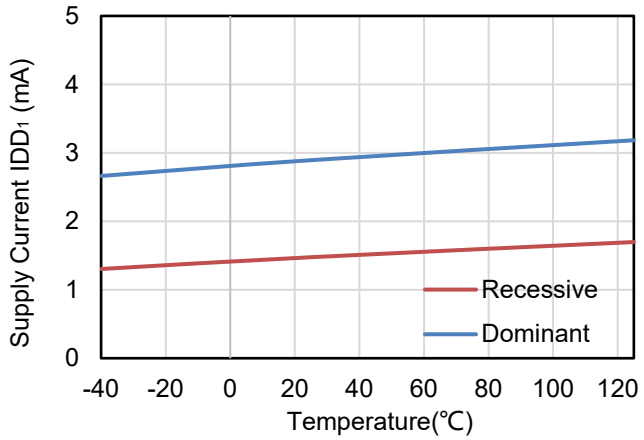
T_A=25℃, $C_{L(RXD)}$=15pF, VDD_2=5V

Figure 6.14. IDD_1 vs Data rate



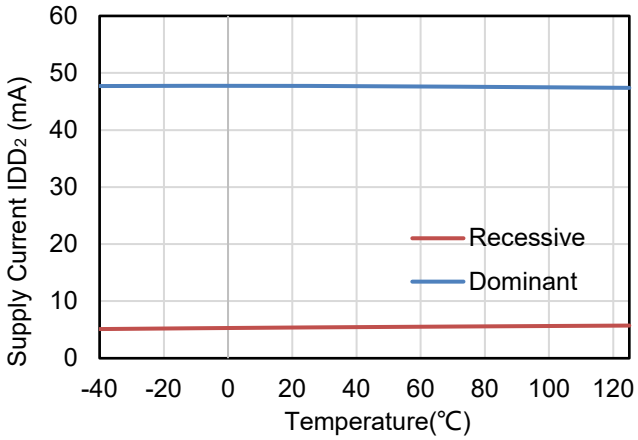
T_A=25℃, R_L=60Ω, VDD_1=5V

Figure 6.15. IDD_2 vs VDD_2 for Recessive, Dominant and 1Mbps CAN Data rates



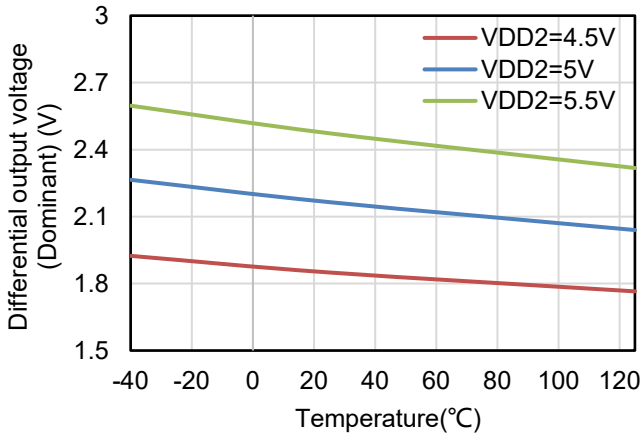
R_L=60Ω, VDD_1=3.3V,VDD_2=5V

Figure 6.16 IDD_1 vs Ambient Temperature for Recessive and Dominant



R_L=60Ω, VDD_1=3.3V,VDD_2=5V

Figure 6.17 IDD_2 vs Ambient Temperature for Recessive and Dominant



VDD_1=3.3V, R_L=60Ω, C_L=Open

Figure 6.18 $V_{OD(DOM)}$ vs Ambient Temperature

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Description	Symbol	Value				Unit	Comments
		DUB8	SOP8 (300mil)	SOP16 (300mil)	SOP8 (600mil)		
Minimum External Clearance	CLR	6.5	8	8	15	mm	IEC 60664-1
Minimum External Creepage	CPG	6.5	8	8	15	mm	IEC 60664-1
Distance Through Insulation	DTI	24				μm	Distance through insulation (internal clearance – capacitive signal isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600				V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I					IEC 60664-1

Description	Test Condition	Value			
		DUB8	SOP8(300mil)	SOP16(300mil)	SOP8(600mil)
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to III	I to IV	I to IV	I to IV
	For Rated Mains Voltage ≤ 600Vrms	/	I to IV	I to IV	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	/	I to III	I to III	I to III
Climatic Classification		40/125/21			
Pollution Degree per DIN VDE 0110		2			

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value				Unit
			DUB8	SOP8 (300mil)	SOP16 (300mil)	SOP8 (600mil)	
DIN EN IEC 60747-17 (VDE 0884-17)							
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	1500	1500	2000	V_{RMS}
	DC voltage		565	2121	2121	2828	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	565	2121	2121	2828	V_{PEAK}
Apparent Charge [1]	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	/	≤5	≤5	≤5	pC

Description	Test Condition	Symbol	Value				Unit
			DUB8	SOP8 (300mil)	SOP16 (300mil)	SOP8 (600mil)	
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10s$						
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1s$ $V_{pd\ (m)}=1.875*V_{IORM}$, $t_m=1s$ （method b1） or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$(method b2)						
Apparent Charge [1]	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60$ s, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10s$.	q_{pd}	≤5	/	/	/	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.3*V_{IORM}$, $t_m=10s$						
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1s$ $V_{pd\ (m)}=1.5*V_{IORM}$, $t_m=1s$（method b1）or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$(method b2)						
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	5300	8000	8000	10600	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	5384	6250	6250	8000	V_{PEAK}
Maximum Surge Isolation Voltage [2]	Test method per IEC62368-1, 1.2/50μs waveform, $V_{IOSM}≥V_{IMP}$ × 1.3.	V_{IOSM}	7000	10000	10000	12800	V_{PEAK}
Isolation Resistance [3]	V_{IO} =500V, T_A=25°C	R_{IO}	>10^{12}				Ω
	V_{IO} = 500 V, 100 °C ≤ T_A ≤ 125 °C		>10^{11}				Ω
	V_{IO} = 500 V, T_A = T_S		>10^{9}				Ω
Isolation Capacitance [3]	f = 1MHz	C_{IO}	0.8	1.2	1.9	0.8	pF
UL1577							
Withstand Isolation Voltage	V_{TEST} = V_{ISO}, t = 60s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 sec, 100% production test	V_{ISO}	3000	5000	5000	7500	V_{RMS}

[1] Apparent charge is electrical discharge caused by a partial discharge (pd).

[2] Testing is carried out in air or insulating oil to determine the intrinsic surge immunity of the isolation barrier.

[3] The side 1 terminals as well as the side 2 terminals of the coupler are connected together forming a two-terminal device.

[4] This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

7.3. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-17 of NSI1150-DDBR

Parameter	Description	Test Condition	Value	Unit
P_S	Safety Supply Power	$R_{\theta JA}$ = 73.3°C/W, T_J = 150°C, T_A = 25°C	1705	mW
I_S	Safety Supply Current	$R_{\theta JA}$ = 73.3°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C	310	mA
T_S	Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of DUB8 package (Thermal Information Table) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

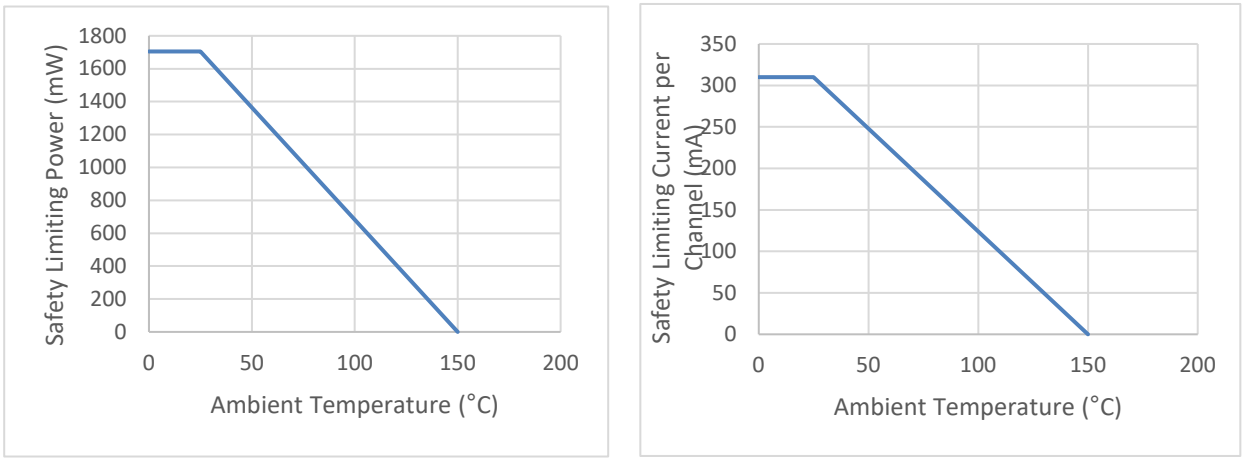


Figure 7.1 NSI1150-DDBR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI1150-DSWR

Parameter	Description	Test Condition	Value	Unit
P_S	Safety Supply Power	$R_{\theta JA}$ = 76°C/W, T_J = 150°C, T_A = 25°C	1645	mW
I_S	Safety Supply Current	$R_{\theta JA}$ = 76°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C	299	mA
T_S	Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package (Thermal Information Table) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

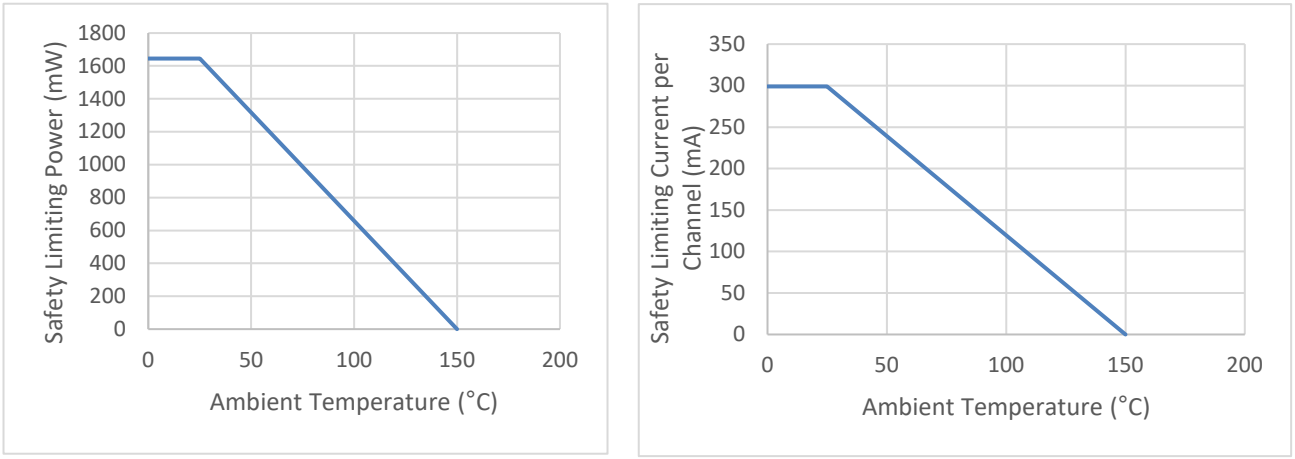


Figure 7.2 NSI1150-DSWR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI1150-DSWVR

Parameter	Description	Test Condition	Value	Unit
P_S	Safety Supply Power	$R_{\theta JA}$ = 84.3 °C/W, T_J = 150 °C, T_A = 25 °C	1483	mW
I_S	Safety Supply Current	$R_{\theta JA}$ = 84.3 °C/ W, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	269	mA
T_S	Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8(300mil) package (Thermal Information Table) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

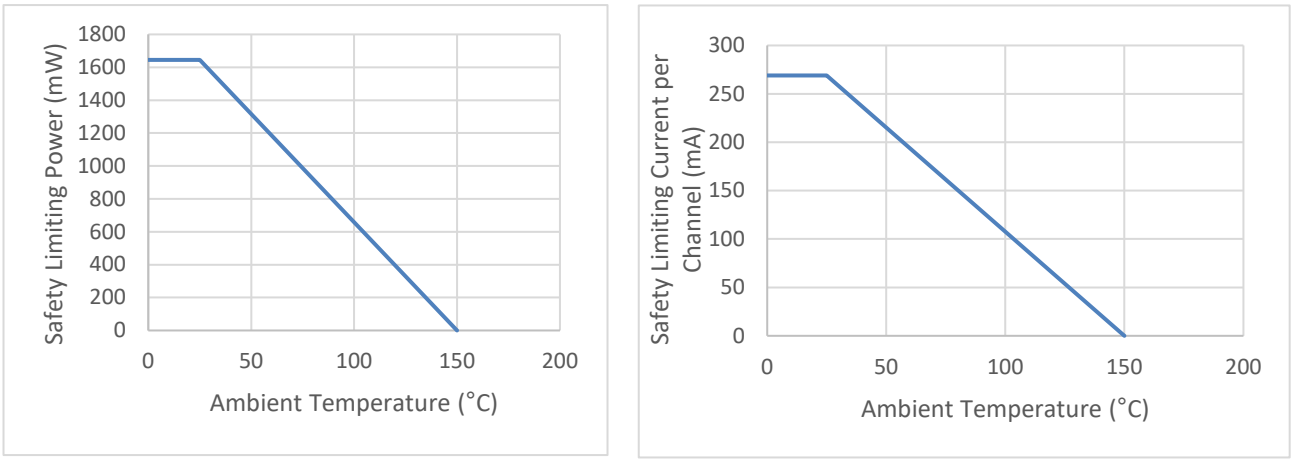


Figure 7.3 NSI1150-DSWVR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI1150-DSWWAR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA}$ = 77.3 °C/W, T_J = 150 °C, T_A = 25 °C	1617	mW
Safety Supply Current	$R_{\theta JA}$ = 77.3 °C/ W, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	294	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8 (600mil) package (Thermal Information Table) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

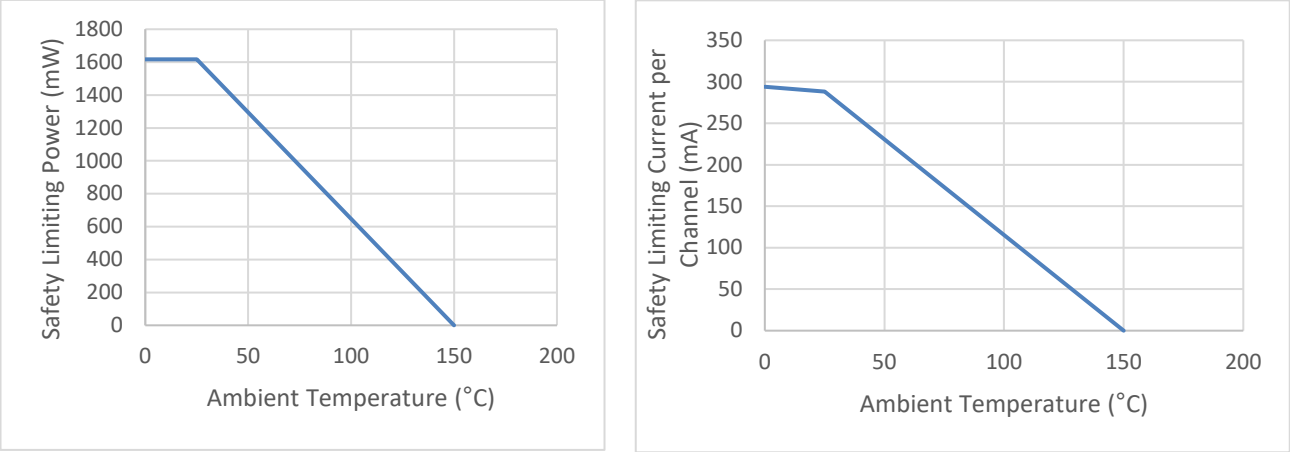


Figure 7.4 NSI1150-DSWWAR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

7.4. Regulatory Information

The NSI1150-DDBR is approved by the organizations listed in table.

UL		*VDE*	*CQC*	*TUV*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 3000 V_{RMS} Isolation voltage	Single Protection, 3000 V_{RMS} Isolation voltage	Basic Insulation V_{IORM}=565V_{PEAK} V_{IOTM}=5300V_{PEAK} V_{IOSM}=7000V_{PEAK}	Basic insulation	3000 V_{RMS} for 1min
E500602		File (pending)	CQC20001263786	R 50574061

The NSI1150-DSWR is approved by the organizations listed in table.

UL		*CQC*	*TUV*	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 5000 V_{RMS} Isolation voltage	Single Protection, 5000 V_{RMS} Isolation voltage	Reinforce insulation	Reinforce Insulation V_{IORM}=2121 V_{PEAK} V_{IOTM}=8000 V_{PEAK} V_{IOSM}=10000 V_{PEAK}	5000 V_{RMS} for 1min
E500602		CQC20001264939	R 50632560	R 50574061

The NSI1150-DSWVR is approved by the organizations listed in table.

UL		CQC	TUV	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 5000 V_{RMS} Isolation voltage	Single Protection, 5000 V_{RMS} Isolation voltage	Reinforced insulation	Reinforce Insulation V_{IORM}=2121 V_{PEAK} V_{IOTM}=8000 V_{PEAK} V_{IOSM}=10000 V_{PEAK}	5000 V_{RMS} for 1min
E500602		CQC20001264938	R 50632560	R 50574061

The NSI1150-DSWWAR is approved by the organizations listed in table.

UL		CQC	TUV	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 7500 V_{RMS} Isolation voltage	Single Protection, 7500 V_{RMS} Isolation voltage	Reinforced insulation	Reinforced Insulation V_{IORM}=2828V_{PEAK} V_{IOTM}=10600V_{PEAK} V_{IOSM}=12800V_{PEAK}	7500 V_{RMS} for 1min
E500602		CQC24001426054	R 50632560	File (pending)

8. Function Description

The NSI1150 is isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSI1150 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSI1150-DSWWAR is safety certified by UL1577 support 7.5kV$_{rms}$ insulation withstand voltages. The NSI1150-DSWR and NSI1150-DSWVR device are safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while the NSI1150-DDBR is safety certified by UL1577 support 3kV$_{rms}$ insulation withstand voltages. The NSI1150 is providing high electromagnetic immunity and low emissions. The data rate of the NSI1150 is up to 5Mbps. The NSI1150 provides thermal protection and transmit data dominant time out function.

8.1. Device Functional Modes

Table 8.1. Driver Function Table

TXD	*CANH*	*CANL*	*BUS STATE*
L	H	L	Dominant
H/ Open	Z	Z	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to V_{DD2}/2

Table 8.2. Receiver Function Table

Device Mode	*V_{ID}=CANH-CANL*	*RXD*	*BUS STATE*
Normal	$V_{ID} \geq V_{IT(Diff)\ (MAX)}$	L	Dominant
	$V_{IT(Diff)\ (MIN)} < V_{ID} < V_{IT(Diff)\ (MAX)}$	X	X
	$V_{ID} \leq V_{IT(Diff)\ (MIN)}$	H	Recessive
	Open	H	Recessive

[1] H= high level; L=low level; X= Uncertain

8.2. TXD Dominant Time-Out Function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

8.3. Current Protection

A current-limiting circuit of the CANH and CANL protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

8.4. Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature TTS, the output drivers will be disabled until the virtual junction temperature becomes lower than TTS and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

9. Application Note

9.1. Typical Application

The NSI1150 requires a 0.1 μF bypass capacitors between VDD_1 and GND_1, VDD_2 and GND_2. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor R_{TERM}, whose value matches the characteristic impedance of the cable. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination can be used, as shown in Figure 9.1. It's good practice to have the bus connectors and termination resistor as close as possible to the CANH and CANL pins.

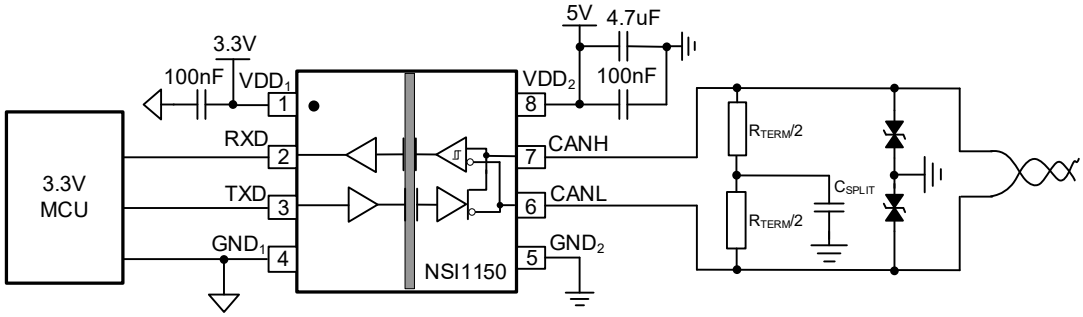
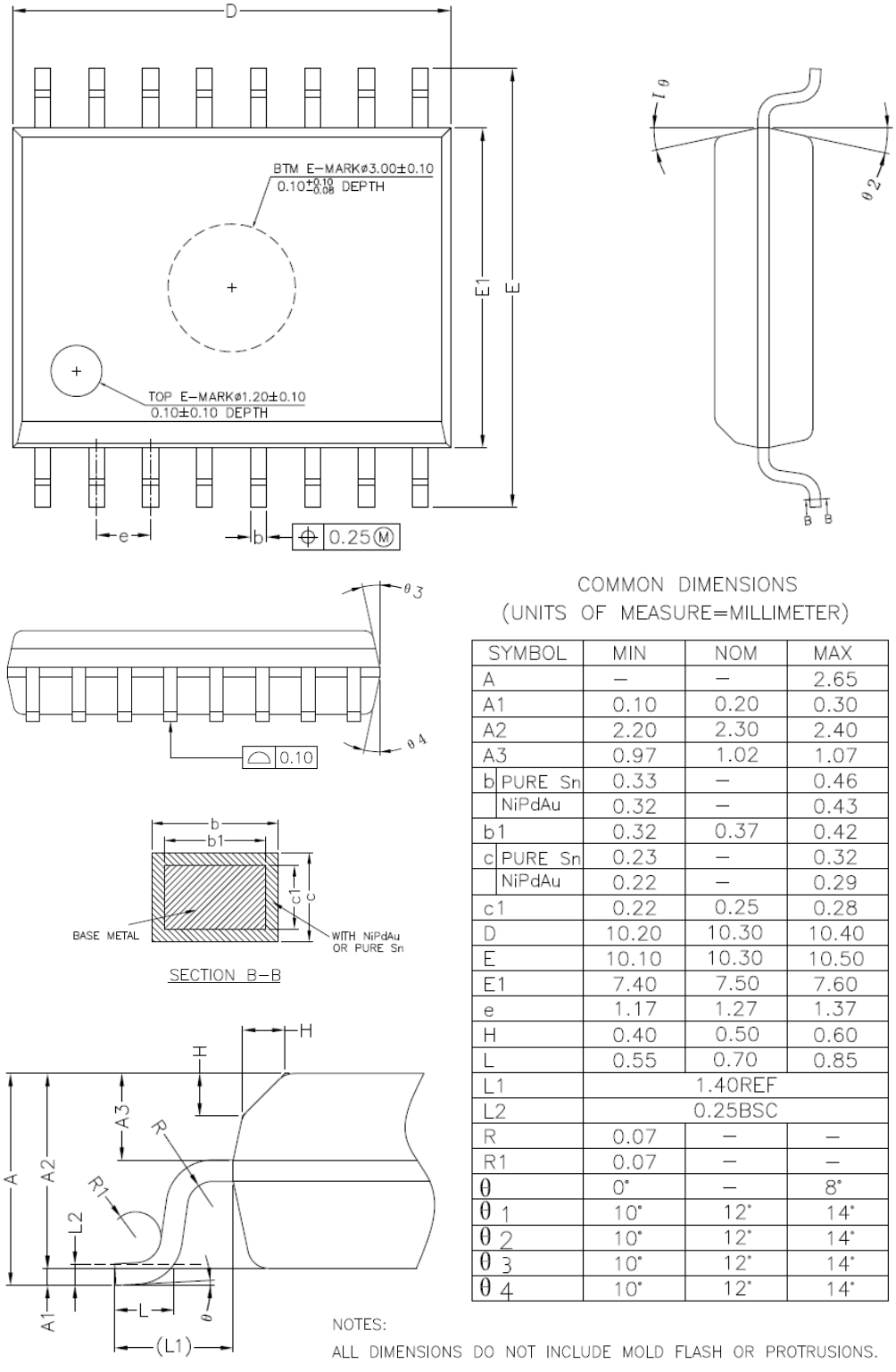


Figure 9.1 Basic schematic of NSI1150

10. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		–	–	2.65
A1		0.10	0.20	0.30
A2		2.20	2.30	2.40
A3		0.97	1.02	1.07
b	PURE Sn	0.33	–	0.46
	NiPdAu	0.32	–	0.43
b1		0.32	0.37	0.42
c	PURE Sn	0.23	–	0.32
	NiPdAu	0.22	–	0.29
c1		0.22	0.25	0.28
D		10.20	10.30	10.40
E		10.10	10.30	10.50
E1		7.40	7.50	7.60
e		1.17	1.27	1.37
H		0.40	0.50	0.60
L		0.55	0.70	0.85
L1		1.40REF		
L2		0.25BSC		
R		0.07	–	–
R1		0.07	–	–
θ		0°	–	8°
θ 1		10°	12°	14°
θ 2		10°	12°	14°
θ 3		10°	12°	14°
θ 4		10°	12°	14°

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOP16(300mil)/ SOW16 Package Shape and Dimension in millimeters

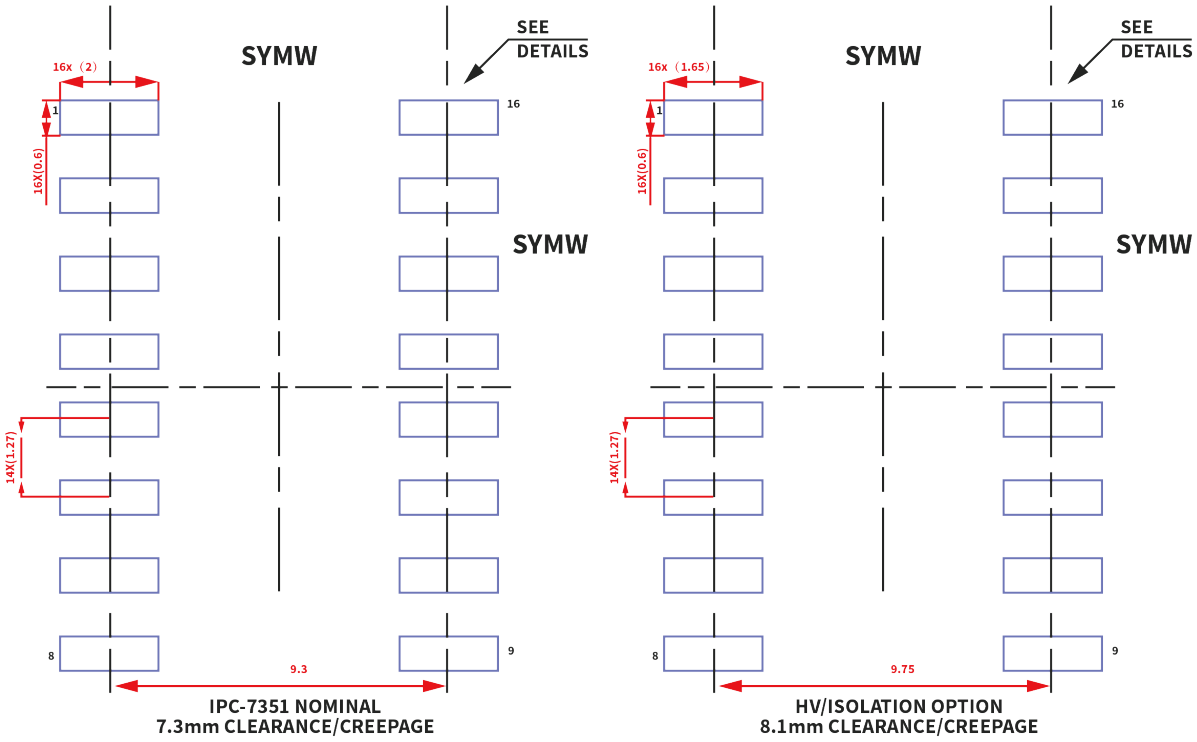
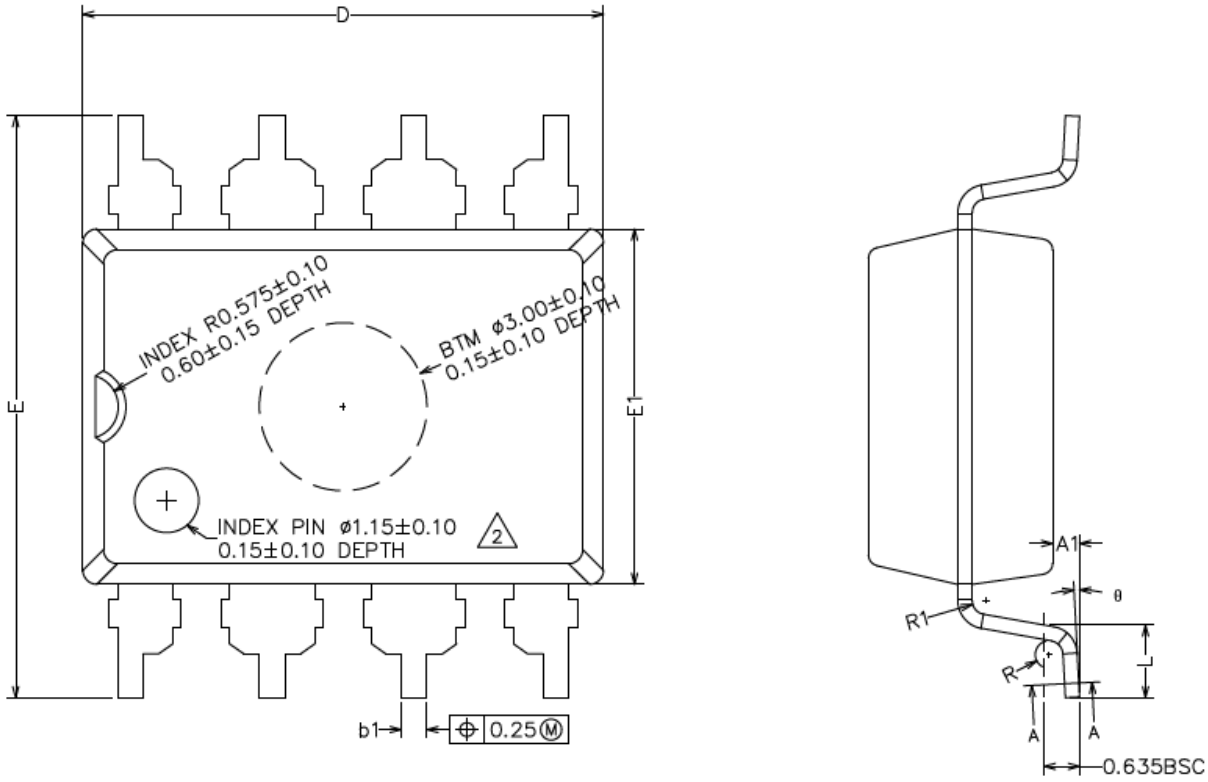
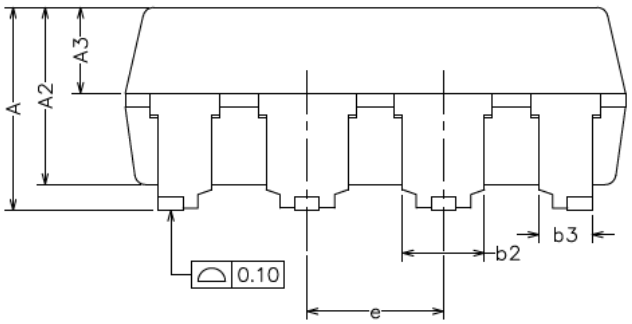
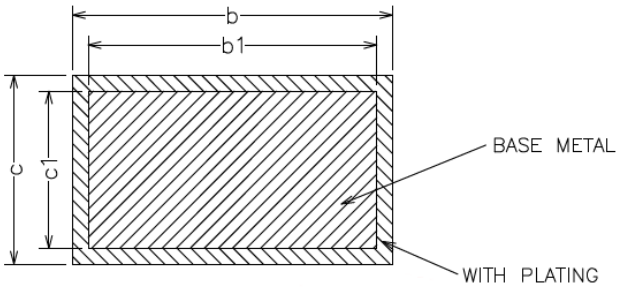


Figure 10.2 SOP16(300mil)/ SOW16 Package Board Layout Example







SECTION

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

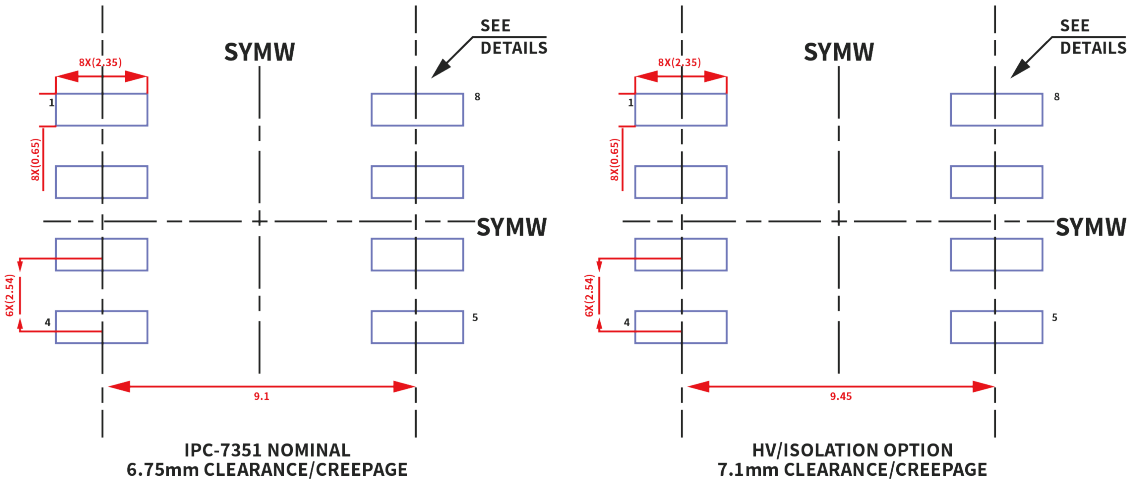
SYMBOL	MIN	NOM	MAX
A	3.58	–	3.98
A1	0.38	0.48	0.58
A2	3.20	3.30	3.40
A3	1.50	1.60	1.70
b	0.42	–	0.56
b1	0.41	0.46	0.51
b2	1.524REF		
b3	0.99REF		
c	0.23	–	0.32
c1	0.22	0.25	0.28
D	9.27	9.32	9.37
E	10.11	10.40	10.69
E1	6.30	6.35	6.40
e	2.44	2.54	2.64
L	1.15	–	1.45
R	0.10	–	–
R1	0.10	–	–
θ	0°	–	8°

NOTES:

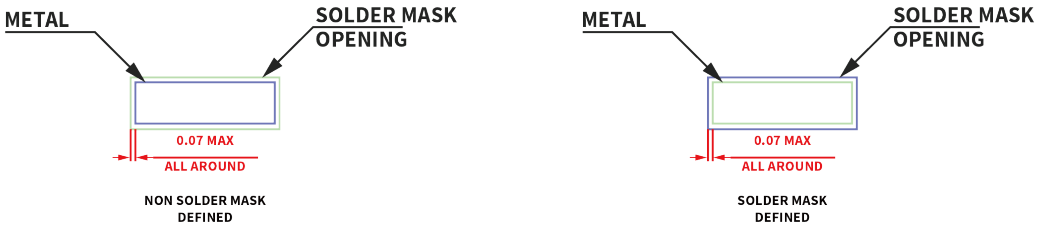
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.3 DUB8 Package Shape and Dimension in millimeters

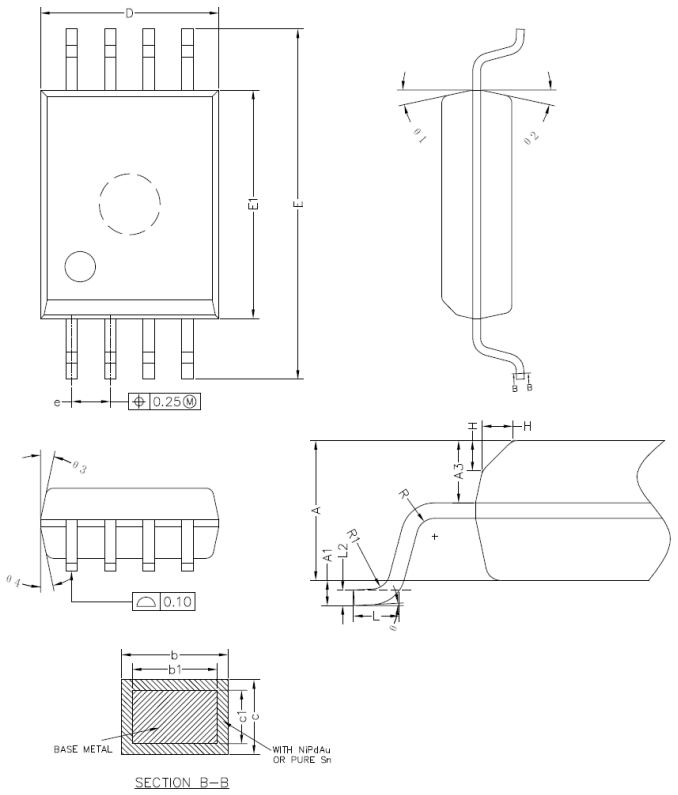


LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 10.4 DUB8 Package Board Layout Example



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

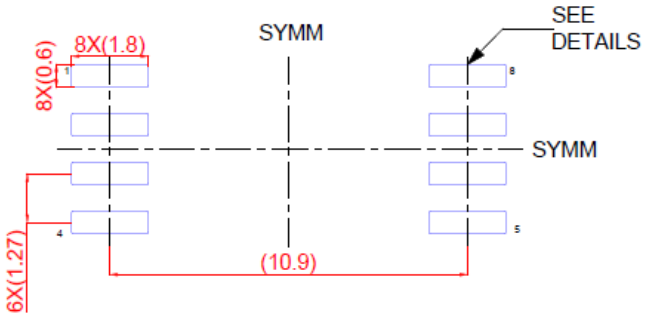
SYMBOL		MIN	NOM	MAX
A		–	–	2.85
A1		0.31	0.41	0.51
A2		2.20	2.30	2.40
A3		0.97	1.02	1.07
b	PURE Sn	0.33	–	0.47
	NiPdAu	0.33	–	0.44
b1		0.33	0.38	0.43
c	PURE Sn	0.22	–	0.32
	NiPdAu	0.22	–	0.29
c1		0.22	0.25	0.28
D		5.75	5.85	5.95
E		11.30	11.50	11.70
E1		7.40	7.50	7.60
e		1.17	1.27	1.37
H		0.40	0.50	0.60
L		0.55	0.75	0.90
L1		2.00REF		
L2		0.25BSC		
R		0.07	–	–
R1		0.07	–	–
θ		0°	–	8°
θ 1		10°	12°	14°
θ 2		10°	12°	14°
θ 3		10°	12°	14°
θ 4		10°	12°	14°

NOTES:

1. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. TOP INDEX E-MARK ø1.00±0.10, DEPTH $0.10^{+0.15}_{-0.08}$, BOTTOM E-MARK ø2.00±0.10, DEPTH $0.15^{+0.15}_{-0.13}$.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

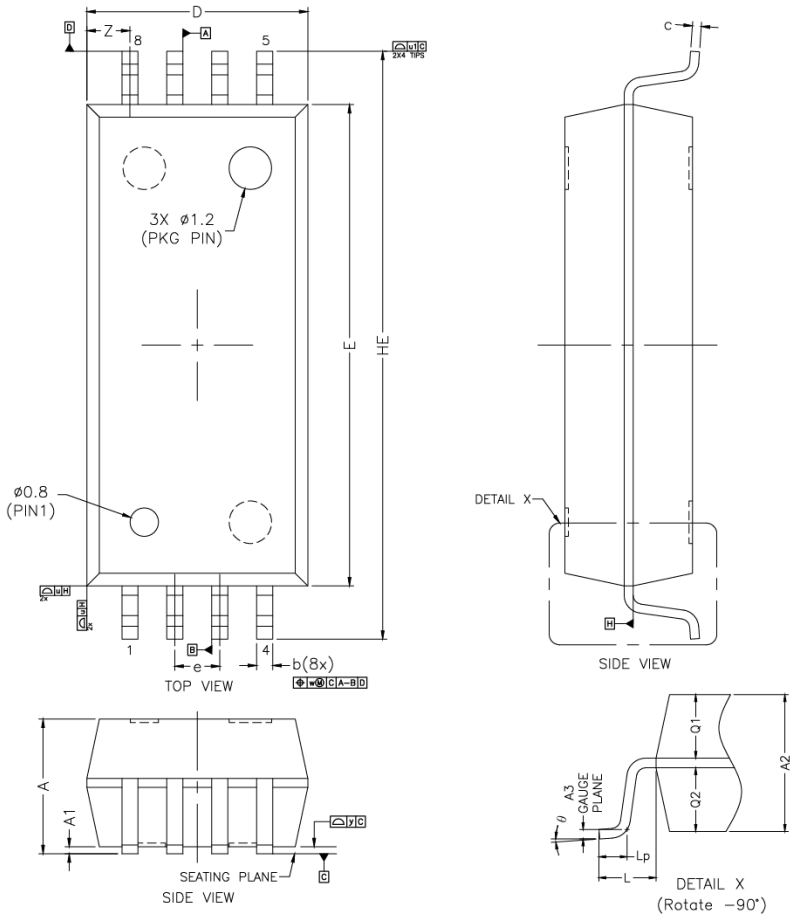
Figure 10.5 SOW8/SOP8(300mil) Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE

SOLDER MASK DETAILS

Figure 10.6 SOW8/SOP8(300mil) Package Board Layout Example



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	3.580	3.807	4.034
A1	0.100	0.200	0.300
A2	3.480	3.607	3.734
b	0.357	0.457	0.557
c	0.254 REF		
D	6.121	6.248	6.375
E	13.473	13.600	13.727
HE	16.36	16.61	16.86
Q1	1.6515	1.6765	1.7015
Q2	1.6515	1.6765	1.7015
e	1.27 BSC		
A3	0.25 REF		
L	1.505 REF		
Lp	0.635	--	1.0
w	0.25		
y	0.10		
u	0.10		
u1	0.20		
Z	1.219		
θ	0°	--	8°

NOTES:
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 PLASTIC OR METAL PROTRUSIONS OF 0.15MM MAXIMUM PER SIDE ARE NOT INCLUDED

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.7 SOWW8/SOP8(600mil) Package Shape and Dimension in millimeters

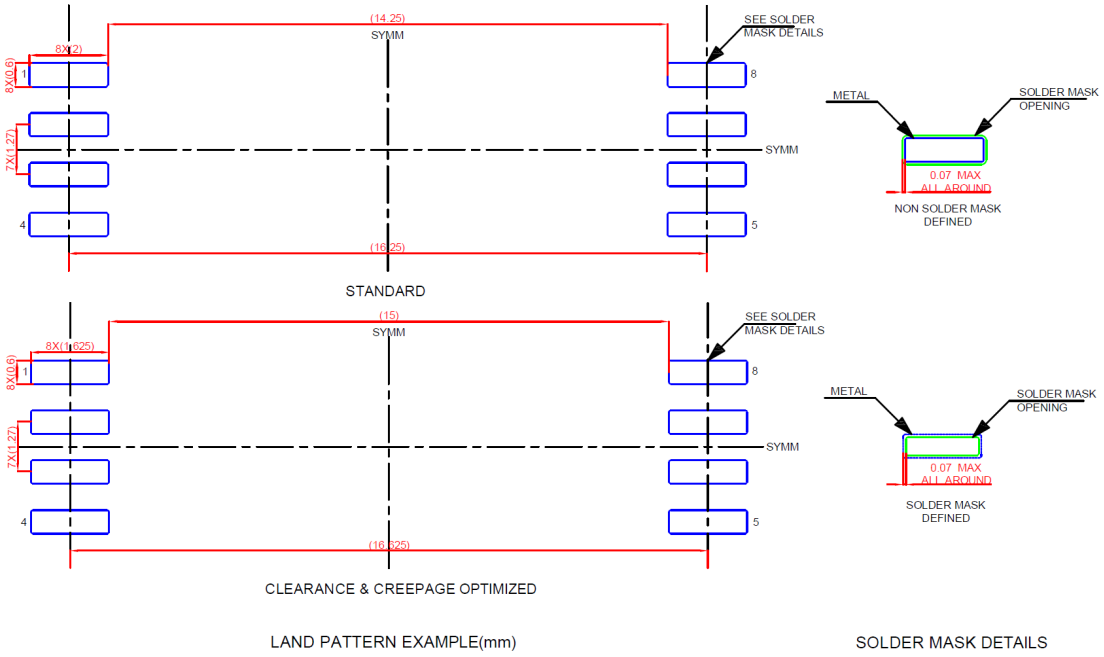
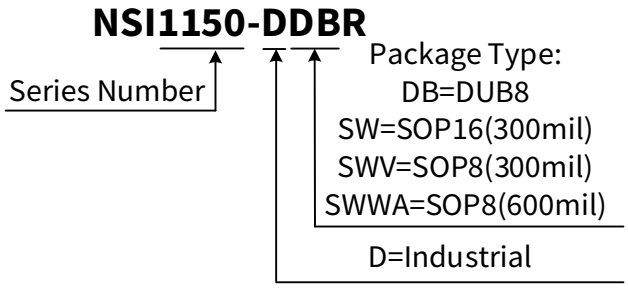


Figure 10.8 SOWW8/SOP8(600mil) Package Board Layout Example

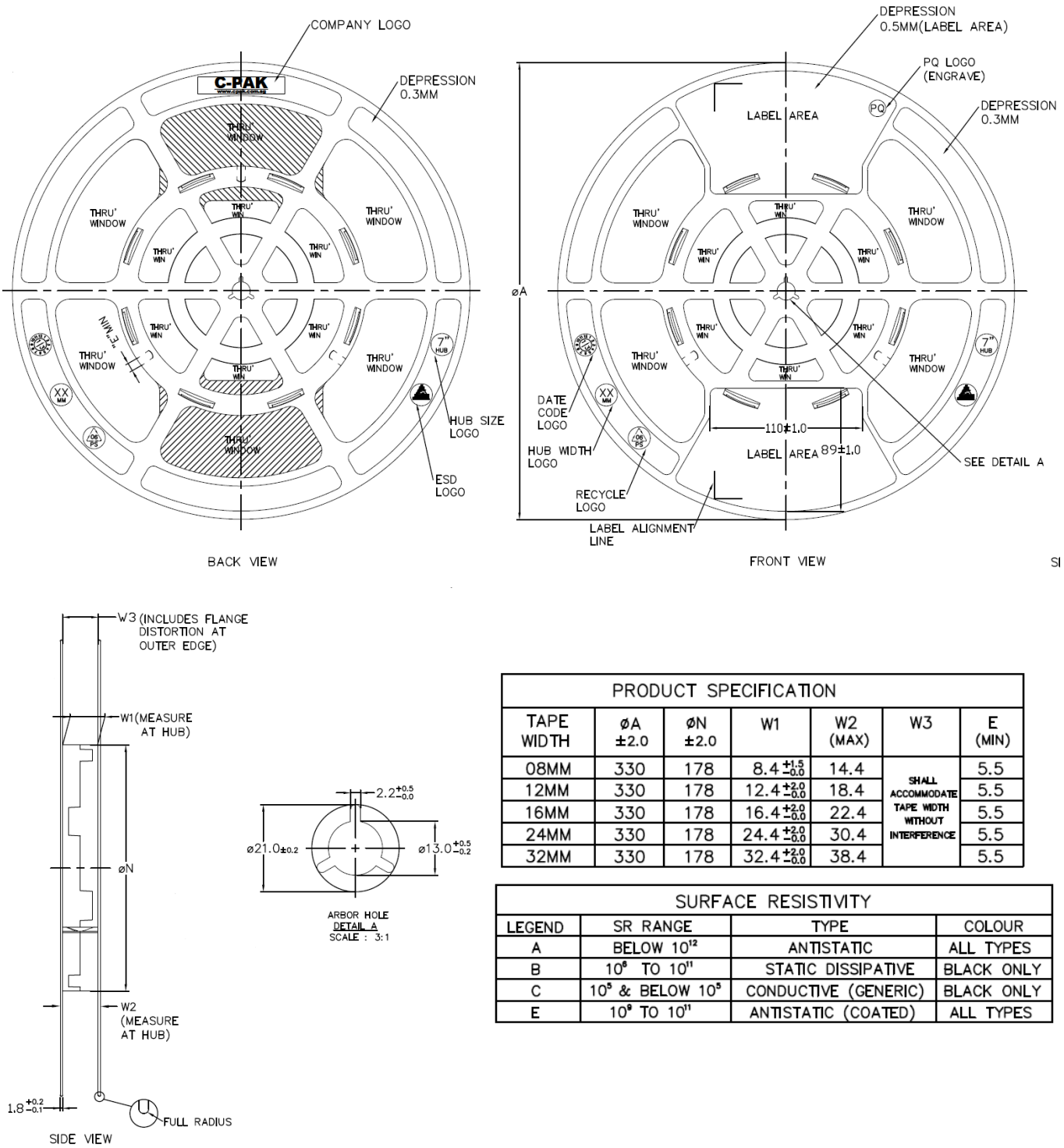
11. Order Information

Orderable Part Number	Isolation Rating (kV)	Max Data Rate (Mbps)	SPQ	MPQ	Package Type	Operating Temperature	MSL
NSI1150-DDBR	3	5	800	800	DUB8	-40 to 125°C	3
NSI1150-DSWR	5	5	1000	1000	SOP16(300mil)	-40 to 125°C	3
NSI1150-DSWVR	5	5	1000	1000	SOP8(300mil)	-40 to 125°C	3
NSI1150-DSWWAR	7.5	5	1000	1000	SOP8(600mil)	-40 to 125°C	3
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.							

Part Number Rule:



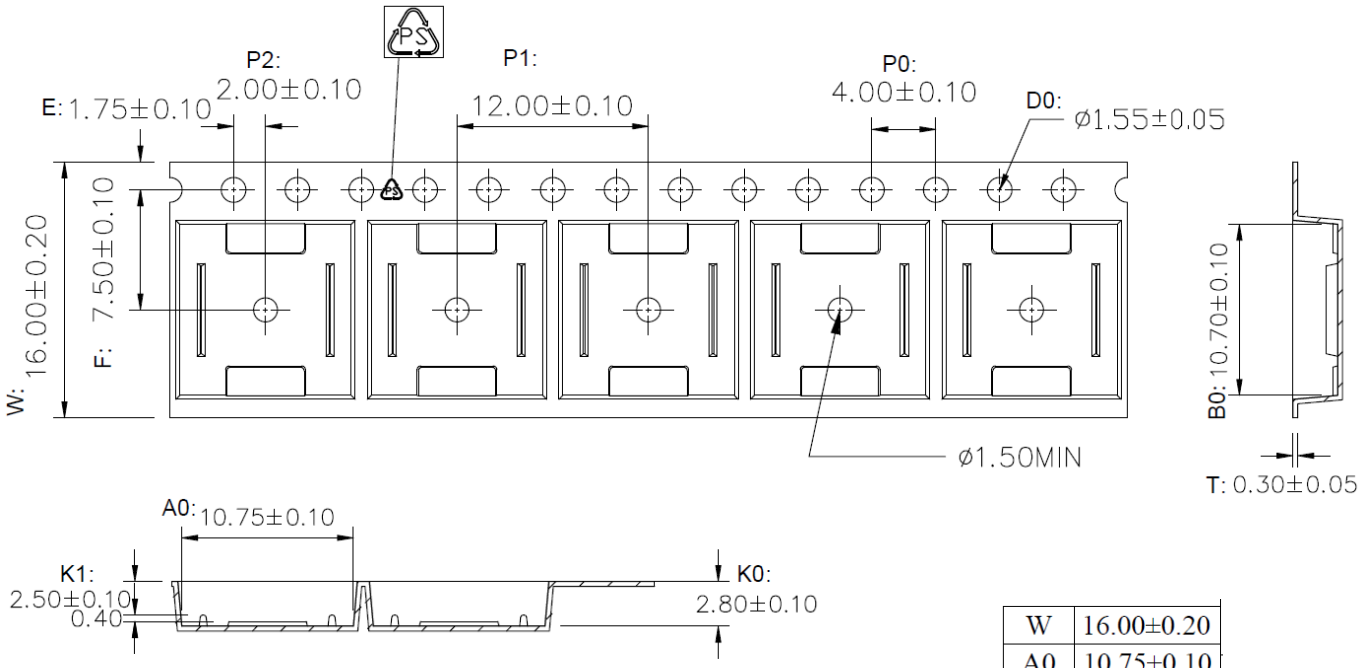
12. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 12.1 Reel Information of SOP16(300mil)/ SOW16 and SOP8(300mil)/ SOW8



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :10^{5} ~ 10^{10}Ω/□

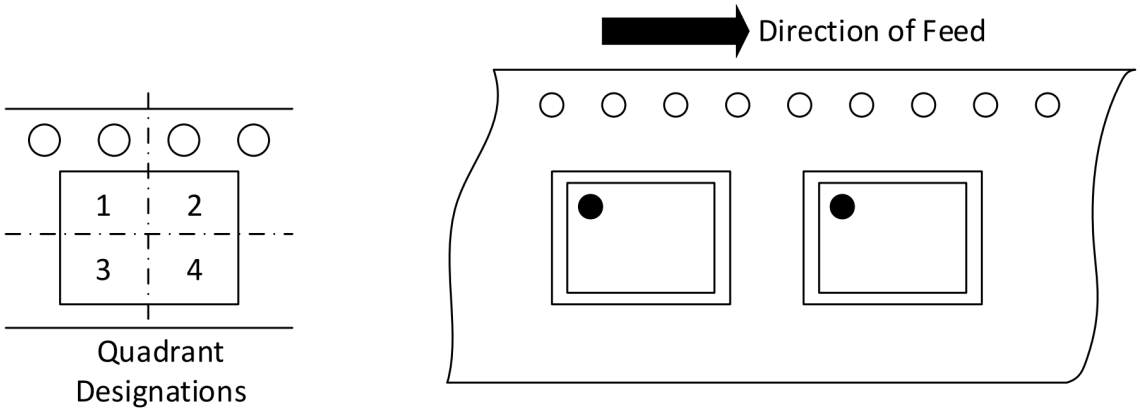


Figure 12.2 Tape Information of SOP16(300mil)/ SOW16

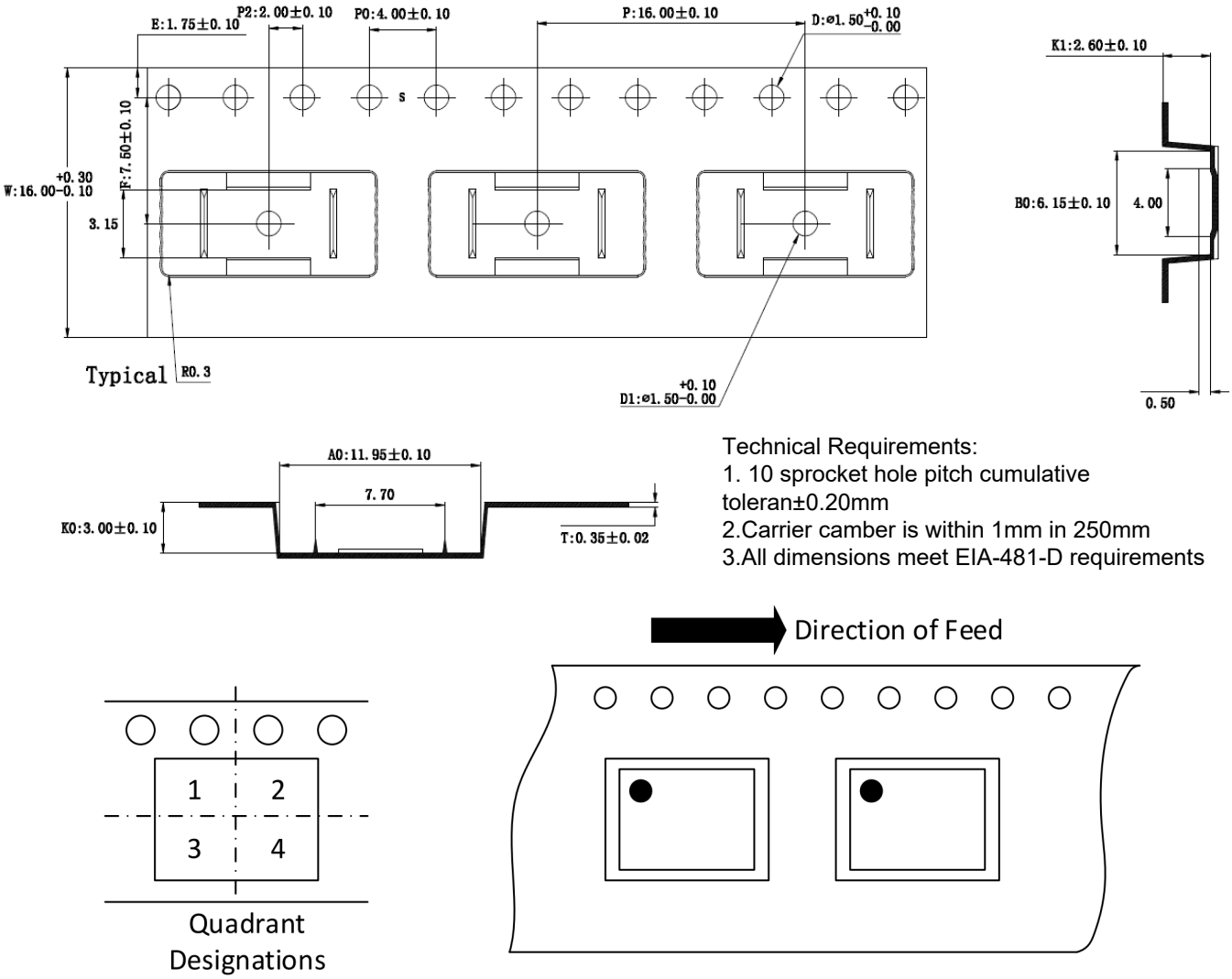
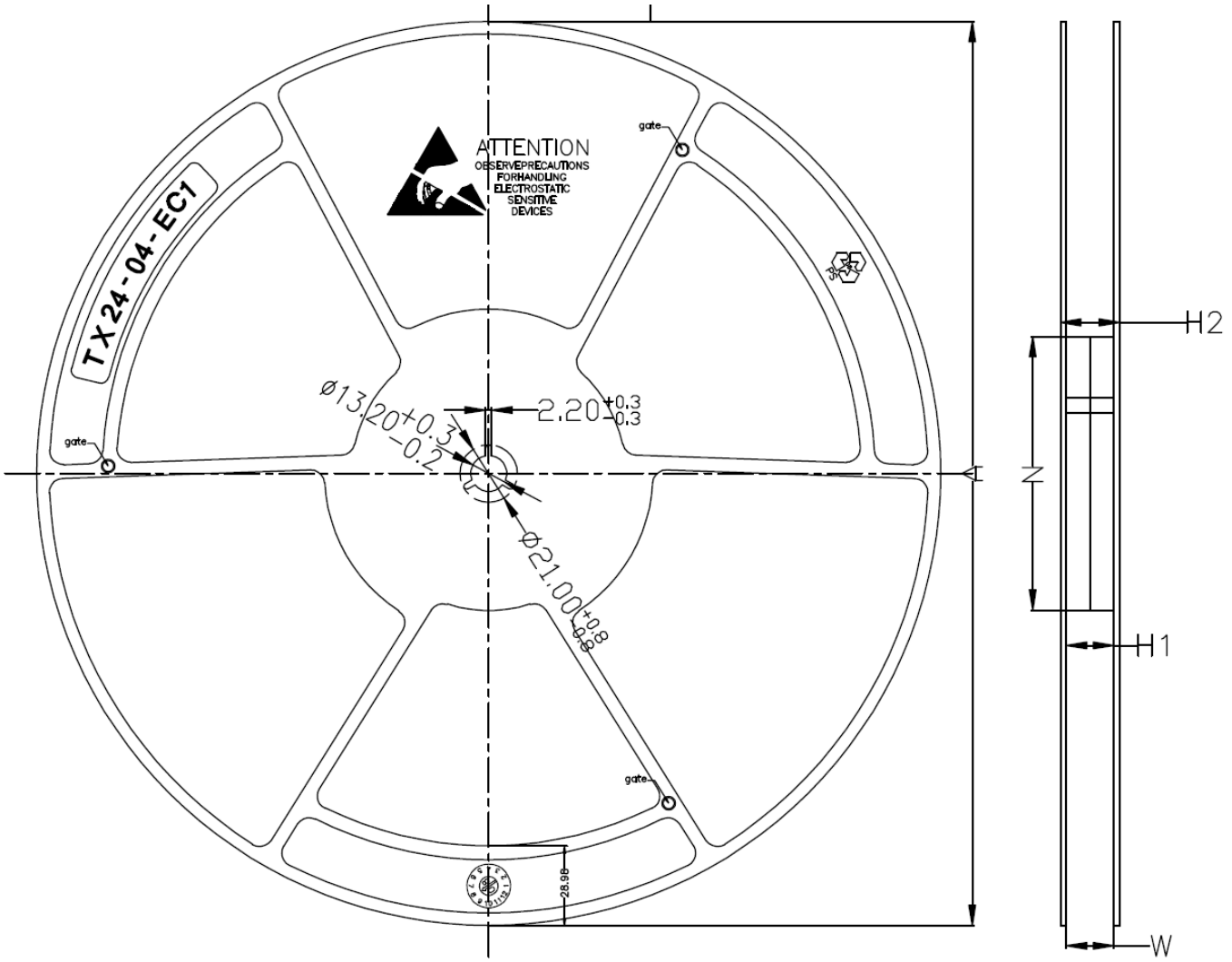


Figure 12.3 Tape Information of SOP8(300mil)/ SOW8



NOTES:
1. MATERIAL: DISSIPATIVE(BLACK)
2. FLANGE WARPAGE: 3 MM MAXIMUM
3. ALL DIMENSIONS ARE IN MM
4. ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5. GENERAL TOLERANCE: ±0.25 MM

PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA $^{+2}_{-2}$	øN $^{+2}_{-2}$	H1 $^{+2}_{-0}$	H2 $^{+1}_{-1}$	W $^{+3.5}_{-0.2}$
24MM	330	100	24.4	28.6	24.4

Figure 12.4 Reel Information of DUB8

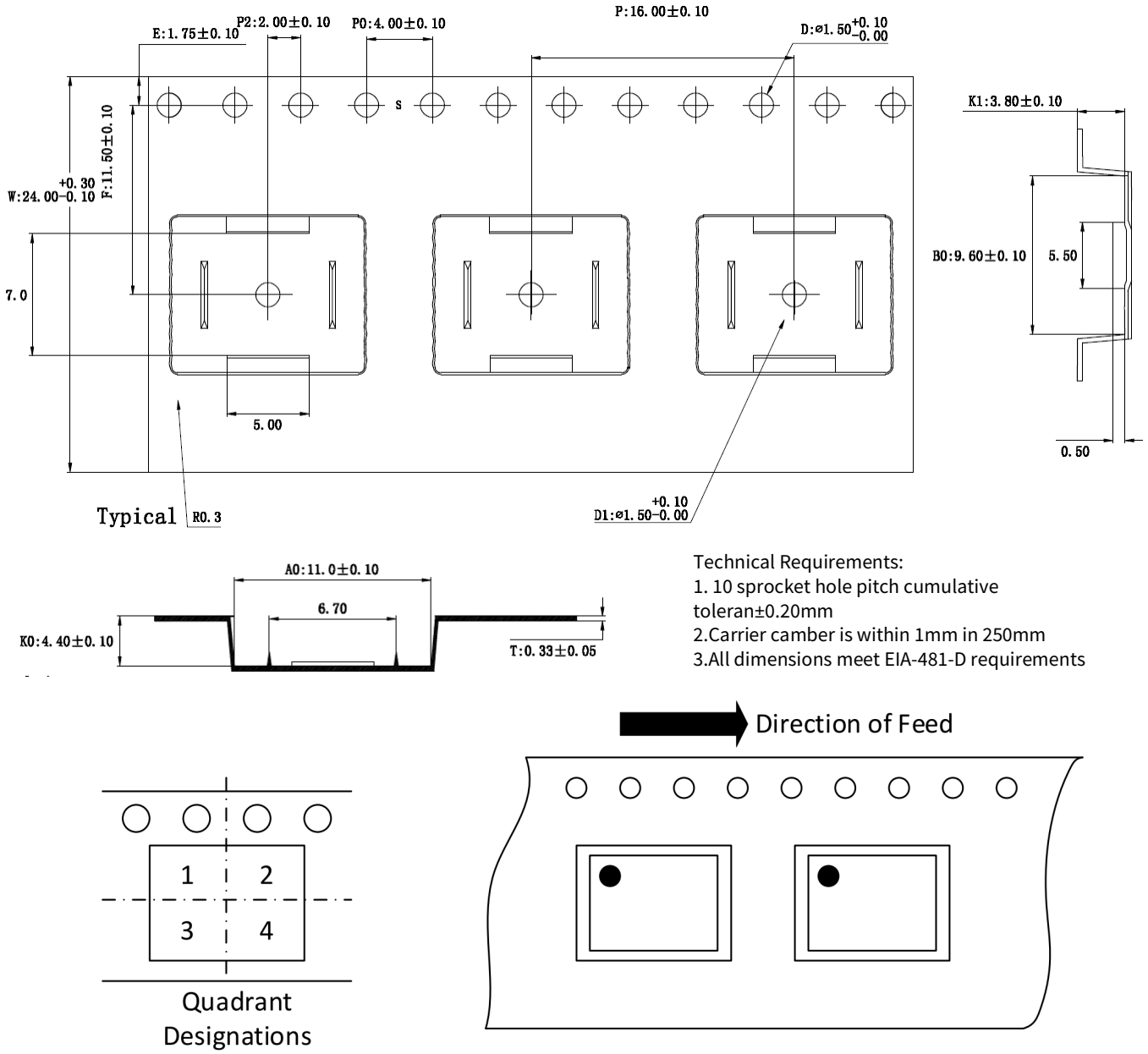
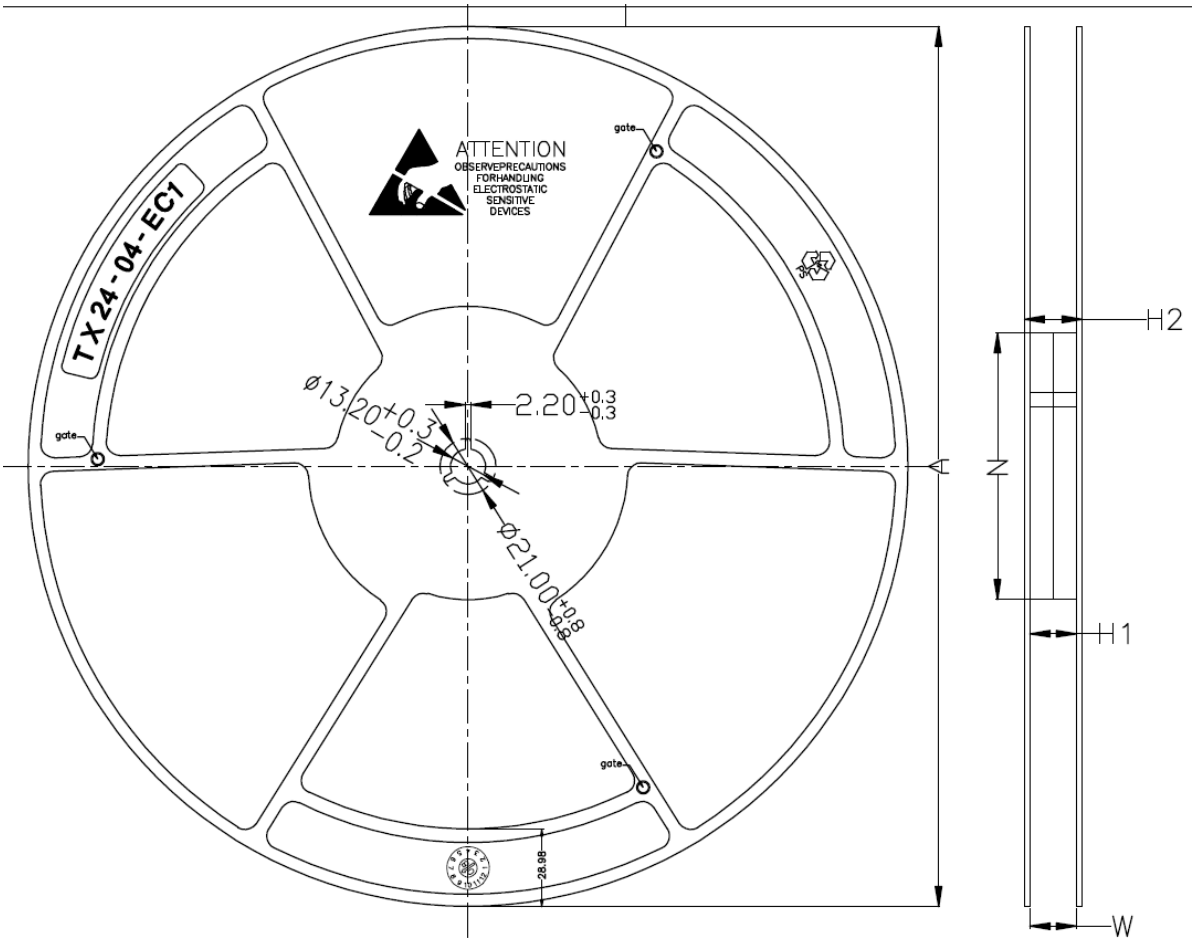


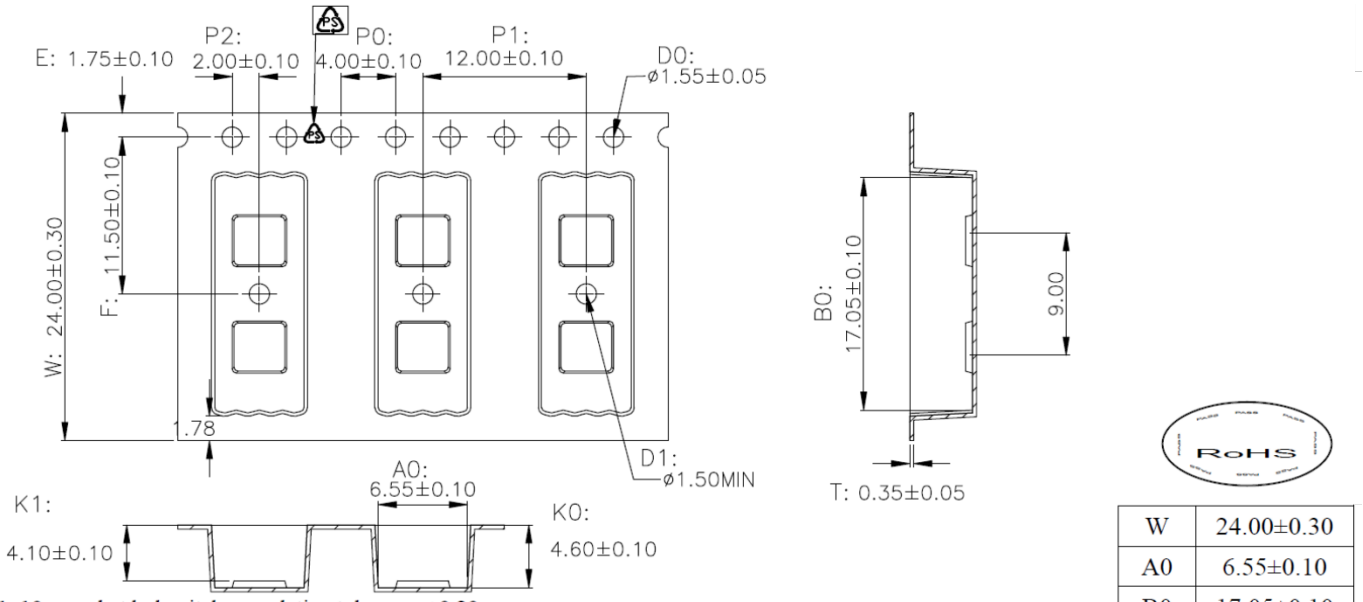
Figure 12.5 Tape Information of DUB8



PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA +2 −2	øN +2 −2	H1 +2 −0	H2 +1 −1	W +3.5 −0.2
24MM	330	100	24.4	28.6	24.4

NOTES:
1.MATERIAL:DISSIPATIVE(BLACK)
2.FLANGE WARPAGE:3 MM MAXIMUM 5
3.ALL DIMENSIONS ARE IN MM
4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5.GENERAL TOLERANCE: ±0.25 MM

Figure 12.6 Reel Information of SOP8(600mil)/ SOWW8



W	24.00±0.30
A0	6.55±0.10
B0	17.05±0.10
K0	4.60±0.10
K1	4.10±0.10

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.35±0.05mm.
6. Packing length per 19" reel :130 Meters. (復卷 1: 10)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : 10^5 ~10^{10} Ω/sq.

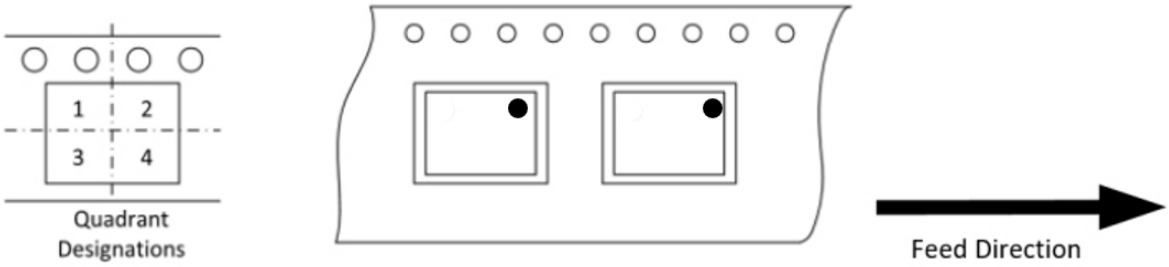


Figure 12.7 Tape Information of SOP8(600mil)/SOWW8

13. Revision History

Revision	*Description*	*Date*
1.0	Initial version.	2025/11/14
1.1	Changes includes: - Added information about NSI1150-DSWVR. - Corrected the annotation information of Figure 6.15.	2026/2/3
1.2	Changes includes: - Added information about NSI1150-DSWWAR. - Updated Regulatory information. - Updated Order Information.	2026/4/8

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