

### Product Overview

The NSDRV401 is an integrated circuit chip designed to control and process signals from magnetic current sensors. The NSDRV401 can adapt to different current sensors and is primarily used for accurately monitoring and measuring alternating current (AC) and direct current (DC).

The NSDRV401 provides an excitation signal for the magnetic field probe, enabling it to detect changes in the magnetic field. It processes the signal from the probe and provides an analog output voltage signal proportional to the primary winding current. It features high-resolution, low-temperature drift measurement performance, making it suitable for applications that require high precision. It supports a wide bandwidth range for various frequency current monitoring. Additionally, it includes overload and fault detection functions, as well as transient noise suppression, to enhance the reliability of measurements and detections.

### Key Features

- Single Supply: 5V
- Excellent DC Precision
- High-Resolution, Low-Temperature Drift
- Built-In Degauss System
- Extensive Fault Detection
- Wide System Bandwidth
- ROHS& REACH Compliance

### Device Information

Part Number	Package	Body Size
NSDRV401-DQCCR	QFN20	5.00 mm × 5.00 mm

### Typical Application

- Photovoltaic Systems
- Frequency and Voltage Inverters
- Motor Drive Controllers
- System Power Consumption

### Functional Block Diagram

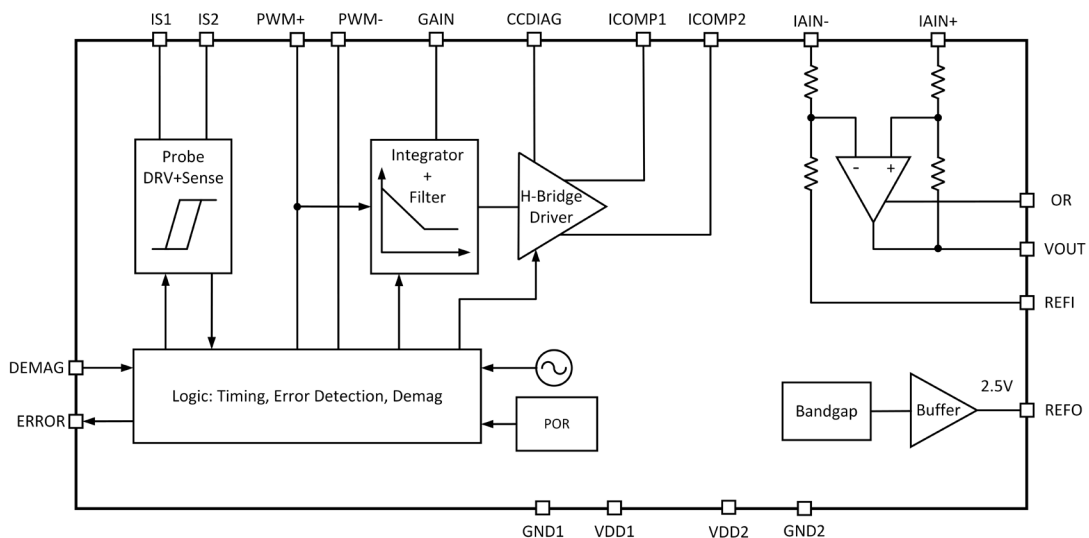


Figure 1. NSDRV401 Functional Block Diagram

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# 1. Pin Configuration and Functions

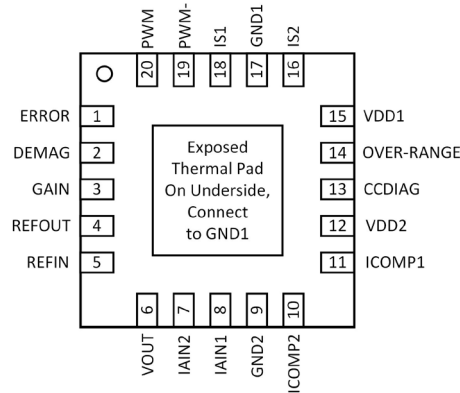


Figure 1-1 NSDRV401 QFN20 Package

Table 1-1 NSDRV401 Pin Configuration and Description

NSDRV401 Pin No.	Symbol	Function
1	ERROR	Error flag: open-drain output, see the Error Conditions section.
2	DEMAG	Control input, see the Demagnetization section.
3	GAIN	Control input for open-loop gain: low = normal, high = -8dB.
4	REFOUT	Output for internal 2.5V reference voltage.
5	REFIN	Input for zero reference to differential amplifier.
6	VOUT	Output for differential amplifier.
7	IAIN2	Noninverting input of differential amplifier.
8	IAIN1	Inverting input of differential amplifier.
9	GND2	Ground connection. Connect to GND1.
10	ICOMP2	Output 2 of compensation coil driver.
11	ICOMP1	Output 1 of compensation coil driver.
12	VDD2	Supply voltage. Connect to VDD1.
13	CCDIAG	Control input for wire-break detection: high = enable.
14	OVER-RANGE	Open-drain output for over-range indication: low = over-range.
15	VDD1	Supply voltage.
16	IS2	Probe connection 2.
17	GND1	Ground connection.
18	IS1	Probe connection 1.
19	PWM-	PWM output from probe circuit (inverted).
20	PWM	PWM output from probe circuit.

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2			7	V	
Storage Temperature	Tstg	-65		150	°C	
Junction Temperature	Tj	-55		150	°C	

## 3. ESD Ratings

Ratings		Value	Unit
Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <ul style="list-style-type: none"> <li>All pins</li> </ul>	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 <ul style="list-style-type: none"> <li>All pins</li> </ul>	±1000	V

## 4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	4.5		5.5	V	
Ambient Temperature	Ta	-40		125	°C	

## 5. Thermal Information

Parameters	Symbol	QFN20	Unit
Junction-to-ambient thermal resistance	$\theta_{JA}$	35.2	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC (top)}$	26.0	°C/W
Junction-to-board thermal resistance	$\theta_{JB}$	11.6	°C/W

## 6. Specifications

### 6.1. Electrical Characteristics

(VDD1=VDD2=5V, Ta=25°C. Unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Unit
<b>DIFFERENTIAL AMPLIFIER</b>		RL = 10kΩ to 2.5V, VREFIN = 2.5V				
Offset Voltage, RTO <sup>1</sup>	V <sub>OS</sub>	Common-Mode Voltage = 2.5V		±10	±50	μV
Offset Voltage Drift, RTO <sup>1 2</sup>	dV <sub>OS</sub> /dT	T <sub>A</sub> = -40°C to +125°C		±0.1	±1	μV/°C
Offset Voltage vs Common-Mode, RTO <sup>1</sup>	CMRR	-1V to +6V, V <sub>REF</sub> = 2.5V		±30	±180	μV/V
Offset Voltage vs Power-Supply, RTO <sup>1</sup>	PSRR	V <sub>REF</sub> not included		±8	±30	μV/V
Common-Mode Input Voltage Range	V <sub>CM</sub>		-1		+6	V
Signal Over-Range Indication (OVER-RANGE), Delay		V <sub>IN</sub> = 1V Step		3		μs
Voltage Output Swing from Negative Rail		I = +2.5mA		50	80	mV
Voltage Output Swing from Positive Rail		I = -2.5mA		50	80	
Short-Circuit Current	I <sub>SC</sub>	V <sub>OUT</sub> Connected To GND/VDD		23		mA
Gain, V <sub>OUT</sub> /V <sub>IN_DIFF</sub>				4		V/V
Gain Error	GE			±0.02	±0.3	%
Gain Error Drift				±0.5		ppm/°C
Linearity Error		R <sub>L</sub> = 1kΩ		10		ppm
Bandwidth	-3dB BW			2		MHz
Slew Rate	SR	CMVR = -1V to = +4V		8.5		V/μs
Settling Time, Large-Signal		dV ± 2V to 1%		0.9		μs
Settling Time		dV ± 0.4V to 0.01%		14		μs
Differential Input Resistance			16	19	22	kΩ
Common-Mode Input Resistance			44	50	56	kΩ
Output Voltage Noise Density, f = 1kHz, RTO <sup>1</sup>				160		nV/√Hz

<sup>1</sup> Parameter value referred to output (RTO).

<sup>2</sup> Not production tested, guaranteed by characterization results.

**Electrical Characteristics (continued)**

(VDD1=VDD2=5V, Ta=25°C. Unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Unit
<b>PROBE COIL LOOP</b>						
Input Voltage Clamp Range			-0.7 to VDD + 0.7			V
Resistance Mismatch Between IS1 and IS2		ppm of R <sub>HIGH</sub> + R <sub>LOW</sub>	150	700		ppm
Total Input Resistance			135	200		Ω
Comparator Threshold Current			23	27	31	mA
Minimum Probe Loop Half-Cycle			260	280	300	ns
Probe Loop Minimum Frequency			250			kHz
No Oscillation Detect (Error) Suppression			32			μs
<b>COMPENSATION LOOP</b>						
Offset Error		Probe f = 430kHz, R <sub>LOAD</sub> = 20Ω Deviation from 50% PWM, Pin Gain = L	0.03			%
Offset Error Drift <sup>1</sup>		T <sub>A</sub> = -40°C to +125°C	7.5			ppm/°C
Gain, Pin Gain = L <sup>1</sup>		V <sub>ICOMP1</sub>   -  V <sub>ICOMP2</sub>	-200	25	200	ppm/V
Power-Supply Rejection Ratio, PSRR		Probe Loop f = 430kHz	300			ppm/V
Open-Loop Gain, Two Modes, 7.8kHz		Pin Gain H/L	24/32			dB
Peak Current		V <sub>ICOMP1</sub> - V <sub>ICOMP2</sub> = 4.0VPP	250			mA
Voltage Swing		R <sub>LOAD</sub> = 20Ω	4.2			V
Output Common-Mode Voltage			VDD2/2			V
Wire Break Detect, Threshold Current		I <sub>COMP1</sub> and I <sub>COMP2</sub> Railed	30			mA
<b>VOLTAGE REFERENCE</b>						
Output Voltage		No Load	2.495	2.5	2.505	V
Temperature Drift <sup>1</sup>	dV <sub>OUT</sub> /dT	T <sub>A</sub> = -40°C to 125°C	±5			±50 ppm/°C
Line Regulation		4.5V ≤ V <sub>IN</sub> ≤ 5.5V	±60			±180 μV/V

<sup>1</sup> Not production tested, guaranteed by characterization results.

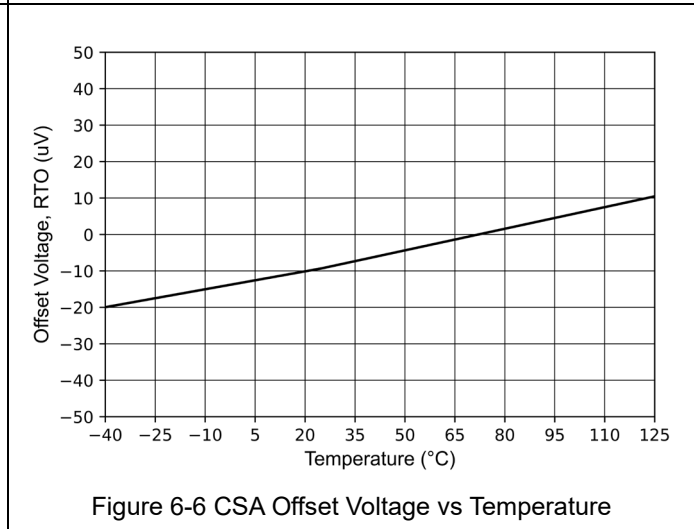
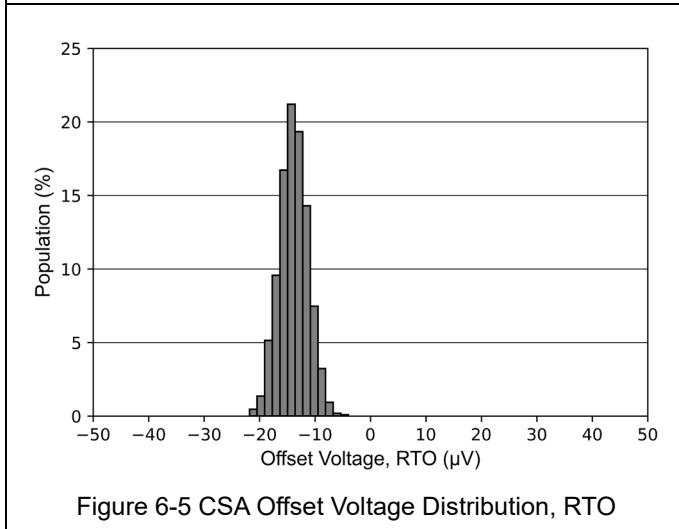
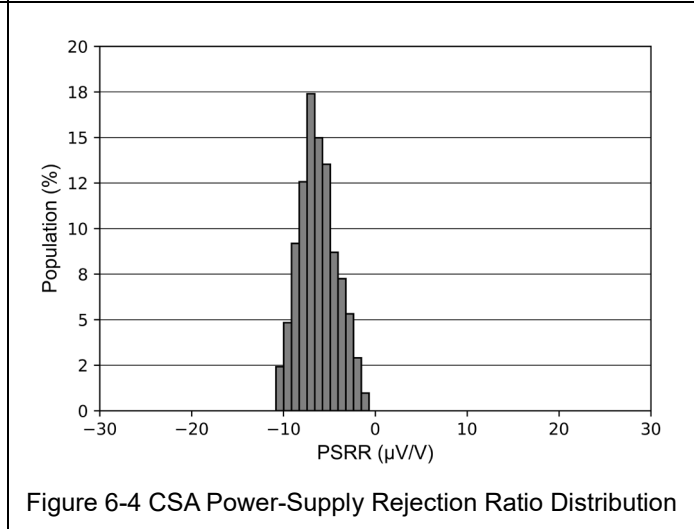
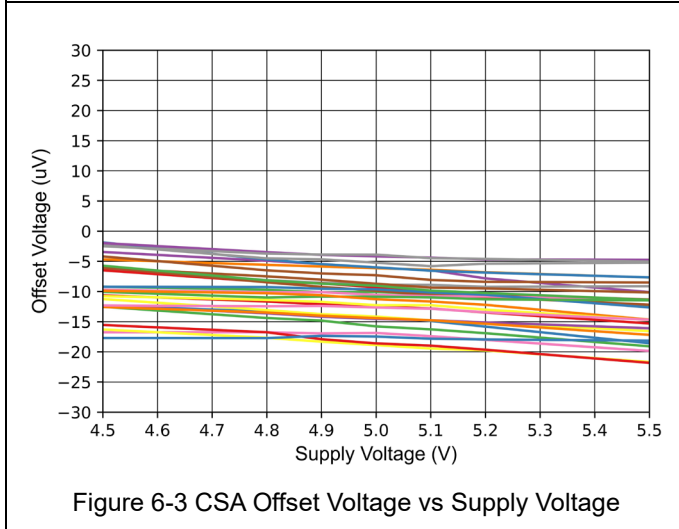
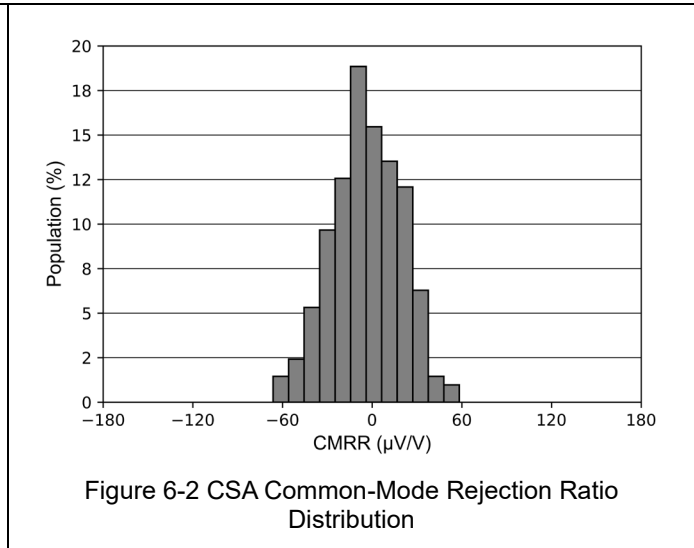
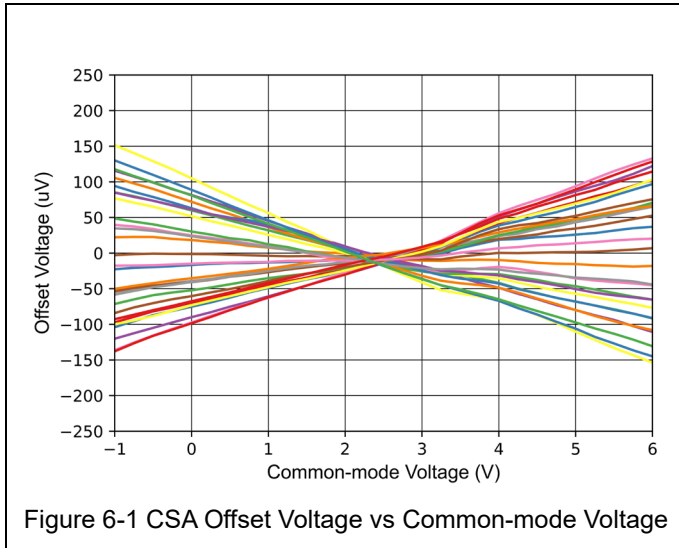
**Electrical Characteristics (continued)**

(VDD1=VDD2=5V, Ta=25°C. Unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Unit
<b>VOLTAGE REFERENCE</b>						
Load Regulation		Load to GND, dI = 0mA to 5mA	±15			µV/mA
		Load to VDD, dI = 0mA to 5mA	±45			µV/mA
Short-Circuit Current		REFOUT Connected to VDD	20			mA
		REFOUT Connected to GND	18			mA
<b>DEMAGNETIZATION</b>						
Duration			106	130		ms
<b>DIGITAL I/O (CCDIAG, DEMAG AND GAIN Pins)</b>						
Pull-Up Low Current (CCdiag, Demag)		0V < VIN < 1.5V	2			µA
Pull-Up High Current (CCdiag, Demag)		3.5V < VIN < 5V	3			µA
Logic Input Leakage Current (Gain)		0V < VIN < VDD	0.05	5		µA
Logic Level, Input: L/H			2.1/2.8			V
Hysteresis			0.7			V
<b>OUTPUTS (ERROR AND OVER-RANGE Pins)</b>						
Logic Level, Output: L		4mA Sink	0.3			V
Logic Level, Output: H			No Internal Pull-up			
<b>POWER SUPPLY</b>						
Specified Voltage Range	VDD	ICOMP = 0mA, Sensor Not Connected	4.5	5	5.5	V
Power-On Reset Threshold	VRST		1.8			V
Quiescent Current [I(VDD1) + I(VDD2)]	IQ		7	8.5		mA
Brownout Voltage Level			4			V
Brownout Indication Delay			100			µs

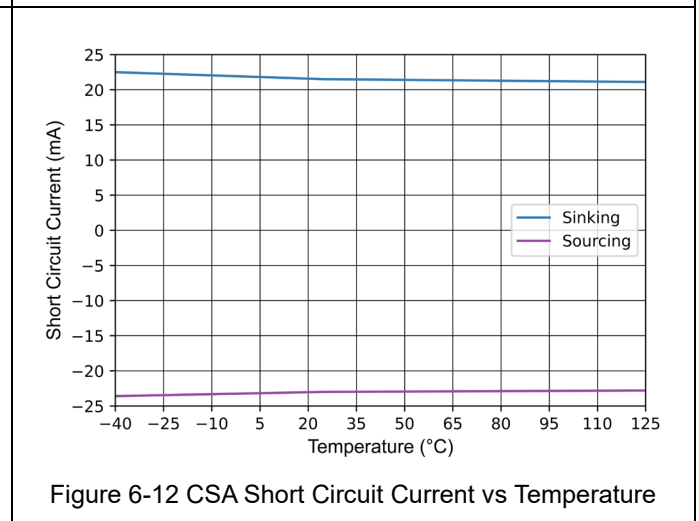
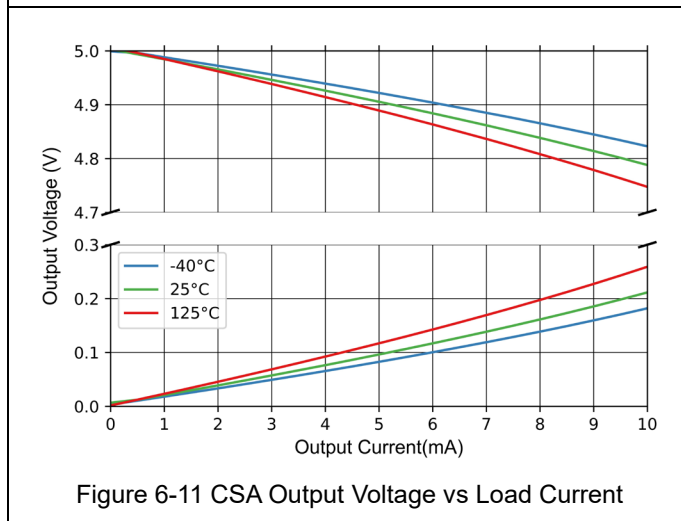
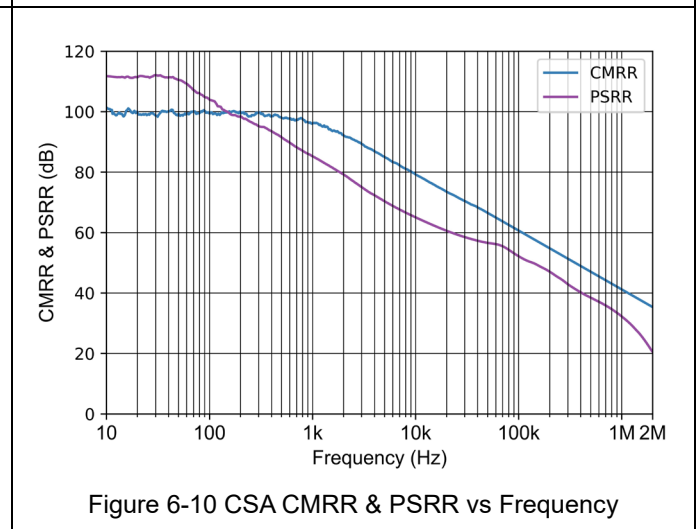
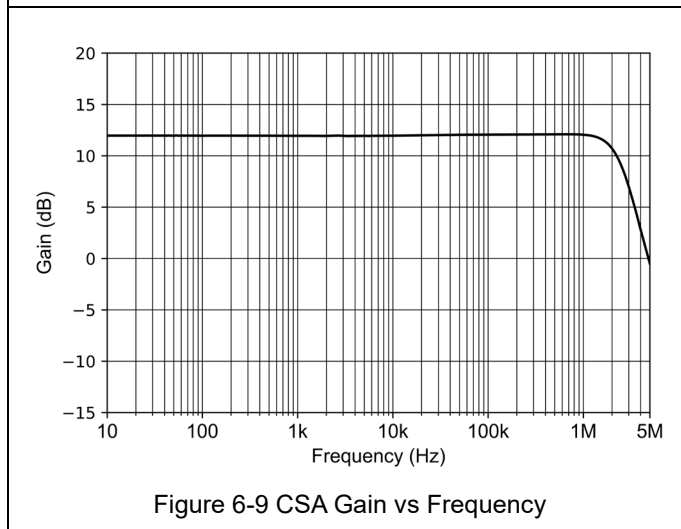
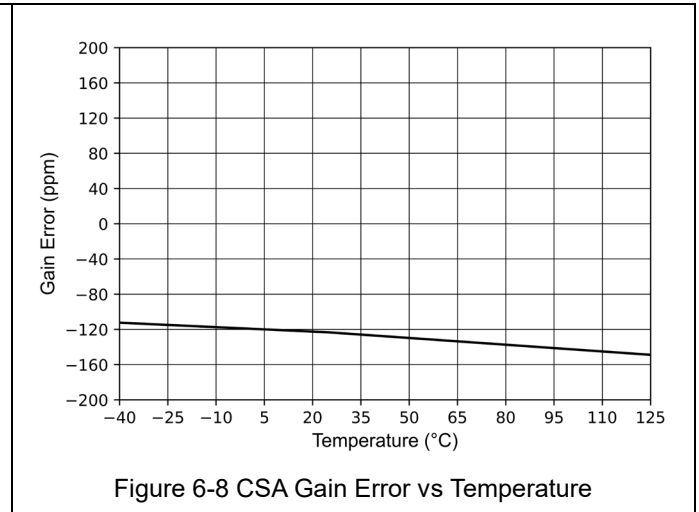
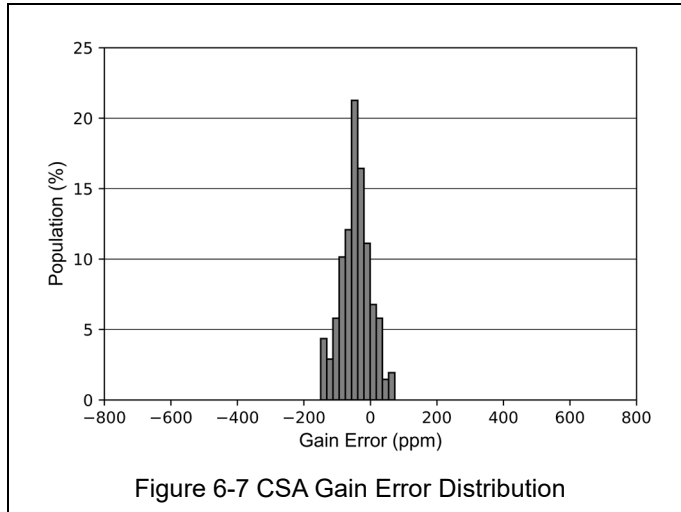
### 6.2. Typical Performance Characteristics

(VDD1=VDD2=5V, Ta=25°C. Unless otherwise noted)



Typical Performance Characteristics (continued)

(VDD1=VDD2=5V, Ta=25°C. Unless otherwise noted)



Typical Performance Characteristics (continued)

(VDD1=VDD2=5V, Ta=25°C. Unless otherwise noted)

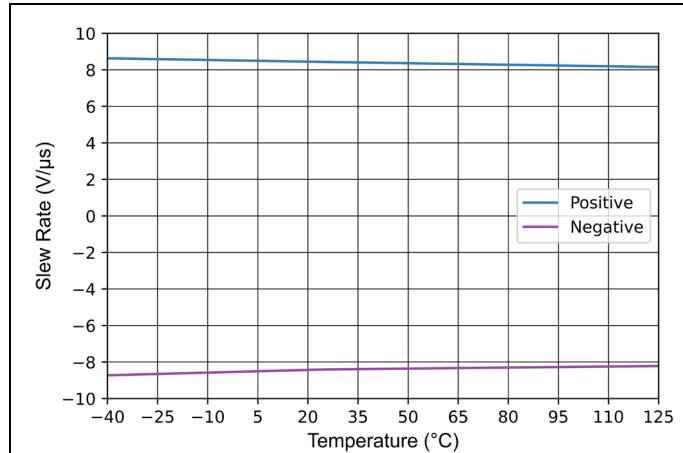


Figure 6-13 CSA Slew Rate vs Temperature

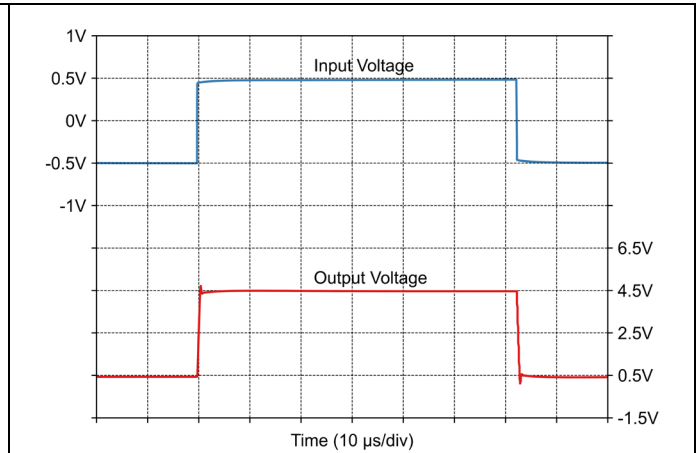


Figure 6-14 CSA Step Response

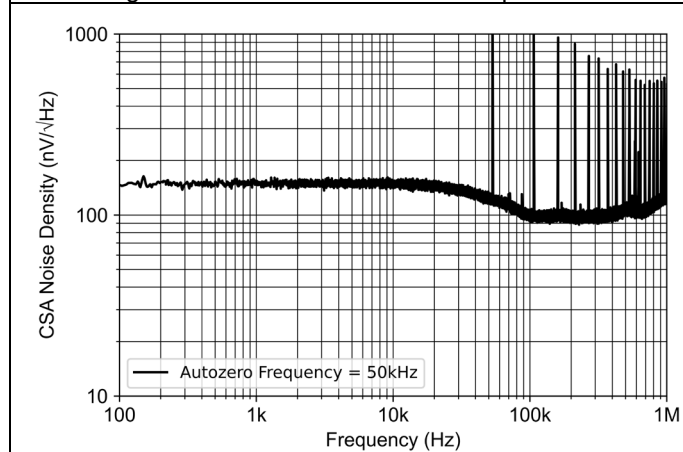


Figure 6-15 CSA Output Voltage Noise Density

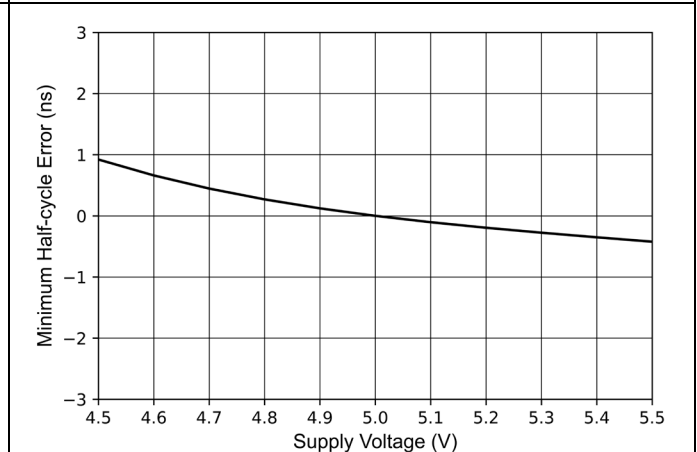


Figure 6-16 Minimum Half-cycle Error vs Supply Voltage

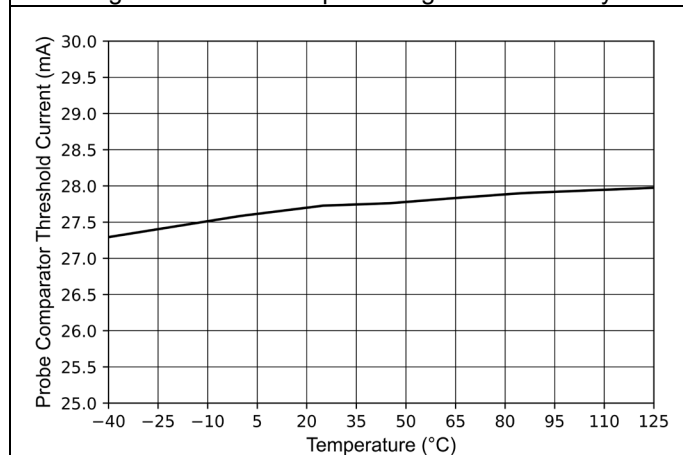


Figure 6-17 Probe Comparator Threshold Current vs Temperature

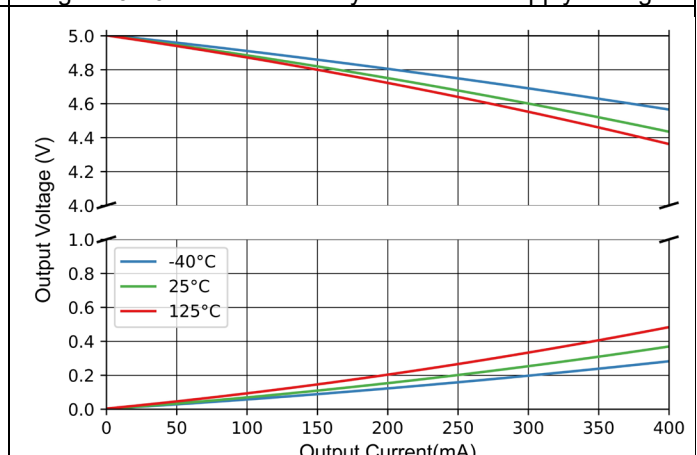


Figure 6-18 Compensation Loop Output Voltage vs Load Current

Typical Performance Characteristics (continued)

(VDD1=VDD2=5V, Ta=25°C. Unless otherwise noted)

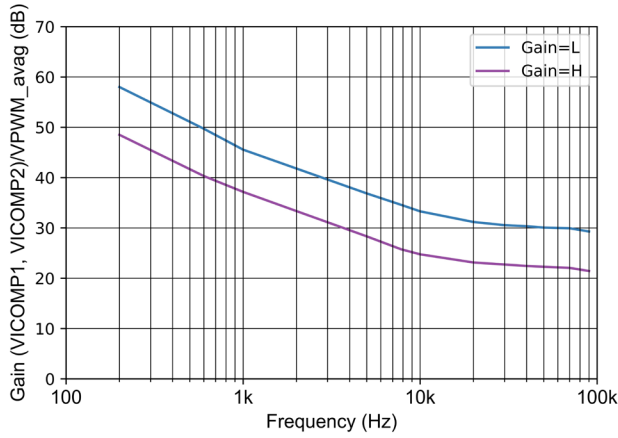


Figure 6-19 Compensation Loop Gain vs Frequency

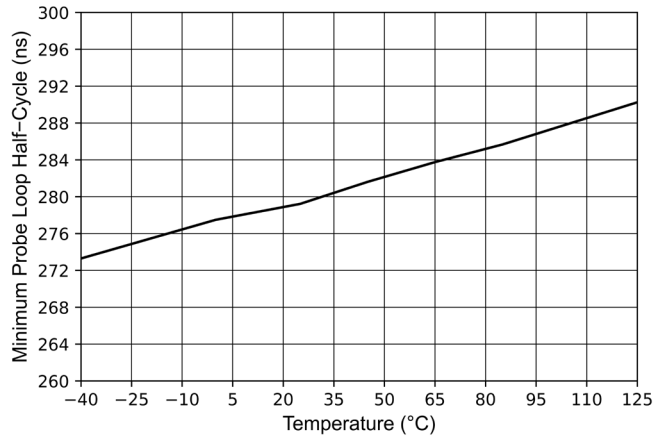


Figure 6-20 Minimum Probe Loop Half-Cycle vs Temperature

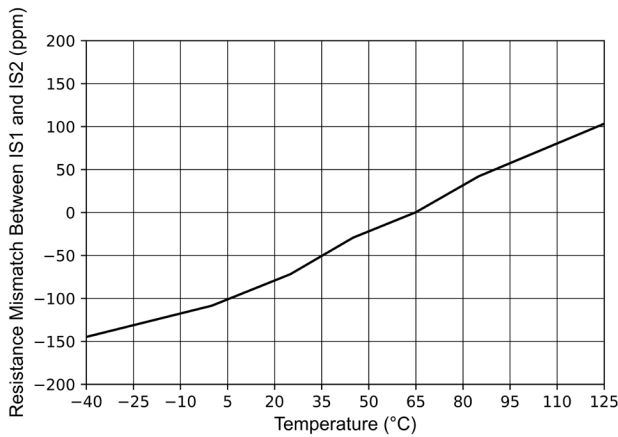


Figure 6-21 Resistance Mismatch vs Temperature

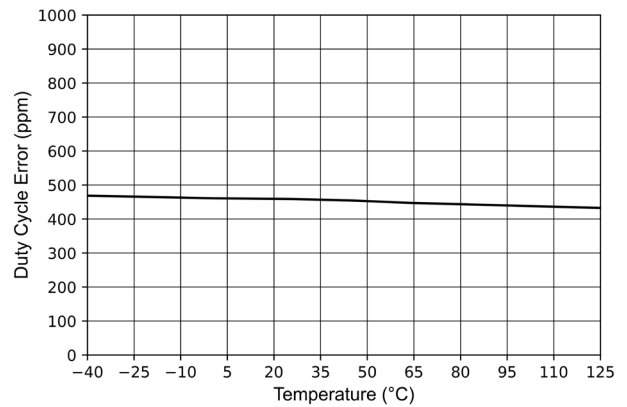


Figure 6-22 Duty Cycle Error vs Temperature

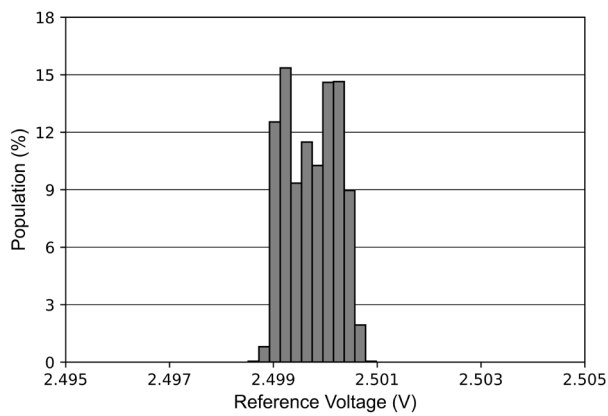


Figure 6-23 Reference Voltage Distribution

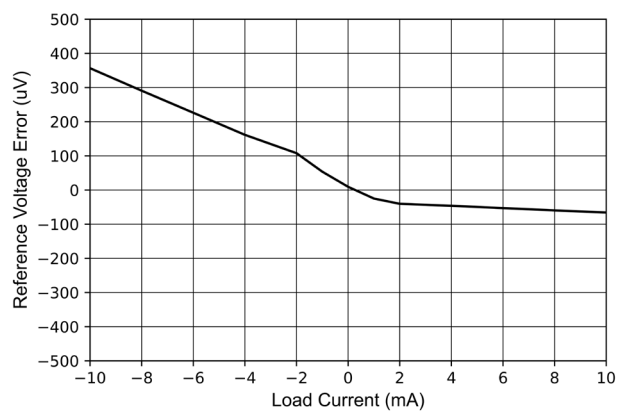
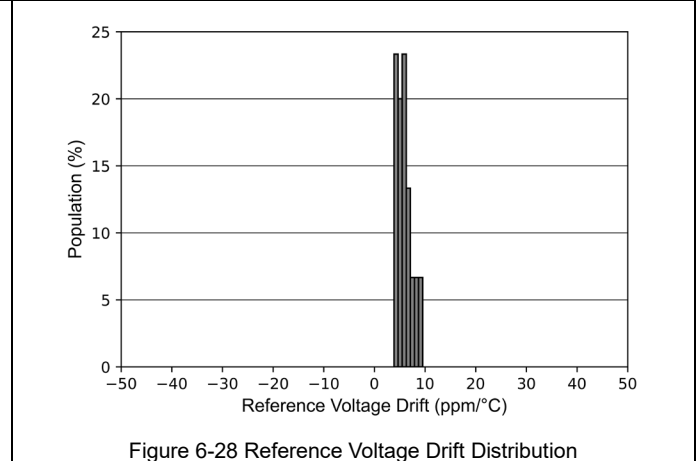
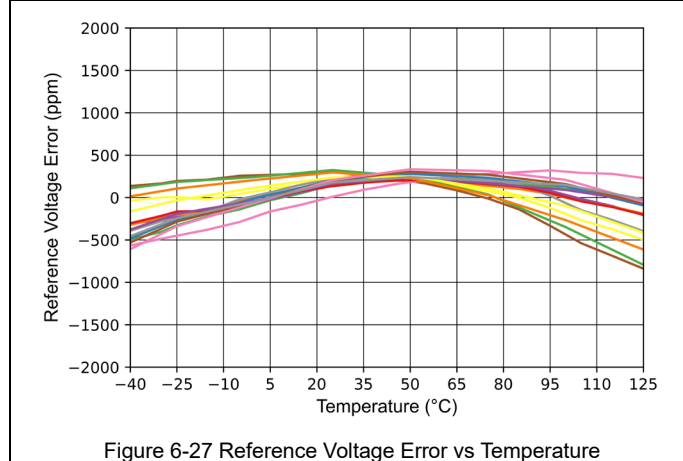
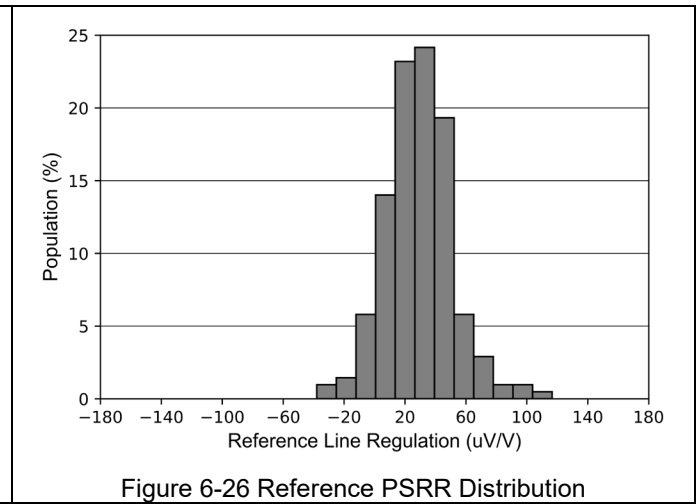
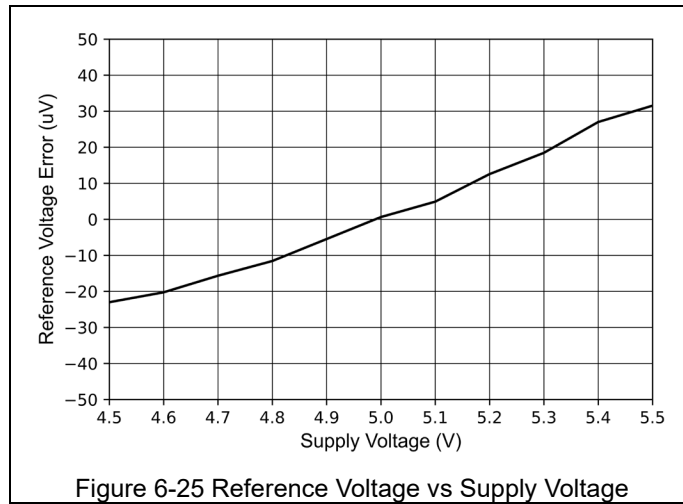


Figure 6-24 Reference Voltage vs Load Current

**Typical Performance Characteristics (continued)**

(VDD1=VDD2=5V, Ta=25°C. Unless otherwise noted)



## 7. Application Note

### 7.1. Functional Overview

The NSDRV401 delivers a complete sensor signal conditioning circuit that directly interfaces with closed-loop fluxgate current sensors, providing all necessary functionalities for sensor operation. It enables non-contact current measurement with broadband frequency coverage including DC, featuring excellent electrical isolation, high resolution, high accuracy, and high reliability.

In DC and low-frequency ranges, the current in the primary winding generates a magnetic field compensated by current flowing through the compensation winding. A magnetic field probe located in the magnetic core loop detects flux and processes the signal to drive the H-bridge compensation driver, which generates compensation coil current. The compensation coil current produces counteracting flux to nullify the primary current-induced flux, maintaining zero total flux. The compensation current is proportional to the primary current and related to the winding ratio. At high frequencies, the compensation winding acts as a current transformer secondary. While the H-bridge driver is disabled, providing low output impedance.

The current-sense amplifier detects the voltage across a shunt resistor in the compensation loop. Its output voltage is referenced to the REFIN voltage, which can be supplied by the internal voltage reference.

### 7.2. Magnetic Probe (Sensor) Interface

The magnetic probe consists of an inductor wound on a soft magnetic core, connected between the IS1 and IS2 pins. During operation, the NSDRV401 initially applies a voltage across IS1 and IS2, causing probe current to increase until saturation. Upon saturation, the current abruptly rises to the detection threshold, triggering a polarity reversal of the IS1/IS2 voltage. This process repeats cyclically, generating a PWM square wave.

The duty cycle of the PWM signal reflects the measured magnetic field strength. When the primary current is zero or fully compensated, the duty cycle is close to 50%. Any uncompensated flux results in a deviation from 50% duty cycle.

The probe oscillation frequency depends on core characteristics and coil parameters. Under severe overload or distortion, the probe enters full saturation, increasing oscillation frequency to 1.6 MHz until limited by internal timing circuits. The minimum half-period is clamped at 280 ns. If three consecutive half-periods fall below 280 ns, the device enters overload latch mode, preserving the compensation current polarity information while maintaining a non-50% duty cycle. The overload condition is cleared when both half-periods exceed 280 ns.

### 7.3. PWM Signal Processing

The differential PWM/PWM- signals represent probe outputs, capable of driving external circuits or reducing ripple. Internally, these signals connect to a switched-capacitor integrator and filter stage that converts PWM to a filtered delta signal for driving the compensation coil driver. The filter's gain roll-off frequency ensures high DC gain and loop stability. External gain additions can be accommodated by setting the GAIN pin high to reduce internal gain by 8 dB.

### 7.4. Compensation Coil Driver

The full-differential compensation coil driver delivers current to the compensation winding (connected between ICOMP1 and ICOMP2). Operating from a single +5V supply, it minimizes coil resistance effects. Compensation current ( $I_{comp}$ ) correlates with primary current ( $I_p$ ) through winding ratios. At high frequencies, the compensation winding operates as a current transformer secondary.

Open-circuit detection is implemented: If either ICOMP pin approaches within 300 mV of ground and sustains current below threshold (Typical 30mA) for >100  $\mu$ s, the ERROR pin asserts low. For sensors with high winding resistance or those connected to an external compensation driver, this function should be disabled by pulling down the CCdiag pin.

### 7.5. Current-Sense Amplifier

The current-sense amplifier features wide bandwidth and high slew rate to accommodate diverse sensors. Auto-zeroing ensures DC stability and precision. With a fixed 4 V/V gain, it measures voltage across the shunt resistor. To achieve >70 dB CMRR, voltage division ratios at the inputs must match within 1/3000. Optimal CMRR is achieved by adding a series resistor  $R_5 = 4 \times R_{SHUNT}$  at the REFIN pin to restore matching.

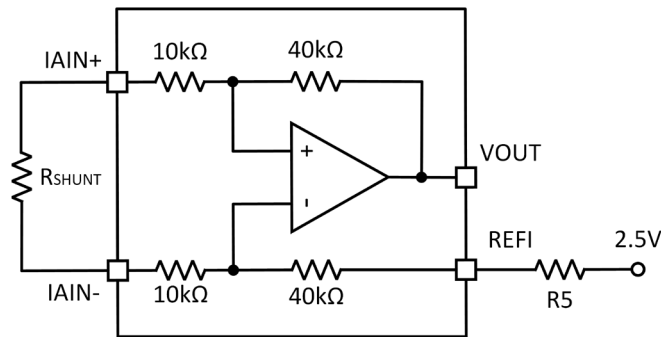


Figure 7-1 Current-Sense Amplifier

Excessive current may overload the current-sense amplifier. The OVER-RANGE pin, an open-drain output, is asserted low by the NSDRV401 to indicate amplifier overvoltage. To prevent false triggering due to noise, the overload condition must persist for over  $3\mu\text{s}$  before the OVER-RANGE pin is pulled low. The pin returns to a high-impedance state  $3\mu\text{s}$  after the overload condition is eliminated.

## 7.6. Voltage Reference

The NSDRV401 integrates a precision 2.5V voltage reference, used for internal configuration and accessible via the REFOUT pin. This reference serves as the output signal reference node for the current-sense amplifier, enabling bipolar signal generation. The buffered reference output provides low impedance with both source and sink current capabilities.

## 7.7. Demagnetization

Magnetic cores are not immune to residual magnetism, which can cause signal offset errors after severe current overloads, particularly under high flux density conditions. To address this, the NSDRV401 includes a demagnetization cycle generator. A digital control pin, DEMAG, initiates the cycle when held high for at least  $25.6\mu\text{s}$ . Shorter pulses are ignored. The cycle lasts approximately 110ms, during which the ERROR flag is pulled low to indicate invalid outputs. If DEMAG pin is high during power-up ( $V_{DD} > 4\text{V}$ ), the demagnetization cycle starts immediately (within  $12\mu\text{s}$ ). Holding DEMAG low prevents power-up demagnetization.

The probe circuitry remains operational during demagnetization, with PWM outputs maintained. The cycle can be aborted by pulling DEMAG low for  $\geq 25\mu\text{s}$ . In typical applications, DEMAG is tied to VDD to trigger demagnetization on every power-up. The demagnetization signal is generated via internal clocks and counters, with maximum compensation coil current limited by the shunt resistor and coil resistance.

## 7.8. Power-Up and Brown-Out

When VDD exceeds 4V and DEMAG pin is high, the demagnetization cycle initiates. During this period, the ERROR flag remains low to indicate a "not ready" state. Holding DEMAG low suppresses power-up demagnetization, allowing the NSDRV401 to become operational  $32\mu\text{s}$  after power-up. If no probe fault (e.g., probe half-periods  $< 32\mu\text{s}$  and  $> 280\text{ns}$ ) is detected within four full cycles, the compensation driver activates, and the ERROR pin transitions high ( $42\mu\text{s}$  post-power-up) to signal readiness.

To ensure normal operation, it is recommended that power pins VDD1 and VDD2 be short-circuited for use. The NSDRV401 monitors brown-out conditions with a threshold of +4V. Brown-Out states lasting  $< 100\mu\text{s}$  are ignored if the probe remains functional. Brown-Out states lasting  $> 100\mu\text{s}$  or power voltage dropping below 1.8V trigger a power-on reset.

Additionally, insufficient supply voltage can disrupt probe driver operation. If the supply voltage is too low to maintain the probe's peak current (determined by probe resistance and driver current-limiting resistors), a brown-out state lasting  $> 32\mu\text{s}$  asserts the ERROR flag.

## 7.9. Error Conditions

The NSDRV401 provides a system error indicator via the open-drain ERROR pin, requiring an external pull-up resistor. The pin is pulled low under fault conditions, including:

- **Probe Open-Circuit:** Caused by open circuit in the probe connections or insufficient supply voltage. The ICOMP driver remains active during the  $32\mu\text{s}$  timeout but disables afterward. Recovery resets the ICOMP driver for 3.3ms, with ERROR held low.
- **Probe Short-Circuit:** The pulse width of the probe driver is less than 280ns for four consecutive cycles. This situation indicates that the probe coil is short-circuited or the sensor is fully saturated at startup. If the duration  $> 25\mu\text{s}$ ,

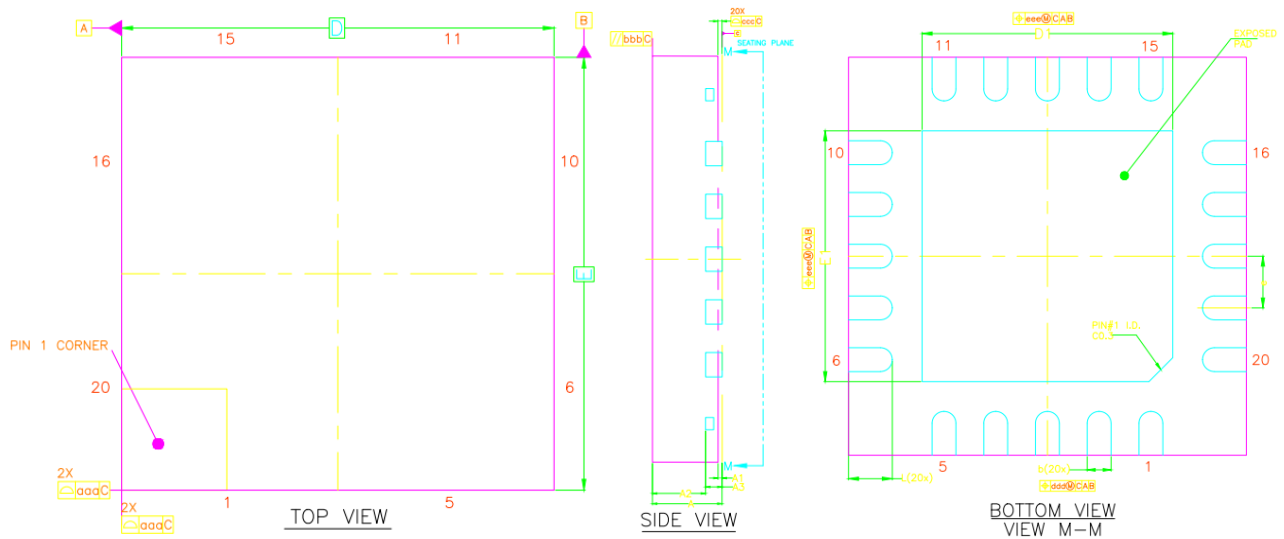


- **I<sub>P</sub>**: Represents the primary current to be measured.
- **K1 and K2**: Connect to the compensation coil.
- **S1 and S2**: Connect to the magnetic probe. The dot markings indicate winding polarity on the sensor's main core.
- **R1 (R<sub>SHUNT</sub>)**: A shunt resistor critical for system accuracy and temperature stability.
- **R3, R4, C3, and C4**: Form a filtering network to suppress residual probe oscillation ripple in the output signal. Component values depend on the sensor type and are adjusted for the best effect.
- **R5**: A dummy shunt resistor to restore symmetry in the differential amplifier inputs.  $R5 = 4 \times R_{SHUNT}$ . Precision is less critical.
- **R6 and R7**: Pull-up resistors for logic outputs.
- **C1 and C2**: Decoupling capacitors. Use low-ESR types placed close to the pins with low-impedance PCB traces. Avoid vias or use multiple vias if necessary. A combination of  $>1\mu\text{F}$  and  $<4.7\text{nF}$  capacitors is recommended.
- **D1 and D2**: Protection diodes for the differential amplifier inputs. Required only if the voltage drop across  $R_{SHUNT}$  exceeds 10V under maximum peak current conditions.

### 7.11. PCB Layout Guidelines

- **Power Supply Decoupling**: Use a 100nF and 1 $\mu\text{F}$  low-ESR capacitor pair connected to the supply pins via low-impedance traces.
- **Grounding**: Connect both ground pins to a single ground plane. For optimal performance, decouple the two power supplies separately (to a local GND plane) and link them to the main supply via ferrite beads.
- **Differential Amplifier Traces**: Ensure low trace resistance and matched lengths for connections to the shunt resistor. Implement Kelvin connections for precision, using two resistors to set the shunt value if required.
- **Signal Routing**: Wires and PCB traces for S1 and S2 should be very close or twisted. ICOMP1 and ICOMP2 should also be wired close together. To avoid capacitive coupling, run a ground shield between the S1/S2 and ICOMP wire pair or keep them distant from each other.
- **Thermal Pad**: The exposed pad on the package bottom is recommended to be soldered to GND, which is beneficial for the heat dissipation of the chip. Proper soldering ensures structural integrity and long-term reliability.

### 8. Package Information



DESCRIPTION	SYMBOL	MILLIMETER			
		MIN	NOM	MAX	
TOTAL THICKNESS	A	0.80	0.85	0.90	
STAND OFF	A1	0.00	--	0.05	
MOLD THICKNESS	A2	0.60	0.65	0.70	
L/F THICKNESS	A3	0.203 REF			
LEAD WIDTH	b	0.25	0.30	0.35	
BODY SIZE	X	D	4.90	5.00	5.10
	Y	E	4.90	5.00	5.10
LEAD PITCH	e	0.65 BSC			
LEAD LENGTH	L	0.50	0.55	0.60	
EP SIZE	X	D1	3.10	3.15	3.20
	Y	E1	3.10	3.15	3.20
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa	0.1			
MOLD FLATNESS	bbb	0.1			
LEAD COPLANARITY	ccc	0.08			
LEAD POSITION OFFSET	ddd	0.1			
EXPOSED PAD OFFSET	eee	0.1			

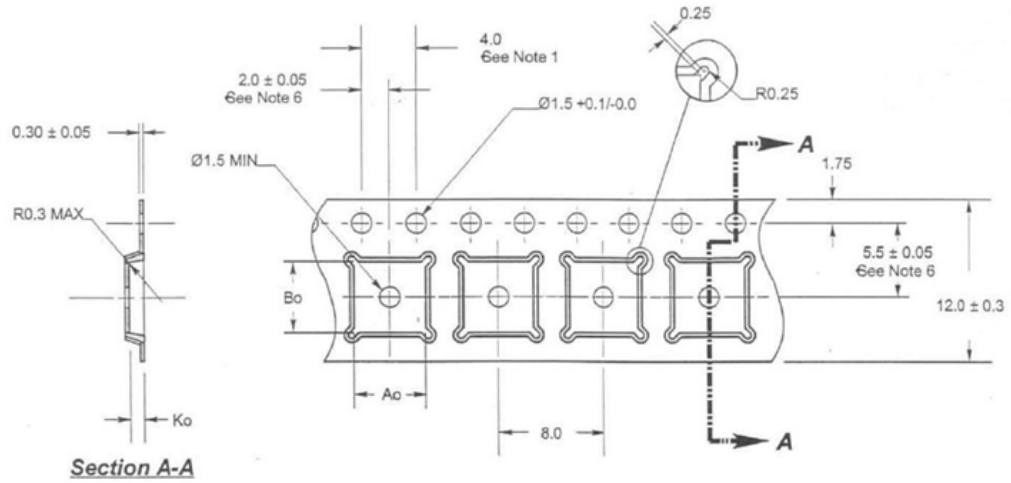
NOTES  
 1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 8-1 QFN20 Package Shape and Dimension in millimeters and (inches)

### 9. Ordering Information

Part Number	Package	MSL Level	Op Temp (°C)	SPQ
NSDRV401-DQCCR	QFN20	2	-40~+125	3000

### 10. Tape and Reel Information



- Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
  2. Camber not to exceed 1mm in 100mm.
  3. Material: PS + C.
  4.  $A_c$  and  $B_o$  measured as indicated.
  5.  $K_o$  measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
  6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

$A_c = 5.25$  mm  
 $B_o = 5.25$  mm  
 $K_o = 1.1$  mm

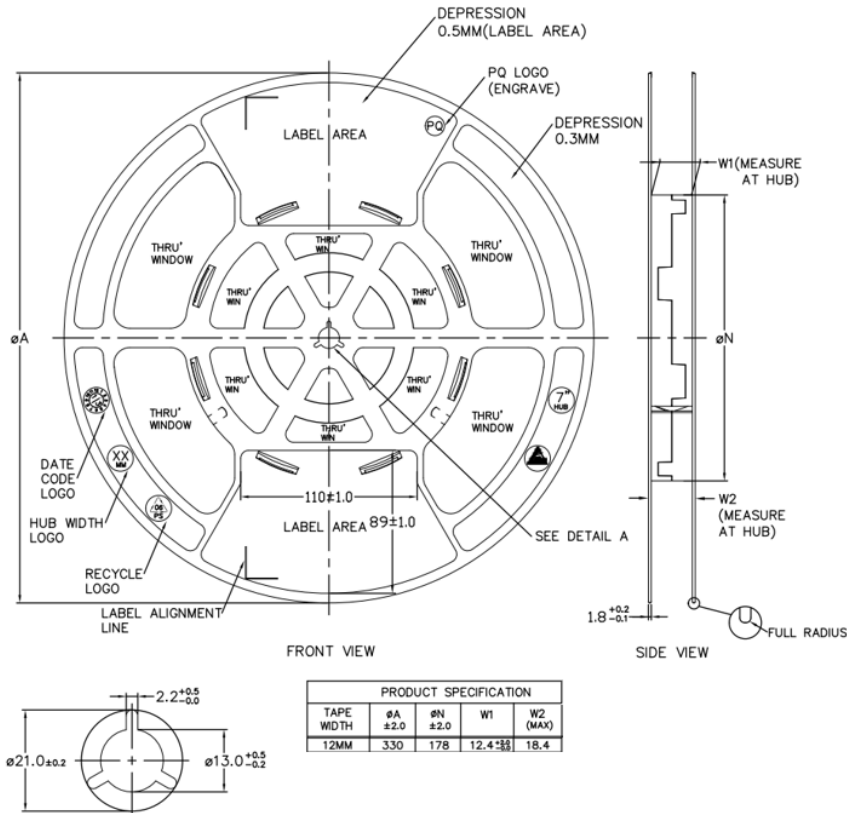
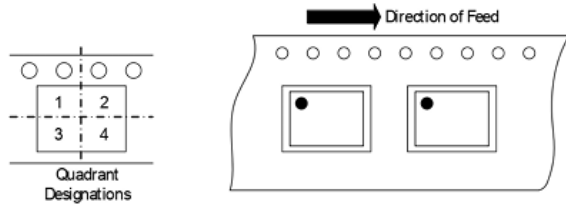


Figure 11-1 Tape and Reel Information of QFN20

## 11. Revision History

Revision	Description	Date
1.0	Initial version.	2025/7/1

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