NOVOSENSE

NSD8389 / NSD8389A

Bipolar Stepper Motor Driver Up to 1/256 Micro-step

Datasheet (EN) 1.2

Product Overview

The NSD8389/NSD8389A is a bipolar stepper motor driver, supporting up to max 1.5A full-scale current, for wide range automotive applications including headlight position, projector adjustment actuator in HUD and other valves or motors used in thermal management application.

The device includes current chopping regulation, internal up to 1/256 micro-step translator and multiple decay modes selection to enable stepper motor smooth motion. Furthermore, configurable full-scale current, external pin as simple STEP / DIR input and SPI controllable HOLD mode, all these functions easy customer management of stepper motor operation.

The device is fully protected from faults and short circuits, including undervoltage, overcurrent and overtemperature. Also, open load diagnosis and stall detection can be individually requested to perform during system running. Both SPI interface and dedicated nFault pin are provided to indicate these fault status & alert to microcontroller.

The device features sleep mode with low quiescent current when EN input is low or VS or VDDIO falls below POR threshold.

Applications

- Headlight adjustment
- HUD
- Actuator control in thermal management

Device information

Part Number	*Package*	*Body Size*
NSD8389-Q1HTSXR	HTSSOP24	7.80mm × 4.40mm
NSD8389A-Q1HTSXR	HTSSOP24	7.80mm × 4.40mm
NSD8389-Q1QBBR	VQFN24	4mm x 4 mm
NSD8389A-Q1QBBR	VQFN24	4mm x 4 mm

Key Features

- Bipolar stepper motor driver with max 1.5A full scale current
  - Wide 4.5-V to 36-V Operating Voltage
  - 900mΩ Typical $R_{DS(ON)}$ (HS + LS), per leg
- Simple input IOs for STEP / DIR & SPI control HOLD
- Programmable step modes:

  Full step, half step, …, up to 1/256 micro step
- Programmable output stage slew rate / dead time
- Selectable decay modes:
- Current regulation loop with integrated internal current sensing
  - programmable off-time in regulation loop
  - selectable ON blank timing
  - Both external VREF pin and Internal configurable bits to set full scale current
- Spread spectrum function for EMC reduction
- Very low power consumption in sleep mode
- SPI Interface with daisy chain support
- HTSSOP24 or VQFN24, wettable flank with exposed pad
- AEC-Q100 Grade 1 Compliance
- Integrated Protection Features
  - VS Undervoltage Lockout (VS UV)
  - Overcurrent Protection (OCP)
  - Thermal Warning (OTW/UTW) and Shutdown (OTSD)
  - Open load detection
  - Stall detection based on BEMF sensing
  - Fault indicating (nFAULT)
- RoHS & REACH Compliance

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1. Pin Configuration and Functions

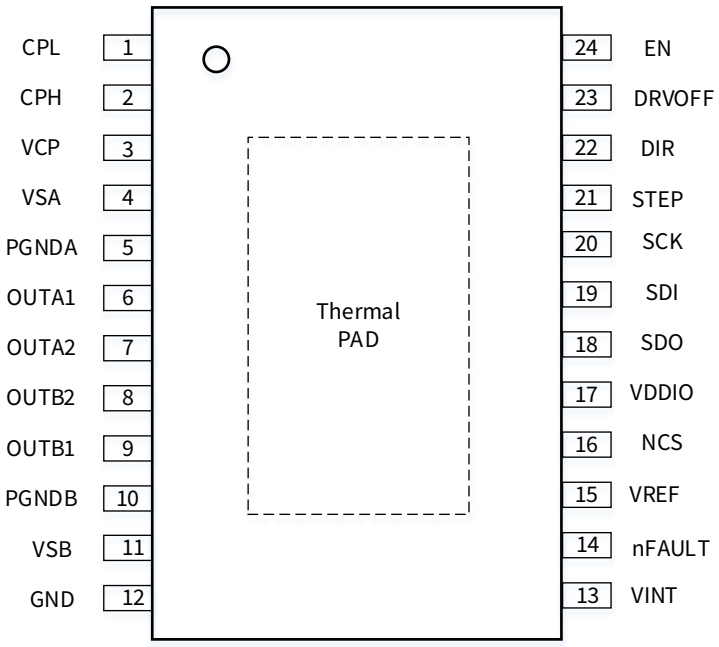

Figure 1-1 NSD8389/NSD8389A HTSSOP24 Pinout (top view)

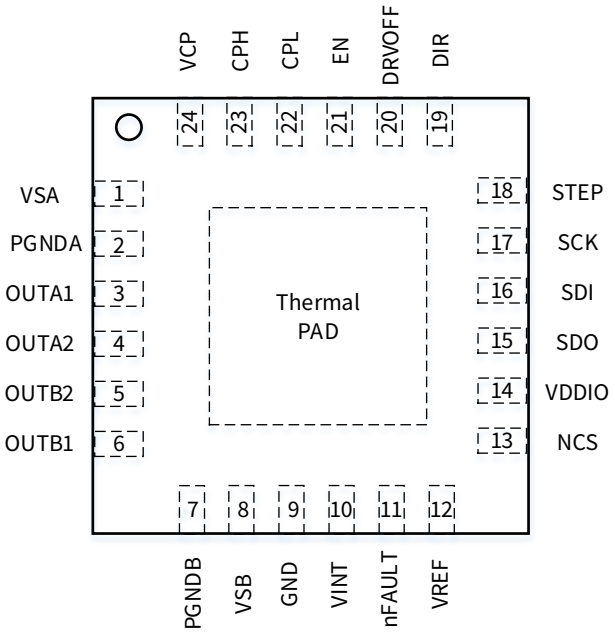

Figure 1-2 NSD8389/NSD8389A VQFN24 Pinout (top view)

Table 1-1. NSD8389/NSD8389A Pin Configuration and Description

NSD8389/NSD8389A PIN			TYPE	DESCRIPTION
NAME	HTSSOP24 NO.	VQFN24 NO.		
CPL	1	22	PWR	Charge pump low side pin, connect a 22nF X7R capacitor between CPH and CPL pins.
CPH	2	23	PWR	Charge pump high side pin, connect a 22nF X7R capacitor between CPH and CPL pins.
VCP	3	24	PWR	Charge pump output. Put 220nF X7R capacitor between VCP and VSx pins.
VSA	4	1	O	5V to 36V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitor needs to guarantee VSx pin voltage in maximum range. Put the 0.1μF and bulk capacitor (≥22μF) close to the VSx pin. VSA and VSB pins should be externally connected together.
PGNDA	5	2	PWR	High-current ground path. Connect PGNDA directly to board ground.
OUTA1	6	3	O	Half-bridge output OUTA1 pin. Connect directly to the motor or other inductive load.

OUTA2	7	4	O	Half-bridge output OUTA2 pin. Connect directly to the motor or other inductive load.
OUTB2	8	5	O	Half bridge output OUTB2 pin. Connect directly to the motor or other inductive load.
OUTB1	9	6	O	Half bridge output OUTB1 pin. Connect directly to the motor or other inductive load.
PGNDB	10	7	PWR	High-current ground path. Connect PGND directly to board ground.
VSB	11	8	PWR	5V to 36V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitor needs to guarantee VSx pin voltage in maximum range. Put the 0.1μF and bulk capacitor (≥22μF) close to the VSx pin. VSA and VSB pins should be externally connected together.
GND	12	9	PWR	Device ground. Connect to system ground.
VINT	13	10	PWR	Internal regulator decoupling output. Connect typ. 470nF X7R ceramic capacitor to ground, the capacitor shall be closed to VINT pin.
nFAULT	14	11	O	Open-drain output for fault indication, pull low when fault (see fault table) happens. Connect external pull up resistor, typ. 4.7k/10k
VREF	15	12	I	Analog input. Apply a voltage between 0.3 to 3.6 V.
NCS	16	13	I	SPI chip select input pin.
VDDIO	17	14	PWR	Digital I/Os supply. Suggest 100nF X7R decoupling capacitor closed to VDDIO pin.
SDO	18	15	O	SPI data output pin.
SDI	19	16	I	SPI data input pin.
SCK	20	17	I	SPI clock input pin.
STEP	21	18	I	Step signal inputs. It has internal pull downs.
DIR	22	19	I	DIR signal inputs. It has internal pull downs.
DRVOFF	23	20	I	Driver off input pin with internal pull up. If DRVOFF input pin is pulled low, all OUTAx/OUTBx are enabled, while DRVOFF input pin is pulled high, outputs are disabled and OFF.
EN	24	21	I	Device-enable input pin with internal pull down (active HIGH). If EN input pin is pulled low, all OUTAx/OUTBx go to tri-state and device move to low-power sleep state.
Thermal PAD	-	-	-	Exposed thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

2. Absolute Maximum Rating

ITEMS	MIN	MAX	UNIT
Power supply voltage (VSA, VSB)	–0.3	40	V
VDDIO voltage	–0.3	5.75	V
VINT voltage	–0.3	5.75	V
EN input (EN)	–0.3	VSx	V
Logic input/ouput voltage (SDI, SDO, NCS, SCK, STEP, DIR, DRVOFF, nFAULT)	–0.3	VDDIO+0.3	V
Analog input (VREF)	–0.3	5.75	V
VCP, CPH charge pump voltage	VS-0.3	VS+6	V
CPL, charge pump negative pin voltage	-0.3	VS	V
Output voltage (OUTA1, OUTA2, OUTB1, OUTB2) DC condition	–0.3	VS+0.3	V
Output voltage (OUTA1, OUTA2, OUTB1, OUTB2) AC condition, Iout=1A for t<500ms, Voutx < VS+1V	-1	VS+1	V

3. ESD Ratings

SYMBOL	DESCRIPTION	VALUE	UNIT
VESD_HBM	Human Body Model(HBM), all pins per ANSI/ESDA/JEDEC JS-001	±2000	V
VESD_CDM	Charged device model(CDM), Corner pin, per JEDEC specification JS-002	±750	V
	Charged device model(CDM), other pins, per JEDEC specification JS-002	±500	V

4. Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VS	VSA, VSB Power supply voltage	4.5		36	V
VDDIO	VDDIO supply voltage	3		5.5	V
EN, NCS, SCK, SDO, SDI, DRVOFF, STEP, DIR, nFAULT	Logic input / output voltage	0		5.5	V
VREF	Analog input voltage	0		3.3	V

STEP	STEP signal low or high timing	2			μs
F_{STEP}	STEP signal frequency			100	kHz
IFS(1)	Motor full scale current			IFSR (MAX 1.5)	A
IRMS(1)	Motor RMS current			IFSR *0.707 (MAX 1.06)	A

(1) The maximum allowable output load current shall be also evaluated considering application scenario, for both power dissipation and thermal condition including ambient temperature, application board thermal condition etc.

5. Thermal Information

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
Ta	Ambient operating ambient temperature	-40		125	°C
Tj	Junction temperature	-40		150	°C
Tstg	Storage temperature	-65		150	°C
Rthjc	HTSSOP24, Thermal resistance, junction to bottom case		3.4		°C/W
Rthjc	VQFN24, Thermal resistance, junction to bottom case		4.1		°C/W
Rthja	HTSSOP24, Thermal resistance, junction to ambient, on 2S2P (4-layer) PCB based on JEDEC standard		31.5		°C/W
Rthja	VQFN24, Thermal resistance, junction to ambient, on 2S2P (4-layer) PCB based on JEDEC standard		39.3		°C/W

6. Functional Description

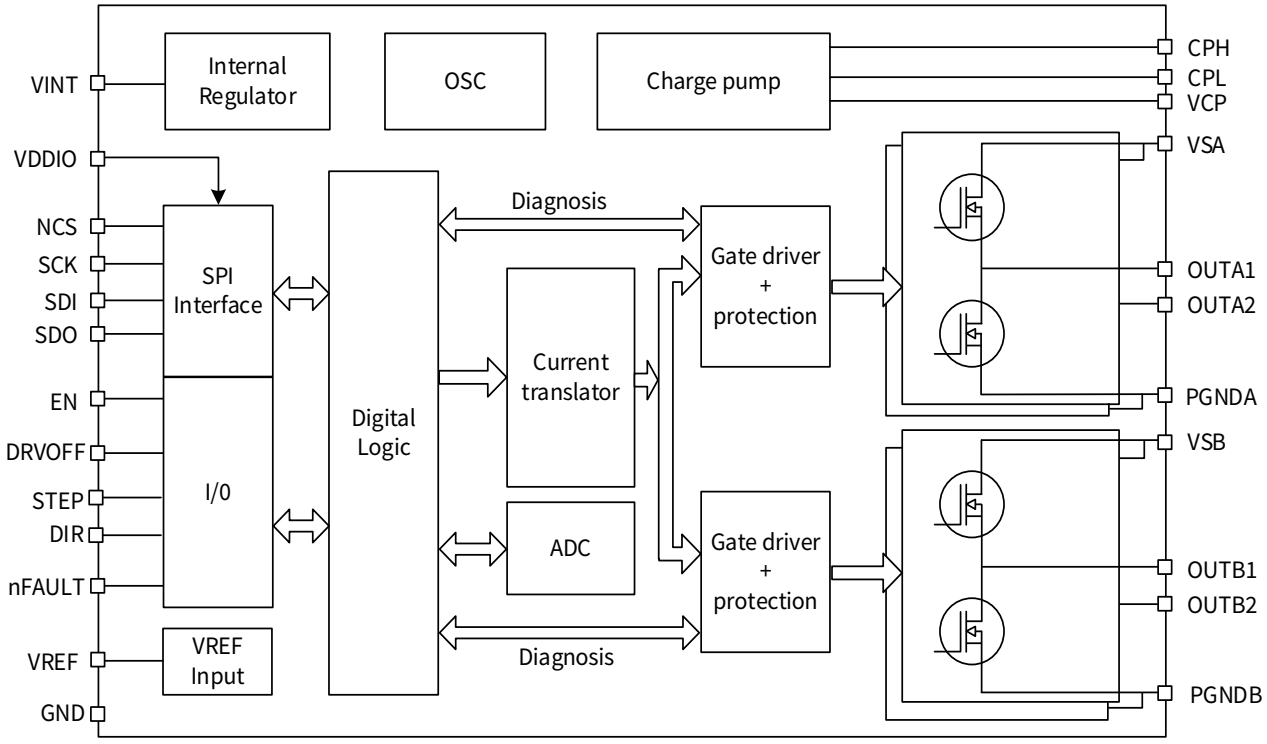

Figure 6-1. Block diagram

6.1. VSA, VSB Input

VS is the supply voltage used for internal H-bridge outputs and change pump; it ranges from 4.5V to 36V with typical case 13.5V power supply. VSA and VSB pins must be shorted together externally on PCB.

During motor operation, electrical energy is stored in the motor coils, and then fed back to the supply voltage VS once motor shut down. Thus, it is required to put at both ceramic and bulk electrolytic capacitor closed to VSA, VSB pin to avoid electrical spike / overstress on VSA and VSB pins.

6.1.1.VS UV, VS RST

When VS power supply pin voltage falls below the undervoltage threshold (VS_UV_L) over 10μs typ. undervoltage deglitch time,

- The corresponding VS undervoltage flag (***VSUV bit*** in ***STA_1*** register) is set to '1';
- Half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2 becomes OFF and charge pump is switched off.

When VS rise above the VS_UV_H longer than 10μs typ. undervoltage deglitch time, then

- Device automatically resumes operation, when ***DRV_DIS*** bit remains unchanged active enable status and charge pump voltage exit CP_UV. In the meantime, the ***VSUV*** flag bit keeps '1' until read & clear command is received.

When VS power supply pin voltage falls below the undervoltage reset threshold (VS_RST_L) over 1μs typ. undervoltage reset deglitch time,

- SPI unavailable.

- Half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2 becomes OFF and charge pump is switched off.

When VS rise above the VS_RST_H threshold longer than 1μs typ. undervoltage deglitch time, then

- Device is reset and all SPI registers are reset to default value.

6.1.2. VS OV diagnosis

When VS power supply pin voltage rises above the overvoltage threshold (VS_OV_H) over 10μs typ. overvoltage deglitch time, no reaction on outputs OUTA1, OUTA2, OUTB1, OUTB2, charge pump; in consequence, no need for overvoltage recovery. Only ***VSOV*** status bit in ***CONFIG_16*** register is alerted.

6.1.3.VS power supply electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VSA, VSB)						
VS	VS operating voltage		4.5		36	V
I_{VS}	VS operating supply current	VSA = VSB = 13.5V, EN=HIGH, all output off		3	7	mA
		VSA = VSB = 13.5V, EN=HIGH, half bridge driver working, no load			10	mA
I_{VS_SLEEP}	VS sleep current	VSA= VSB = 13.5V, -40≤Tj≤85ºC EN=LOW, I(VSA)+I(VSB) Half bridge driver output = GND			10	μA
VS_UV_L	VS undervoltage threshold	VSx falls until VSUV triggers	4	4.25	4.5	V
VS_UV_H		VSx rises until operation recovers	4. 1	4.35	4.6	V
V_{UV_HYS}	VS undervoltage hysteresis			100		mV
t_{UV}	VS undervoltage deglitch time	Guaranteed by digital scan	7	10	13	μs
VS_RST_L	VS undervoltage reset	VSx fall until reset triggers	3.2	3.6	4	V
VS_RST_H		VSx rise until reset	3.3	3.7	4.1	V
$V_{UV\_RST\_HYS}$	VS undervoltage reset hysteresis			100		mV
VS_OV_H	VS overvoltage		28		33	V
VS_OV_L			25		30	V
V_{OV_HYS}	VS overvoltage hysteresis			3		V
t_{OV}	VS overvoltage deglitch time	Guaranteed by digital scan	7	10	13	μs
C_{VS}	Capacitor on VSA, VSB pin	Application information		100		nF
C_{VS_BULK}	Bulk Capacitor on VSx pin	Application information		22		μF

6.2. VINT internal regulator

A linear voltage regulator is integrated into the device to supply internal blocks.

For proper operation, connect the VINT pin to GND using a ceramic capacitor which typical value is 470nF and min/max ranges from 100nF~1uF.

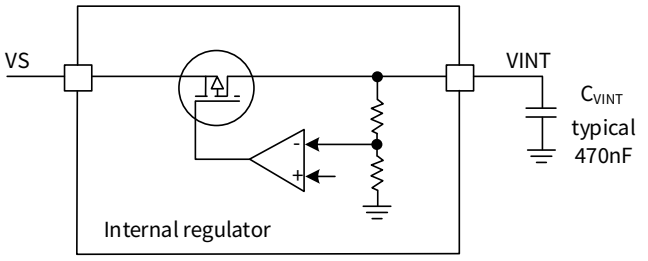

Figure 6-2. Internal regulator block diagram

During sleep state, the internal regulator is disabled.

6.2.1. VINT internal regulator electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal regulator (VINT)						
V_{VINT}	VINT internal regulator voltage	Load current 0~2mA	4.65	5	5.35	V
C_{VINT}	Capacitor on VINT pin	Application information	100	470	1000	nF

6.3. VDDIO Supply Input

VDDIO pin accepts wide external supply range from 3V to max 5.5V, which intends for the compatibility with both 3.3V and 5V system supply. 100nF X7R ceramic capacitor is suggested to put closed to VDDIO pin.

When VDDIO drops below VDDIO_RST_L, SPI interface, digital output will be inactive, also including charge pump and all half bridge drivers are switched off.

Once VDDIO > VDDIO_RST_H, internal digital is reset and back to normal working state.

6.3.1. VDDIO internal regulator electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDIO supply input (VDDIO)						
I_{VDDIO}	Input current of VDDIO	EN=High, outputs off			1	mA
I_{VDDIO_SLEEP}	Input current of VDDIO in sleep mode	EN=LOW, SPI inactive -40≤Tj≤85 ºC		3.5	10	μA
$V_{VDDIO\_RST\_H}$	VDDIO reset high threshold,	VDDIO increasing	2	2.5	3	V

$V_{VDDIO\_RST\_L}$	VDDIO reset low threshold	VDDIO decreasing	1.8	2.3	2.8	V

6.4. Charge pump

To drive internal high side output, a charge pump is used to generate the high side gate driving voltage which is above VS. In the meanwhile, external fly capacitor between CPH and CPL, also external tank capacitor between VS and VCP, are required.

Additionally, a built-in monitoring circuit checks if the charge pump output voltage is sufficient high. In case of VCP undervoltage ($V_{CP} < V_{CP\_UV}$), the outputs (OUTA1, OUTA2, OUTB1, OUTB2) are actively turned off and ***CPUV bit*** **in** ***STA_0*** register is set and latched.

- Output stage automatically resumes operation if V_{CP} rise above V_{CP_UV} with t_{CP_UV}. The CPUV bit keeps latch until CLR_FLT bit '1' is written or EN pin receives fault clear short pulse.

The charge pump nominal frequency is 420kHz, it also has the possibility to enable internal frequency with modulation through spread spectrum.

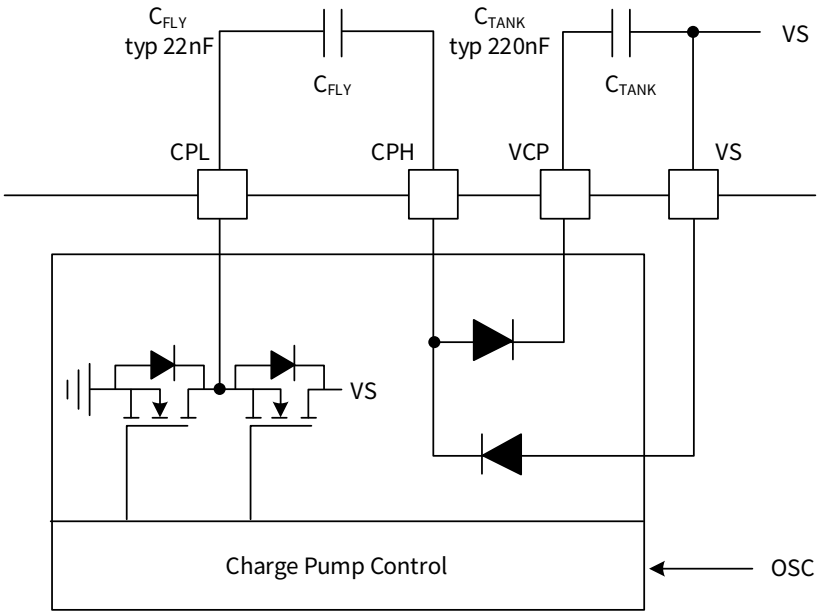

Figure 6-3. Charge pump block diagram

6.4.1.VCP charge pump electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge pump (VCP)						
V_{CP}	Charge pump output voltage	VSx >=9V, I_{VCP}=3mA	VS+4.5	VS+5		V
		6v<VSx <9V, I_{VCP}=3mA	VS+4			V
V_{CP_UV}	Charge pump undervoltage	VCP falling		VS+3		V

$V_{CP\_UV\_HYS}$	Charge pump undervoltage hysteresis			500		mV
t_{CP_UV}	Charge pump undervoltage digital deglitch filter	Guaranteed by digital scan		10		μs
F_{CP}	Charge pump frequency			420		kHz
C_{FLY}	Fly capacitor between CPH and CPL pin	Application information		22		nF
C_{TANK}	Tank capacitor between VS and VCP pin	Application information		220		nF

6.5. Digital Input EN & DRVOFF & STEP/DIR & SPI SDI/SCK/NCS

NCS / SDI / SCK is the typical CMOS schmitt trigger as SPI inputs.

EN, SCK, SDI and STEP, DIR input pins have typ. 100kohm internal pull-down resistance, while 100kohm internal pull up is applied on NCS and DRVOFF pin.

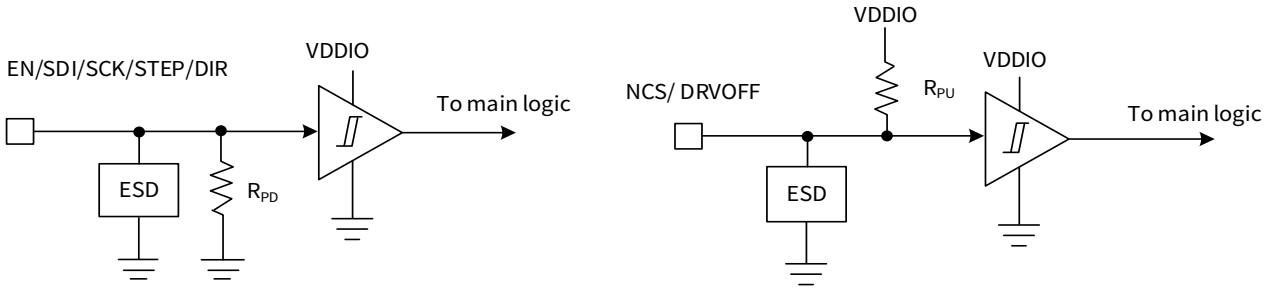

Figure 6-4. Digital input pins block diagram

6.5.1.EN Function

The EN pin can be used as a sleep/active mode control signal, but is also available for fault clear. The following figure shows how the timing of the EN pin is related to the function of the EN pin.

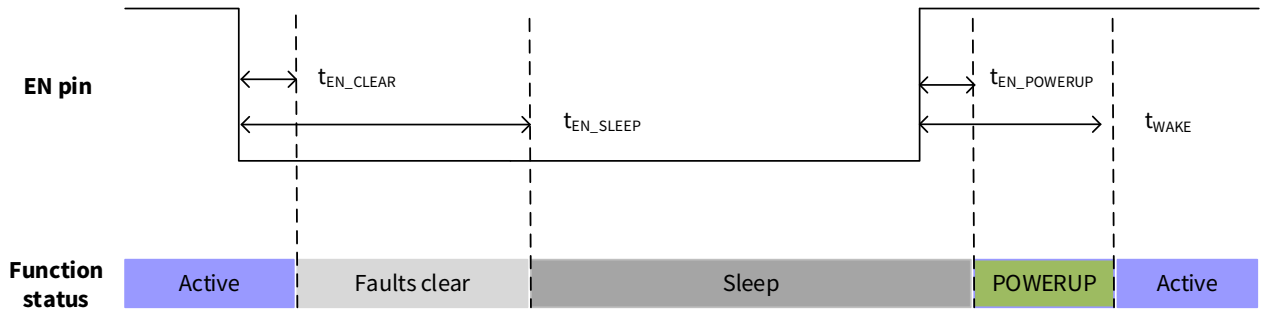

Figure 6-5. EN input pin timing and function

When EN pin is driven low, depends on the duration of EN low timing

- The EN pin low timing less than $t_{EN\_CLEAR,}$, device function keep active.
- The EN pin low timing ranges from [$t_{EN\_CLEAR,}$ $t_{EN\_SLEEP,}$], latched faults and SPI flag are cleared, same as CLR_FLT bit function
- The low timing over $t_{EN\_SLEEP,}$ internal logic / register is reset, charge pump / all outputs OUTA1/A2, OUTB1/OUTB2 are disabled, and device enter sleep mode.

When EN transition from low to high

- If it is for lasting over $t_{EN\_POWERUR}$ at VDDIO>$V_{VDDIO\_RST\_H}$ & VS>V_{UV_RST}, device come out sleep mode and starting powerup.
- Once device move from sleep to normal operation. a t_{WAKE} timing shall be wait, it is used to setup internal circuit / block, such as SPI, digital logic, and charge pump.

6.5.2.Logical control input pins electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic Control Input (EN, NCS, SDI, SCK, DRVOFF, STEP, DIR)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2			V
V_{HYS}	Input logic hysteresis			0.3		V
R_{PD}	Pulldown resistance	EN, SDI, SCK, STEP, DIR	50	100	160	kΩ
R_{PU}	Pullup resistance	NCS, DRVOFF	50	100	160	kΩ
C_{IN}	Input capacitance	NCS, SDI, SCK, DRVOFF, STEP, DIR pin Specified by design			15	pF
t_{EN_CLEAR}	Deglitch filter on EN falling to clear fault	Specified by design	6	12	18	μs
t_{EN_SLEEP}	Deglitch filter on EN falling to sleep mode	Specified by design	30	56	75	μs
$t_{EN\_POWERUP}$	Deglitch filter on EN rising to powerup	Specified by design	6	12	18	μs
t_{WAKE}	wake-up time	From EN low to high transition until SPI ready, specified by design			200	μs
		From EN low to high transition until Output transition, specified by design			0.9	ms

6.6. Digital output SDO and nFault

SDO is push-pull structure, which transfers internal register values to microcontroller. It also features SDO tristate at NCS high when device SPI interface is not selected.

The fault indicator pin, nFault, is the output with open-drain structure.

6.6.1.Digital output pins electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDO output (push-pull)						
V_{OL_SDO}	SDO output low voltage	I_O = 2 mA		0.2	0.5	V
V_{OH_SDO}	SDO Output high	I_O = 2 mA	VDDIO -0.5			V
I_{leak_SDO}	SDO Output leakage current	NCS high, 0<V_{SDO}<VDDIO	-1		1	μA
C_{SDO}	Digital output capacitance	Specified by design			60	pF
nFault output (open-drain)						
V_{OL_nFault}	nFault output low voltage	I_O = 2 mA		0.1	0.5	V
I_{leak_nFault}	nFAULT output leakage current	0<V_{nFAULT}<VDDIO	-1		1	μA

6.7. Stepper operation

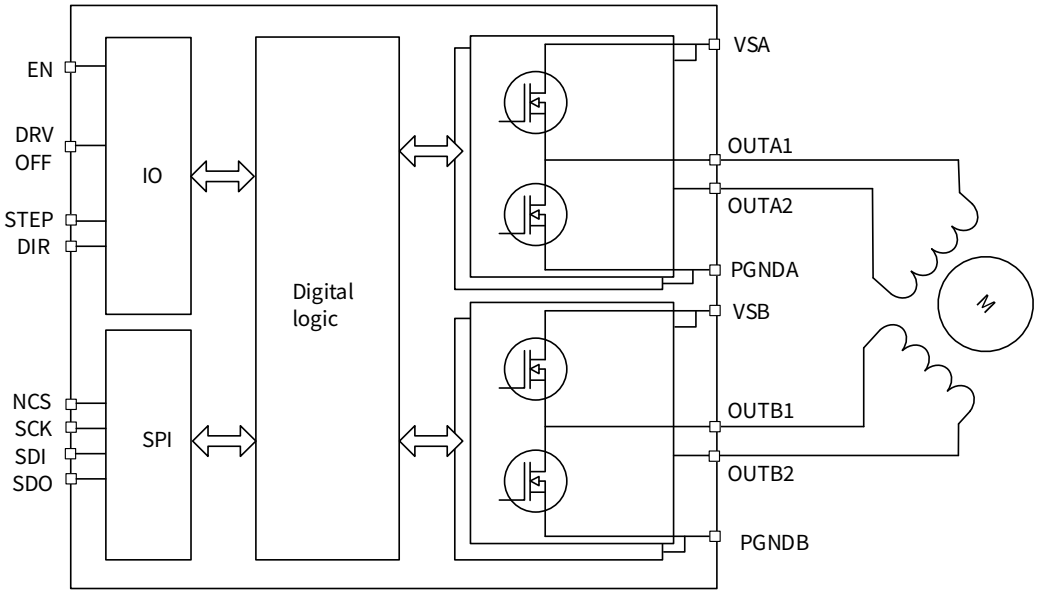

Figure 6-6. stepper motor control

6.7.1.Stepper driver activation – DRVOFF pin and DRV_DIS bit

The activation of output power stage and the truth table for stepper mode control is shown as table 6-1.

Table 6-1. Stepper motor control table

EN pin	*DRVOFF pin*	*DRV_DIS* bit in *CONFIG_2*	OUTx	Description
LOW	x	x	HIZ	Sleep, output stage HIZ
HIGH	HIGH	x	HIZ	Output stage not enable, HIZ
HIGH	LOW	'1'	HIZ	Output stage not enable, HIZ
HIGH	LOW	'0'	ACTIVE	Output stage active, controlled by internal digital logic

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Note:

- The default value of DRV_DIS bit in NSD8389A is '1', which means output disable in default. On the contrary, DRV_DIS bit in NSD8389 is '0' in default.

6.7.2.Stepper mode selection

A total of eleven different step modes can be selected, from standard full step to high resolution microstep up to 1/256, depending on the step resolution required by the application.

Set the *CONFIG_3* register ***STEPPER_MODE[3:0]*** bits to selects the step mode as required.

Table 6-2. Stepper mode selection table

STEPPER_MODE[3:0] in *CONFIG_3* register	Step mode
2b'0000'	Full step with 100% current (default value)
2b'0001'	Full step with 71% current
2b'0010'	Non-circular 1/2 step
2b'0011'	1/2 half step
2b'0100'	1/4 mini step
2b'0101'	1/8 micro step
2b'0110'	1/16 micro step
2b'0111'	1/32 micro step
2b'1000'	1/64 micro step
2b'1001'	1/128 micro step
2b'1010'	1/256 micro step
others	reserved

After device POWER ON RESET (caused by VSx, EN, VDDIO), the internal step mode is reset to default (STEPPER_MODE[3:0] full step with 100% full scale current) and coil current translator moves to the position 45 degree.

6.7.3.Stepper motor coil current translator

Under micro step operation mode, the translator starts from position 0, and the next position is increased (DIR=1) or decreased (DIR=0) with 1 of the same columns. As shown in Table 6-3, the relative coil A current and coil B current vs. step modes are listed using 1/2 half step~1/32 micro step as example.

Positive current is defined as current flowing from OUTA1 to OUTA2 or OUTB1 to OUTB2, in contrast, current from OUTA2 to OUTA1 or OUTB2 to OUTB1 is considered as negative.

Table 6-3. Step translator of micro step modes

1/32 micro step	1/16 micro step	1/8 micro step	1/4 mini step	1/2 half step	coil A % of IFS	coil B % of IFS
0	0	0	0	0	70.71	70.71
1					74.1	67.16
2	1				77.3	63.44
3					80.32	59.57
4	2	1			83.15	55.56
5					85.77	51.41
6	3				88.19	47.14
7					90.4	42.76
8	4	2	1		92.39	38.27
9					94.15	33.69
10	5				95.69	29.03
11					97	24.3
12	6	3			98.08	19.51
13					98.92	14.67
14	7				99.52	9.8
15					99.88	4.91
16	8	4	2	1	100	0
17					99.88	-4.91
18	9				99.52	-9.8
19					98.92	-14.67
20	10	5			98.08	-19.51
21					97	-24.3
22	11				95.69	-29.03
23					94.15	-33.69
24	12	6	3		92.39	-38.27

25					90.4	-42.76
26	13				88.19	-47.14
27					85.77	-51.41
28	14	7			83.15	-55.56
29					80.32	-59.57
30	15				77.3	-63.44
31					74.1	-67.16
32	16	8	4	2	70.71	-70.71
33					67.16	-74.1
34	17				63.44	-77.3
35					59.57	-80.32
36	18	9			55.56	-83.15
37					51.41	-85.77
38	19				47.14	-88.19
39					42.76	-90.4
40	20	10	5		38.27	-92.39
41					33.69	-94.15
42	21				29.03	-95.69
43					24.3	-97
44	22	11			19.51	-98.08
45					14.67	-98.92
46	23				9.8	-99.52
47					4.91	-99.88
48	24	12	6	3	0	-100
49					-4.91	-99.88
50	25				-9.8	-99.52
51					-14.67	-98.92
52	26	13			-19.51	-98.08
53					-24.3	-97
54	27				-29.03	-95.69
55					-33.69	-94.15

56	28	14	7		-38.27	-92.39
57					-42.76	-90.4
58	29				-47.14	-88.19
59					-51.41	-85.77
60	30	15			-55.56	-83.15
61					-59.57	-80.32
62	31				-63.44	-77.3
63					-67.16	-74.1
64	32	16	8	4	-70.71	-70.71
65					-74.1	-67.16
66	33				-77.3	-63.44
67					-80.32	-59.57
68	34	17			-83.15	-55.56
69					-85.77	-51.41
70	35				-88.19	-47.14
71					-90.4	-42.76
72	36	18	9		-92.39	-38.27
73					-94.15	-33.69
74	37				-95.69	-29.03
75					-97	-24.3
76	38	19			-98.08	-19.51
77					-98.92	-14.67
78	39				-99.52	-9.8
79					-99.88	-4.91
80	40	20	10	5	-100	0
81					-99.88	4.91
82	41				-99.52	9.8
83					-98.92	14.67
84	42	21			-98.08	19.51
85					-97	24.3
86	43				-95.69	29.03

87					-94.15	33.69
88	44	22	11		-92.39	38.27
89					-90.4	42.76
90	45				-88.19	47.14
91					-85.77	51.41
92	46	23			-83.15	55.56
93					-80.32	59.57
94	47				-77.3	63.44
95					-74.1	67.16
96	48	24	12	6	-70.71	70.71
97					-67.16	74.1
98	49				-63.44	77.3
99					-59.57	80.32
100	50	25			-55.56	83.15
101					-51.41	85.77
102	51				-47.14	88.19
103					-42.76	90.4
104	52	26	13		-38.27	92.39
105					-33.69	94.15
106	53				-29.03	95.69
107					-24.3	97
108	54	27			-19.51	98.08
109					-14.67	98.92
110	55				-9.8	99.52
111					-4.91	99.88
112	56	28	14	7	0	100
113					4.91	99.88
114	57				9.8	99.52
115					14.67	98.92
116	58	29			19.51	98.08
117					24.3	97

118	59				29.03	95.69
119					33.69	94.15
120	60	30	15		38.27	92.39
121					42.76	90.4
122	61				47.14	88.19
123					51.41	85.77
124	62	31			55.56	83.15
125					59.57	80.32
126	63				63.44	77.3
127					67.16	74.1

Table 6-4 shows full step operation with 100% full scale current. 71% full scale current in full step operation is similar, difference is only coil current maxim value.

Table 6-4. Full step with 100% full scale current

Full step mode	Coil A current (% of IFS)	Coil B current (% of IFS)
0	100	100
1	100	-100
2	-100	-100
3	-100	100

Table 6-5 shows non-circle 1/2 step operation. Comparing with 1/2 step operation, this step mode provides higher torque as more load current in running.

Table 6-5. Non-circle 1/2 step

Non-circle 1/2 step	Coil A current (% of IFS)	Coil B current (% of IFS)
0	100	100
1	100	0
2	100	-100
3	0	-100
4	-100	-100
5	-100	0
6	-100	100
7	0	100

6.7.4.Step update – STEP / DIR

The functions in NSD8389 / NSD8389A, such as stepper STEP pulse / DIRECTION input, can be directly controlled by microcontroller I/Os through the STEP / DIR digital input pins or partially use I/O with the combination of SPI.

A typical example can be step pin as STEP updating function connecting to MCU PWM function I/O, while DIR pin is floating and not connected. The direction control function is controlled by SPI register, also HOLD operation in SPI.

Anyhow, if minimizing MCU I/O numbers are required, the STEP updating/Direction control/HOLD all SPI control are feasible.

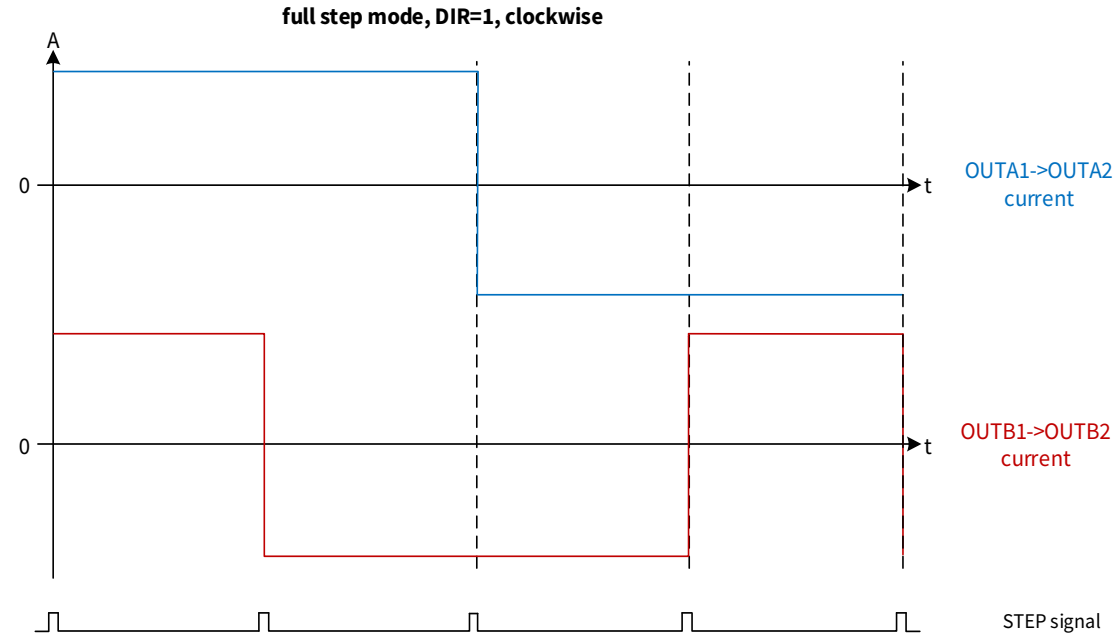
The above-mentioned STEP / DIR pin and SPI control are defined by SP bits (***SPI_STEP, SPI_DIR, STEP, DIR***) in ***CONFIG_3*** register, and the details are summarized in Table 6-6.

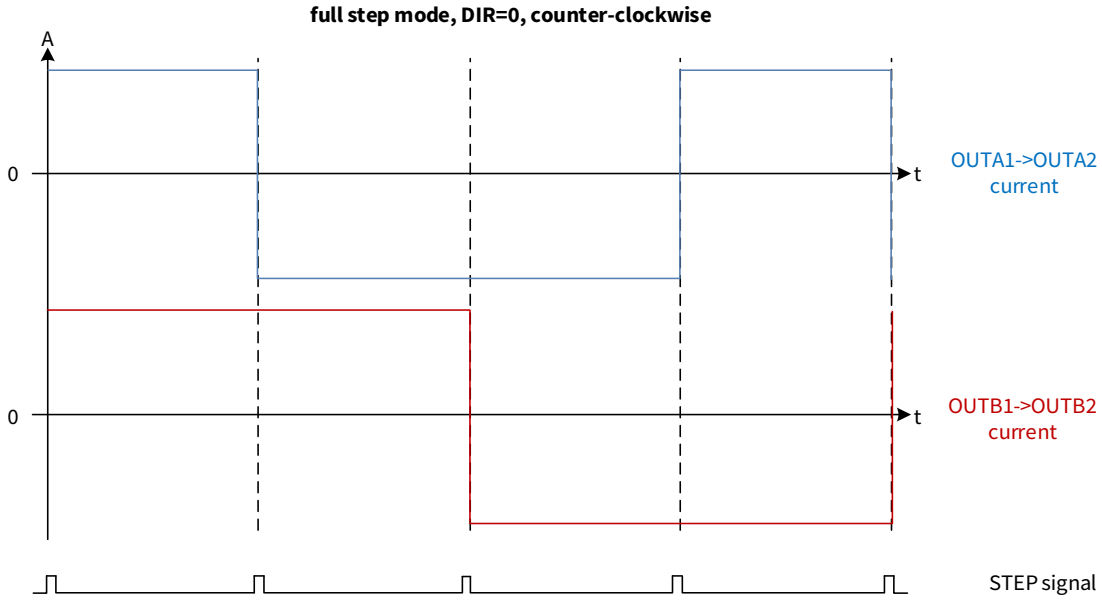
Table 6-6. STEP updating / Direction control summary

Function	Register configuration		Pin	Comment
	CONFIG_3			
STEP update	Bit D4, ***SPI_STEP***='0'	Bit D6, ***STEP bit***	STEP pin input	**Default setting, after power up.** STEP pin as stepper mode - STEP update signal input..
	Bit D4, ***SPI_STEP***='1'	Bit D6, ***STEP bit***	STEP pin input	STEP update signal is not related to STEP pin under SP_STEP bit =1. STEP updating is controlled by writing ***STEP*** bit in ***CONFIG_3.*** Note: STEP bit in CONFIG_3 is automatically becomes '0' after writing '1' command is executed, therefore, everytime write STEP bit =1 to cause internal logic to move next step.
Direction control	Bit D5, ***SPI_DIR***='0'	Bit D7, ***DIR bit***	DIR pin input	**Default setting, after power up** DIR input pin as stepper mode Direction control signal input. DIR pin logic high set operation in clockwise, while logic low means counter-clockwise
	Bit D5, ***SPI_DIR***='1'	Bit D7, ***DIR bit***	DIR pin input	Direction control signal is not related to DIR pin under SPI_DIR bit = 1. It is controlled by SPI DIR bit in CONFIG_3, by write ‘0’ for counter-clock wise and ‘1’ for clockwise.

Note:

- STEP pin pulse is recognized at rising edge with internal filter, thus min 2μs high in STEP pulse is suggested.


full step mode, DIR=1, clockwise
A
0
t
OUTA1->OUTA2
current
0
t
OUTB1->OUTB2
current
STEP signal


full step mode, DIR=0, counter-clockwise
A
0
t
OUTA1->OUTA2
current
0
t
OUTB1->OUTB2
current
STEP signal

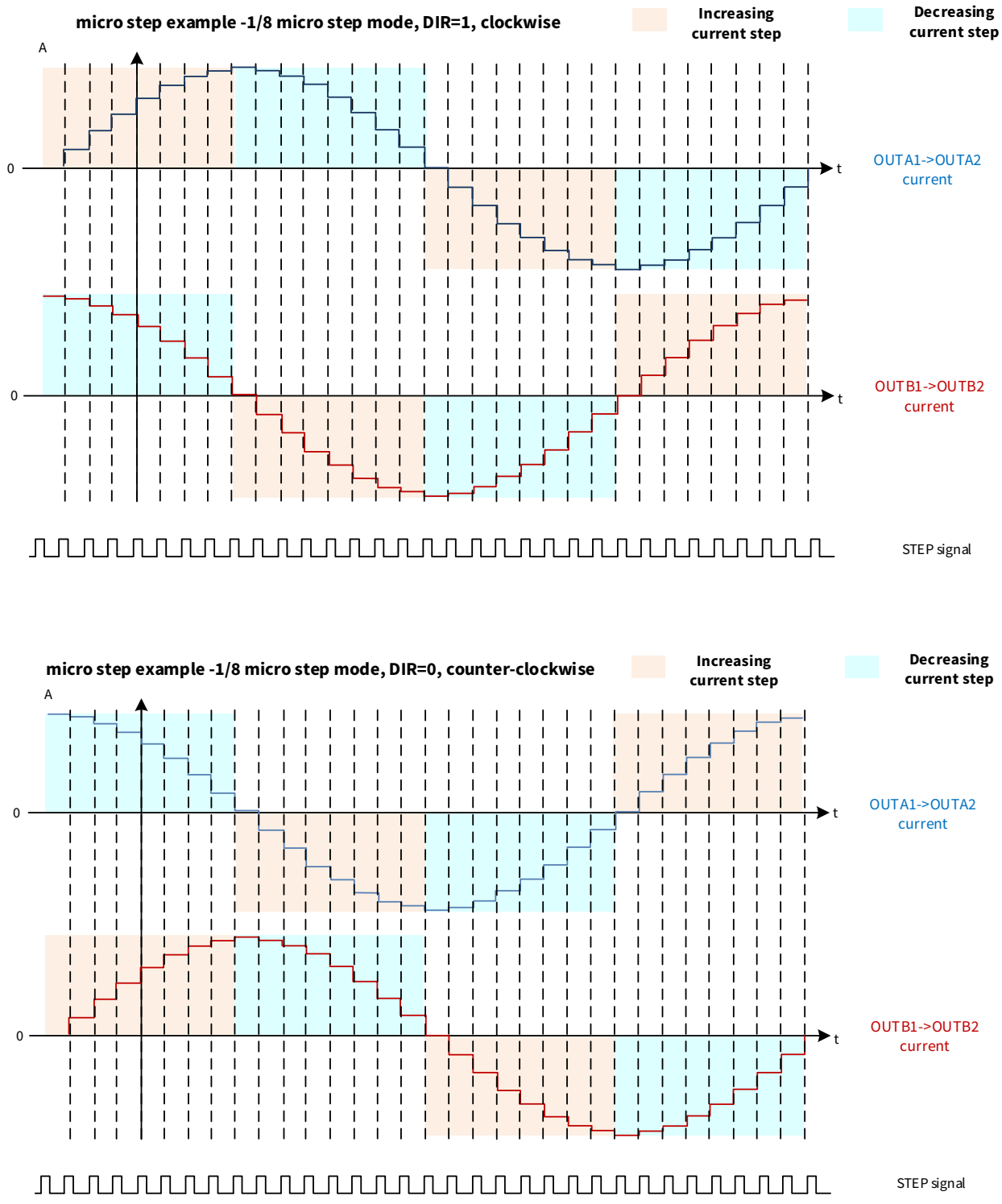


Figure 6-7. Step update example

6.7.5.Current regulation

To regulate the coil current in specific level of each step, an internal current control loop is implemented. Several blocks (current monitor/ comparator / DAC / digital timing and control logic) are including.

The current monitor of each low-side sources a current image which has a fixed ratio of the instantaneous coil current. These current images are compared with the DAC-controlled current limit in current regulation loop. This loop comparator generates the control signal which turns on or turn off the output H-bridge stage. Therefore, two phases (ON and OFF) of current regulation are established.

During current regulation ON phase, H-bridge is turning on, the current monitor output is ignored for a programmable period (t_{BLANK}), then after the blanking time, the internal regulation loop automatically moves the H-Bridge output into current regulation OFF phase, when the coil current reaches the limit at which the timing elapses over t_{FT}.

During current regulation OFF phase, fixed off-time is used, tOFF can be select among 7us, 16us(default), 24us and 32us, through ***TOFF_SEL[1:0]*** bits in **CONFIG_2** register. Short tOFF timing helps to reduce the overall current ripple amplitude.

Note:

- The blanking time also sets the minimum driving ON time. In case large capacitor used in output terminal or from stepper motor parasitic effect, long tBLANK timing is suggest.
- The value of tBLANK in NSD8389A is related on output slew rate selection (***SR_SEL[1:0]*** bits in **CONFIG_1** register) and additional control bit (***TBLANK_SR_EN*** bit in **CONFIG_5** register), while tBLANK for NSD8389 is fixed. The detailed difference is shown in table below.

Device	***TBLANK_SR_EN bit in CONFIG_5 register***	***SR_SEL[1:0]* in *CONFIG_1* register**	**tBLANK timing**
NSD8389	X	XX	0.5us
NSD8389A	0	XX	0.5us
	1	2b'00'	5.6us
	1	2b'01'	2us
	1	2b'10'	1.5us
	1	2b'11'	0.86us

6.7.6.Decay modes

During current regulation ON phase, once the current limit is reached over t_{FT}, the H-bridge switch to current regulation OFF state and begins current decay. It can operate in two different basic states, slow decay or fast decay. If the slow decay mode is used, both low side FETs will be turn on to reduce coil current until next current regulation cycle. In fast decay, as it runs, the H-bridge first turns on the opposite HS and LS to reduce the current in fast decay; as the load current drop and approach zero current for t_{FT}, then the bridge output stage is changed to slow decay to avoid reverse current. Figure 6-8 shows the above two working phases. Mixed decay is a combination of fast decay and slow decay, it begins as fast decay for a time, followed by slow decay for the remainder.

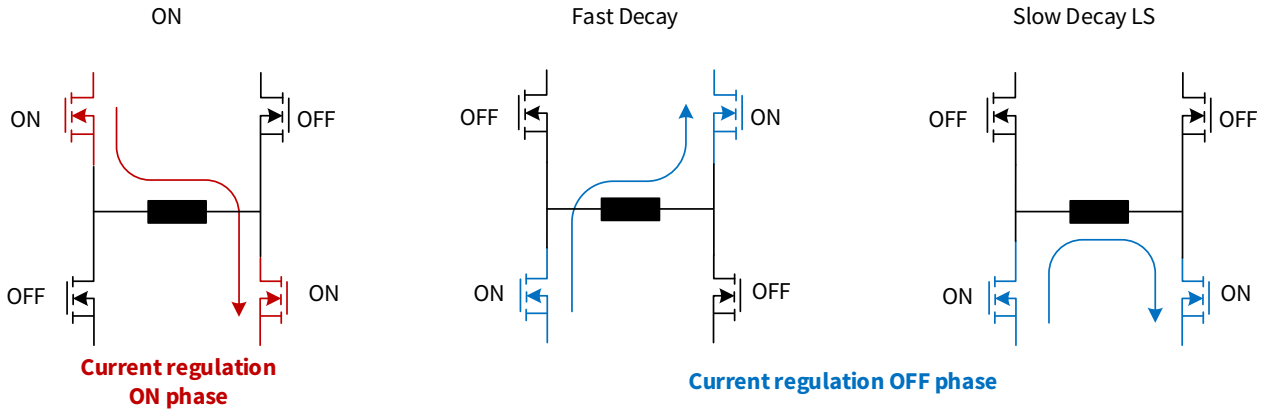


Figure 6-8. Current regulation ON and OFF phase example

Furthermore, to provide the low current ripple of entire steps, the difference of increasing current steps and decreasing current steps has to be considered. So the device provides eight decay selections (***DECAY_SEL[2:0]*** bits in ***CONFIG_2*** register) to cover the scenario, especially the auto decay and auto decay with ripple control mode. Table 6-7 lists the decay mode details of increasing and decreasing current step.

Table 6-7. Decay modes selection

***CONFIG_2* register *DECAY_SEL2:0]* setting**	**Increasing current steps**	**Decreasing current steps**
2b'000'	Slow decay	Slow decay
2b'001'	Slow decay	MIXED: 30% fast + 70% slow
2b'010'	Slow decay	MIXED: 60% fast + 40% slow
2b'011'	Slow decay	Fast decay
2b'100'	MIXED: 30% fast + 70% slow	MIXED: 30% fast + 70% slow
2b'101'	MIXED: 60% fast + 40% slow	MIXED: 60% fast + 40% slow
2b'110'	Auto decay	Auto decay
2b'111' (default)	Auto decay with ripple control	Auto decay with ripple control

---

Note:

- Slow decay features the smallest current ripple of the decay modes. However, during decreasing current steps of slow decay, the current decreases very slowly and takes longer time to settle to the new current step. So slow decay may not properly regulate current where some cases (low coil current, but long t_{BLANK} or t_{FT} timing), this may cause a loss of current regulation, and a more aggressive decay mode (mixed decay or auto decay) is recommended for these cases.
- In mixed decay for both increasing and decreasing current steps scenario, the current ripple of this mode is larger than slow decay. However, on decreasing current steps, mixed decay settles to the new current step faster than slow decay, therefore, in cases motor at very low stepping speeds, or low coil current, mixed decay mode allows the motor current level to stay in regulation.
- Auto decay mode which combine the advantage of low current ripple in slow decay and fast response in mixed decay for both increasing current steps and decreasing current steps.

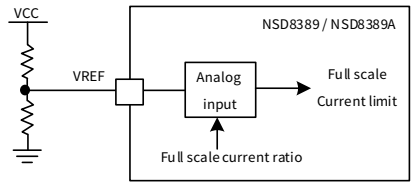
6.7.7.Full scale current setting-

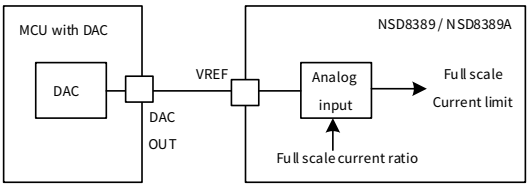
The full scale current is determined by two factors: one is external input on VREF pin, another one is the ***IFS_DAC[3:0]*** setting value of ***CONFIG_1*** register

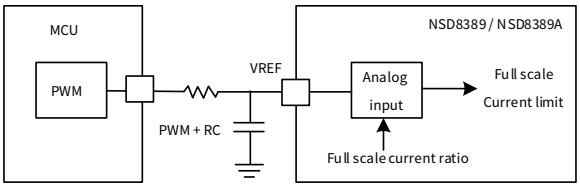
The full scale current calculation formula is written as below:

$$I_{FS} = \frac{VREF}{2.2} \times IFS\_DAC[3:0]\ setting\ ratio$$

VREF pin accepts the input voltage with max up to 3.3V. It can be a fixed voltage level using simple resistor divider, or the adjustable value from a dedicated DAC or using microcontroller PWM to generate an analog output together with RC low pass filter.







To adjust the second factor, full scale current setting ratio in SPI register, table 6-8 can be referred.

Table 6-8. Full scale current ratio

***IFS_DAC[3:0]* in *CONFIG_1* register**	**Full scale current setting ratio**
2b'0000'	0000b = 100% (default)
2b'0001'	0001b = 93.75%
2b'0010'	0010b = 87.5%
2b'0011'	0011b = 81.25%
2b'0100'	0100b = 75%
2b'0101'	0101b = 68.75%
2b'0110'	0110b = 62.5%
2b'0111'	0111b = 56.25%
2b'1000'	1000b = 50%
2b'1001'	1001b = 43.75%

2b'1010'	1010b = 37.5%
2b'1011'	1011b = 31.25%
2b'1100'	1100b = 25%
2b'1101'	1101b = 18.75%
2b'1110'	1110b = 12.5%
2b'1111'	1111b = 6.25%

6.7.8.Run mode and Hold mode

The driver has two stepper modes, RUN mode and HOLD mode.

RUN mode is the major used mode to drive stepper motor, the coil current changes along with the STEP / DIR updating.

In HOLD mode, STEP pulse is ignored and phase counter is hold during HOLD mode, thus the motor can be HOLD in place using a relatively low coil current.

Two methods allow device shift from RUN mode to HOLD mode.

- Set ***CONFIG_15*** register ***HOLD_MODE_EN*** bit = '1' to enter HOLD mode. On the contray, ***HOLD_MODE_EN*** bit =0 to exit HOLD mode
- If the coil voltage measurement function is enabled (***CONFIG_5*** register ***STALL_EN*** bit) and ***CONFIG_15*** register ***STALL_HOLD_EN*** bit is also set for precondition, when the sampled coil voltage is below CVLL threshold for the consecutive conversion number over ***CONFIG_5*** register ***CV_STALL_NUM[2:0]*** bits setting, then the ***STALL*** flag in ***STA_0*** register is asserted and the ***HOLD_MODE_EN*** bit is also automatically asserted to enter HOLD mode. In this condition, **STALL_HOLD_EN** bit setting must be cleared before **HOLD_MODE_EN** bit can be configured or reset to 0.

6.7.9.Stepper operation electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal current regulation						
t_{OFF}	Fixed off time in current regulation	TOFF_SEL[1:0] = '00'		7		μs
		TOFF _SEL[1:0] = '01'		16		μs
		TOFF _SEL[1:0] = '10'		24		μs
		TOFF _SEL[1:0] = '11'		32		μs
t_{BLANK} (1)	Current regulation blanking time	NSD8389		0.5		μs
		SR_SEL[1:0] = 'XX' & TBLANK_SR_EN bit = '0' in NSD8389A		0.5		μs
		SR_SEL[1:0] = '00' & TBLANK_SR_EN bit = '1' in NSD8389A		5.6		μs
		SR_SEL[1:0] = '01' & TBLANK_SR_EN bit = '1' in NSD8389A		2		μs
		SR_SEL[1:0] = '10' & TBLANK_EXT bit = '1' in NSD8389A		1.5		μs
		SR_SEL[1:0] = '11' & TBLANK_EXT bit = '1' in NSD8389A		0.86		μs
t_{FT} (1)	Current regulation filter timing	TFILTER[1:0] = '00'		0.5		μs
		TFILTER[1:0] = '01'		1		μs
		TFILTER[1:0] = '10'		2		μs
		TFILTER[1:0] = '11'		3		μs

(1) Guaranteed by digital scan

6.8. output stage, OUTA1/OUTA2, OUTB1/OUTB2

Each half bridge output stage is built by an internally connected high side and a low-side FET. Due to the integrated body diodes of the HS/LS output stage, inductive loads can be directly driven without external freewheeling diodes. To reduce the power dissipation during decay condition, the internal PWM controller will switch-on the output low side as synchronous rectification.

The half bridges are cross-current protected by an internal delay timing t_{CC} which depends on slew rate configuration (***SR_SEL[1:0]*** bits in ***CONFIG_1*** register)

6.8.1.Output stage electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output (OUTA1, OUTA2, OUTB1, OUTB2)						
$R_{DS(ON)}$	HS/LS FET on resistance	I = 0.5 A, Tj=25°C,		0.45		Ω
		I = 0.5 A, Tj=150°C,			0.9	Ω
t_{RISE}, t_{FALL},	Output rise time Output fall time High side or low side	VS = 13.5 V, SR_SEL[1:0]= ‘00’ resistive load 100 ohm,		10		V/µs
		VS = 13.5 V, SR_SEL[1:0]= ‘01’ resistive load 100 ohm,		35		V/µs
		VS = 13.5 V, SR_SEL[1:0]= ‘10’ resistive load 100 ohm,		50		V/µs
		VS = 13.5 V, SR_SEL[1:0]= ‘11’ resistive load 100 ohm,		100		V/µs
t_{CC}	Cross protection time, high to low / low to high. Test by digital scan	VS = 13.5 V, SR_SEL[1:0]= ‘00’ resistive load 100 ohm,		1.5		µs
		VS = 13.5 V, SR_SEL[1:0]= ‘01’ resistive load 100 ohm,		1		µs
		VS = 13.5 V, SR_SEL[1:0]= ‘10’ resistive load 100 ohm,		0.9		µs
		VS = 13.5 V, SR_SEL[1:0]= ‘11’ resistive load 100 ohm,		0.8		µs

6.9. Protection and diagnosis function

6.9.1.Overcurrent protection

The integrated overcurrent protection function provides the half bridge high side against short to ground or half bridge low side against short to battery.

The coil current passes the half bridge high side (VS -> highside -> OUTx) or flow into the half bridge low side (OUTx -> low side -> GND), once I_{OC} overcurrent threshold is exceeded, an overcurrent deglitch filter t_{OC} starts and internal overcurrent circuit also limits the short circuit current.

Upon the overcurrent condition last until t_{OC} expiration, overcurrent protection is triggered. Thus, the particular half bridge (including high side and low side) is disabled, and the OC status bit shall report the corresponding HS or LS which trigger OC, see ***STA_0*** & ***STA_1*** register description. nFault pin is also asserted to low.

For example, if only OUTA1 LS is short to battery and detected, then ***STA_1*** register ***OC_OUTA1_LS*** bit and ***STA_0*** register ***OC*** bit is asserted, OC status bit ***OC_OUTA1_HS*** or other corresponding OUTA2/OUTB1/OUTB2 bits are not impacted.

If ***OCP_MODE*** = '0', (default), during overcurrent protection state, the output stage is latched off, to resume normal driving, besides the overcurrent condition disappearing, it is also required to clear the ***OC*** status bit in ***STA0*** & ***STA1*** register by two methods (CLR_FLT bit '1' is written or EN pin receives fault clear short pulse).

If ***OCP_MODE*** = '1, after overcurrent happens, the relevant output stage is off for the duration t_{RETRY}, and then the device automatically resumes to work. While overcurrent fault is still present, the protection and auto-retry repeats; otherwise the device moves to normal operation state.

Anyhow if overcurrent condition short than t_{OC} deglitch filter, the OC event is not confirmed, and stepper/half bridge outputs keep normal status.

6.9.1.1. Overcurrent protection electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overcurrent protection						
I_{OC}	Over current threshold	Half bridge low side	2.0	2.7	3.7	A
		Half bridge high side	-3.7	-2.7	-2.0	A
t_{OC}	OC deglitch filter time(1)	VS < VS_OV_L		3		µs
		VS > VS_OV_H		1.5		
t_{RETRY}	Overcurrent retry time(1)	OCP_MODE=1		4		ms

(1) Guaranteed by digital scan

6.9.2.Over temperature warning and shut down

To protect power stage from overheat, dedicated thermal sensor is placed close to half bridge power stage, if the temperature increases above the OT_{WARN}, a temperature fault flag (***FAULT_TJ***) is set in SPI ***STA_0*** register, and also (***OTW***) in SPI ***STA_2*** register, while stepper / half bridge output operation is not impacted. Once the sensed temperature over the second higher OT_{SD} threshold, the corresponding ***OTSD*** flag is set and power FET channel is automatically disabled.

nFAULT pin can be configured for OT_{WARN} event report upon ***CONFIG_4*** register ***TW_NMASK_FLT*** bit setting to '1'. Anyhow OTSD will always asserted nFAULT to low.

For over temperature warning recovery, Both ***OTW*** / ***FAULT_TJ*** flag and nFAULT pin status, it is automatically cleared once temperature drops below OT_{WARN}-T_{HYS_OTW}.

For over temperature shutdown recovery,

- If ***OTSD_MODE*** = '0', (default), in order to reactive the output stage after OTSD and release nFAULT pin, the temperature drops below OT_{SD}-T_{HYS_OTSD}, and the thermal shutdown ***OTSD*** bit is cleared by CLR_FLT bit '1' is written or EN pin receives fault clear short pulse.
- If ***OTSD_MODE*** = '1', when the temperature drops below OT_{SD}-T_{HYS_OTSD}, the output stage is automatically recovery, while the thermal shutdown ***OTSD*** bit is latched until CLR_FLT bit '1' is written or EN pin receives fault clear short pulse.

6.9.2.1. Thermal protection electrical characteristics

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal protection						
OT_{WARN}	Thermal warning temperature (1)		135	150	165	°C
T_{HYS_OTW}	Thermal warning hysteresis			20		°C
OT_{SD}	Thermal shutdown temperature (1)		145	160	175	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis			20		°C

(1) OT_{WARN}, OT_{SD} threshold is not overlap.

6.9.3.Under temperature warning

If the device internal temperature falls below the under-temperature warning threshold, the ***UTW*** flag is set in SPI register ***STA_2***, *also* ***FAULT_TJ*** is set in SPI ***STA_0*** register, device operation is NOT impacted. When the temperature rises and exceeds the UTwarn + T_{HYS_UTW}, the ***UTW*** and ***FAULT_TJ*** flag is automatically cleared.

nFAULT pin can be also active for UTwarn event report upon ***CONFIG_4*** register ***TW_NMASK_FLT*** bit setting to '1'.

6.9.3.1. Under temperature warning electrical specifications

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Under temperature protection						
UT_{WARN}	Under temperature warning temperature		-30	-16	0	°C
T_{HYS_UTW}	Under temperature warning hysteresis			10		°C

6.9.4.Open load in ON state

The load current is monitored in each activated output stage for open load detection in ON state under stepper mode.

Starting from any PWM current regulation cycle, if the coil current is NOT reaching the current limit for at least t_{OL} for consecutive PWM cycles, the corresponding open load bit is set in status register (***OPL_OUTA*** or ***OPL_OUTB*** bit in ***STA2*** register, ***OPL*** bit in ***STA0*** register). The OL status bits (***STA0*** & ***STA2*** corresponding bits) are latched until CLR_FLT bit '1' is written or EN pin receives fault clear short pulse when open load condition is disappeared.

The open load is only as information flag and stepper operation not impacted. nFAULT pin is also asserted low once open load detected.

Note:

- For stepper application, the open load detection is not asserted in below condition
  i. Output driver disabled (DRV_DIS=1, TSD, OCP, CPUV, VSUV).
  ii. When the stepper motor position is 0°/ 180° (stop open load detection only in OUTA side, as OUTA coil current equals 0 in 0°/ 180°), 90°/ 270° (stop open load detection only in OUTB side, as OUTB coil current equals 0 in 90°/ 270°)
- ON state open load detection filter timing t_{OL} can be programmable (***OPL_FLT*** bit in ***CONFIG_5*** register)
- ON state open load detection can be disabled by ***OPL_ON_EN*** bit in ***CONFIG_4*** register, in case ON state open load not required.

6.9.4.1. open load electrical characteristics

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON state open load protection						
t_{OL}	Open load filter time (1)	NSD8389, OPL_ON_EN = 1b		200		ms
		NSD8389A, OPL_ON_EN = 1b, OPL_FILT = 00b		200		ms
		NSD8389A, OPL_ON_EN = 1b, OPL_FILT = 01b		125		ms
		NSD8389A, OPL_ON_EN = 1b, OPL_FILT = 10b		75		ms
		NSD8389A, OPL_ON_EN = 1b, OPL_FILT = 11b		3		ms

(1) Guaranteed by digital scan

6.9.5.Stall detection in stepper mode

As figure 6-9 & 6-10 shown, there is a clear relation between the coil current and stepper motor BEMF. When the motor load increases, the BEMF shifts and cause voltage difference at coil current equals 0. The NSD8389 takes advantage of this phenomenon. When the stepper motor position is 0°/ 180 °/ 90°/ 270 °, one coil current is typically programmed at zero amps, this makes it possible to measure the induced BEMF voltage through sampling the voltage across the motor terminal.

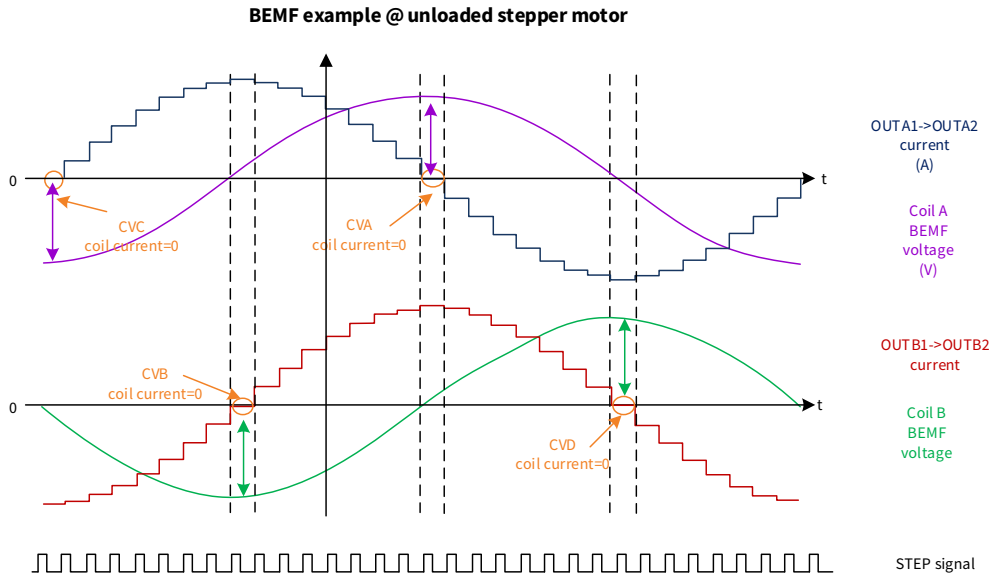


Figure 6-9. BEMF example in unloaded stepper motor

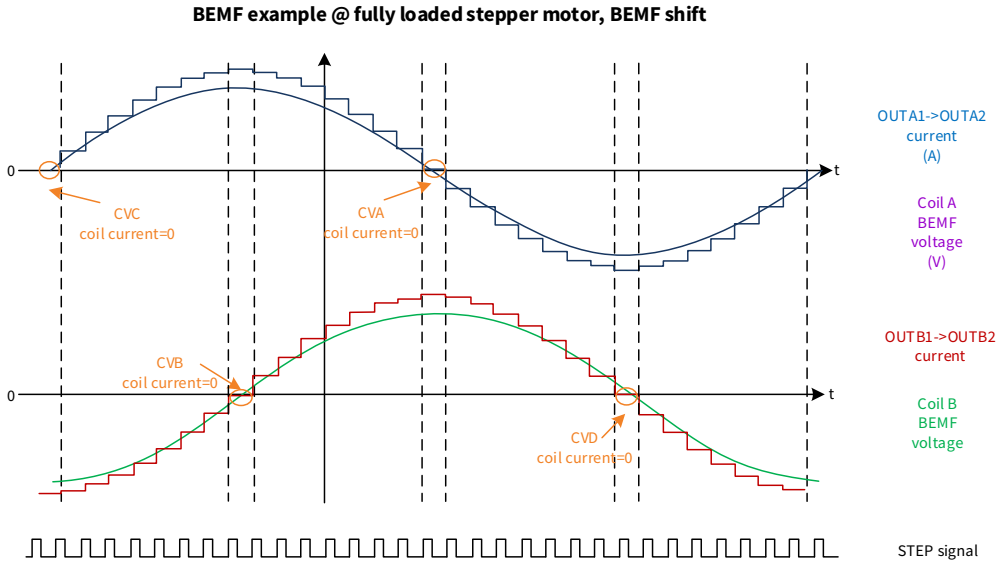


Figure 6-10. BEMF example in fully loaded stepper motor

As soon as the zero current step (0°/ 180 °/ 90°/ 270 °) starts, the half bridge PWM driving signals are switched off. If coil voltage conversion is enabled by SPI ***CONFIG_5*** register ***STALL_EN*** bit, after the cross current protection

timing, the opposite low side is switched on to measure the motor terminal voltage difference refer to GND. The four corresponding digital values are stored into SPI register CVA, CVB, CVC, CVD, as Table 6-9 explained.

Table 6-9. BEMF voltage conversion operation table

Step position	PHASE COUNTER PH[9:0]	DIR=0 (reverse, phase counter decreasing)		DIR=1 (forward, phase counter increasing)		SPI store register
		Switch on low side	Sampling	Switch on low side	Sampling	
0°	0010000000	OUTB2	OUTB1	OUTB1	OUTB2	CVB
90°	1110000000	OUTA1	OUTA2	OUTA2	OUTA1	CVA
180°	1010000000	OUTB1	OUTB2	OUTB2	OUTB1	CVD
270°	0110000000	OUTA2	OUTA1	OUTA1	OUTA2	CVC

The full scale BEMF measurement is range from min 150mV to max 28V, and the converted BEMF (CVA,CVB,CVC,CVD) is defined as below formula:

$$V_{BEMF} = \frac{\text{CVA or CVB or CVC or CVD, 8bit register decimal value} + 1}{256} \times V_{BEMF\_IN} \text{ set by CV\_GAIN}$$

6.9.5.1. BEMF voltage measurement sample point

Motor related operating condition, like motor speed & load torque, has effect on BEMF voltage and timing. The key of right detecting the stall condition is to sample the BEMF at the proper point.

CONFIG_14 register ***CV_DELAY[2:0]*** bits allow user to adjust the BEMF sample point by the number of PWM periods after zero current step starts.

Default setting of ***CV_DELAY[2:0]*** is '00000', it is defined as sampling the BEMF at the end of zero current step. This is useful for detection at continuous movement in fast speeds. To detect the stall condition at low speed, the sample point shall be close to the beginning of zero current step, in hence, ***CV_DELAY[2:0]*** setting value shall be not too high.

In case the phase counter update or step command is given before the ***CV_DELAY[2:0]*** PWM periods expired, the zero current step is extended and next step movement is delayed, until coil voltage conversion ready.

6.9.5.2. BEMF voltage measurement gain

The ***CV_GAIN[1:0]*** bit in the ***CONFIG_14*** register select the gain ratio (1x/2x/5x/10x). Multiplying the ratio by 2.5v gives the BEMF measurement full scale voltage range.

6.9.5.3. BEMF voltage measurement indicator CV_RDY signal / CV_REG_IND[1:0] bits

CV_REG_IND[1:0] bits in ***CONFIG_16*** register always report the last updated CVx register where the new conversion value stored.

Additionally, the device provides digital signal 'CV_RDY' output which indicates the coil voltage (BEMF) measurement is ready and available the respective CVx register. When the new conversion triggers, the CV_RDY signal goes from high to low, then it returns to high once the voltage measurement is updated.

CV_RDY signal can be mux on nFault pin, when ***CY_RDY_NMASK_FLT*** in ***CONFIG_15*** register is set.

6.9.5.4. BEMF voltage measurement comparison and stall detection

The threshold related to stall detection can be configured by SPI registers.

- ***CVLL*** (coil BEMF voltage low limit) -> recommend for the lowest threshold

Depending on the comparison result between coil BEMF voltage measurement value and the CVLL threshold, the device asserts and reports the corresponding flag bit.

- ***CVLLAF*** bit in ***CONFIG_16*** register is set if the coil conversion voltage is lower than CVLL threshold. It is automatically cleared when new value exceeds CVLL.

If the conversion value is lower than CVLL threshold for lasting over the number of consecutive conversions in zero current step, which equals the ***CV_STALL_NUM[2:0]*** bits in ***CONFIG_14*** register value, then the ***STALL*** flag bit in ***STA_0*** **&** ***STA_2*** is set.

Both ***CVLL*** and ***STALL*** flags do NOT impact device operating state.

STALL signal can be mux on nFault pin, if ***STALL_NMASK_FLT*** in ***CONFIG_5*** register is set.

6.9.5.5. BEMF voltage conversion electrical specification

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BEMF voltage adc conversion						
V_{BEMF_IN}	BEMF voltage adc measurement range	CV_GAIN[1:0] = '00', ratio 1x		2.5		V
		CV_GAIN[1:0] = '01', ratio 2x		5		V
		CV_GAIN[1:0] = '10', ratio 5x		12.5		V
		CV_GAIN[1:0] = '11', ratio 10x		25		V
V_{BEMF_RES}	BEMF voltage adc measurement resolution (LSB)	Design information, CV_GAIN[1:0] = '00'		9.8		mV
V_{BEMF_ERR}	BEMF voltage adc measurement error			+/- 3		LSB

6.9.6. Fault table summary

FAULT EVENT	Condition	Configuration	ERR indicator	Output status	Charge pump	Digital logic	SPI Comm	Recovery action
VSx UV	VS < VS_UV_L	NA	a.VSUV bit in STA_0 b. nFAULT is asserted to low	OFF	OFF	Normal	Normal	Power stage output, charge pump and internal translator automatically recover when VS>VS_UV_H rising edge. VSUV flag remains latch until CLR_FLT bit '1' is written or EN pin is received fault clear short pulse.
VSx POR	VS < VS_RST_L	NA	NA	OFF	OFF	RESET	OFF	Automatically work after VS > VS_RST_H
VSx OV	VS > VS_OV_H	NA	VSOV bit in CONFIG_16	Normal	Normal	Normal	Normal	NA
VDDIO POR	VDDIO < $V_{VDDIO\_RST\_L}$	NA	NA	OFF	OFF	RESET	OFF	Automatically get back to work after VDDIO > $V_{VDDIO\_RST\_H}$
CP UV	$V_{CP} < V_{CP\_UV}$	NA	a. CPUV bit in STA_0 b. nFAULT is asserted to low	OFF	Normal	Normal	Normal	Output stage automatically recovery if $V_{CP} > V_{CP\_UV}$ with t_{CP_UV}. CPUV flag keeps latch until CLR_FLT bit '1' is written or EN pin is received fault clear short pulse.
OCP	IOUT > I_{OC}	OCP_MODE=0 (default)	a. OC bit in STA_0 b. OCP_OUTA1_HS or OCP_OUTA1_LS or OCP_OUTA2_HS or OCP_OUTA2_LS or OCP_OUTB1_HS or OCP_OUTB1_LS or OCP_OUTB2_HS or OCP_OUTB2_LS bits in STA_1 b. nFAULT is asserted to low	HIZ	Normal	Normal	Normal	The relevant OC flags, output stages off are latched until CLR_FLT bit '1' is written or EN pin is received fault clear short pulse and OC condition removed.
		OCP_MODE=1		HIZ	Normal	Normal	Normal	Output stages get back to work automatically with t_{RETRY} interval
OPEN LOAD (ON MODE)	Load open / not connected	OPL_ON_EN=1	a. OPL bit in STA_0 b. OPL_OUTA or OPL_OUTB bits in STA_2 b. nFAULT is asserted to low	Normal	Normal	Normal	Normal	Stepper operation is not impact during open load condition. The open load status bits OPL / OPL_OUTA / OPL_OUTB keep latch until CLR_FLT bit '1' is written or EN pin is received fault clear short pulse.
STALL	Motor stuck	STALL_NMASK_FLT = 0	STALL bit in STA_0 & STA_2	Normal	Normal	Normal	Normal	STALL flag can be cleared by CLR_FLT bit '1' is written or EN pin is received fault clear short pulse, after BEMF voltage conversion value is higher than CVLL setting value.
		STALL_NMASK_FLT = 1 (default)	a. STALL bit in STA_0 & STA_2 b. nFAULT is asserted to low	Normal	Normal	Normal	Normal	

OTSD	Tj > OT_{SD}	OTSD_MODE=0 (default)	a. FAULT_TJ in STA_0 b. OTSD bit in STA_2 c. nFAULT is asserted to low	OFF	OFF	Normal	Normal	FAULT_TJ & OTSD flag, output stage off and charge pump off are latched until CLR_FLT bit '1' is written or EN pin is received fault clear short pulse after Tj < OT_{SD} - T_{HYS_OTSD}
		OTSD_MODE=1		OFF	OFF	Normal	Normal	Automatically recovery of output and charge pump after Tj < OT_{SD} - T_{HYS_OTSD} . FAULT_TJ & OTSD flag keep latch until CLR_FLT bit '1' is written or EN pin is received fault clear short pulse
OTWARN	Tj > OT_{WARN}	TW_NMASK_FLT =0 (default)	OTW bit in STA_2	Normal	Normal	Normal	Normal	Automatically clear of OTW bit when Tj < OT_{WARN} - T_{HYS_OTW}
		TW_NMASK_FLT =1	a. OTW bit in STA_2 b. nFAULT is asserted to low	Normal	Normal	Normal	Normal	
UTWARN	Tj < UT_{WARN}	TW_NMASK_FLT =0 (default)	UTW in STA_2	Normal	Normal	Normal	Normal	Automatically clear of UTW bit Tj > UT_{WARN} + T_{HYS_UTW}
		TW_NMASK_FLT =1	a. UTW bit in STA_2 b. nFAULT is asserted to low	Normal	Normal	Normal	Normal	

6.10. SPI interface

The following table summarizes the SPI interface designed.

Table 6-10. SPI Interface quick look

Parameter	Description
Protocol	in frame
Single Frame Length	16 bit, MSB first
Frame protection	frame length check
Max. Frequency	10 MHz
CPOL	0
CPHA	1
Master/Slave configuration	Slave

The falling edge of NCS defines the start of the SPI frames. It samples the SDI line at the falling edge of SCK, while the output data is shifted out on SDO line at the rising edge of SCK (CPOL= '0' CPHA = '1'). The end of SPI frame is defined by a rising edge of NCS.

6.10.1. Frame Length Check

For each command received, the SPI peripheral checks the number of clock edges at SCK pin. If the total number of edges is not a multiple of 16, the frame content is discarded and an SPI_ERR bit will be returned upon next iteration.

6.10.2. Error Frame

In case one of the following errors occurs, the SPI_ERR diagnosis bit will be returned upon next communication iteration:

- Frame Length error

6.10.3. SPI Frame structure

Each SDI input frame has 24 bits with the following structure:

- 2-bit operation code C1 / C0
  - '00' for write operation,
  - '01' for read operation,
- 5-bit ADDRESS, A[4] to A[0], represent REG_ADDR + 1-bit don't care
- 8-bit DATA, including D7~D0 bit

Table 6-11. SPI SDI frame

	MSB								LSB
BIT	15	14	13	12	11	10	9	8	[7:0]
SDI	C1	C0	A[4]	A[3]	A[2]	A[1]	A[0]	X	DATA

Register frame SDO responses the selected address and register content bit values. It has with the following structure:

- 2bit, ‘11’ , reserved
- 6bits, VSUV, CPUV event, Overtemperature and power stage status OC, OPL, STALL
- 8-bit return data

	MSB								LSB
BIT	15	14	13	12	11	10	9	8	[7:0]
SDO	1	1	VSUV	CPUV	OC	STALL	FAULT_TJ	OPL	DATA

Table 6-12. SPI SDO frame

Note:

- A SPI SDI frame given example of reading STA_1 register (REG_ADDR 0x01) is group as below:

  ‘01’ + ‘00001’ + ‘0’ + ‘00000000’ -> sending 0x 42 00

- Bit 8 in SDI frame, labelled as ‘1-bit don’t care’, can be set to either ‘0’ or ‘1’, but cannot be omitted.

6.10.4. Parallel and multi-devices communication

SPI communication between microcontroller (SPI master) and multiple these devices (slave) can be operated in parallel or in daisy chain

Parallel operation: several slave devices are connected to one SPI channel, which share communication lines SDI, SDO and SCK, but every slave connects dedicated own NCS.

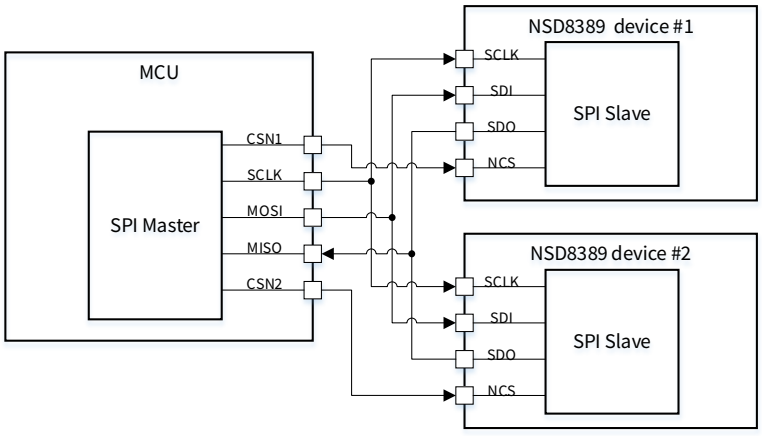


Figure 6-11. SPI in parallel connection

Daisy chain operation:

multi devices are connected with shared one NCS and SCK, while each device SDI and SDO are daisy-chain connected. An example of 3 devices in daisy chain as below figure 6-12:

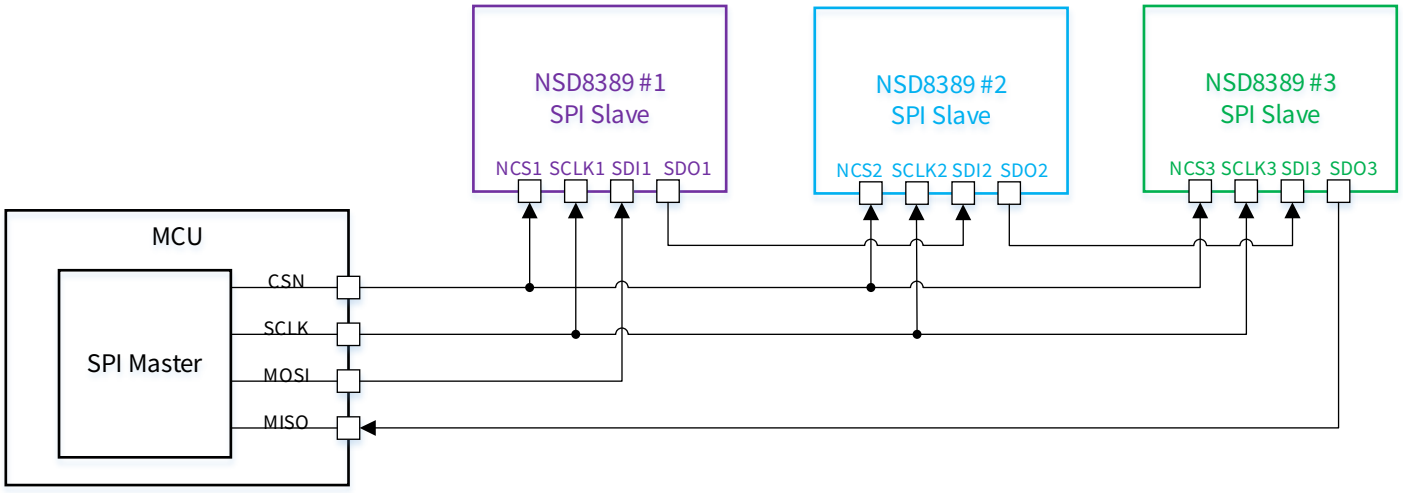
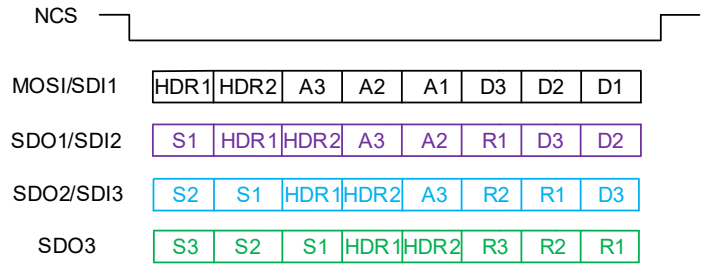


Figure 6-12. SPI in daisy chain connection for 3 device

The SPI format for daisy chain SPI operation as below, A1~A3, D1~D3, S1~S3, R1~R3 have same meaning/definition with single device operation described



There are two header bytes dedicated for daisy chain operation

- HDR1 byte contain information of the number of devices connected in the chain by N5~N0 bits, so device support up to 63 devices, other bits are fixed. For example, 3 device in daisy chain connection, N5~N0 bits should set as '000011'.
- HDR2 byte contain CLR bit which can trigger SPI clear command for all device in daisy chain, other bits are fixed (bit7 and bit6) or not care(bit0~bit4)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HDR1	1	0	N5	N4	N3	N2	N1	N0

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HDR2	1	0	CLR	X	X	X	X	X

Note: Internal logic will count number of status bytes it receives before HDR1 and HDR2 to know the position of itself in the chain, also by HDR1 it knows how many devices in the chain, so it only loads the relevant address and data byte in its buffer and bypass the other bytes.

6.10.5. SPI Physical Layer

It implements an SPI Slave with the following timing requirements:

Figure 6-13. SPI Timing Diagram

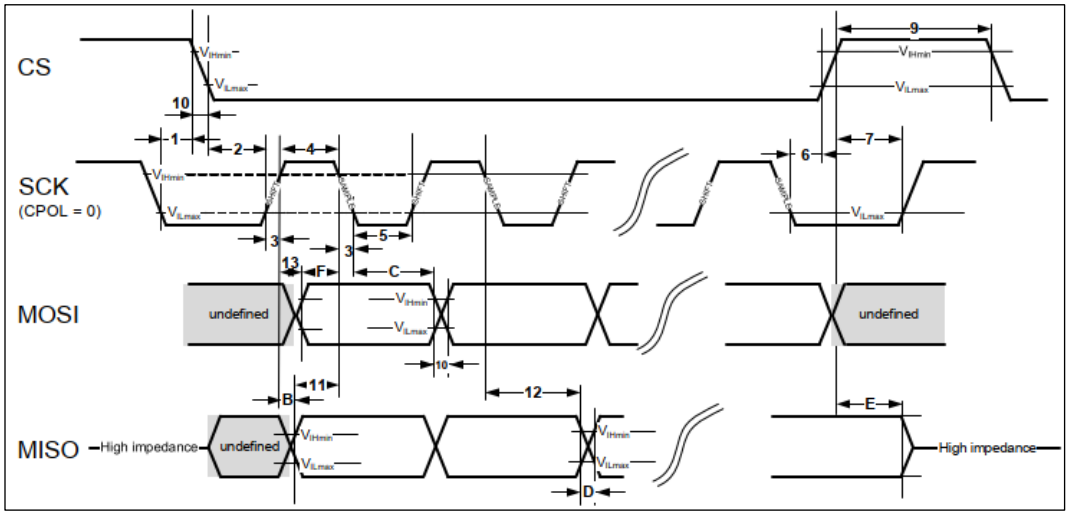


Table 6-13. SPI AC Characteristics

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{cll}	Minimum time CLK = LOW (5)	Application info	37			ns
T_{clh}	Minimum time CLK = HIGH (4)	Application info	37			ns
T_{pcld}	Propagation delay (SCLK to data at SDO active) (B)	Cload=30pF			30	ns
T_{lead}	CLK change L/H after NCS = LOW (2)	Application info	100			ns
T_{scld}	SDI input setup time (CLK change H/L after SDI data valid) (F)	Application info	25			ns
T_{hcld}	SDI input hold time (SDI data hold after CLK change H/L) (C)	Application info	25			ns
T_{sclch}	CLK low before NCS low (1)	Application info	125			ns
T_{lag}	CLK low before NCS high (6)	Application info	25			ns
T_{hclch}	CLK high after NCS high	Application info	25			ns
T_{onncs}	NCS min high time (9)	Application info	450			ns

T_{pchdz}	NCS L/H to SDO @ high impedance (E)	Cload=30pF			50	ns
F_{CLK_SPI}	CLK frequency (50% duty cycle)	Application info			10	MHz

6.10.6. Registers map

Table 6-14. Registers map table

SECT	REG_NAME	REG_ADDR	bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Status registers	STA_0	0x00	FAULT	SPI_ERROR	VSUV	CPUV	OC	STALL	FAULT_TJ	OPL
	STA_1	0x01	OC_OUTB2_LS	OC_OUTB2_HS	OC_OUTB1_LS	OC_OUTB1_HS	OC_OUTA2_LS	OC_OUTA2_HS	OC_OUTA1_LS	OC_OUTA1_HS
	STA_2	0x02	UTW	OTW	OTSD	Reserved	STALL	Reserved	OPL_OUTB	OPL_OUTA
Control registers	CONFIG_1	0x03	IFS_DAC[3:0]				Reserved	Reserved	SR_SEL[1:0]	
	CONFIG_2	0x04	DRV_DIS	Reserved	Reserved	TOFF_SEL[1:0]		DECAY_SEL[2:0]		
	CONFIG_3	0x05	DIR	STEP	SPI_DIR	SPI_STEP	STEPPER_MODE[3:0]			
	CONFIG_4	0x06	CLR_FLT	LOCK[2:0]			OPL_ON_EN	OCP_MODE	OTSD_MODE	TW_NMASK_FLT
	CONFIG_5	0x07	Reserved	Reserved	Reserved	STALL_EN	STALL_NMASK_FLT	OPL_FILT[1:0]		TBLANK_SR_EN
	CONFIG_6	0x08	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CONFIG_7	0x09	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CONFIG_8	0x0A	Reversed	Reserved	Reserved	Reserved	DEVICE_ID[3:0]			
	CONFIG_9	0x0B	CVA[7:0]							
	CONFIG_10	0x0C	CVB[7:0]							
	CONFIG_11	0x0D	CVC[7:0]							
	CONFIG_12	0x0E	CVD[7:0]							
	CONFIG_13	0x0F	CVLL[7:0]							
	CONFIG_14	0x10	CV_DELAY[2:0]			CV_STALL_NUM[2:0]			CV_GAIN[1:0]	
	CONFIG_15	0x11	DITHER_EN[2:0]			HOLD_MODE_EN	STALL_HOLD_EN	CV_RDY_NMASK_FLT	TFILTER[1:0]	
	CONFIG_16	0x12	VSOV	CV_REG_IND[1:0]		CVLLF	Reserved	Reserved	PH[9:8]	
	CONFIG_17	0x13	PH[7:0]							
	CONFIG_18	0x14	TJ[7:0]							
	CONFIG_19	0x15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PH_CLR

6.10.7. SPI – status and control registers

Table 6-15. STA_0 status register (REG_ADDR = 0x00)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	FAULT	SPI_ERROR	VSUV	CPUV	OC	STALL	FAULT_TJ	OPL
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-1. STA_0 status register description

Bit	Field Name	Description
7	FAULT	Link with nfault pin status. When nFAULT pin is at High (external pull up), FAULT logic bit is '0'. When nFAULT pin is at Low (external pull up), FAULT logic bit is '1'
6	SPI_ERROR	1 : SPI communication error happens 0' : SPI communication has no fault.
5	VSUV	0: No VS undervoltage detected (default value) 1: VS undervoltage detected. Error latched and all outputs disabled.
4	CPUV	0: No VCP undervoltage detected (default value) 1: Charge pump output undervoltage detected. Error latched and all outputs disabled.
3	OC	0: No overcurrent detected (default value) 1: overcurrent detected in at least one of power stages. Error latched and all outputs disabled.
2	STALL	0: No stall detected (default value) 1: Stall detected . Error flag latched
1	FAULT_TJ	OR combined logic of UTW, OTWARN, OTSD 0: No internal temperature fault detected (default value) 1: Temperature fault detected, at least one of UTW, OTWARN, OTSD happens.
0	OPL	OR combined logic of open load detected in OUTA1, OUTA2, OUTB1, OUTB2 0: No open load in OUTA / OUTB detected (default value) 1: Open load detected . Error flag latched

Table 6-2. STA_1 status register (REG_ADDR = 0x01)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	OC_OUTB2_LS	OC_OUTB2_HS	OC_OUTB1_LS	OC_OUTB1_HS	OC_OUTA2_LS	OC_OUTA2_HS	OC_OUTA1_LS	OC_OUTA1_HS
Operation Type	RO	RO	RO	RO -	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-3. STA_1 status register description

Bit	Field Name	Description
7	OC_OUTB2_LS	0: No overcurrent in OUTB2 low side detected (default value) 1: Overcurrent detected in OUTB2 low side. Error flag latched
6	OC_OUTB2_HS	0: No overcurrent in OUTB2 high side detected (default value) 1: Overcurrent detected in OUTB2 high side. Error flag latched
5	OC_OUTB1_LS	0: No overcurrent in OUTB1 low side detected (default value) 1: Overcurrent detected in OUTB1 low side. Error flag latched
4	OC_OUTB1_HS	0: No overcurrent in OUTB1 high side detected (default value) 1: Overcurrent detected in OUTB1 high side. Error flag latched
3	OC_OUTA2_LS	0: No overcurrent in OUTA2 low side detected (default value) 1: Overcurrent detected in OUTA2 low side. Error flag latched
2	OC_OUTA2_HS	0: No overcurrent in OUTA2 high side detected (default value) 1: Overcurrent detected in OUTA2 high side. Error flag latched
1	OC_OUTA1_LS	0: No overcurrent in OUTA1 low side detected (default value) 1: Overcurrent detected in OUTA1 low side. Error flag latched,

0	OC_OUTA1_HS	0: No overcurrent in OUTA1 high side detected (default value) 1: Overcurrent detected in OUTA1 high side. Error flag latched,

Table 6-19. STA_2 status register (REG_ADDR = 0x02)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	UTW	OTW	OTSD	Reserved	STALL	Reserved	OPL_OUTB	OPL_OUTA
Operation Type	RO	RO	RO	RO -	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-20. STA_2 status register description

Bit	Field Name	Description
7	UTW	0: under temperature not happen (default value) 1: under temperature happens
6	OTW	0: No over temperature warning (default value) 1: over temperature warning detected.
5	OTSD	0: No over temperature shut down (default value) 1: Over temperature shut down detected. Error flag latched
4	Reserved	0: reversed (default value).
3	STALL	0: No stall detected (default value) 1: Stall detected . Error flag latched
2	Reserved	0: reversed (default value).
1	OPL_OUTB	0: No open load in OUTB detected (default value) 1: Open load in OUTB detected. Error flag latched.
0	OPL_OUTA	0: No open load in OUTA detected (default value) 1: Open load in OUTA detected. Error flag latched.

Table 6-21. CONFIG_1 control register (REG_ADDR = 0x03)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	IFS_DAC[3:0]				Reserved	Reserved	SR_SEL[1:0]	
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Table 6-4. CONFIG_1 register description

Bit	Field Name	Description
7 6 5 4	IFS_DAC[3:0]	0000b = 100% (default) 0001b = 93.75% 0010b = 87.5% 0011b = 81.25% 0100b = 75% 0101b = 68.75% 0110b = 62.5% 0111b = 56.25% 1000b = 50% 1001b = 43.75% 1010b = 37.5% 1011b = 31.25% 1100b = 25% 1101b = 18.75% 1110b = 12.5% 1111b = 6.25%
3	Reserved	0: reversed (default value).
2	Reserved	0: reversed (default value).
1 0	SR_SEL[1:0]	OUTA, OUTB slew rate selection 00: 10v/us (default value) 01: 35v/us 10: 50v/us 11: 100v/us"

Table 6-5. CONFIG_2 control register (REG_ADDR = 0x04)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DRV_DIS	Reserved	Reserved	TOFF_SEL[1:0]		DECAY_SEL[2:0]		
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0/1 (1)	0	0	0	1	1	1	1

Table 6-6. CONFIG_2 register description

Bit	Field Name	Description
7	DRV_DIS	0: all output enable 1: all output disable --- Note: (1) default value of DRV_DIS bit in NSD8389 is '0' default value of DRV_DIS bit in NSD8389A is '1' ---
6	Reserved	0: Reversed (default value).
5	Reserved	0: Reversed (default value).
4	TOFF_SEL[1:0]	00: 7us 01: 16us (default value) 10: 24us 11: 32us
3		
2	DECAY_SEL[2:0]	000b = Increasing SLOW, decreasing SLOW 001b = Increasing SLOW, decreasing MIXED 30% 010b = Increasing SLOW, decreasing MIXED 60% 011b = Increasing SLOW, decreasing FAST 100b = Increasing MIXED 30%, decreasing MIXED 30% 101b = Increasing MIXED 60%, decreasing MIXED 60% 110b = Auto decay 111b = Auto decay with ripple control (default value)
1		
0		

Table 6-7. CONFIG_3 control register (REG_ADDR = 0x05)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DIR	STEP	SPI_DIR	SPI_STEP	STEPPER_MODE[3:0]			
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Table 6-26. CONFIG_3 register description

Bit	Field Name	Description
7	DIR	When SPI_DIR =1, SPI DIR bit controls the direction. 0: counter-clockwise (default value) 1: clockwise "
6	STEP	When SPI_STEP=1, writing SPI STEP bit =1 causes internal logic translator to advance one step. This bit is automatically becomes '0' after writing '1' command is executed .
5	SPI_DIR	0: internal logic translator direction follows DIR input pin (default value) 1: internal logic translator direction follows SPI DIR bit
4	SPI_STEP	0: internal logic translator movement follows STEP input pin (default value) 1: internal logic translator movement follows SPI STEP bit
3 2 1 0	STEPPER_MODE [3:0]	0000 = Full step with 100% current (default value) 0001 = Full step with 71% current 0010 = Non-circular 1/2 step 0011 = 1/2 step 0100 = 1/4 step 0101 = 1/8 step 0110 = 1/16 step 0111 = 1/32 step 1000 = 1/64 step 1001 = 1/128 step 1010 = 1/256 step 1011 to 1111 = Reserved

Table 6-8. CONFIG_4 control register (REG_ADDR = 0x06)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CLR_FLT	LOCK[2:0]			OPL_ON_EN	OCP_MODE	OTSD_MODE	TW_NMASK_FLT
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	1	1	0	0	0	0

Table 6-9. CONFIG_4 register description

Bit	Field Name	Description
7	CLR_FLT	Writing SPI CLR_FLT bit =1 causes internal logic to clear all latched fault bits. This bit is automatically becoming '0' after writing '1' command is executed.
6 5 4	LOCK[2:0]	011: unlock all register writing operation (default value) 110: lock all register, writing command is ignored, excepted CLR_FLT bit
3	OPL_ON_EN	0: disable OUTA/OUTB ON state OPL diagnosis (default value) 1: enable OUTA/OUTB ON state OPL diagnosis
2	OCP_MODE	0: OCP latch (default value) 1: OCP auto retry"
1	OTSD_MODE	0: OTSD latch (default value) 1: OTSD automatic recovery
0	TW_NMASK_FLT	0: OTW or UTW is not reported on nFAULT pin (default value) 1: Both OTW and UTW are reported on nFAULT pin.

Table 6-10. CONFIG_5 control register (REG_ADDR = 0x07)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved	Reserved	Reserved	STALL_EN	STALL_NMASK_FLT	OPL_FILT[1:0]		TBLANK_SR_EN
Operation Type	RO	RW	RO	RW	RW	RW	RW	RW
Default	0	0	0	0	1	0	0	0

Table 6-11. CONFIG_5 register description

Bit	Field Name	Description
7	Reserved	0: Reversed (default value).
6	Reserved	0: Reversed (default value).
5	Reserved	0: Reversed (default value).
4	STALL_EN	0: Disable stall detection (default value) 1: Enable stall detection, also related function (output mux, ADC sample & comparison)
3	STALL_NMASK_FLT	0: Stall is not reported on nFault pin 1: Stall is reported on nFAULT pin (default value)
2 1	OPL_FLT[1:0]	00: 200ms (max) open load detection filter timing (default value) 01: 125ms (max) open load detection filter timing 10: 75ms (max) open load detection filter timing 11: 3ms (max) open load detection filter timing --- Note: OPL_FLT[1:0] configurable options work in NSD8389A, while open load filter timing is fixed at 200ms in NSD8389 ---
0	TBLANK_SR_EN	0: tblank fixed 0.5us (default value) 1: tblank relative to slew rate setting --- Note: TBLANK_SR_EN selection bit works in NSD8389A, while tblank timing is fixed at 0.5us in NSD8389 ---

Table 6-12. CONFIG_6 control register (REG_ADDR = 0x08)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Table 6-13. CONFIG_6 register description

Bit	Field Name	Description
7 6 5 4 3 2 1 0	Reserved	0: Reversed (default value).

Table 6-14. CONFIG_7 register (REG_ADDR = 0x09)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-15. CONFIG_7 register description

Bit	Field Name	Description
7	Reserved	0: Reversed (default value).
6		
5		
4		
3		
2		
1		
0		

Table 6-16. CONFIG_8 register (REG_ADDR = 0x0A)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved	Reserved	Reserved	Reserved	DEVICE_ID[3:0]			
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	X	X	0	0

Table 6-17. CONFIG_8 register description

Bit	Field Name	Description
7	Reserved	0: Reversed (default value).
6		
5		
4		
3	DEVICE_ID[3:0]	Default value depends on device internal configuration. Device ID bits ('1100' NSD8389A, '1000' NSD8389) .
2		
1		
0		

Table 6-18. CONFIG_9 register (REG_ADDR = 0x0B)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVA[7:0]							
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-19. CONFIG_9 register description

Bit	Field Name	Description
7	CVA[7:0]	Coil BEMF voltage conversion digital value at phase counter 0° $V_{BEMF} = \frac{8bit\ register\ decimal\ value + 1}{256} \times V_{BEMF\_IN}$ set by CV_GAIN
6		
5		
4		
3		
2		
1		
0		

Table 6-20. CONFIG_10 register (REG_ADDR = 0x0C)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVB[7:0]							
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-21. CONFIG_10 register description

Bit	Field Name	Description
7	CVB[7:0]	Coil BEMF voltage conversion digital value at phase counter 90° $V_{BEMF} = \frac{8bit\ register\ decimal\ value + 1}{256} \times V_{BEMF\_IN}$ set by CV_GAIN
6		
5		
4		
3		
2		
1		
0		

Table 6-22. CONFIG_11 register (REG_ADDR = 0x0D)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVC[6:0]							
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-23. CONFIG_11 register description

Bit	Field Name	Description
7	CVC[7:0]	Coil BEMF voltage conversion digital value at phase counter 180° $V_{BEMF} = \frac{8bit\ register\ decimal\ value + 1}{256} \times V_{BEMF\_IN}$ set by CV_GAIN
6		
5		
4		
3		
2		
1		
0		

Table 6-24. CONFIG_12 register (REG_ADDR = 0x0E)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVD[7:0]							
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-25. CONFIG_12 register description

Bit	Field Name	Description
7	CVD[7:0]	Coil BEMF voltage conversion digital value at phase counter 270° $V_{BEMF} = \frac{8bit\ register\ decimal\ value + 1}{256} \times V_{BEMF\_IN}$ set by CV_GAIN
6		
5		
4		
3		
2		
1		
0		

Table 6-26. CONFIG_13 register (REG_ADDR = 0x0F)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVLL[7:0]							
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Table 6-27. CONFIG_13 register description

Bit	Field Name	Description
7 6 5 4 3 2 1 0	CVLL[7:0]	Coil voltage low limit threshold setting $V_{CVLL} = \frac{8\text{bit register decimal value} + 1}{256} \times V_{BEMF\_IN}$ set by CV_GAIN CVLLF flag is asserted, if the last conversion voltage below CVLL[7:0] setting. Otherwise, CVLLF flag is cleared.

Table 6-28. CONFIG_14 control register (REG_ADDR = 0x10)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CV_DELAY[2:0]			CV_STALL_NUM[2:0]			CV_GAIN[1:0]	
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	1

Table 6-29. CONFIG_14 register description

Bit	Field Name	Description
7 6 5	CV_DELAY[2:0]	Coil voltage conversion delay timing configuration 000b: sample the coil voltage at the end of zero current step 001b: sample the coil voltage, 100us after zero current starts 010b: sample the coil voltage, 200us after zero current starts 011b: sample the coil voltage, 400us after zero current starts 100b: sample the coil voltage, 800us after zero current starts 101b: sample the coil voltage, 1600us after zero current starts 110b: sample the coil voltage, 3200us after zero current starts 111b: sample the coil voltage, 6400us after zero current starts
4 3 2	CV_STALL_NUM[2:0]	Coil voltage conversion number configuration for stall detection It sets the required number of coil voltage consecutive conversion which bellows CVLL until stall detection asserted. The minimum value is 1, even CV_STALL_NUM[2:0] is configured to 0. 000b: 1 001b: 1 010b: 2 011b: 3 100b: 4 101b: 5 110b: 6 111b: 7
1 0	CV_GAIN[1:0]	00b: gain = 1, V_{BEMF_IN} range 2.5V 01b: gain = 2, V_{BEMF_IN} range 5V (default value) 10b: gain = 5, V_{BEMF_IN} range 12.5V 11b: gain = 10, V_{BEMF_IN} range 25V

Table 6-30. CONFIG_15 control register (REG_ADDR = 0x11)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DITHER_EN[2:0]			HOLD_MODE_EN	STALL_HOLD_EN	CV_RDY_NMASK_FLT	TFILTER[1:0]	
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Table 6-31. CONFIG_15 register description

Bit	Field Name	Description
7 6 5	DITHER_EN[2:0]	Internal OSC spread spectrum configuration: 000: spread spectrum disable. (default value) 001: modulation frequency 15.625k, spread spectrum deviation +/- 3% 010: modulation frequency 15.625k, spread spectrum deviation +/- 6% 011: modulation frequency 15.625k, spread spectrum deviation +/- 12% 100: modulation frequency 62.5k, spread spectrum deviation +/- 3% 101: modulation frequency 62.5k, spread spectrum deviation +/- 6% 110: modulation frequency 62.5k, spread spectrum deviation +/- 12% 111: spread spectrum disable.
4	HOLD_MODE_EN	0: HOLD mode disabled (default value) 1: HOLD mode enable
3	STALL_HOLD_EN	Automatic hold mode enable configuration during stall event detected 0: Not automatically enter HOLD mode when stall event detected (default value) 1: Automatically enter HOLD mode when HOLD_EN bit =1 and stall event detected
2	CV_RDY_NMASK_FLT	0: CV_RDY signal is not reported on nFault pin (default value) 1: CV_RDY is reported on nFAULT pin
1 0	TFILTER[1:0]	Current regulation tfilter selection 00: 0.5us (default value) 01: 1us 10: 2us 11: 3us

Table 6-32. CONFIG_16 register (REG_ADDR = 0x12)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VSOV	CV_REG_IND[1:0]		CVLLF	Reserved	Reserved	PH[9:8]	
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-33. CONFIG_16 register description

Bit	Field Name	Description
7	VSOV	0: No VS overvoltage detected (default value) 1: VS overvoltage detected.
6 5	CV_REG_IND	Last coil voltage conversion store register 00: CVB 01: CVC 10: CVD 11: CVA
4	CVLLF	0: No conversion voltage CVA / CVB / CVC / CVD under CVLL low limit A detected (default value) 1: Conversion voltage CVA or CVB or CVC or CVD, one or multiple, under CVLL low limit detected.
3	Reserved	0: Reversed (default value).
2	Reserved	0: Reversed (default value).
1 0	PH[9:8]	Phase counter values bit9~bit8 in stepper mode, it relates to the current profile applied on OUTA / OUTB and reports the step position

Table 6-53. CONFIG_17 register (REG_ADDR = 0x13)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PH[7:0]							
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-54. CONFIG_17 register description

Bit	Field Name	Description
7	PH[7:0]	Phase counter values bit7~bit0 in stepper mode, it relates to the current profile applied on OUTA / OUTB and reports the step position
6		
5		
4		
3		
2		
1		
0		

Table 6-55. CONFIG_18 register (REG_ADDR = 0x14)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TJ[7:0]							
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-56. CONFIG_18 register description

Bit	Field Name	Description
7	TJ[7:0]	Junction temperature calculation formula: Tj = 2.015 * TJ[7:0] – 283.3
6		
5		
4		
3		
2		
1		
0		

Table 6-57. CONFIG_19 register (REG_ADDR = 0x15)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PH_CLR
Operation Type	RO	RO	RO	RO	RO	RO	RO	RW
Default	0	0	0	0	0	0	0	0

Table 6-58. CONFIG_19 register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value).
6		
5		
4		
3		
2		
1		
0	PH_CLR	0: phase counter not impact （default value） 1: when CONFIG4 lock<2:0> = 0b'011', setting PH_CLR=1 will reset internal phase counter to home state. Note: be careful about the usage of phase counter reset function, due to phase counter value is directly linked with AOUT / BOUT output state and driving current.

7. Application Diagram

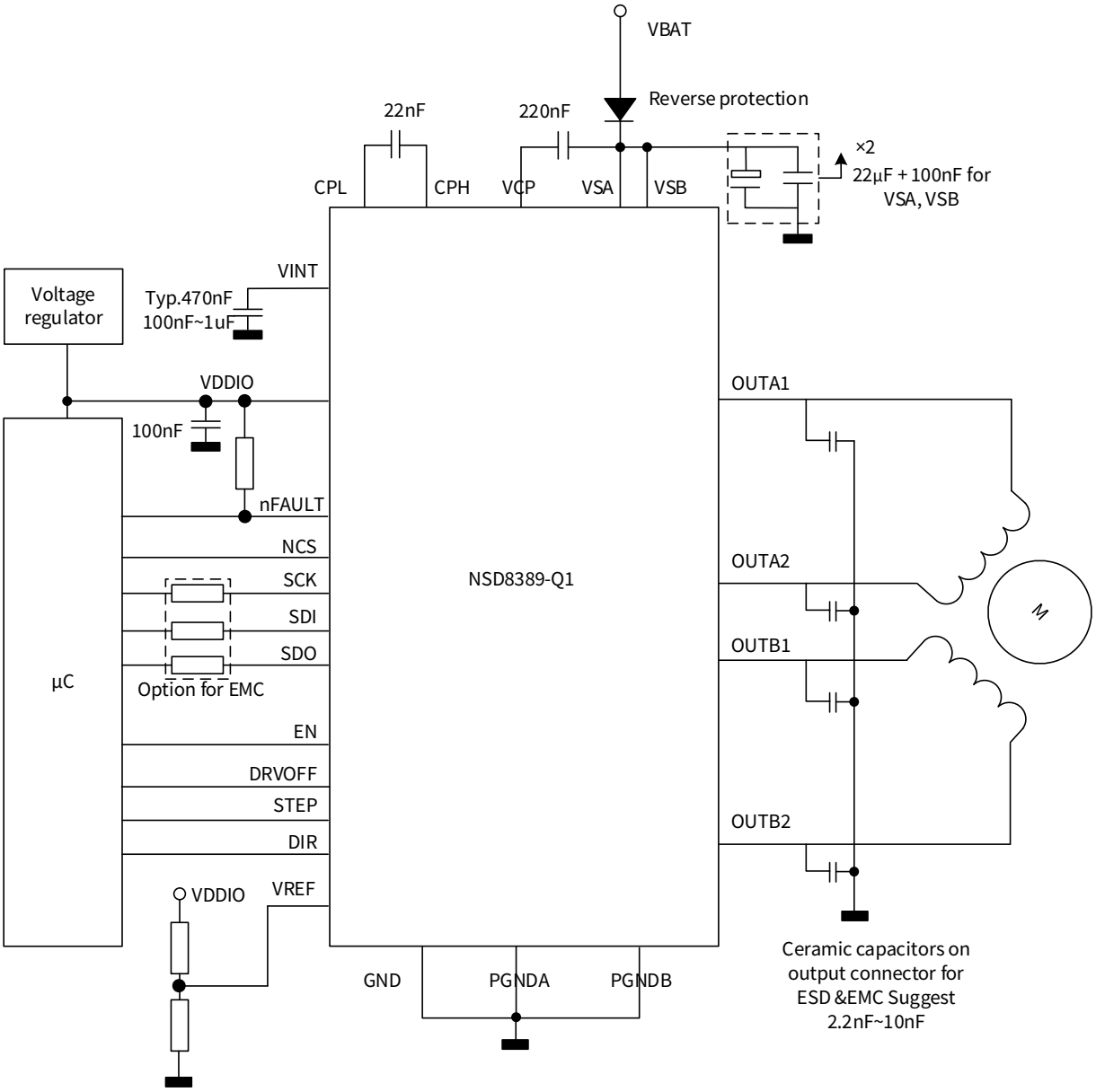
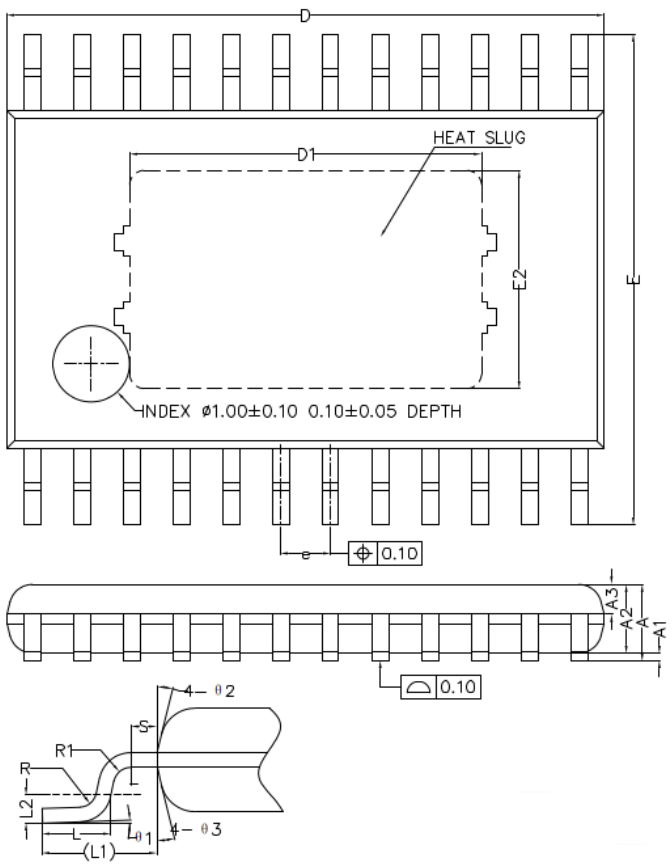


Figure 7-1. Typical application connection for stepper motor

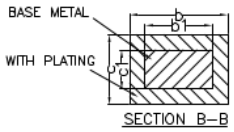
8. Package Information

8.1. HTSSOP24 package information



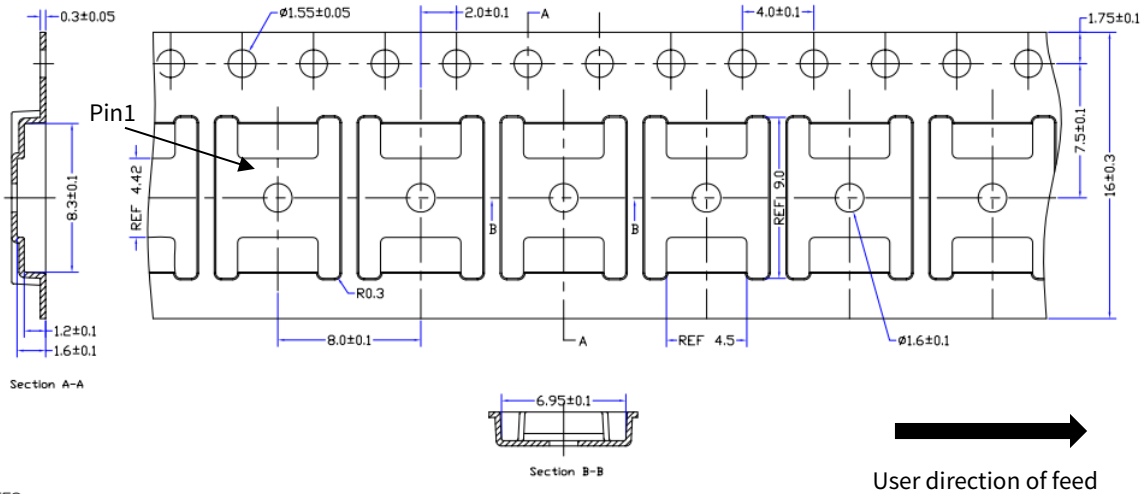
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.20	–	0.29
b1	0.19	0.22	0.25
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	7.70	7.80	7.90
D1		4.60REF	
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2		2.85REF	
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	12°	14°	16°
θ3	12°	14°	16°



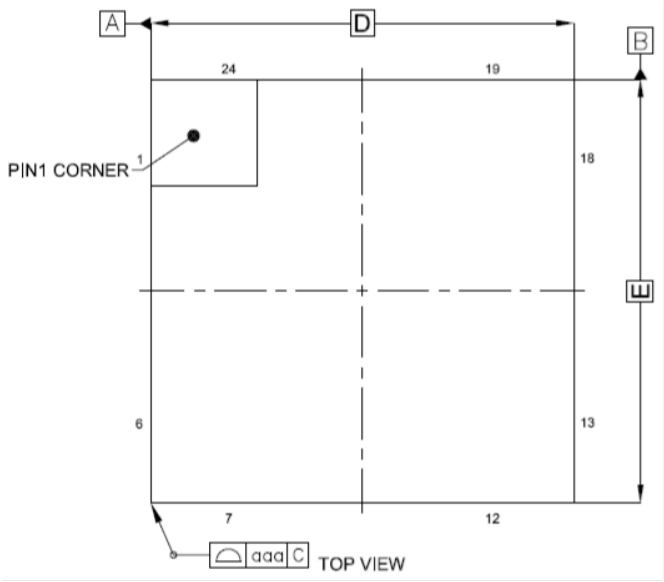
NOTES:
1.ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 ADT
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. 'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

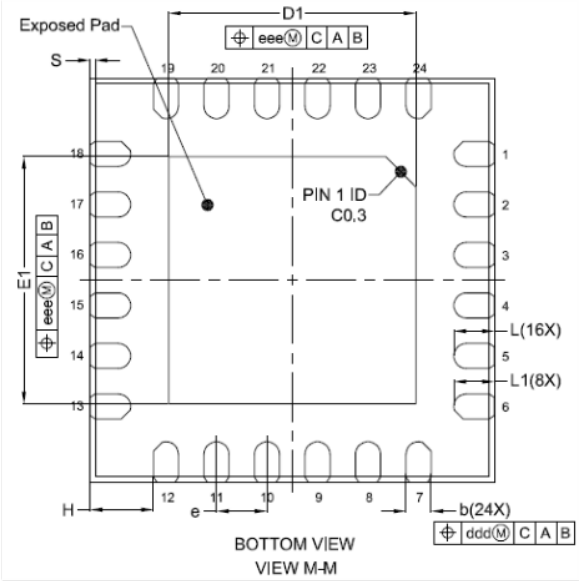
8.2. HTSSOP24 packing information



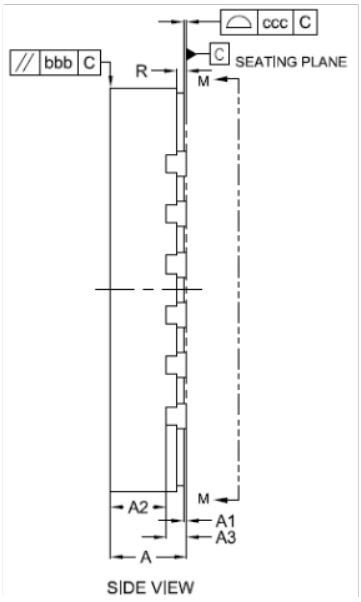
NOTES:
1.MATERIAL:Black conductive polystyrene
2.ALL DIMS IN MM

8.3. VQFN24 package information

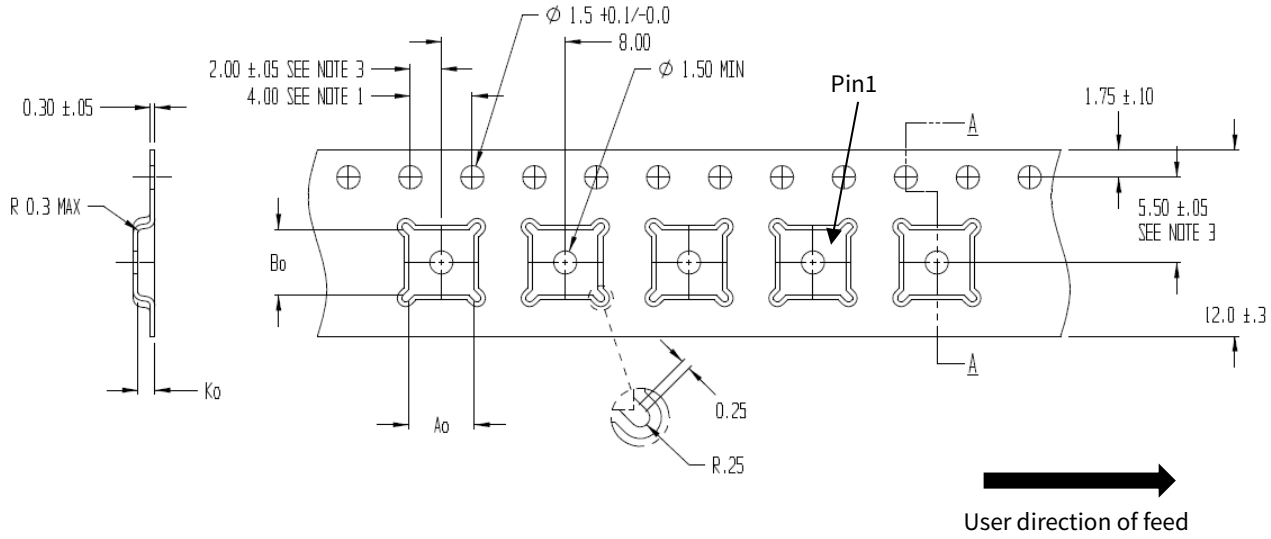




DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.50	0.55	0.60
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	X	D	3.90	4.00	4.10
	Y	E	3.90	4.00	4.10
LEAD PITCH		e	0.50 BSC		
LEAD WIDTH		b	0.20	0.25	0.30
LEAD LENGTH		L	0.35	0.40	0.45
		L1	0.33	0.40	0.47
EP SIZE	X	D1	2.40	2.45	2.50
	Y	E1	2.40	2.45	2.50
LEAD EDGD TO PKG EDGE		H	0.625 REF		
STEP CUT WIDTH		S	0.001	0.05	0.09
STEP CUT HEIGHT		R	0.05	0.10	0.15
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa	0.10		
MOLD FLATNESS		bbb	0.10		
LEAD COPLANARITY		ccc	0.08		
LEAD POSITION OFFSET		ddd	0.10		
EXPOSED PAD OFFSET		eee	0.10		



8.4. VQFN24 packing information



9. Ordering Information

Part Number	Automotive / Industrial	Package Type	MSL	SPQ
NSD8389-Q1HTSXR	Automotive	HTSSOP24	MSL3	4000
NSD8389A-Q1HTSXR	Automotive	HTSSOP24	MSL3	4000
NSD8389-Q1QBBR	Automotive	VQFN24	MSL2	3000
NSD8389A-Q1QBBR	Automotive	VQFN24	MSL2	3000
Note: All packages are RoHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.				

10. Revision History

Revision	Description	Date
0.1	Initial version	2024/6/25
0.2	Correct the typo in SPI SDI frame Update the block diagram with adding VREF block Correct the VBEMF calculation formula Update the VINT regulator output capacitor min/max value Correct the typo in CPL, CPH charge pump fly capacitor recommend value Update the EN pin absolute maxim rating, as EN pin can sustain up to VS Add the difference between NSD8389 and NSD8389A in register CONFIG_2 and CONFIG_5 Update thermal information parameters (Rthjc, Rthja)	2024/11/8
1.0	Correct the typo in DRVOFF description. Improve the calculation formula of Tj ADC sense value Add SPI SDI frame example in SPI description section Revise a few parameter 'CP frequency', RPD, RPU maximum value, OCP min value Revise VQFN MSL level, update from MSL3 to MSL2 Revise datasheet format.	2025/6/20
1.1	Correct the typo of register Config13 default value from 0x00 to 0xFF Correct the typo of VQFN24 SPQ (Standard Pack Quantity) number from 5000 to 3000 Revise register Config16 bit5-6 CV_REG_IND[1:0] description	2025/08/08
1.2	Correct the typo of register Config 2 address value from 0x01 to 0x02	2025/09/03

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