NOVOSENSE

NSD7315-Q1

Automotive H-Bridge Motor Driver

Datasheet (EN) 1.0

Product Overview

The NSD7315-Q1 device is an integrated driver IC for driving a brushed DC motor in automotive applications. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that drive motors bi-directionally with up to 10A peak current.

A PH/EN or PWM interface allows simple interfacing to controller circuits. Alternatively, independent half-bridge control is available to drive two solenoid loads.

Integrated current sensing provides an output current proportional to the motor load current of both hide-side FETs without the need for high-power sense resistors. This can be used to detect motor stall or change in load conditions.

A low-power sleep mode is provided to achieve very low quiescent current draw by shutting down much of the internal circuitry. Internal protection functions are provided for undervoltage lockout, charge pump faults, overcurrent protection, short-circuit protection, open-load detection, and overtemperature detection. Fault conditions are indicated on an nFAULT pin and through the SPI registers.

Key Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C T_A
- N-channel H-bridge motor driver
- 10A Peak current drive
- Low Rds(on) (High Side + Low Side)
  - 150mΩ at T_J = 25°C, 13.5V
  - 220mΩ at T_J = 150°C, 13.5V
- Integrated current sensing
  - Proportional current output (IPROPI)
- Offer configurable control modes
  - PH/EN
  - PWM(IN1/IN2)
  - Independent Half-Bridge control
- SPI or Hardware interface options
- Supports 1.8V, 3.3V, 5V logic inputs
- Low-power sleep mode
- Protection Features:
  - UVLO: VM undervoltage lockout
  - CPUV: Charge pump undervoltage
  - OCP: Overcurrent protection
  - OL: Open load detection
  - TSD: Thermal shutdown and thermal warning
  - Fault condition output (nFAULT/SPI)
- RoHS & REACH Compliance

Applications

- Electronic throttle control
- Exhaust gas recirculation
- Side-view mirror fold
- Air-flow diverter valve control
- E-lock

Device Information

Part Number	Package	Body Size
NSD7315H-Q1	HTSSOP24	7.7mm × 4.4mm
NSD7315S-Q1		

Functional Block Diagrams

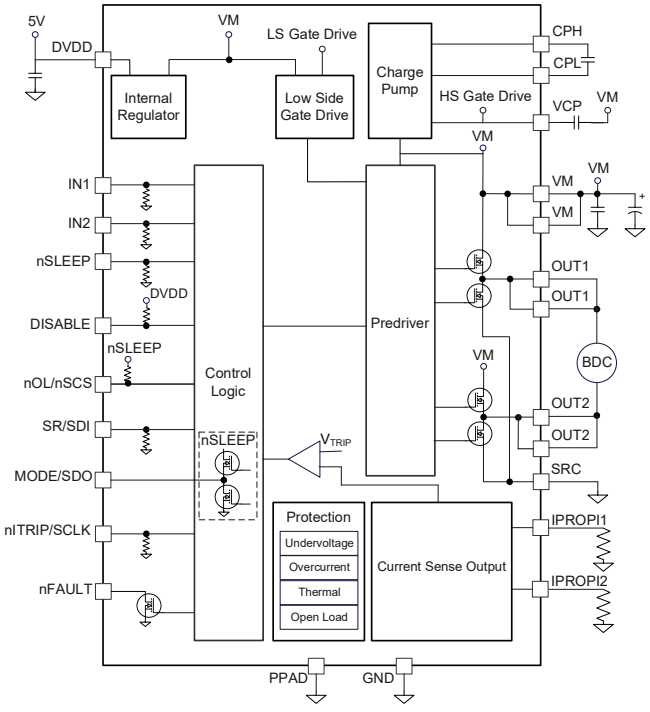

Figure 1. NSD7315-Q1 Block Diagram

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1. Pin Configuration and Functions

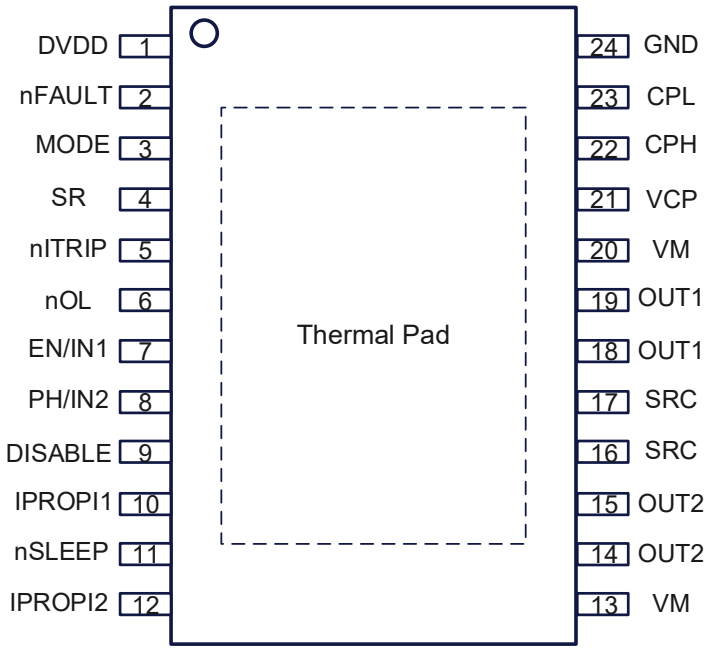


Figure 1.1 NSD7315H-Q1 Pinout (Top View)

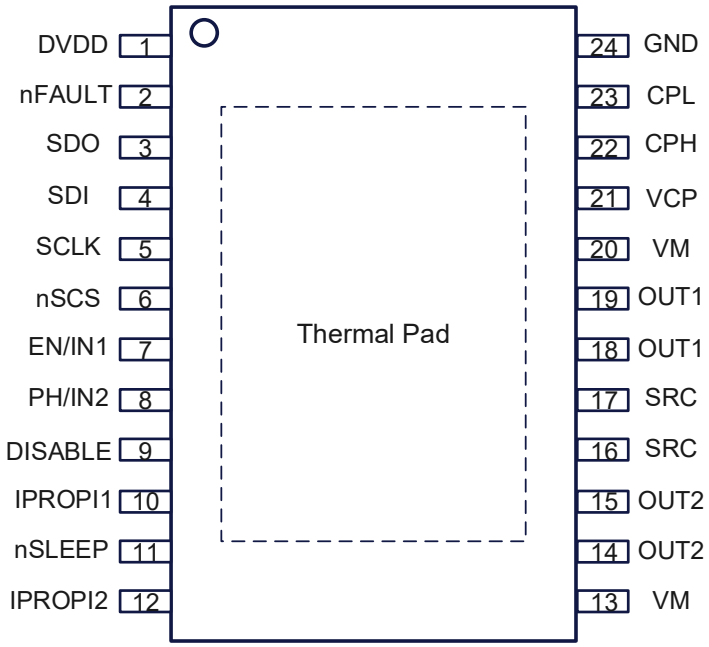


Figure 1.2 NSD7315S-Q1 Pinout (Top View)

Table 1.1 NSD7315-Q1 Pin Configuration and Description

Symbol	No. NSD7315H-Q1	No. NSD7315S-Q1	Type (1)	Description	External Components or Connections
DVDD	1	1	PWR	5V internal digital regulator output	Bypass this pin to GND with a 6.3V, 1μF ceramic capacitor.
nFAULT	2	2	OD	Fault indication pin	Pulled logic low with a fault condition. This open-drain output requires an external pullup resistor.
MODE	3	-	I	Input mode pin	Sets the PH/EN, PWM, or Independent half bridge mode.
SDO	-	3	PP	Serial data output	Data is shifted out on the rising edge of the SCLK pin. This is a push-pull output.
SR	4	-	I	Slew rate adjust pin	Sets the slew rate of the H-bridge outputs.
SDI	-	4	I	Serial data input	Data is captured on the falling edge of the SCLK pin.
nITRIP	5	-	I	Internal current-regulation control pin (ITRIP)	To enable the ITRIP feature, do not connect this pin (or tie it to GND). To disable the ITRIP feature, connect this pin to the DVDD pin.
SCLK	-	5	I	Serial clock input	Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
nOL	6	-	I	Open-load diagnostic control pin	To run the open-load diagnostic at power up, tie it to ground. Connect it to DVDD (or not connect), open-load diagnostic will be disabled.
nSCS	-	6	I	Serial chip select	An active low on this pin enables the serial interface communications. Internal pullup to nSLEEP.
EN/IN1	7	7	I	Control inputs	This pin has an internal pulldown resistor to GND.
PH/IN2	8	8	I	Control inputs	This pin has an internal pulldown resistor to GND.
DISABLE	9	9	I	Bridge disable input	A logic high on this pin disables the H-bridge Hi-Z. Internal pullup to DVDD.
IPROPI1	10	10	O	High-side FET current	The analog current proportional to the current flowing in the half bridge.
nSLEEP	11	11	I	Sleep input	To enter a low-power sleep mode, set this pin logic low.
IPROPI2	12	12	O	High-side FET current	The analog current proportional to the current flowing in the half bridge.
VM	13	13	PWR	Power supply	Bypass this pin to GND with a 0.1μF ceramic capacitor and a bulk capacitor.
OUT2	14	14	O	Half-bridge output 2	Connect this pin to the motor or load.
OUT2	15	15	O	Half-bridge output 2	Connect this pin to the motor or load.
SRC	16	16	O	Power FET source	SRC pin is connected to GND internally. Just tie this pin directly to GND externally.
SRC	17	17	O	Power FET source	SRC pin is connected to GND internally. Just tie this pin directly to GND externally.
OUT1	18	18	O	Half-bridge output 1	Connect this pin to the motor or load.
OUT1	19	19	O	Half-bridge output 1	Connect this pin to the motor or load.
VM	20	20	PWR	Power supply	Bypass this pin to GND with a 0.1μF ceramic capacitor and a bulk capacitor.
VCP	21	21	O	Charge pump output	Connect a 16V, 1μF ceramic capacitor from this pin to the VM supply.
CPH	22	22	O	Charge pump switching node	Connect a X7R capacitor with a value of 47nF between the CPH and CPL pins.
CPL	23	23	O	Charge pump	Connect a X7R capacitor with a value of 47nF

				switching node	between the CPH and CPL pins.
GND	24	24	PWR	Ground pin	

(1) I = input, O = output, OD = open-drain output, PP = push-pull output, PWR = power supply

2. Absolute Maximum Ratings (1)

Items		Min	Max	Unit
Power supply voltage	VM	-0.3	40	V
Charge pump voltage	VCP, CPH	-0.3	V_{VM} + 5.7	V
Charge pump switching pin	CPL	-0.3	V_{VM}	V
Internal logic regulator voltage	DVDD	-0.3	5.7	V
Digital pin voltage	EN/IN1, PH/IN2, nSLEEP, DISABLE, nFAULT, SCLK, SDI, SDO, nSCS	-0.3	5.7	V
Analog pin voltage	IPROPI1, IPROPI2	0	5.5	V
Phase node pin voltage	OUT1, OUT2	V_{SRC} - 1	V_{VM} + 1	V
Open drain output current	nFAULT	0	10	mA
Push-pull output current	SDO	0	10	mA
Operating junction temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3. ESD Ratings

Symbol	Description		Value	Unit
VESD_HBM	Human body model (HBM), per AEC Q100–002 HBM ESD Classification Level 2(1)	All pins	± 2000	V
VESD_CDM	Charged device model (CDM), per AEC Q100–011 CDM ESD Classification Level C4B	Corner pins (1, 12, 13, and 24)	± 750	V
		Other pins	± 500	V

(1) AEC Q100–002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS–001 specification.

4. Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
V_{VM}	Power supply voltage	4.5	35	V
V_I	Logic level input voltage	0	5.5	V
f_{PWM}	Applied PWM frequency (EN/IN1, PH/IN2)		100	kHz
T_A	Operating ambient temperature	-40	125	°C

5. Thermal Information (1)

Symbol	Description	Typ	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	3.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	°C/W

(1) Based on thermal simulations using JEDEC 51-7 board.

6. Electrical Characteristics

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supplies (VM, DVDD)						
V_{VM}	VM operating voltage		4.5		35	V
I_{VMQ}	VM sleep mode supply current	V_{VM} = 13.5V; nSLEEP = 0		3	30	μA
I_{VM}	VM operating supply current	V_{VM} = 13.5V; nSLEEP = 1; DISABLE = 0		1.3	6	mA
V_{DVDD}	Internal logic regulator voltage	2mA load; V_{VM} > 5.5V	4.8	5	5.2	V
t_{on}	Turn-on time	V_{VM} > V_{UVLO}; nSLEEP = 1; to output transition		0.4	1	ms
t_{WAKE}	Wake-up time	nSLEEP high to device ready for input signals		0.4	1	ms
t_{SLEEP}	Sleep time	nSLEEP low to start device shutdown	50			μs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to only clear fault registers	2		20	μs
$t_{DISABLE}$	DISABLE deglitch time	DISABLE signal transition		4.5		μs
Charge Pump (VCP, CPH, CPL)						
V_{VCP}	Charge pump regulator voltage	with respect to VM		V_{VM}+5		V
I_{VCP}	VCP current	V_{VM} = 13.5V		7	10	mA
f_{VCP}	Charge pump switching frequency	V_{VM} > V_{UVLO}; nSLEEP = 1		410		kHz
t_{CP}	Charge pump active time	DVDD active to charge pump active		155		μs
Logic Control Inputs (EN/IN1, PH/IN2, nSLEEP, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		1.6		5.3	V
V_{HYS}	Input logic hysteresis			200		mV
I_{IL}	Input logic low current	V_{IN} = 0V	-2		2	μA
I_{IH}	Input logic high current	V_{IN} = 5V		50		μA
$I_{IH,nSLEEP}$	Input logic high current (nSLEEP pin)	V_{IN} = 5V; nSCS is High			80+I_{SDO}	μA
R_{PD}	Internal pull-down resistance	to GND		100		kΩ
t_{PD}	Propagation delay (EN/IN1, PH/IN2 to OUTx = 50%)	SR = 000b; I_O = 1A		0.8		μs
		SR = 001b; I_O = 1A		1		
		SR = 010b; I_O = 1A		1.5		
		SR = 011b; I_O = 1A		1.8		

		SR = 100b; I_O = 1A		2		
		SR = 101b; I_O = 1A		2.5		
		SR = 110b; I_O = 1A		3		
		SR = 111b; I_O = 1A		5		
Logic Control Input (DISABLE)						
$V_{IL,DIS}$	Input logic low voltage		0		0.8	V
$V_{IH,DIS}$	Input logic high voltage		1.6		5.3	V
$R_{PU,DIS}$	Internal pull-up resistance	DISABLE to DVDD		100		kΩ
Logic Control Input (nSCS)						
$V_{IL,nSCS}$	Input logic low voltage		0		0.8	V
$V_{IH,nSCS}$	Input logic high voltage		1.6		5.3	V
$R_{PU,nSCS}$	Internal pull-up resistance	nSCS to nSLEEP		570		kΩ
Three-Level Input (MODE)						
R_{IN-1}	Input mode1	Tied to GND			105	Ω
R_{IN-2}	Input mode2	Tied to GND	190			kΩ
R_{IN-3}	Input mode3	Tied to DVDD			105	Ω
Push-Pull Output (SDO)						
$R_{PD,SDO}$	Internal pull-down resistance	With respect to GND		20	50	Ω
$R_{PU,SDO}$	Internal pull-up resistance	With respect to nSLEEP		120	240	Ω
Open Drain Output (nFAULT)						
V_{OL}	Output logic low voltage	I_O = 5mA			0.45	V
I_{OZ}	Output high-impedance leakage	V_O = 5V	-2		2	μA
Motor Driver Outputs (OUT1, OUT2)						
$R_{DS(ON)\_HS}$	High-side MOSFET resistance	V_{VM} = 13.5V; T_A = 25°C; T_J = 25°C		75		mΩ
		V_{VM} = 13.5V; T_A = 25°C; T_J = 150°C		110	155	
$R_{DS(ON)\_LS}$	Low-side MOSFET resistance	V_{VM} = 13.5V; T_A = 25°C; T_J = 25°C		75		mΩ
		V_{VM} = 13.5V; T_A = 25°C; T_J = 150°C		110	155	
$V_{F(DIODE)}$	Body diode forward voltage	I_O = 0.1A		0.75		V
t_{DEAD}	Output dead time	SR = 000b		200		ns
		SR = 100b		500		
		SR = 111b		800		
I_{SINK}	Sink current when OUTx = Hi-Z	nSLEEP = 0		25		μA
		nSLEEP = 1; DISABLE = 1		50		
SR	Slew rate (H/W Device) OUTx 10% to 90% changing	I_O = 1A; Connect to GND		55		V/μs
		I_O = 1A; R_{SR} = 22kΩ ± 5% to GND		32		
		I_O = 1A; R_{SR} = 68kΩ ± 5% to GND		17		
		I_O = 1A; No connect (Hi-Z)		13		
		I_O = 1A; R_{SR} = 51kΩ ± 5% to DVDD		8		
		I_O = 1A; Connect to DVDD		2.6		
SR	Slew rate (SPI Device) OUTx 10% to 90% changing	I_O = 1A; SR = 000b		55		V/μs
		I_O = 1A; SR = 001b		32		
		I_O = 1A; SR = 010b		17		
		I_O = 1A; SR = 011b		13		
		I_O = 1A; SR = 100b		10		
		I_O = 1A; SR = 101b		8		

		I_O = 1A; SR = 110b		5		
		I_O = 1A; SR = 111b		2.6		
Current Sense Outputs (IPROPI1, IPROPI2)						
K	Current mirror scaling factor			1100		A/A
K_{ERR}	Current mirror scaling error	I_O ≤ 1A	-70		70	mA
		I_O > 1A	-7		7	%
t_{IPROPI}	OUTx to IPROPI	SR = 000b		0.7		µs
		SR = 111b		1.6		
Current Regulation						
I_{TRIP}	Current limit threshold	ITRIP_LVL = 00b; V_{VM} = 13.5V	3.35	4	4.5	A
		ITRIP_LVL = 01b; V_{VM} = 13.5V	4.6	5.4	6.2	
		ITRIP_LVL = 10b; V_{VM} = 13.5V	5.5	6.5	7.5	
		ITRIP_LVL = 11b; V_{VM} = 13.5V	6	7	8	
t_{OFF}	PWM off-time	TOFF = 00b		20		µs
		TOFF = 01b		40		
		TOFF = 10b		60		
		TOFF = 11b		80		
t_{DEG}	Current regulation deglitch time			1		µs
t_{BLANK}	Current regulation blanking time			4		µs
Protection Circuits						
V_{UVLO}	VM undervoltage lockout	VM falling; UVLO report		4.33	4.45	V
		VM rising; UVLO recovery		4.5	4.7	
t_{UVLO}	VM UVLO falling deglitch time	VM falling; UVLO report		10		µs
V_{RST}	VM UVLO reset	VM falling; UVLO report; device reset		3.5	4.1	V
$V_{VCP(UV)}$	Charge pump undervoltage	V_{VM} = 13.5V; CPUV report		V_{VM}+2.3		V
		V_{VM} = 13.5V; CPUV recovery		V_{VM}+3.5		V
I_{OCP}	Overcurrent protection trip level		10			A
t_{OCP}	Overcurrent protection deglitch time			3.5	6	µs
t_{RETRY}	Overcurrent protection retry time (SPI Device)	OCP_TRETRY = 00b		0.5		ms
		OCP_TRETRY = 01b		1		
		OCP_TRETRY = 10b		2		
		OCP_TRETRY = 11b		4		
V_{OLA}	Open load active mode threshold voltage		120	270	450	mV
t_{OLA}	Open load active mode diagnostic filter time			100		ns
$t_{d(OL)}$	Open load passive mode diagnostic delay time	OL_DLY = 0b		0.3		ms
		OL_DLY = 1b		1.2		
I_{OL}	Open load passive mode diagnostic current			3		mA
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	140	150	160	°C

T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	165	175	185	°C
T_{HYS}	Thermal shutdown hysteresis	Die temperature (T_J)		20		°C
SPI Timing Requirements						
t_{READY}	SPI ready, VM > V_{UVLO}			1		ms
t_{CLK}	SCLK minimum period		100			ns
t_{CLKH}	SCLK minimum high time		50			ns
t_{CLKL}	SCLK minimum low time		50			ns
$t_{su(SDI)}$	SDI input setup time		20			ns
$t_{h(SDI)}$	SDI input hold time		30			ns
$t_{d(SDO)}$	SDO output delay time, SCLK high to SDO valid, C_L = 20 pF				30	ns
$t_{su(nSCS)}$	nSCS input setup time		50			ns
$t_{h(nSCS)}$	nSCS input hold time		50			ns
t_{HI_nSCS}	nSCS minimum high time before active low		500			ns
$t_{dis(nSCS)}$	nSCS disable time, nSCS high to SDO high impedance			10		ns

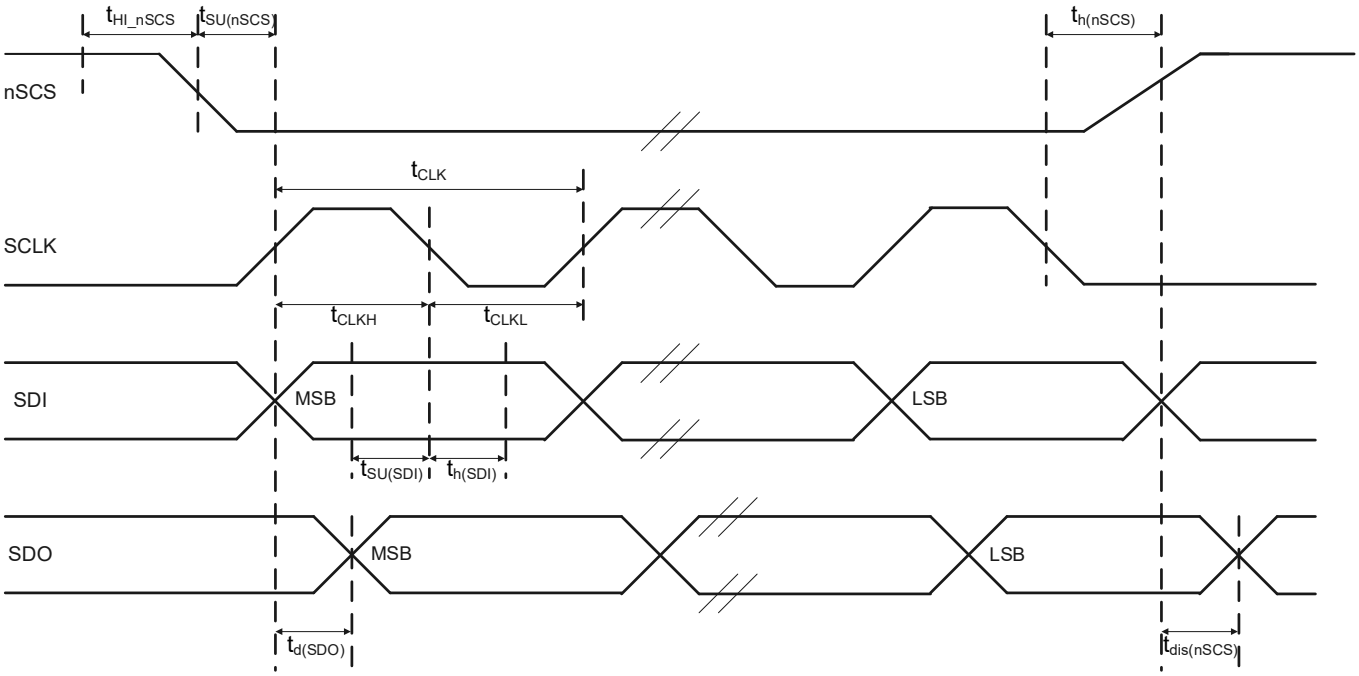


Figure 6.1 SPI Slave-Mode Timing Definition

7. Functional Description

7.1. Overview

NSD7315-Q1 is an integrated, 4.5V to 35V motor driver for automotive brushed-motor applications. The device is capable of high output-current drive using low $R_{DS(ON)}$ integrated MOSFETs.

A standard 4-wire serial peripheral interface (SPI) decreases the device pin count by allowing the various device settings and fault reporting to be managed through an external controller. Alternatively a hardware interface option device is available for easy configuration with less detailed control of all device functions.

The device integrates a current mirror which provides an output current proportional to the motor load current of both hide-side FETs. This feature allows the system to monitor the motor current without the need for a large high-power resistor for current sensing. The device has a built-in current regulation feature with a fixed off-time current-chopping scheme. The current-chopping level is selected through SPI in the SPI version of the device and in the hardware version of the device it is a fixed value.

Internal protection functions are provided for power supply undervoltage lockout, charge pump undervoltage lockout, overcurrent protection, output short to battery and short to ground protection, open-load detection, and overtemperature protection. Fault conditions are indicated on an nFAULT pin and through the SPI registers.

The device integrates a pulse skipping feature for internal charge pump. This feature combined with output slew rate control minimizes the radiated emissions from the device.

The device is available in a 24-pin HTSSOP package with a thermal pad.

7.2. Feature Description

7.2.1. Bridge Control

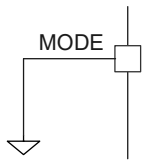
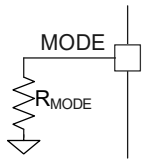
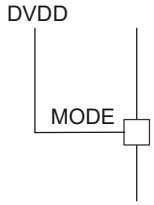
NSD7315-Q1 output has four N-channel MOSFETs configured in a H-bridge. The driver can be controlled using a PH/EN, PWM, or Independent half-bridge input mode. Table 7.1 lists the control mode configurations.

Table 7.1 Control Mode Configuration

Hardware Device Mode Pin	SPI Device Mode Register	Control Mode
L	00b	PH/EN
H	01b (default)	PWM
200kΩ ± 5% to GND	10b	Independent half bridge
Not applicable	11b	Input disabled, bridge Hi-Z

In the hardware version of the device, the MODE pin determines the control interface and latches on power-up or when exiting sleep mode. During the device power-up sequence, the DVDD pin is enabled first, and then the MODE pin latches. Any additional changes to the signal at the MODE pin are ignored by the device. To change the mode settings, a power cycle or sleep reset must be performed on the device. Tying the MODE pin directly to ground sets the mode to phase and enable. Tying the MODE pin to the DVDD pin, or an external 5V rail, sets the mode to PWM. Connecting the MODE pin to ground with a 200kΩ± 5% resistor (or left as no connect) sets the mode to independent half-bridge where the two half-bridges can be independently controlled by their respective input (INx) pins. Table 7.2 lists the different MODE pin settings.

Table 7.2 NSD7315H-Q1 Mode Pin Settings

Connection	Mode	Circuit
Connect to GND	PH/EN	
200kΩ ± 5% to GND	Independent half bridge	
Connect to DVDD	PWM	

In the SPI version of the device, the mode setting can be changed by writing to the MODE register in the IC1 control register because this device version has no dedicated MODE pin. The device mode gets latched when the DISABLE signal transitions from high to low.

7.2.1.1. Control Modes

The device output consists of four N-channel MOSFETs that are designed to drive high current. The MOSFETs are controlled by two logic inputs, EN/IN1 and PH/IN2, in three different input modes to support various commutation and control methods, as shown in below logic tables (Table7.3, Table7.4, Table7.5).

Table 7.3 PH/EN Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2	Function
0	X	X	X	Hi-Z	Hi-Z	Sleep
1	1	X	X	Hi-Z	Hi-Z	Disable
1	0	0	X	H	H	Brake (High-Side Slow Decay)
1	0	1	0	L	H	Reverse (OUT2 -> OUT1)
1	0	1	1	H	L	Forward (OUT1 -> OUT2)

Table 7.4 PWM Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2	Function
0	X	X	X	Hi-Z	Hi-Z	Sleep
1	1	X	X	Hi-Z	Hi-Z	Disable
1	0	0	0	Hi-Z	Hi-Z	Coast
1	0	0	1	L	H	Reverse (OUT2 -> OUT1)
1	0	1	0	H	L	Forward (OUT1 -> OUT2)
1	0	1	1	H	H	Brake (High-Side Slow Decay)

Table 7.5 Independent Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2	Function
0	X	X	X	Hi-Z	Hi-Z	Sleep
1	1	X	X	Hi-Z	Hi-Z	Disable
1	0	0	0	L	L	Brake (Low-Side Slow Decay)
1	0	0	1	L	H	Reverse (OUT2 -> OUT1)
1	0	1	0	H	L	Forward (OUT1 -> OUT2)
1	0	1	1	H	H	Brake (High-Side Slow Decay)

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM mode (MODE = 1), switching between driving and braking typically is best. For example, to drive a motor forward with 50% of its maximum revolutions per minute (RPM), the IN1 pin is high and the IN2 pin is low during the driving period. During the other period in this example, the IN1 pin is high and the IN2 pin is high.

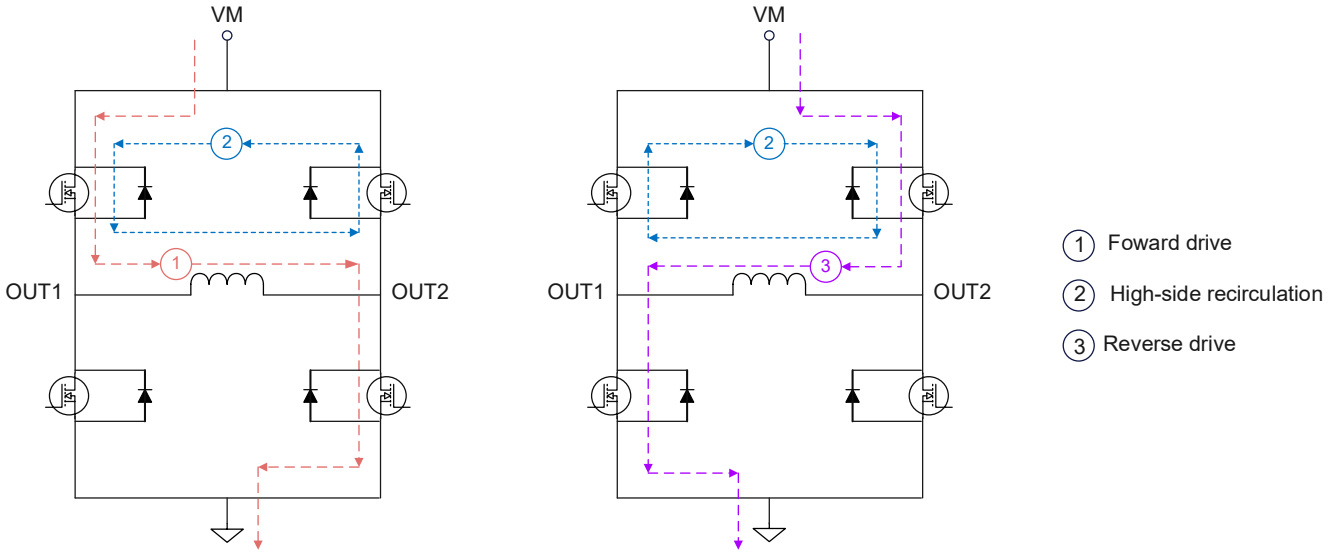


Figure 7.1 Full-Bridge Current Paths

7.2.1.2. Half-Bridge Operation

The device can be used to drive two solenoids or unidirectional brushed DC-motor loads instead of a brushed DC motor in full H-bridge configuration. Independent half-bridge control is preferred for operation in this mode. However, using the PH/EN or PWM modes is not restricted if the correct driving and braking states can be achieved.

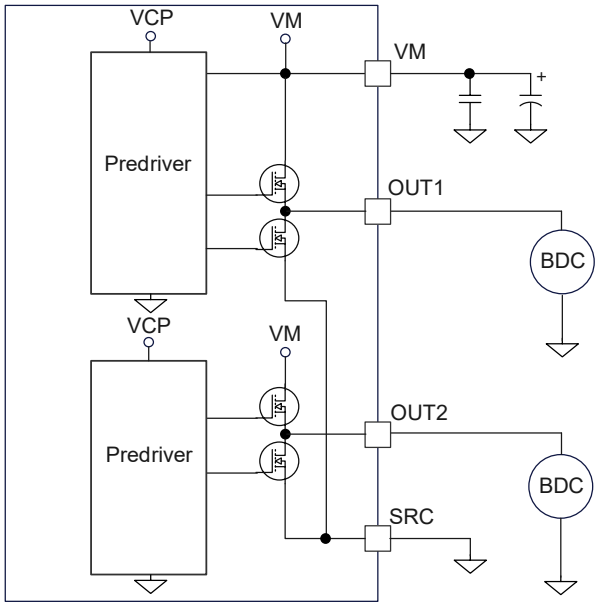


Figure 7.2 Independent Half-Bridge Mode Driving Two Low-Side Loads

Depending on how the loads are connected on the outputs pin, some of the features offered by the device could have reduced functionality. For example, having a load between the OUTx and GND pins, as shown in Figure 7.2, results in false trips of the open-load diagnosis in active-mode (OLA). While having a load tied between the OUTx and VM pins restricts the use of internal current regulation because no means of measuring current flowing through the load with the current mirror block is available. Table 7.6 lists these use cases.

Table 7.6 Half-Bridge Mode Configuration

Load Connections		Functions	
Node1	**Node2**	**OLA**	**Current Regulation (I_{TRIP})**
OUTx	GND	Not Available	Operational
OUTx	VM	Operational	Not Available

In the independent half-bridge mode, to independently put the outputs of the half bridge in the high-impedance (Hi-Z) state, the OUT1_DIS or OUT2_DIS bit in the IC3 register must be set to 1b. Writing a logic 1 to the OUT1_DIS bit disables the OUT1 output. Writing a logic 1 to the OUT2_DIS bit disables the OUT2 output. The default value in these registers is 0b. The option to independently set the outputs of the half bridge in the Hi-Z state is not available for the hardware version of the device.

In the independent half-bridge mode, the fault handling is performed independently for each half bridge. For example, if an overcurrent condition (OCP) is detected in half-bridge 1, only the half-bridge 1 output (OUT1) is disabled and half-bridge 2 continues to operate based on the IN2 input.

We do not recommend tying the OUT1 and OUT2 pins together and drive a load. The half bridges may be out of synchronization in this configuration and any mismatch in the input commands can momentarily result in shoot through condition. This mismatch can be mitigated by adding an inductor in-line with the outputs.

7.2.1.3. Internal Current Sense and Current Regulation

The IPROPI pin outputs an analog current that is proportional to the current flowing in the H-bridge. The output current is typically 1/1100 of the current in both high-side FETs. The IPROPI pin is derived from the current through either of the high-side FETs. Because of this, the IPROPI pin does not represent the half bridge current when operating in a fast decay mode or low-side slow decay mode. The IPROPI pin represents the H-bridge current under forward drive, reverse drive, and high-side slow decay. The IPROPI output is delayed by approximately 1µs for the fastest slew-rate setting (55V/µs) after the high-side FET is switched on.

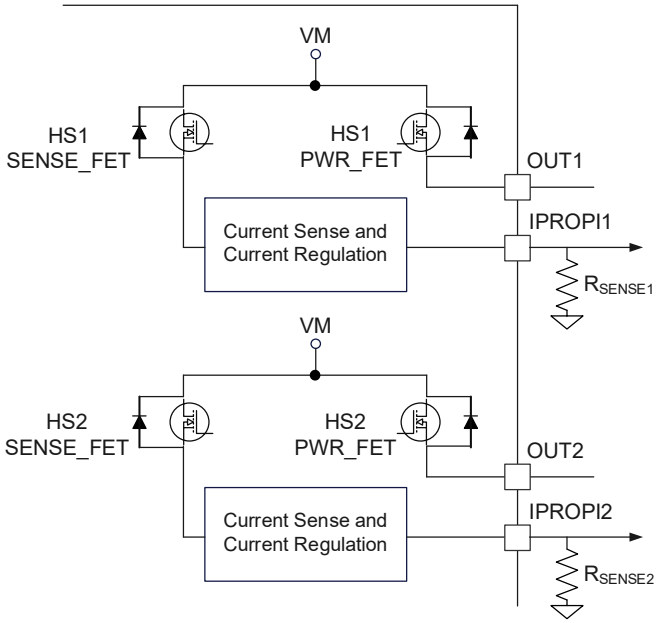


Figure 7.3 Current Sense Block Diagram

The selection of the external resistor should be such that the voltage on the IPROPI pin is less than 5V. Therefore the resistor must be sized less than this value based on Equation 1. If the external resistor is selected too large cause IPROPI voltage higher than 5V, IPROPI pin will be clamped. And in this condition, current regulation is disabled. The range of current that can be monitored is from 100mA to 10A assuming the selected external resistor meets the calculated value from Equation 1. If the current exceeds 10A, the device could reach overcurrent protection (OCP) or overtemperature shutdown (TSD). Below is the sense resistor selection guideline.

$$R_{SENSE(max)} = K \times 5V / I_{O(max)} \quad (1)$$

where

- K is the current mirror scaling factor, which is typically 1100.
- $I_{O(max)}$ is the maximum drive current to be monitored.

The IPROPI1 pin represents the current flowing through the HS1 MOSFET of half-bridge 1. The IPROPI2 pin represents the current flowing through the HS2 MOSFET of half-bridge 2. To measure current with one sense resistor, the IPROPI1 and IPROPI2 pins must be connected together with the R_{SENSE} resistor as shown in Figure 7.4. In this configuration, the current-sense output is proportional to the sum of the currents flowing through the both high-side FETs.

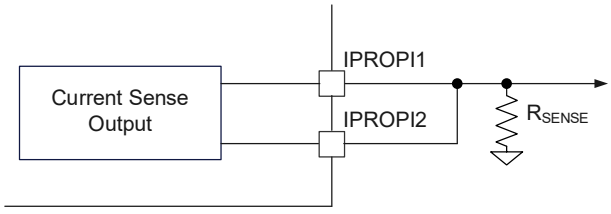


Figure 7.4 Current Sense Output

The current regulation feature is enabled by default on both the outputs (OUT1 and OUT2). To disable current regulation in the hardware version of the device, the nITRIP pin must be connected to DVDD. To disable current regulation in the SPI version of the device, the DIS_ITRIP bits in the IC4 Control register must be written as Table 7.7.

Table 7.7 Current Regulation Configuration

Hardware Device nITRIP pin	SPI Device DIS_ITRIP BIT	Current Regulation
Open or Connect to GND	00b (default)	Enable
	01b	Disable OUT1 current regulation
	10b	Disable OUT2 current regulation
Connect to DVDD	11b	Disable both OUT1 and OUT2 current regulation

The SPI version of the device limits the output current based on the trip level set in the SPI registers as Table 7.8. In the hardware version of the device, the current trip limit is set to 6.5A.

Table 7.8 Control Regulation Threshold

Parameter	ITRIP_LVL BIT	Min	Typ	Max	Unit
I_{TRIP} Current limit threshold	ITRIP_LVL = 00b	3.35	4	4.5	A
	ITRIP_LVL = 01b	4.6	5.4	6.2	A
	ITRIP_LVL = 10b (default)	5.5	6.5	7.5	A
	ITRIP_LVL = 11b	6	7	8	A

When the I_{TRIP} current has been reached and last for t_{DEG}, the device enforces slow current decay by enabling both the high-side FETs for a time of t_{OFF}. In the hardware version of the device, the t_{OFF} time is 40μs. The t_{OFF} time is selectable through SPI in the SPI version of the device, as shown in Table 7.9.

Table 7.9 PWM Off Time Settings

Parameter	TOFF BIT	t_{OFF} Duration	Unit
t_{OFF} PWM off time	TOFF = 00b	20	μs
	TOFF = 01b (default)	40	μs
	TOFF = 10b	60	μs
	TOFF = 11b	80	μs

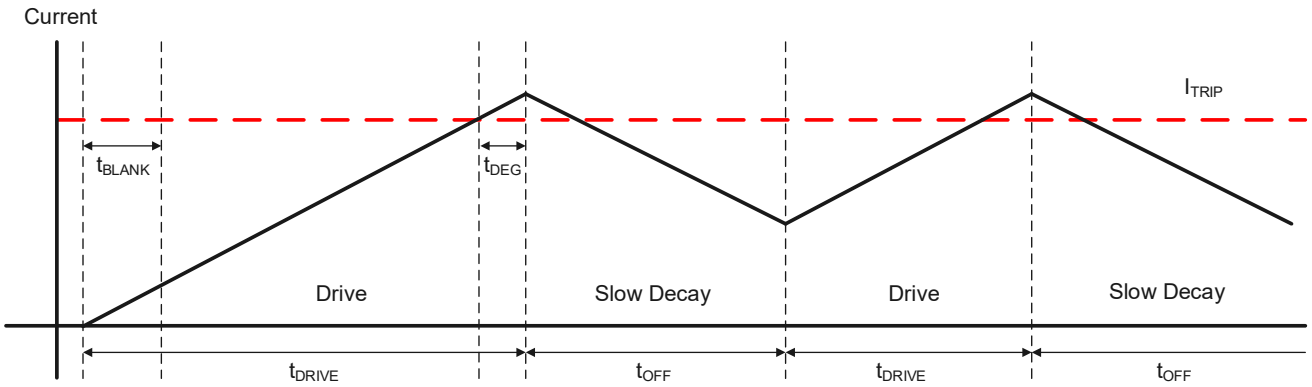


Figure 7.5 Current Regulation Time Period

The t_{OFF} time can't be interrupted when input changes state before t_{OFF} time ends, means that the device continues to decay until t_{OFF} ends. When the t_{OFF} time has elapsed and the current level falls below the current regulation (I_{TRIP}) level, the output is re-enabled according to the inputs. In PH/EN and PWM mode, if after the t_{OFF} time has elapsed but the current is still higher than the I_{TRIP} level, the device enforces another t_{OFF} time period of the same duration until current drops below I_{TRIP}. While in independent half-bridge mode, if after the t_{OFF} time has elapsed but the current is still higher than the I_{TRIP} level, the device drives t_{BLANK} time then enforces t_{OFF} decay time until current drops below I_{TRIP}.

The drive time (t_{DRIVE}) occurs until another ITRIP event is reached and last for t_{DEG}. It depends heavily on the VM voltage, the back-EMF of the motor, and the inductance of the motor. During the t_{DRIVE} time, the current-sense regulator does not enforce the ITRIP limit until the t_{BLANK} time has elapsed.

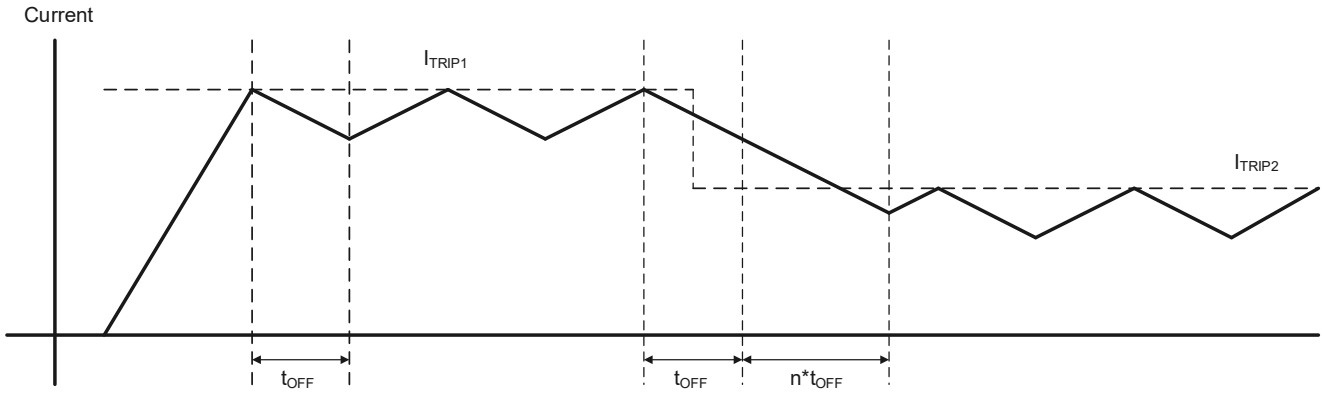


Figure 7.6 Current Regulation in PH/EN and PWM mode

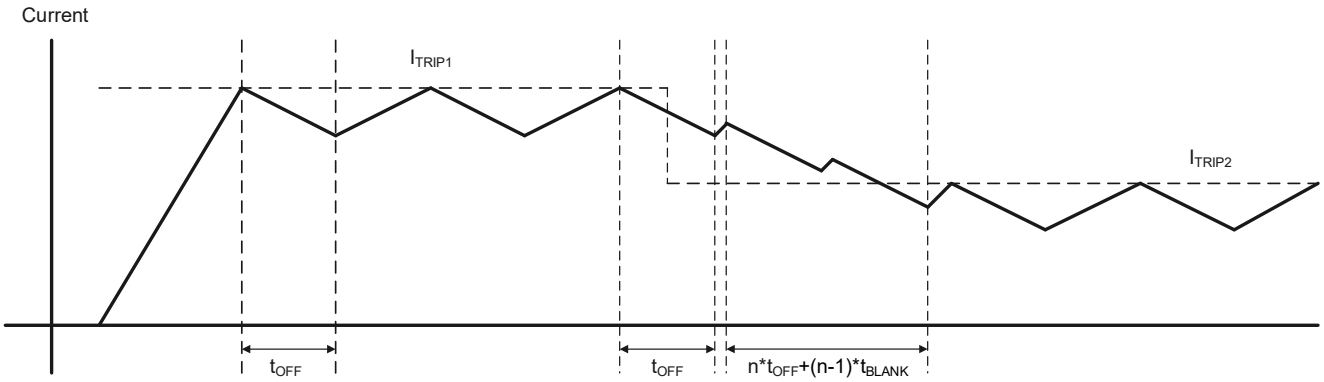


Figure 7.7 Current Regulation in Independent Half-Bridge mode

ITRIP1 and ITRIP2 bit can indicate the output is in current regulation or not. And ITRIP_REP bit in the IC2 Control register can configure current regulation whether is reported on nFAULT and the FAULT bit.

7.2.1.4. Slew Rate Control

The rise and fall times (t_r and t_f) of the outputs can be adjusted on the hardware version of the device by changing the value of an external resistor connected from the SR pin to ground or DVDD. On the SPI version of the device, the slew rate can be adjusted through the SPI. The output slew rate is adjusted internally to the device by controlling the ramp rate of the driven FET gate. Table 7.10 and Table 7.11 list the slew rate settings in H/W device and SPI device.

Table 7.10 Slew Rate Settings in H/W Device

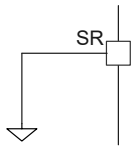
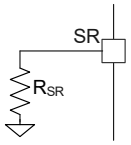
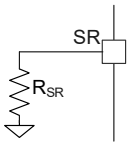
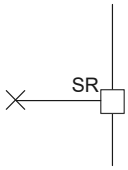
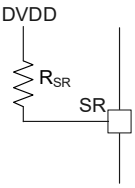
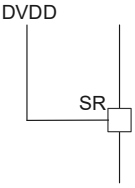
SR Pin Connection	SR (V/μs)	Circuit
Connect to GND	55	
22 kΩ ± 5% to GND	32	
68 kΩ ± 5% to GND	17	
> 2MΩ to GND (Hi-Z)	13	
51 kΩ ± 5% to DVDD	8	
Connect to DVDD	2.6	

Table 7.11 Slew Rate Settings in SPI Device

SR	Rise Time (V/μs)	Fall Time (V/μs)
000b	55	55
001b	32	32
010b	17	17
011b	13	13
100b	10	10
101b	8	8
110b	5	5
111b	2.6	2.6

7.2.1.5. Dead Time

The dead time (t_{DEAD}) is measured as the time when the OUTx pin is in the Hi-Z state between turning off one of the half bridge MOSFETs and turning on the other. For example, the output is in the Hi-Z state between turning off the high-side MOSFET and turning on the low-side MOSFET, or turning on the high-side MOSFET and turning off the low-side MOSFET.

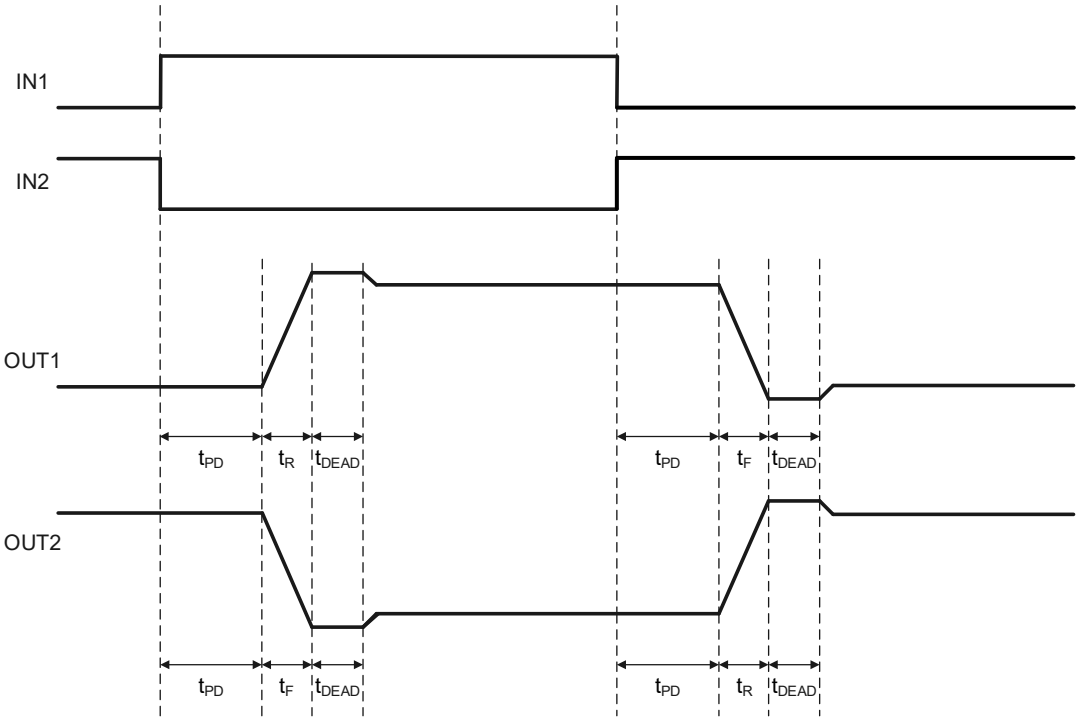


Figure 7.8 Propagation Delay Time

If the output pin is measured during the t_{DEAD} time the voltage depends on the direction of the current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. The diode drop is associated with the body diode of the high-side or the low-side FET. The dead time is dependent on the slew-rate setting because a portion of the FET gate ramp includes the observable dead time.

7.2.1.6. Propagation Delay

The propagation delay time (t_{PD}) is measured as the time between an input edge to an output change. This time comprises two parts: an input deglitcher and output slewing delay. The input deglitcher prevents noise on the input pins from affecting the output state. The adjustable slew rate also contributes to the propagation delay time. For the fastest slew-rate setting, the t_{PD} time is typically 0.8µs, and for the slowest slew-rate setting, the t_{PD} time is typically 5µs. For the output to change state during normal operation, one FET must first be turned off.

7.2.1.7. nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5V or 3.3V supply. When a fault is detected, the nFAULT line is logic low. For a 5V pullup the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3V pullup, an external 3.3V supply must be used.

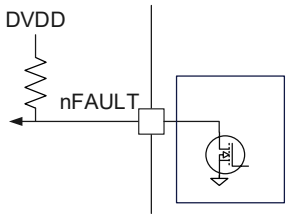


Figure 7.9 nFAULT Pin

During the device power-up sequence, or when exiting sleep mode, the nFAULT pin is held low until the digital core is alive and functional. This low level signal on the nFAULT line does not represent a fault condition. The signal can be used by the external MCU to determine when the digital core of the device is ready; however, this does not mean that the device is ready to accept input commands via the INx pins.

7.2.1.8. nSLEEP as SDO Reference

The nSLEEP pin manages the state of the device. The device goes into sleep mode with a logic-low signal, and comes out of sleep mode when the nSLEEP pin goes high. The signal level when the nSLEEP pin goes high determines the logic level on the SDO output in the SPI version of the device. A 3.3V signal on the nSLEEP pin provides a 3.3V output on the SDO output. A 5V signal on the nSLEEP pin provides a 5V output on the SDO pin. If the sleep feature is not required, the nSLEEP pin can be connected to the MCU power supply. In that case, when the MCU is powered-up, the motor driver device is also be powered-up.

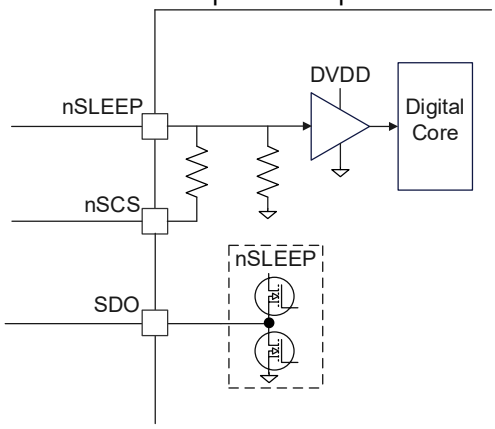


Figure 7.10 nSCS and nSLEEP Circuit

In the SPI version of the device, if the nSLEEP reset pulse is used to clear faults, the SDO voltage reference is not available for the duration of the nSLEEP reset pulse. No data can be transmitted on the SDO line for the duration when the nSLEEP pin is held low. Therefore recommend using the CLR_FLT bit in the IC3 control register to clear the faults.

7.2.2. Motor Driver Protection Features

The device is protected against VM undervoltage conditions, charge-pump undervoltage conditions, overcurrent events, and overtemperature events.

7.2.2.1. VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage, V_{UVLO}, for the voltage supply, all the outputs (OUTx) are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. The FAULT and UVLO bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed. The UVLO bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.

If the voltage on the VM pin falls below the UVLO reset voltage, V_{RST}, for the voltage supply, chip is reset and SPI is inactive.

Note: During the power-up sequence VM must exceed V_{UVLO} recovery max limit in order to power-up and function properly. After a successful power-up sequence, the device can operate down to the V_{UVLO} report limit before going into the undervoltage lockout condition.

7.2.2.2. VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the $V_{VCP(UV)}$ voltage for the charge pump, all the outputs (OUTx) are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. The FAULT and CPUV bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The CPUV bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.
This protection feature can be disabled by setting the DIS_CPUV bit high.

7.2.2.3. Overcurrent Protection (OCP)

If the current in any FET exceeds the I_{OCP} limits for longer than the t_{OCP} time, all FETs in the half bridge are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. The overcurrent protection can operate in four different modes: latched shutdown, automatic retry, report only, and disabled.
In the independent half-bridge mode (MODE = 10b or MODE pin to ground with a 200kΩ ± 5% resistor), the fault handling is performed independently for each half-bridge based on the OCP mode selected.
This protection scheme protects the outputs from short to battery and short to ground.

When current reaches higher than I_{TRIP} value, in order to determine the device to enter overcurrent mode or current regulation mode, below scenario is enforced.
If current rise to I_{OCP} before t_{BLANK} expires, the device enters overcurrent mode. OCP fault will be reported after current higher than I_{OCP} and lasts for t_{OCP}.
If current rise to I_{OCP} before t_{DEG} expires, the device enters overcurrent mode. OCP fault will be reported after current higher than I_{OCP} and lasts for t_{OCP}.
If current doesn't rise to I_{OCP} when t_{DEG} expires, the device enters current regulation mode. When current reaches I_{TRIP} and lasts for t_{DEG}, the device enforces slow current decay.

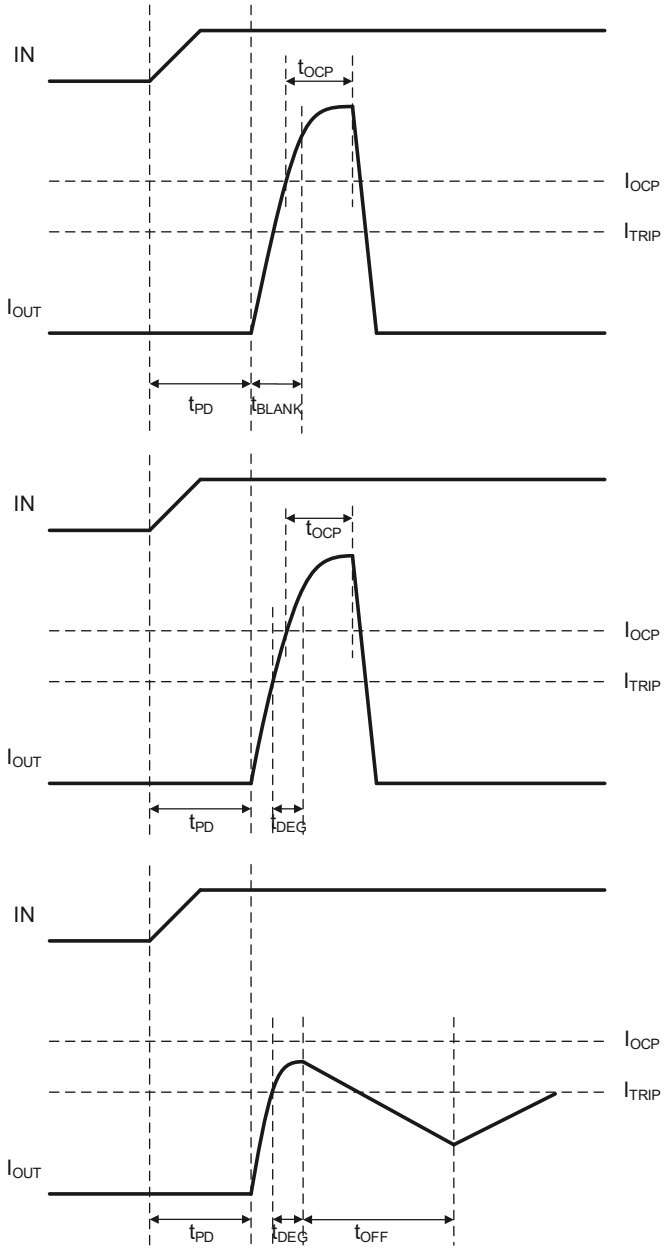


Figure 7.11 OCP Scenario

7.2.2.3.1. Latched Shutdown (OCP_MODE=00b)

In this mode, after an OCP event, all the outputs (OUTx) are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the OCP condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. This mode is the default mode for an OCP event for both the hardware version and SPI version of the device.

7.2.2.3.2. Automatic Retry (OCP_MODE=01b)

In this mode, after an OCP event, all the outputs (OUTx) are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation resumes

automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.2.2.3.3. Report Only (OCP_MODE=10b)

In this mode, no protective action is performed when an overcurrent event occurs. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, OCP, and corresponding MOSFET OCP bits high in the SPI registers. The motor driver continues to operate. The external controller acts appropriately to manage the overcurrent condition. The reporting is cleared (nFAULT released) when the OCP condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.

7.2.2.3.4. Disabled (OCP_MODE=11b)

In this mode, no protective or reporting action is performed when an overcurrent event occurs. The device continues to drive the load based on the input signals.

7.2.2.4. Open-Load Detection (OLD)

If the motor is disconnected from the device, an open-load condition is detected and the nFAULT pin is latched low until a clear faults command is issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse. The fault also clears when the device is power cycled or comes out of sleep mode.
Open load detection works in both standby mode (OLP) and active mode (OLA). OLP detects the presence of the motor prior to commutating the motor. OLA detects the motor disconnection from the driver during commutation.

7.2.2.4.1. Open-Load Detection in Passive Mode (OLP)

The OLP test is available in all three modes of operation (PN/EN, PWM, and Independent half-bridge). When the open load test is running, the internal power MOSFETs are disabled.
The OLP is designed for applications that have capacitance less than 15nF when the OLP_DLY bit set to 0b and for less than 60nF when the OLP_DLY bit is set to 1b on the OUTx pins. This setting is equivalent to measuring the resistance values listed in Table 7.12.

Table 7.12 Resistance for Open Load Detection

Node1	Node2	Resistance	Comments
OUT1	OUT2	3kΩ	
OUTx	VM	13kΩ	V_{VM} = 13.5V
OUTx	GND	4kΩ	

The open-load passive diagnostic (OLP) is different for the hardware and SPI version of the device.
For the hardware version of the device, the OLP test is performed only one time after power-up or after exiting sleep mode if the nOL pin is tied to GND. If the nOL pin is tied to the DVDD pin (or an external 5V rail) or left as a no connect pin, the OLP test is not performed by the device. The following sequence shows how to perform the OLP test after the device powers up or after exiting sleep mode:
1. Power up the device or nSLEEP turns high.
2. Perform the OLP test before the t_{on} or t_{WAKE} time expires.
   • If an open load (OL) is detected, the nFAULT pin is driven low after $t_{d(OL)}$=300μs elapse from internal diagnosis current sources enabled. When the OL condition is removed, nSLEEP reset pulse must be issued to release nFAULT signal.
3. Set the DISABLE pin low so that the device drives the motor or load based on the input signals.

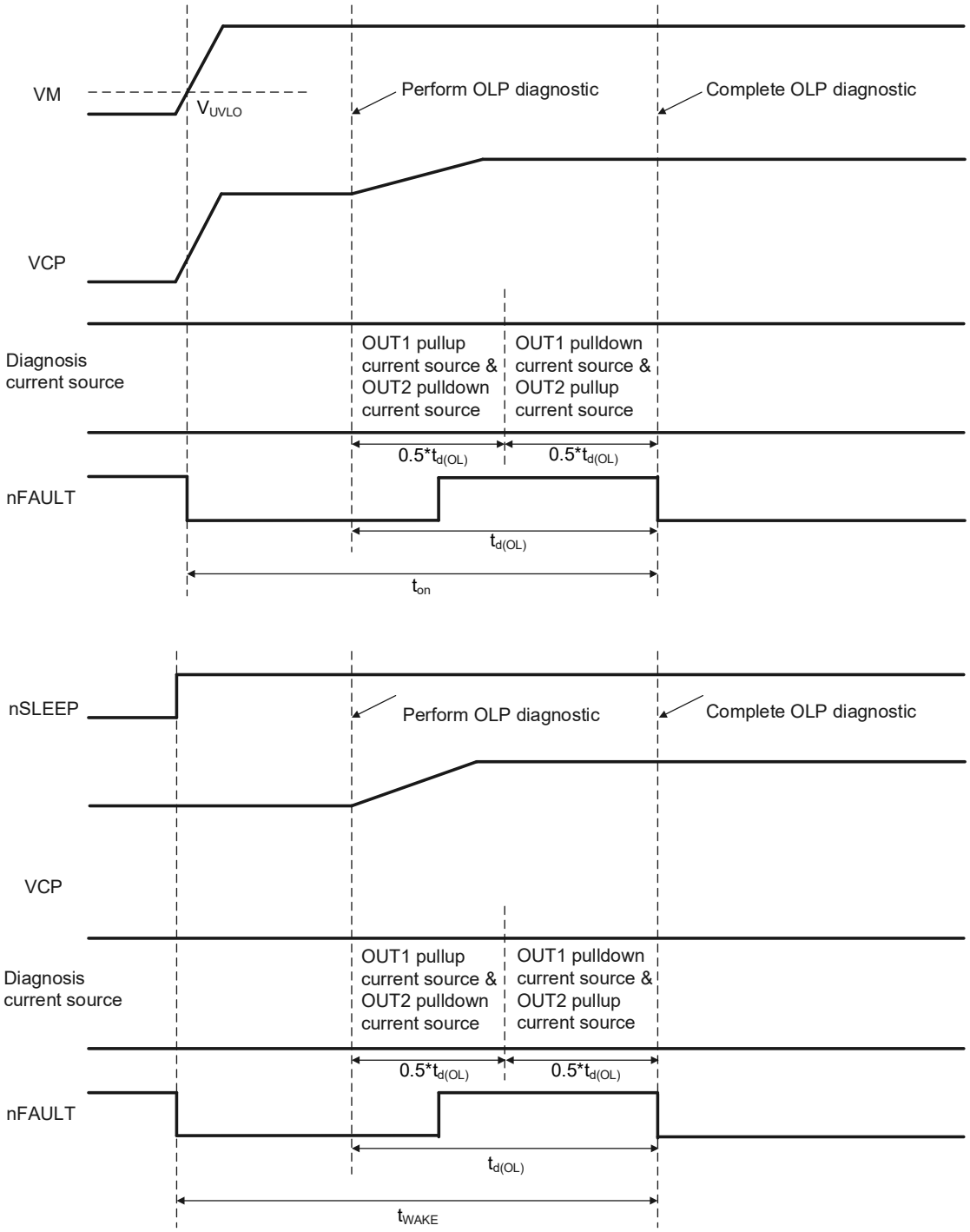


Figure 7.12 OLP Sequence of Hardware version

For the SPI version of the device, the OLP test is performed when commanded. The following sequence shows how to perform the OLP test directly after the device powers up:

1. Power up the device (DISABLE pin high).
2. Select the mode through SPI.
3. Wait for the $t_{DISABLE}$ time to expire.
4. Write 1b to the EN_OLP bit in the IC1 register.
5. Perform the OLP test.

• If an open load (OL) is detected, the nFAULT pin is driven low, the FAULT, OLD and OLx bits are latched high. When the OL condition is removed, a clear faults command must be issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse.
• After OLP detection completed, the EN_OLP bit returns to the default setting (0b) after the $t_{d(OL)}$ time expires.
6. Set the DISABLE pin low so that the device drives the motor or load based on the input signals.

If an OLP diagnostic is performed at any other time, the following sequence must be followed:
1. Set the pin DISABLE high (to disable the half bridge outputs).
2. Wait for the $t_{DISABLE}$ time to expire.
3. Write 1b to the EN_OLP bit in the IC1 register.
4. Perform the OLP test.
• If an OL condition is detected, the nFAULT pin is driven low, and the FAULT, OLD and OLx bits are latched high. When the OL condition is removed, a clear faults command must be issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse.
• After OLP detection completed, the EN_OLP bit returns to the default setting (0b) after the $t_{d(OL)}$ time expires.
5. Set the DISABLE pin low so that the device drives the motor or load based on the input signals.

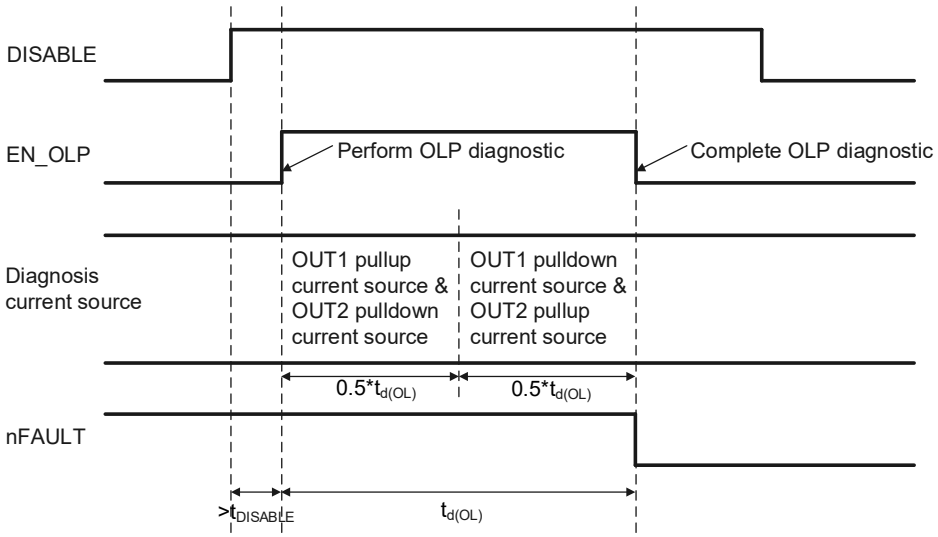


Figure 7.13 OLP Sequence of SPI version

For the SPI version of the device, if perform several times OLP diagnostic through write several times 1b to EN_OLP bit in the IC1 register, the last diagnostic result will overwrite the former diagnostic results. For example, if open load condition exists, after write 1b to EN_OLP bit, the nFAULT pin and FAULT, OLD and OLx bits report OL fault. Then if open load condition is removed, after write 1b to EN_OLP bit again, nFAULT is released and FAULT, OLD and OLx bits are reset.

The EN_OLP register maintains the written command until the diagnostic is complete. The signal on the DISABLE pin must remain high for the entire duration of the test. While the OLP test is running, if the DISABLE pin goes low, the OLP test is aborted to resume normal operation and no fault is reported. The OLP test is not performed if the motor is energized.

The OLP test checks for a high-impedance connection on the OUTx pins. The diagnostic runs in two steps. First enable the OUT1 pullup current source and OUT2 pulldown current source for $0.5*t_{d(OL)}$. If a load is connected, the current passes through the pullup resistor and the OLx_PU comparator output remains low. If an OL condition exists, the current through the pullup resistor goes to 0A and the OLx_PU comparator trips high. Second enable the OUT1 pulldown current source and OUT2 pullup current source for the other $0.5*t_{d(OL)}$. In the same way, the OLx_PD comparator output either remains low to indicate that a load is connected, or trips high to indicate an OL condition.
If both the OLx_PU and OLx_PD comparators report an OL condition, the OLx bit in the SPI register latches high and the nFAULT line goes low to indicate an OUTx OL fault. When the OL condition is removed, a clear faults command

must be issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse which resets the OL1 and OL2 register bits. The charge pump remains active during this fault condition.

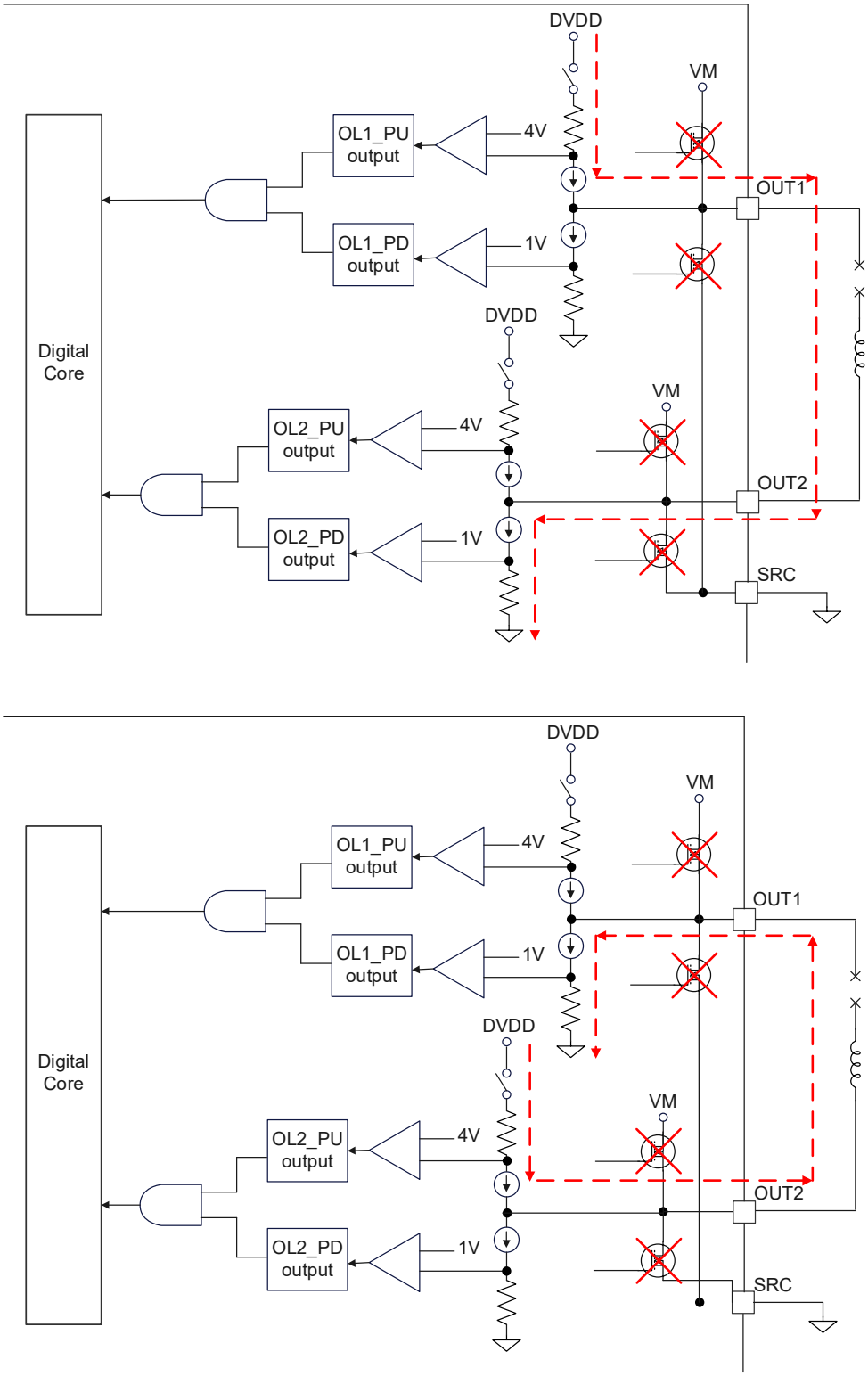


Figure 7.14 Open Load Detection Circuit

7.2.2.4.2. Open-Load Detection in Active Mode (OLA)

Open load in active mode is detected when the OUT1 and OUT2 voltages do not exhibit overshoot greater than the V_{OLA} over VM for longer than t_{OLA} between the time the low-side FET is switched off and the high-side FET is switched on during an output PWM cycle, as shown in Figure 7.15. An open load is not detected if the energy stored in the inductor is high enough to cause an overshoot greater than the V_{OLA} over VM caused by the flyback current flowing through the body diode of the high-side FET.
The OLA diagnostic is disabled by default and can be enabled by writing a 1b to the EN_OLA bit in IC4 control register for the SPI version.

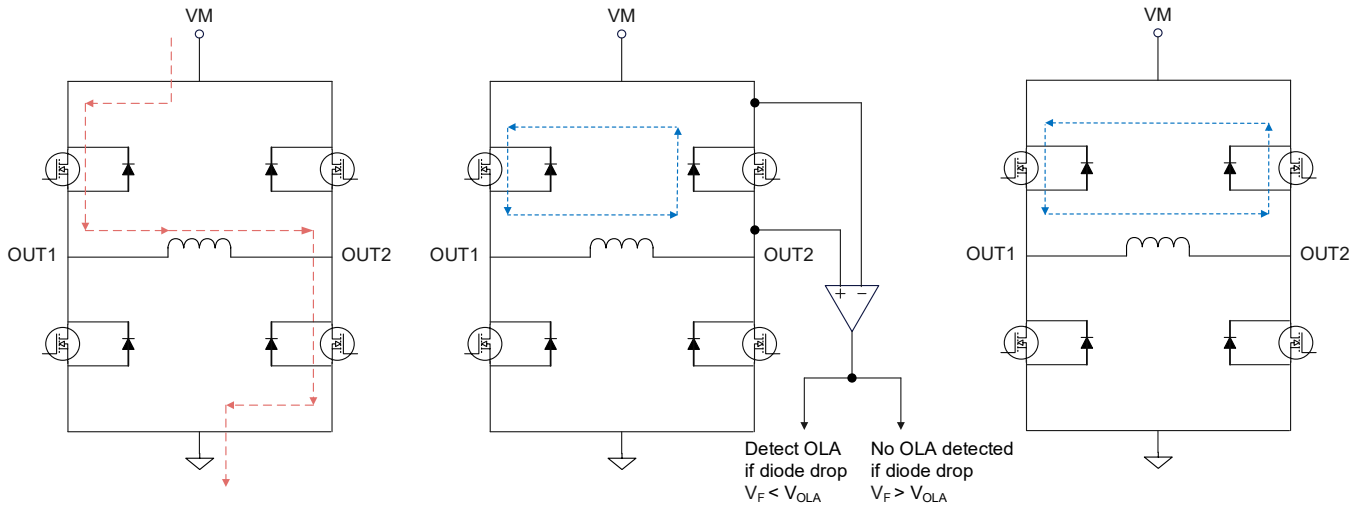


Figure 7.15 Open Load Active Mode Circuit

In PH/EN and PWM mode, the motor current decays by high-side recirculation. In independent half-bridge mode, the motor can enter the brake state either by high-side or low-side recirculation. If the motor enters the brake state using low-side recirculation, the diode V_F voltage of high-side FET is less than the V_{OLA} voltage which flags an open load fault even though the load is connected across the OUT1 and OUT2 pins. In this case, the OLA mode should not be used. If high-side current recirculation is done with independent half-bridge mode, the OLA mode functions properly.

In the hardware version of the device, OLA mode is active when the nOL pin is tied to GND. If low-side current recirculation is done with independent PWM control, an open load condition is detected even though the load is connected. To avoid this false trip, the OLD must be disabled by taking the nOL pin high; however, both OLA and OLP diagnostics will be disabled.

Note: The OLA mode is functional only when high-side recirculation of the motor current occurs. Depending on the operation conditions and external circuitry, such as the output capacitors, an open load condition could be indicated even though the load is present. This case might occur, for example, during a direction change or for small load currents with respectively small PWM duty cycles. Therefore, recommend that evaluating the open load diagnosis only in known, suitable operating conditions and to ignore it otherwise.

To avoid inadvertently triggering the open load diagnosis, a failure counter is implemented. Three consecutive occurrences of the internal open-load signal must occur, essentially three consecutive PWM pulses without freewheeling detected, before an open load condition is reported by the nFAULT pin and in the respective SPI register. If an OL condition is detected, the nFAULT pin is driven low, and the FAULT, OLD and OLx bits are latched high. When the OL condition is removed, a clear faults command must be issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse which release nFAULT and resets the OLD and OLx register bits.

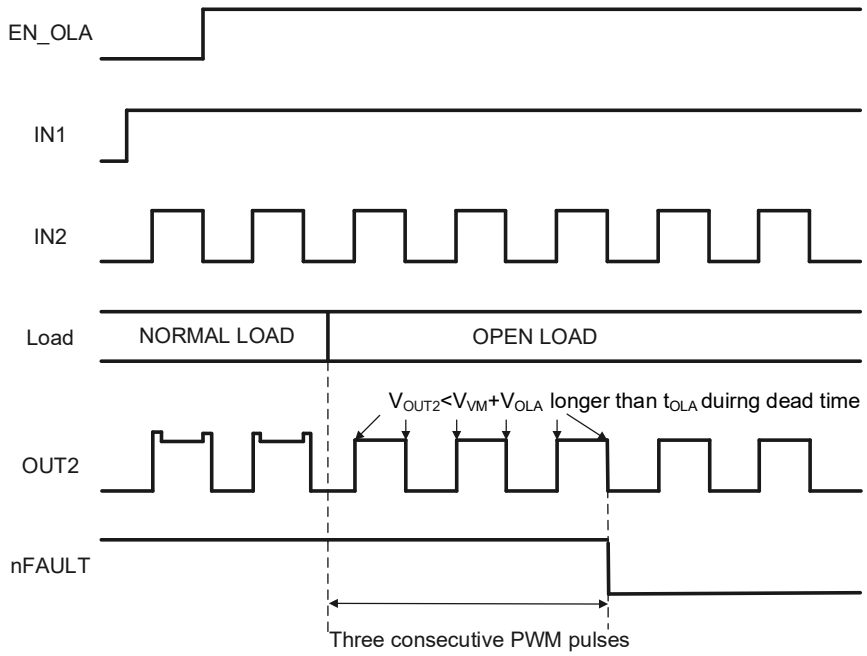


Figure 7.16 OLA Sequence for SPI version

7.2.2.5. Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown limit, the half bridges are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. In addition, the FAULT bit and TSD bit are latched high. This protection feature cannot be disabled. The overtemperature protection can operate in two different modes: latched shutdown and automatic recovery.

7.2.2.5.1. Latched Shutdown (TSD_MODE=0b)

In this mode, after a TSD event, all the outputs (OUTx) are disabled and the nFAULT pin is driven low. The FAULT and TSD bits are latched high in the SPI register. Normal operation resumes (motor-driver operation and the nFAULT line released) when the TSD condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. This mode is the default mode for a TSD event in the SPI version of the device.

7.2.2.5.2. Automatic Recovery (TSD_MODE=1b)

In this mode, after a TSD event, all the outputs (OUTx) are disabled and the nFAULT pin is driven low. The FAULT and TSD bits are latched high in the SPI register. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis (T_{TSD}–T_{HYS}). The TSD bit remains latched high indicating that a thermal event occurred until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse. This mode is the default mode for a TSD event in the hardware version of the device.

7.2.2.6. Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of SPI devices. The device performs no additional action and continues to function. When the die temperature falls below the hysteresis point of the thermal warning, the OTW bit clears automatically. The OTW bit can also be configured to report on the nFAULT pin, and set the FAULT bit in the SPI version of the device, by setting the OTW_REP bit to 1b through the SPI registers. The charge pump remains active during this condition.

Table 7.13 Fault Response

Fault	Condition	Configuration	Report	Half Bridge	Logic	Recovery
VM undervoltage (UVLO)	V_{VM} < V_{UVLO} (maximum 4.45V)	-	nFAULT FAULT, UVLO bit	Hi-Z	Active	Automatic: V_{VM} > V_{UVLO} (maximum 4.7V); UVLO bit remains set until CLR_FLT/ nSLEEP
VM UVLO reset	V_{VM} < V_{RST} (maximum 4.1V)	-	Disable	Hi-Z	Reset	Automatic: V_{VM} > V_{UVLO}
Charge pump undervoltage (CPUV)	V_{VCP} < $V_{VCP(UV)}$ (typical V_{VM}+2.3V)	DIS_CPUV = 0b	nFAULT FAULT, CPUV bit	Hi-Z	Active	Automatic: V_{VCP} > $V_{VCP(UV)}$ (typical V_{VM} + 3.5V); CPUV bit remains set until CLR_FLT/ nSLEEP
		DIS_CPUV = 1b	None	Active	Active	No Action
Overcurrent (OCP)	I_O > I_{OCP} (minimum 10A)	OCP_MODE = 00b	nFAULT FAULT, OCP, OCP_xx bit	Hi-Z	Active	Latched: CLR_FLT/ nSLEEP
		OCP_MODE = 01b	nFAULT FAULT, OCP, OCP_xx bit	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT FAULT, OCP, OCP_xx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
		OCP_MODE = 11b	None	Active	Active	No Action
Open load (OLD)	No load detected	EN_OLP = 1b	nFAULT FAULT, OLD, OLx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
		EN_OLA = 1b	nFAULT FAULT, OLD, OLx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
Current regulation (ITRIP)	I_O > I_{TRIP_LVL}	ITRIP_REP = 0b	ITRIPx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
		ITRIP_REP = 1b	nFAULT FAULT, ITRIPx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
Thermal shutdown (TSD)	T_J > T_{TSD} (minimum 165°C)	TSD_MODE = 0b	nFAULT FAULT, TSD bit	Hi-Z	Active	Latched: CLR_FLT/ nSLEEP
		TSD_MODE = 1b	nFAULT FAULT, TSD bit	Hi-Z	Active	Automatic: T_J < T_{TSD} - T_{HYS} TSD bit remains set until CLR_FLT/ nSLEEP
Thermal Warning (OTW)	T_J > T_{OTW} (minimum 140°C)	OTW_REP = 0b	OTW bit	Active	Active	Automatic: T_J < T_{OTW} - T_{HYS}
		OTW_REP = 1b	nFAULT FAULT, OTW bit	Active	Active	Automatic: T_J < T_{OTW} - T_{HYS}

7.2.3. Hardware Interface

The hardware-interface device option lets the device be configured without a SPI, however not all of the functionality is configurable. The following configuration settings are fixed for the hardware interface device option:
• CPUV is enabled
• OCP_MODE is latched shutdown
• TSD_MODE is automatic recovery
• OLP_DLY is 300µs
• OLP and OLA is activated when the open load diagnostic is enabled by the nOL pin
• ITRIP level is 6.5A if current regulation is enabled by the nITRIP pin
• TOFF is 40µs
• ITRIP not trigger nFAULT
• OTW not trigger nFAULT
• No option to independently set the outputs (OUTx) to the Hi-Z state

7.2.3.1. MODE (Tri-Level Input)

The MODE pin of the hardware version of the device determines the control interface and latches on power-up or when exiting sleep mode. Table 7.14 lists the different control interfaces that can be set with the MODE pin.

Table 7.14 NSD7315H-Q1 Mode Settings

Mode	Control Mode
L	PH/EN
H	PWM
Hi-Z (200kΩ ± 5% to GND)	Independent half bridge

When the MODE pin is latched on power-up or when exiting sleep mode, any additional changes to the signal at the MODE pin are ignored by the device. To change the mode settings, a power cycle or sleep reset must be performed on the device. To use the device in PWM mode, tie the MODE pin to either the DVDD pin or an external 5V rail. To use the device in independent half-bridge mode, the MODE pin must be connected to with a 200kΩ ± 5% resistor to GND (or left as no connect). Tying the MODE pin to the GND pin puts the device in phase and enable (PH/EN) mode.

7.2.3.2. Slew Rate

The rise and fall times of the outputs can be selected based on the configuration listed in Table 7.15 for the hardware version of the device.

Table 7.15 NSD7315H-Q1 Slew Rate Settings

SR Pin Connection	Rise Time (V/µs)	Fall Time (V/µs)
Connect to GND	55	55
22 kΩ ± 5% to GND	32	32
68 kΩ ± 5% to GND	17	17
> 2MΩ to GND (Hi-Z)	13	13
51 kΩ ± 5% to DVDD	8	8
Connect to DVDD	2.6	2.6

7.3. Device Functional Modes

7.3.1. Sleep Mode (nSLEEP=0)

The nSLEEP pin sets the state of the device. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled, DVDD output is disabled; the charge pump is disabled, and the SPI is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device goes from sleep mode automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

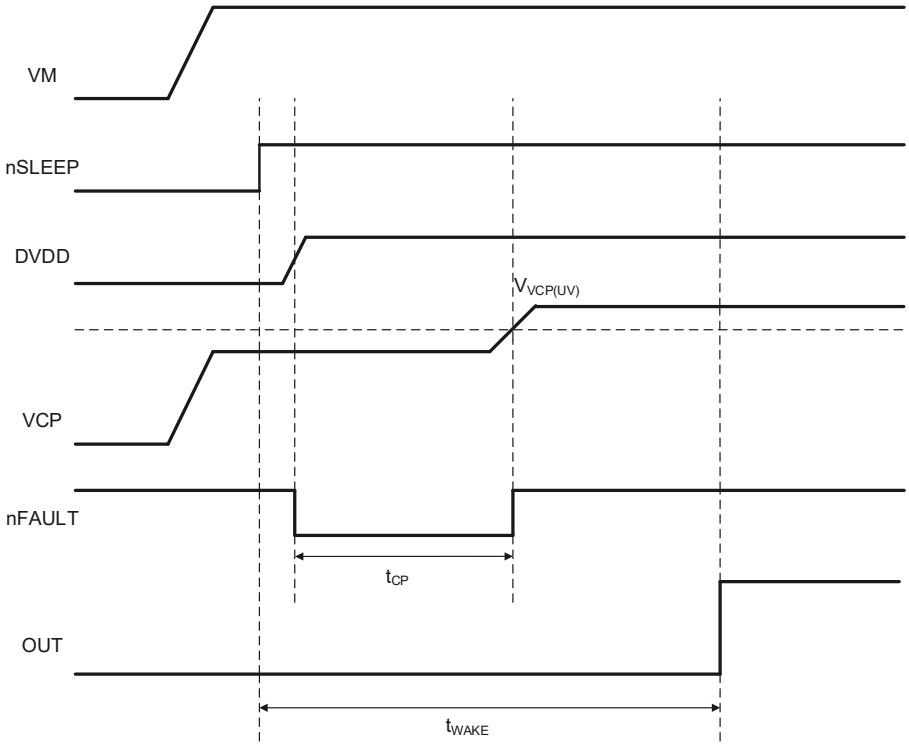


Figure 7.17 Exit Sleep Mode Sequence

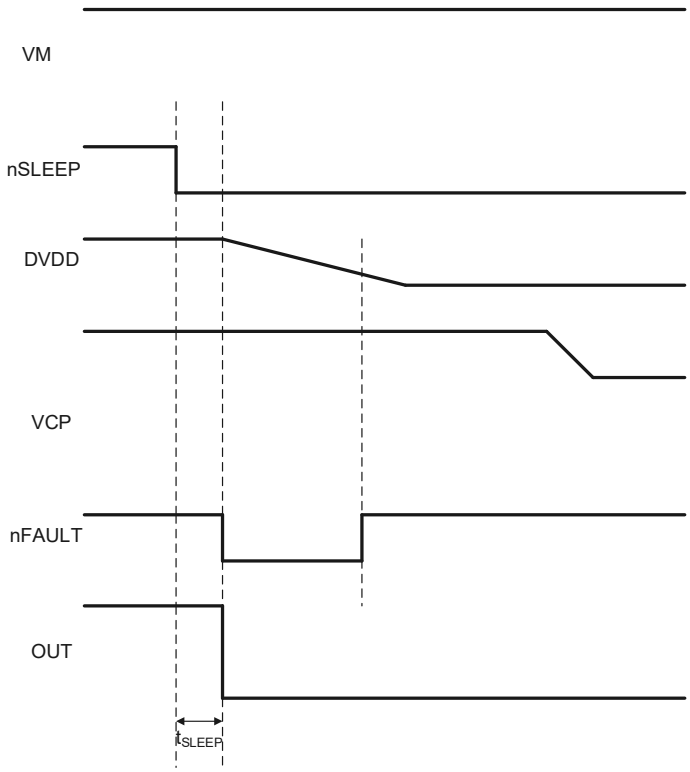


Figure 7.18 Enter Sleep Mode Sequence

7.3.2. Disable Mode (nSLEEP=1, DISABLE=1)

The DISABLE pin is used to enable or disable the half bridge in the device. When the DISABLE pin is high, the output drivers are disabled in the Hi-Z state. In this mode, the open-load diagnostic can be performed for the SPI version of the device because the SPI remains active.

7.3.3. Operating Mode (nSLEEP=1, DISABLE=0)

When the nSLEEP pin is high, the DISABLE pin is low, and VM > V_{UVLO}, the device enters the active mode. The t_{on} time must elapse before the device is ready for inputs. In this mode, the charge pump and low-side gate regulator are enabled.

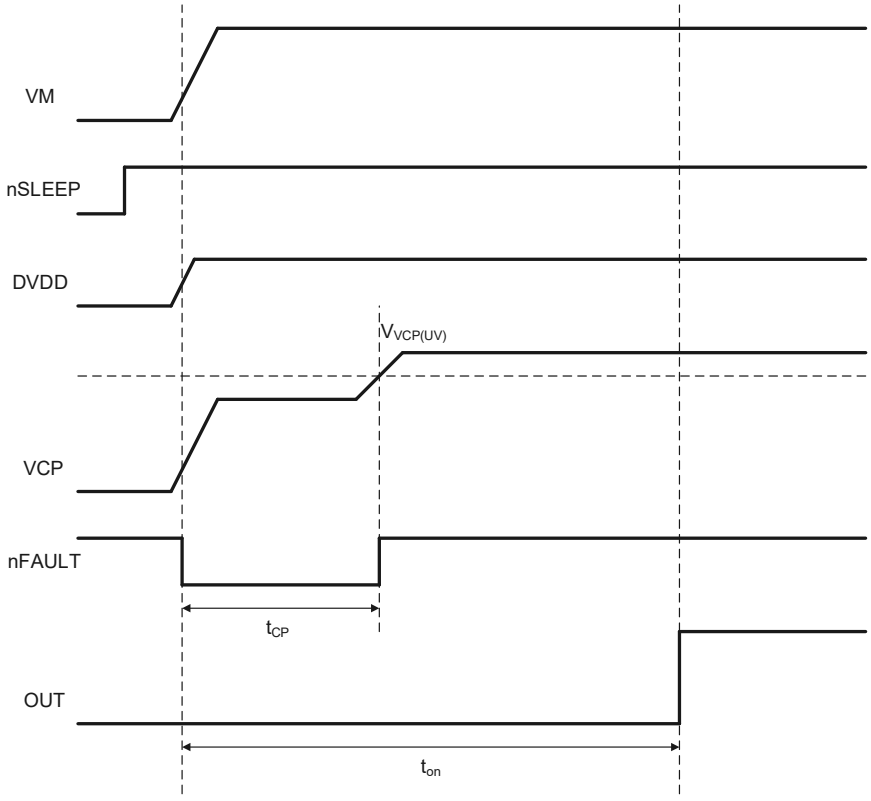


Figure 7.19 Fast Power Up Sequence

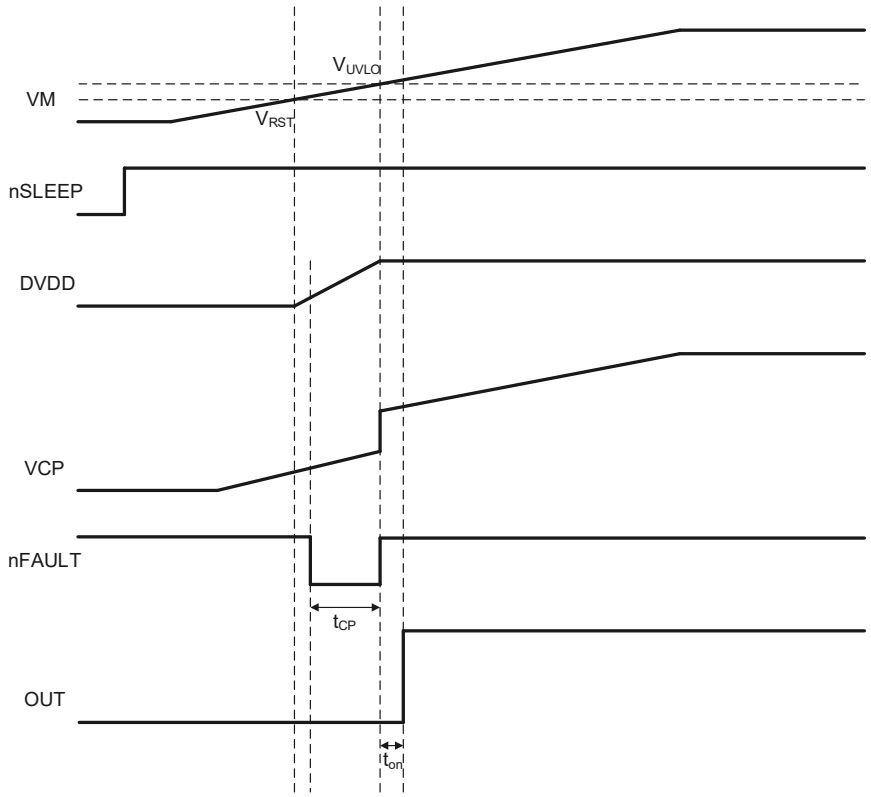


Figure 7.20 Slow Power Up Sequence

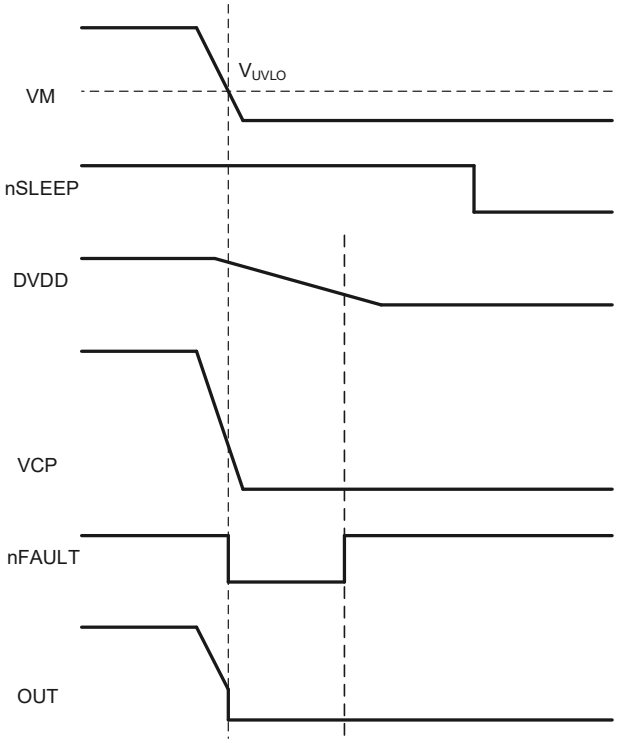


Figure 7.21 Power Down Sequence

7.3.4. nSLEEP Reset Pulse

In addition to the CLR_FLT bit in the SPI register, a latched fault can be cleared through a quick nSLEEP pulse. This pulse must be greater than the nSLEEP deglitch time of 2µs and shorter than 20µs. If nSLEEP is low for longer than 20µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 7.22). This reset pulse resets any SPI faults and does not affect the status of the charge pump or other functional blocks.

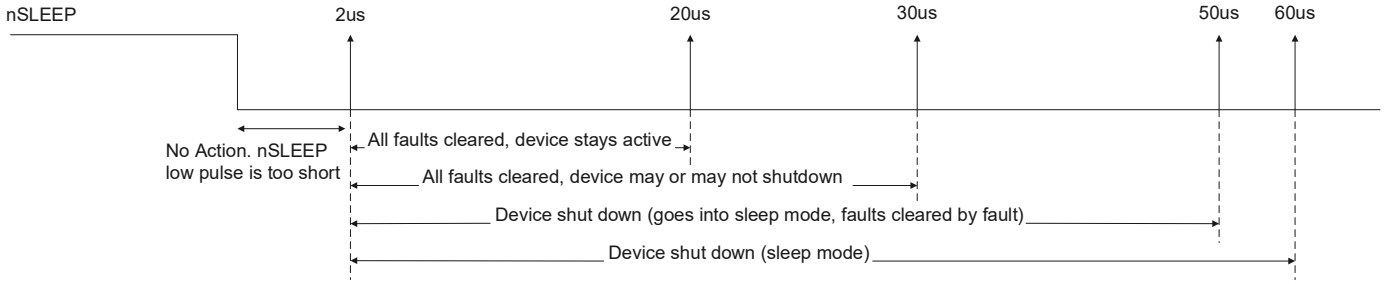


Figure 7.22 nSLEEP Reset Pulse

7.4. Programming

7.4.1. Serial Peripheral Interface (SPI) Communication

The SPI version of the device has full duplex, 4-wire synchronous communication. This section describes the SPI protocol, the command structure, and the control and status registers. The device can be connected with the MCU in the following configurations:

- One slave device
- Multiple slave devices in parallel connection
- Multiple slave devices in series (daisy chain) connection

7.4.1.1. SPI Format

The SDI input data word is 16 bits long and consists of the following format:
• 1 read or write bit, W (bit 14)
• 5 address bits, A (bits 13 through 9)
• 8 data bits, D (bits 7 through 0)

The SDO output-data word is 16 bits long and the first 8 bits make up the Status Register (S1). The Report word (R1) is the content of the register being accessed.
For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.
For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 7.16 SDI Input Data Word Format

	R/W	Address						Data							
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	W0	A4	A3	A2	A1	A0	X	D7	D6	D5	D4	D3	D2	D1	D0

Table 7.17 SDO Output Data Word Format

Status								Report							
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
1	1	OTW	UVLO	CPUV	OCP	TSD	OLD	D7	D6	D5	D4	D3	D2	D1	D0

7.4.1.2. SPI for a Single Slave Device

The SPI is used to set device configurations, operating parameters, and read out diagnostic information. The device SPI operates in slave mode. The SPI input-data (SDI) word consists of a 16-bit word, with 8 bits command and 8 bits of data. The SPI output data (SDO) word consists of 8 bits of status register with fault status indication and 8 bits of register data. Figure 7.23 shows the data sequence between the MCU and the SPI slave driver.

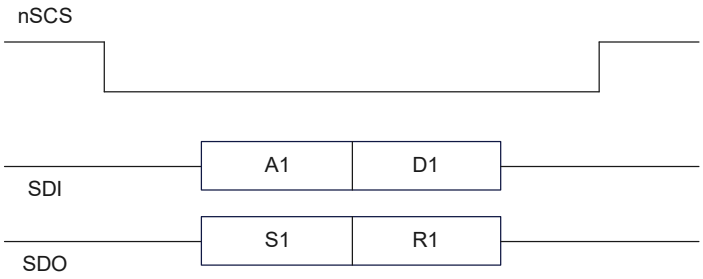


Figure 7.23 SPI Transaction Between MCU and SPI version of the device

A valid frame must meet the following conditions:
• The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
• The nSCS pin should be taken high for at least 500 ns between frames.
• When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high-impedance state (Hi-Z).
• Full 16 SCLK cycles must occur.
• Data is captured on the falling edge of the clock and data is driven on the rising edge of the clock.
• The most-significant bit (MSB) is shifted in and out first.
• If the data word sent to SDI pin is less than 16 bits or more than 16 bits, a frame error occurs and the data word is ignored.
• For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

7.4.1.3. SPI for Multiple Slave Devices in Parallel Configuration

Multiple devices can be connected in parallel as shown in Figure 7.24. In this configuration, all the slave devices can share the same SDI, SDO, and CLK lines from the micro-controller, but has dedicated chip-select pin (CSx) for each device from the micro-controller.
The micro-controller activates the SPI of a given device via that device's chip-select input, the other devices remain inactive for SPI transactions. This configuration helps reduce micro-controller resources for SPI transactions if multiple slave devices are connected to the same micro-controller.

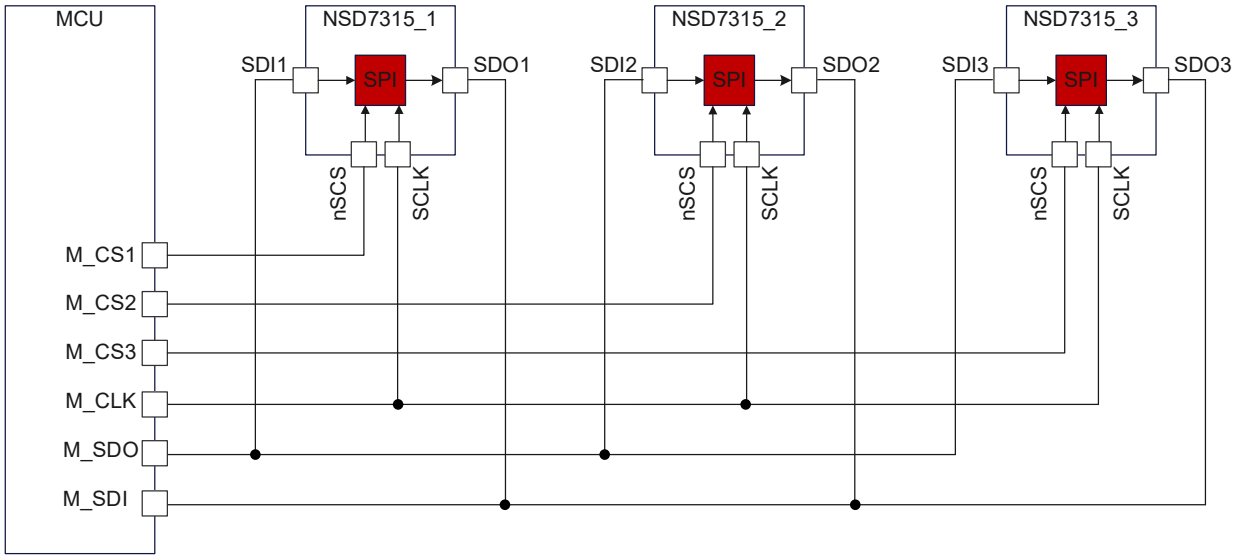


Figure 7.24 Three NSD7315S-Q1 Devices Connected in Parallel Configuration

7.4.1.4. SPI for Multiple Slave Devices in Daisy Chain Configuration

The device can be connected in a daisy chain configuration to keep GPIO ports available when multiple devices are communicating to the same MCU. Figure 7.25 shows the topology when three devices are connected in series.

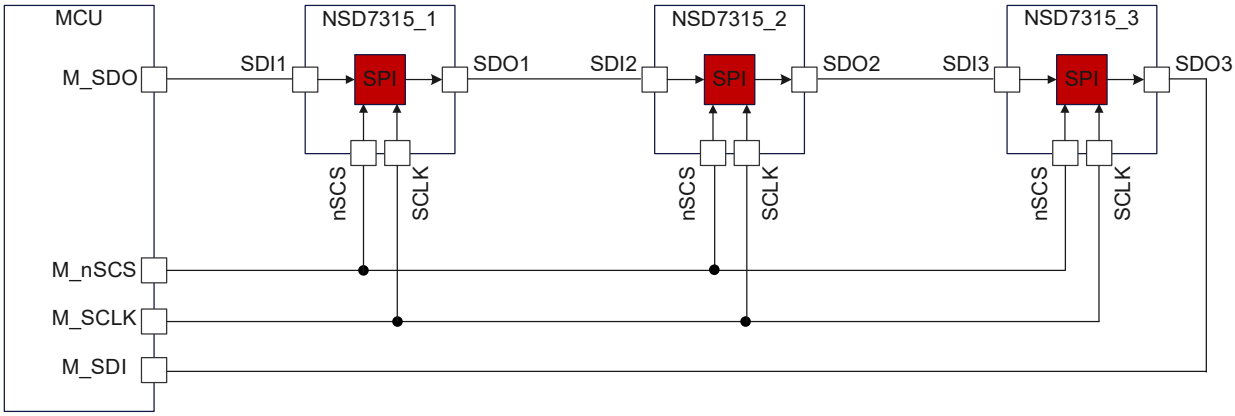


Figure 7.25 Three NSD7315S-Q1 Devices Connected in Daisy Chain

The first device in the chain receives data from the MCU in the following format for 3-device configuration: 2 bytes of header (HDRx) followed by 3 bytes of address (Ax) followed by 3 bytes of data (Dx).

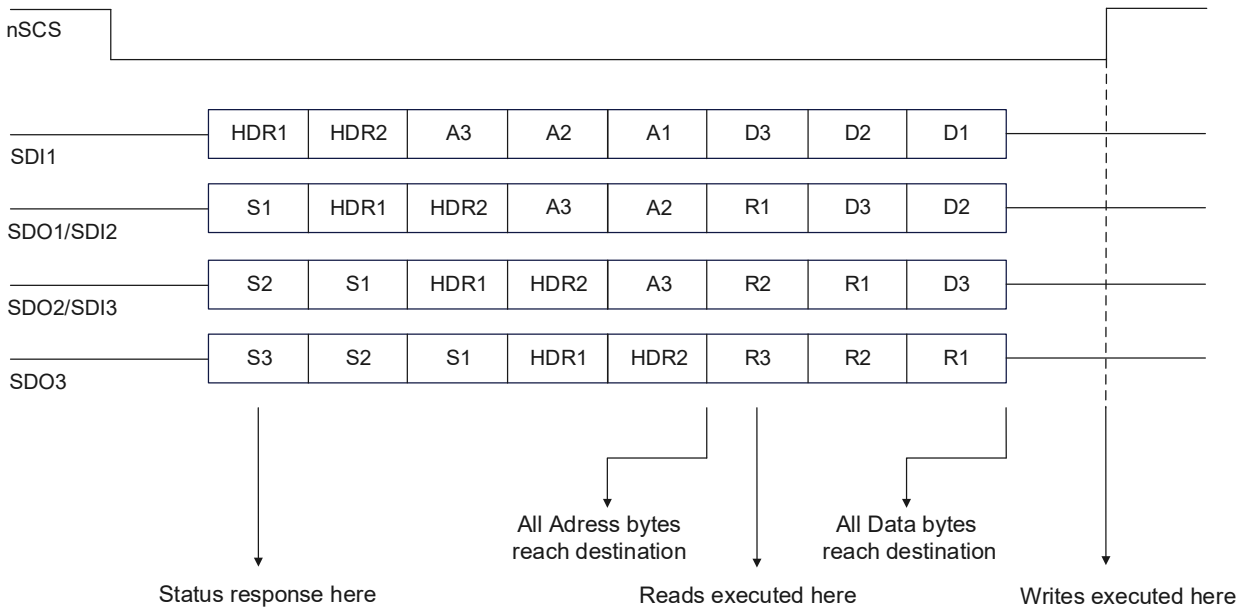


Figure 7.26 SPI Frame with Three NSD7315S-Q1 Devices

After the data has been transmitted through the chain, the MCU receives the data string in the following format for 3-device configuration: 3 bytes of status (Sx) followed by 2 bytes of header followed by 3 bytes of report (Rx).

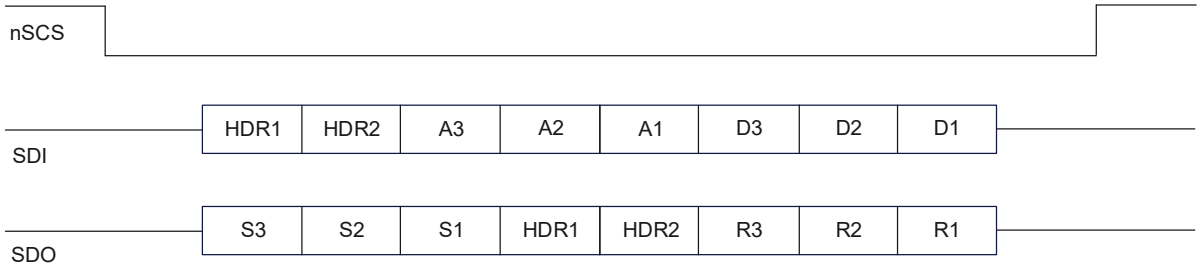


Figure 7.27 SPI Data Sequence for Three NSD7315S-Q1 Devices

The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. Header values N5 through N0 are 6 bits dedicated to show the number of devices in the chain. Up to 63 devices can be connected in series for each daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

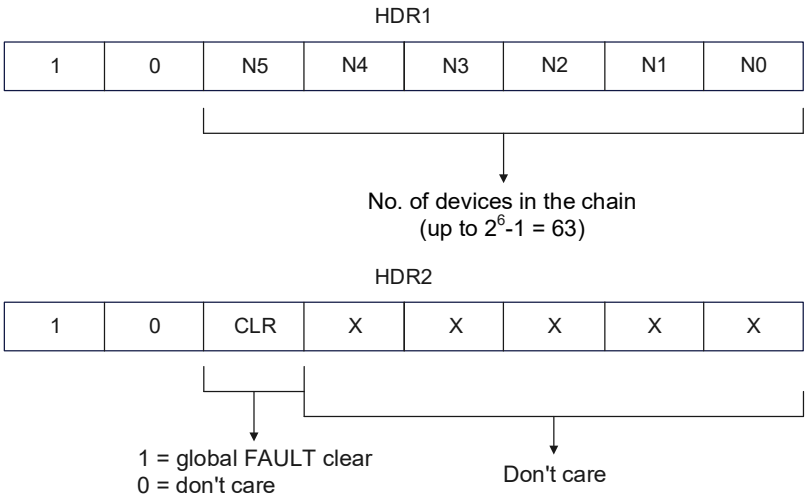


Figure 7.28 Header Bytes

The status byte provides information about the fault status register for each device in the daisy chain so that the MCU does not have to initiate a read command to read the fault status from any particular device. This keeps additional read commands for the MCU and makes the system more efficient to determine fault conditions flagged in a device. Status bytes must start with 1 and 1 for the two MSBs.

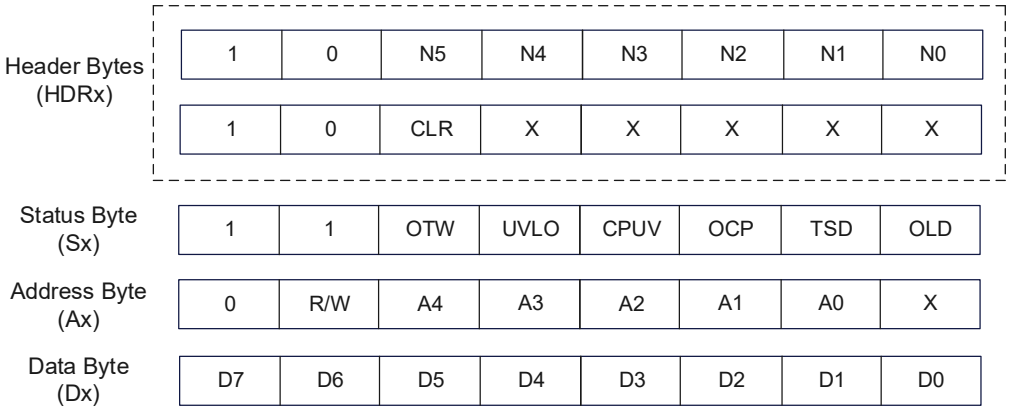


Figure 7.29 Contents of Header, Status, Address and Data Bytes

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives followed by the first header byte. For example, in this 3-device configuration, device 2 in the chain receives two status bytes before receiving the HDR1 byte which is then followed by the HDR2 byte.

From the two status bytes, the data can determine that its position is second in the chain. From the HDR2 byte, the data can determine how many devices are connected in the chain. In this way, the data only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a 1-device connection. The report bytes (R1 through R3), as shown in Figure 7.27, are the content of the register being accessed.

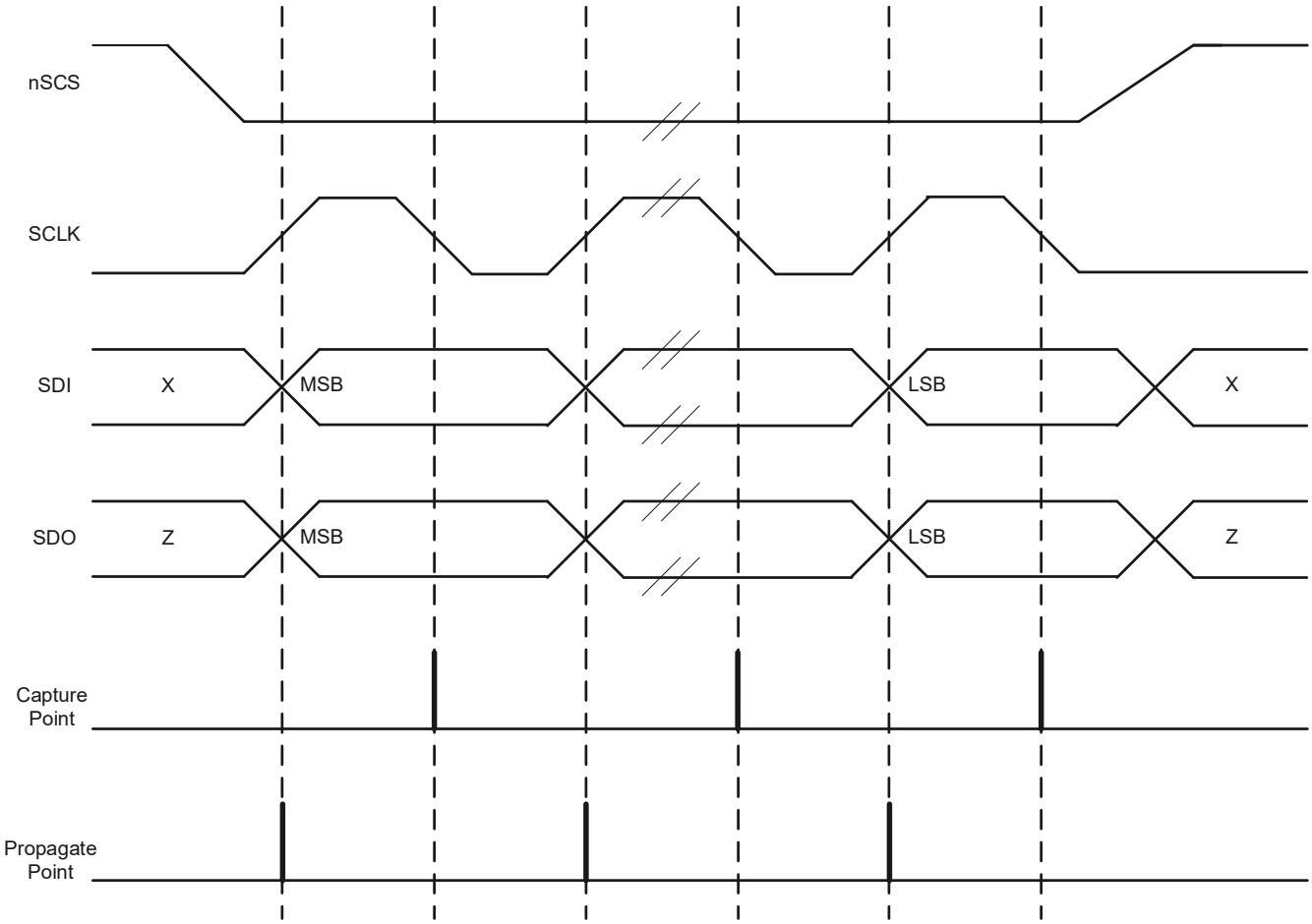


Figure 7.30 SPI Transaction

7.5. Register Maps

Table 7.18 lists the memory-mapped registers for the device. All register addresses not listed in should be considered as reserved locations and the register contents should not be modified.

Table 7.18 Memory Map

Register Name	7	6	5	4	3	2	1	0	Access Type	Address
FAULT Status	RSVD	FAULT	OTW	UVLO	CPUV	OCP	TSD	OLD	R	0x00
DIAG Status	OL1	OL2	ITRIP1	ITRIP2	OCP_H1	OCP_L1	OCP_H2	OCP_L2	R	0x01
IC1 Control	TOFF		SPI_IN	SR			MODE		RW	0x02
IC2 Control	ITRIP_REP	TSD_MODE	OTW_REP	DIS_CPUV	OCP_TRETRY		OCP_MODE		RW	0x03
IC3 Control	CLR_FLT	LOCK			OUT1_DIS	OUT2_DIS	EN_IN1	PH_IN2	RW	0x04
IC4 Control	RSVD	EN_OLP	OLP_DLY	EN_OLA	ITRIP_LVL		DIS_ITRIP		RW	0x05

Complex bit access types are encoded to fit into small table cells. Table 7.19 shows the codes that are used for access types in this section.

Table 7.19 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1. Status Registers

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers. Table 7.20 lists the memory-mapped registers for the status registers. All register offset addresses not listed in should be considered as reserved locations and the register contents should not be modified.

Table 7.20 Status Registers Summary Table

Address	Register Name
0x00	FAULT status
0x01	DIAG status

7.5.1.1. FAULT Status Register Name (address=0x00)

FAULT status is shown in Table 7.21 and described in Table 7.22.
Read-only

Table 7.21 FAULT Status Register

7	6	5	4	3	2	1	0
RSVD	FAULT	OTW	UVLO	CPUV	OCP	TSD	OLD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7.22 FAULT Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R	0b	Reserved
6	FAULT	R	0b	Global FAULT status register. Compliments the nFAULT pin
5	OTW	R	0b	Indicates overtemperature warning
4	UVLO	R	0b	Indicates UVLO fault condition
3	CPUV	R	0b	Indicates charge-pump undervoltage fault condition
2	OCP	R	0b	Indicates an overcurrent condition
1	TSD	R	0b	Indicates an overtemperature shutdown
0	OLD	R	0b	Indicates an open-load detection

7.5.1.2. DIAG Status Register Name (address=0x01)

DIAG status is shown in Table 7.23 and described in Table 7.24.
Read-only

Table 7.23 DIAG Status Register

7	6	5	4	3	2	1	0
OL1	OL2	ITRIP1	ITRIP2	OCP_H1	OCP_L1	OCP_H2	OCP_L2
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7.24 DIAG Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	OL1	R	0b	Indicates open-load detection on half bridge 1
6	OL2	R	0b	Indicates open-load detection on half bridge 2
5	ITRIP1	R	0b	Indicates the current regulation status of half bridge 1 0b = Indicates output 1 is not in current regulation 1b = Indicates output 1 is in current regulation
4	ITRIP2	R	0b	Indicates the current regulation status of half bridge 2 0b = Indicates output 2 is not in current regulation 1b = Indicates output 2 is in current regulation
3	OCP_H1	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1
2	OCP_L1	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1
1	OCP_H2	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2
0	OCP_L2	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2

7.5.2. Control Registers

The IC control registers are used to configure the device. Control registers are read and write capable.
Table 7.25 lists the memory-mapped registers for the control registers. All register offset addresses not listed in should be considered as reserved locations and the register contents should not be modified.

Table 7.25 Control Registers Summary Table

Address	Register Name
0x02	IC1 control
0x03	IC2 control
0x04	IC3 control
0x05	IC4 control

7.5.2.1. IC1 Control Register (address=0x02)

IC1 control is shown in Table 7.26 and described in Table 7.27.
Read/Write

Table 7.26 IC1 Control Register

7	6	5	4	3	2	1	0
TOFF		SPI_IN	SR			MODE	
R/W-01b		R/W-0b	R/W-100b			R/W-01b	

Table 7.27 IC1 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	TOFF	R/W	01b	00b = 20μs **01b = 40μs** 10b = 60μs 11b = 80μs
5	SPI_IN	R/W	0b	**0b = Outputs follow input pins (INx)** 1b = Outputs follow SPI registers EN_IN1 and PH_IN2
4-2	SR	R/W	100b	000b = 55V/μs rise time 001b = 32V/μs rise time 010b = 17V/μs rise time 011b = 13V/μs rise time **100b = 10V/μs rise time** 101b = 8V/μs rise time 110b = 5V/μs rise time 111b = 2.6V/μs rise time
1-0	MODE	R/W	01b	00b = PH/EN **01b = PWM** 10b = Independent half bridge 11b = Input disabled; bridge Hi-Z

7.5.2.2. IC2 Control Register (address=0x03)

IC2 control is shown in Table 7.28 and described in Table 7.29.
Read/Write

Table 7.28 IC2 Control Register

7	6	5	4	3	2	1	0
ITRIP_REP	TSD_MODE	OTW_REP	DIS_CPUV	OCP_TRETRY		OCP_MODE	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b		R/W-00b	

Table 7.29 IC2 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	ITRIP_REP	R/W	0b	**0b = ITRIP is not reported on nFAULT or the FAULT bit** 1b = ITRIP is reported on nFAULT and the FAULT bit
6	TSD_MODE	R/W	0b	**0b = Overtemperature condition causes a latched fault** 1b = Overtemperature condition causes an automatic recovery fault
5	OTW_REP	R/W	0b	**0b = OTW is not reported on nFAULT or the FAULT bit** 1b = OTW is reported on nFAULT and the FAULT bit
4	DIS_CPUV	R/W	0b	**0b = Charge pump undervoltage fault is enabled** 1b = Charge pump undervoltage fault is disabled
3-2	OCP_TRETRY	R/W	11b	00b = Overcurrent retry time is 0.5ms

				01b = Overcurrent retry time is 1ms 10b = Overcurrent retry time is 2ms **11b = Overcurrent retry time is 4ms**
1-0	OCP_MODE	R/W	00b	**00b = Overcurrent condition causes a latched fault** 01b = Overcurrent condition causes an automatic retrying fault 10b = Overcurrent condition is report only but no action is taken 11b = Overcurrent condition is not reported and no action is taken

7.5.2.3. IC3 Control Register (address=0x04)

IC3 control is shown in Table 7.30 and described in Table 7.31.
Read/Write

Table 7.30 IC3 Control Register

7	6	5	4	3	2	1	0
CLR_FLT	LOCK			OUT1_DIS	OUT2_DIS	EN_IN1	PH_IN2
R/W-0b	R/W-100b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7.31 IC3 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write a 1b to this bit to clear the fault bits. This bit is automatically reset after a write.
6-4	LOCK	R/W	100b	Write 011b to this register to lock all register settings in the IC1 control register except to these bits and address 0x04, bit 7 (CLR_FLT) Write 100b to this register to unlock all register settings in the IC1 control register
3	OUT1_DIS	R/W	0b	Enabled only in the independent half bridge mode **0b = Half bridge 1 enabled** 1b = Half bridge 1 disabled (Hi-Z)
2	OUT2_DIS	R/W	0b	Enabled only in the independent half bridge mode **0b = Half bridge 2 enabled** 1b = Half bridge 2 disabled (Hi-Z)
1	EN_IN1	R/W	0b	EN/IN1 bit to control the outputs through SPI (when SPI_IN = 1b)
0	PH_IN2	R/W	0b	PH/IN2 bit to control the outputs through SPI (when SPI_IN = 1b)

7.5.2.4. IC4 Control Register (address=0x05)

IC4 control is shown in Table 7.32 and described in Table 7.33.
Read/Write

Table 7.32 IC4 Control Register

7	6	5	4	3	2	1	0
RSVD	EN_OLP	OLP_DLY	EN_OLA	ITRIP_LVL		DIS_ITRIP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-10b		R/W-00b	

Table 7.33 IC4 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved
6	EN_OLP	R/W	0b	Write 1b to run open load diagnostic in standby mode. When open load test is complete, EN_OLP returns to 0b (status check)

5	OLP_DLY	R/W	0b	**0b = Open load diagnostic delay is 300μs** 1b = Open load diagnostic delay is 1.2ms
4	EN_OLA	R/W	0b	**0b = Open load diagnostic in active mode is disabled** 1b = Enable open load diagnostics in active mode
3-2	ITRIP_LVL	R/W	10b	00b = 4A 01b = 5.4A **10b = 6.5A** 11b = 7A
1-0	DIS_ITRIP	R/W	00b	**00b = Current regulation is enabled** 01b = Current regulation is disabled for OUT1 10b = Current regulation is disabled for OUT2 11b = Current regulation is disabled for both OUT1 and OUT2

8. Application and Implementation

8.1. Application Information

The device is used mainly to drive a brushed DC motor. The on-board current regulation allows for limiting the motor current during start-up and stall conditions. The design procedures in the section 8.2 highlight how to use and configure the SPI version of the device.

8.2. Typical Application

Figure 8.1 and 8.2 show the typical application schematic for the SPI version and HW version of the device.

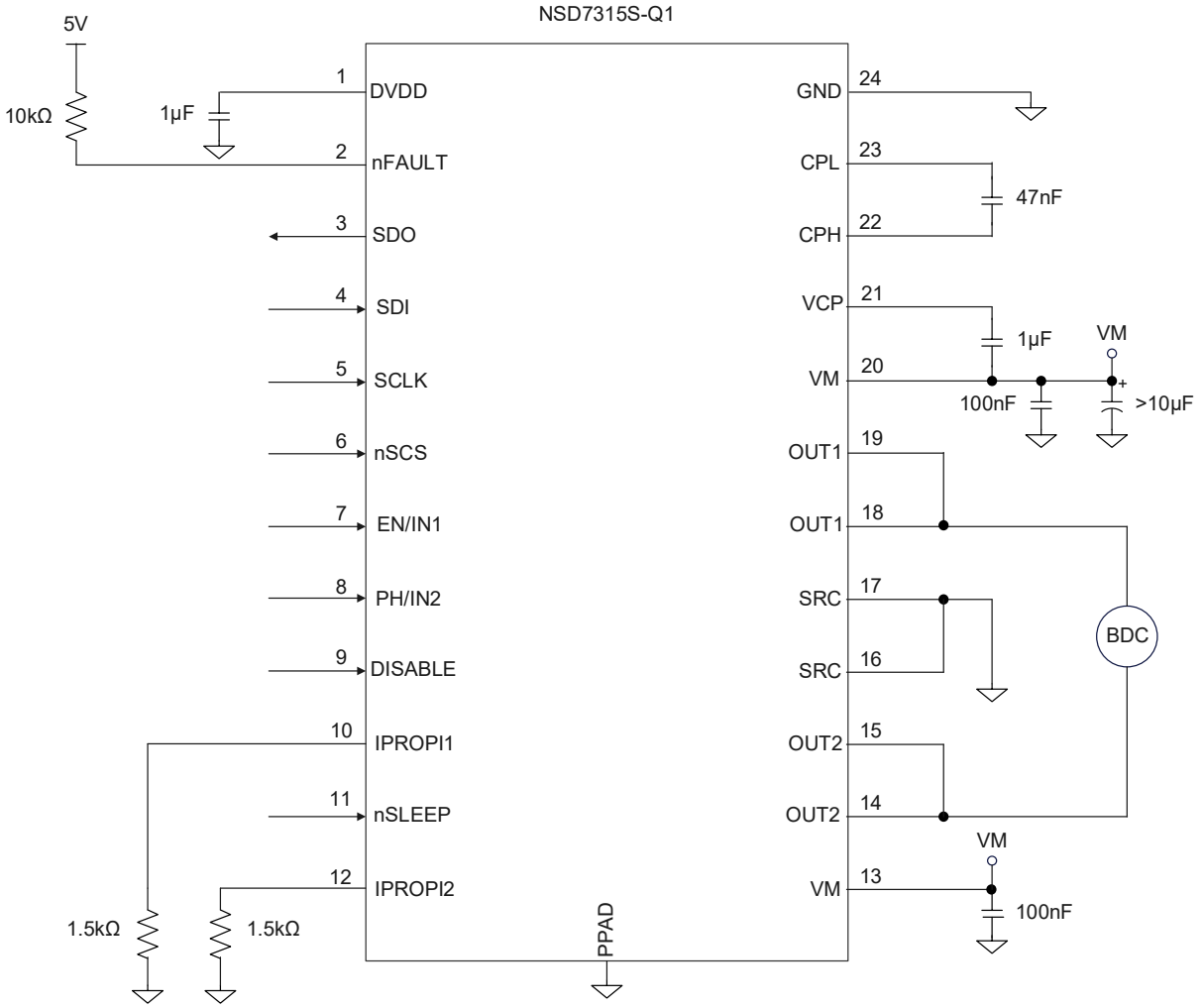


Figure 8.1 Typical application schematic of SPI version

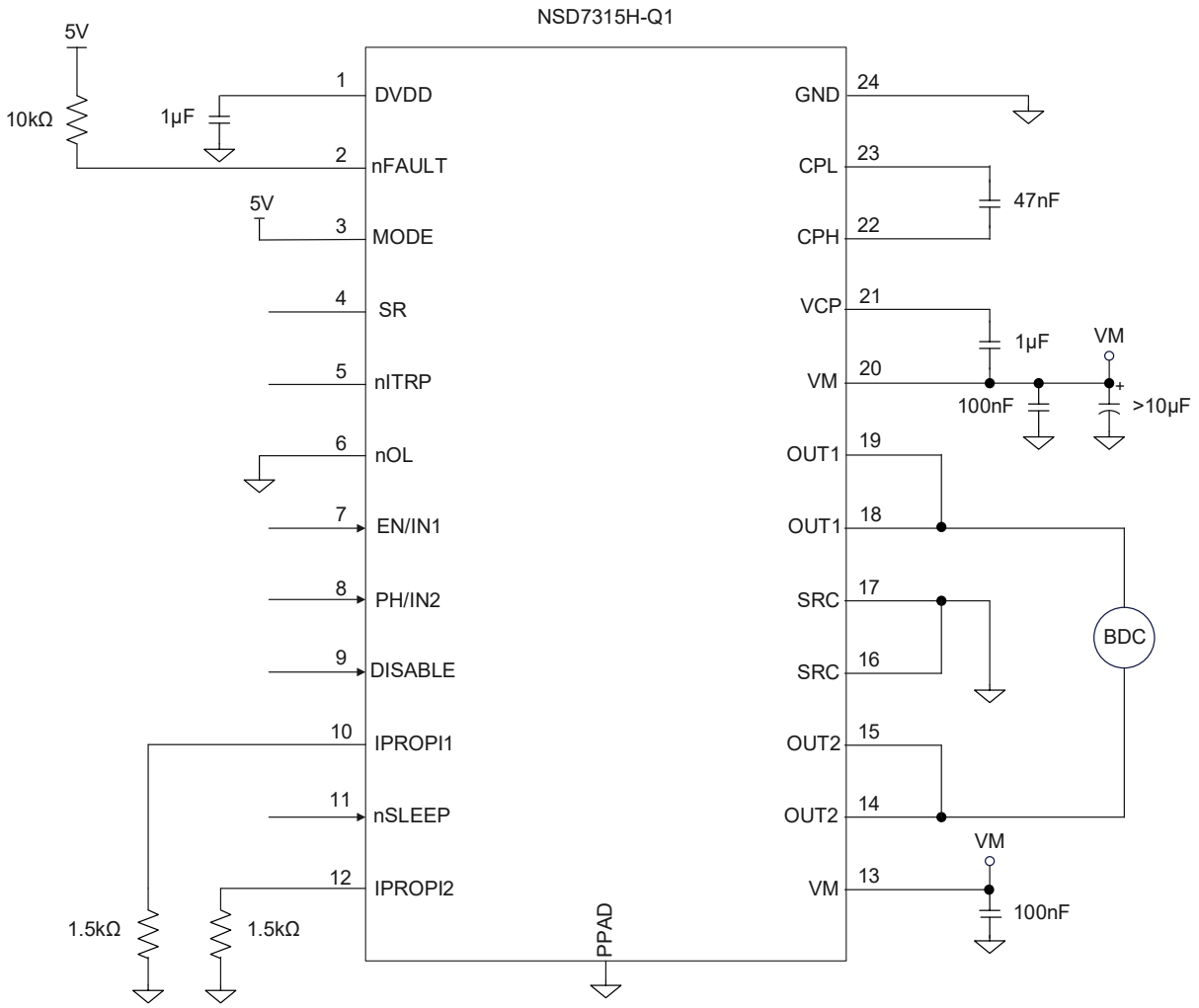


Figure 8.2 Typical application schematic of HW version

Table 8.1 lists the recommended external components for the device.

Table 8.1 External Components

Component	PIN1	PIN2	Recommended
C_{VM1}	VM	GND	100nF ceramic capacitor rated for VM
C_{VM2}	VM	GND	Bulk capacitor rated for VM
C_{VCP}	VCP	VM	16V, 1μF ceramic capacitor
C_{FLY}	CPH	CPL	47nF capacitor rated for VM
C_{DVDD}	DVDD	GND	6.3V, 1μF ceramic capacitor
R_{nFAULT}	5V	nFAULT	≥10kΩ pullup resistor to external 5V supply
$R_{SENSE-1}$	IPROPI1	GND	Resistors to convert mirrored current into a voltage
$R_{SENSE-2}$	IPROPI2	GND	Resistors to convert mirrored current into a voltage

8.2.1. Design Requirements

Table 8.2 lists the example input parameters for the system design.

Table 8.2 Design Parameters

Design Parameters	Reference	Example Value
Supply voltage	VM	13.5V
Motor RMS current	I_{RMS}	2.5A
Motor winding inductance	L_M	2.9mH
Motor current trip point	I_{TRIP}	6.5A
PWM frequency	f_{PWM}	10kHz
Sense resistor	R_{SENSE}	1.5kΩ
Rise and fall times (slew rate)	t_{SR}	1μs

8.2.1.1. Motor Voltage

The motor voltage used depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.1.2. Drive Current and Power Dissipation

The current path is through the high-side sourcing power driver, motor winding, and low-side sinking power driver. The amount of current the device can drive depends on the power dissipation without going into thermal shutdown. The amount of current that can be power dissipation losses in one source and sink power driver are calculated in Equation 2.

$$P_D = I_{RMS}^2 \times (R_{DS(on)High\text{-}side} + R_{DS(on)Low\text{-}side}) \quad (2)$$

The I_{OUT} current is equal to the average current drawn by the DC motor. At 25^0C ambient temperature, the power dissipation becomes $(2.5A)^2 \times (150m\Omega) = 0.94W$.

The temperature that the device reaches depends on the thermal resistance to the air and PCB. Soldering the device thermal PAD to the PCB ground plane, with vias to the top and bottom board layers, is important to dissipate heat into the PCB and reduce the device temperature. In the example used here, the device had an effective thermal resistance $R_{\theta JA}$ of 29.5^0C/W. The junction temperature T_J value becomes as shown in Equation3.

$$T_J = T_A + P_D \times R_{\theta JA} = 25^0C + 0.94W \times 29.5^0C/W = 53^0C \quad (3)$$

At start-up and fault conditions, the current flowing through the motor is much higher than normal running current; these peak currents and their duration must also be considered. High PWM frequency also results in higher switching losses. Typically, switching the inputs at 100kHz compared to 10kHz causes 20% more power loss in heat.

Power dissipation in the device is dominated by the power dissipated of the internal MOSFET resistance. The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Total power dissipation for the device is composed of three main components. These are the supply current dissipation, the power MOSFET switching losses, and the power MOSFET $R_{DS(ON)}$ (conduction) losses. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

$$P_{TOT} = P_{VM} + P_D + P_{SW} \quad (4)$$

P_{VM} can be calculated from the nominal supply voltage (V_M) and the supply current (I_{VM}) in active mode.

$$P_{VM} = V_M \times I_{VM} = 13.5V \times 1.3mA = 17.6mW \quad (5)$$

P_{SW} can be calculated from the nominal supply voltage (V_M), average output current (I_{RMS}), switching frequency (f_{PWM}) and the device output rise and fall times (t_{SR}) time specifications.

$$P_{SW} = P_{SW\_RISE} + P_{SW\_FALL} = 0.17W + 0.17W = 0.34W \quad (6)$$

$$P_{SW\_RISE} = 0.5 \times V_M \times I_{RMS} \times t_{SR} \times f_{PWM} = 0.5 \times 13.5V \times 2.5A \times 1\mu s \times 10kHz = 0.17W \quad (7)$$

$$P_{SW\_FALL} = 0.5 \times V_M \times I_{RMS} \times t_{SR} \times f_{PWM} = 0.5 \times 13.5V \times 2.5A \times 1\mu s \times 10kHz = 0.17W \quad (8)$$

Therefore, total power dissipation (P_{TOT}) at 25^0C ambient temperature becomes = $P_{VM} + P_{SW} + P_D$ = 17.6mW +0.34W + 0.94W = 1.3W.

P_{TOT} makes the junction temperature (T_J) of the device to be

$$T_J = T_A + P_{TOT} \times R_{\theta JA} = 25^0C + 1.3W \times 29.5^0C/W = 63^0C \quad (9)$$

The power dissipation from power MOSFET switching losses and quiescent supply current dissipation results is approximately 10^0C rise in the junction temperature (different between Equation 9 and Equation 3). Care must be taken when doing the PCB layout and heatsinking the motor driver device so that the thermal characteristics are properly managed.

8.2.1.3. Sense Resistor

For optimal performance, the sense resistor must have the following features:
• Surface-mount device
• Low inductance
• Placed closely to the motor driver device
Use Equation 10 to calculate the power dissipation (P_D) of the sense resistor.

$$P_D = (I_{RMS} / k)^2 \times R_{SENSE} \quad (10)$$

In this example, for the RMS motor current is 2.5A, the sense resistor of 1.5kΩ dissipates approximately 7.5mW of power. The power quickly increases with higher current levels. Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components that generate heat, the system designer should add margin. Measuring the actual sense resistor temperature in a final system is best.

8.2.2. Detailed Design Procedure

8.2.2.1. Thermal Considerations

The device has thermal shutdown (TSD) at 165°C (mininum). If the die temperature exceeds this TSD threshold, the device will be disabled.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high the ambient temperature.

8.2.2.2. Heatsinking

The package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.
In general, the more copper area that can be provided, the more power can be dissipated.

9. Layout

9.1. Layout Guidelines

Each VM pin must be bypassed to ground using low ESR ceramic bypass capacitors with recommended values of 0.1μF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

Additional bulk capacitance is required to bypass the high current path. This bulk capacitance should be placed such that it minimizes the length of any high current paths. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 47nF, rated for VM, and be of type X5R or X7R. Additionally, place a low ESR ceramic capacitor between the VCP and VM pins. This capacitor should be 1μF, rated for 16V, and be of type X5R or X7R.

The current sense resistors should be placed as close as possible to the device pins to minimize trace inductance between the device pin and resistors.

9.2. Layout Example

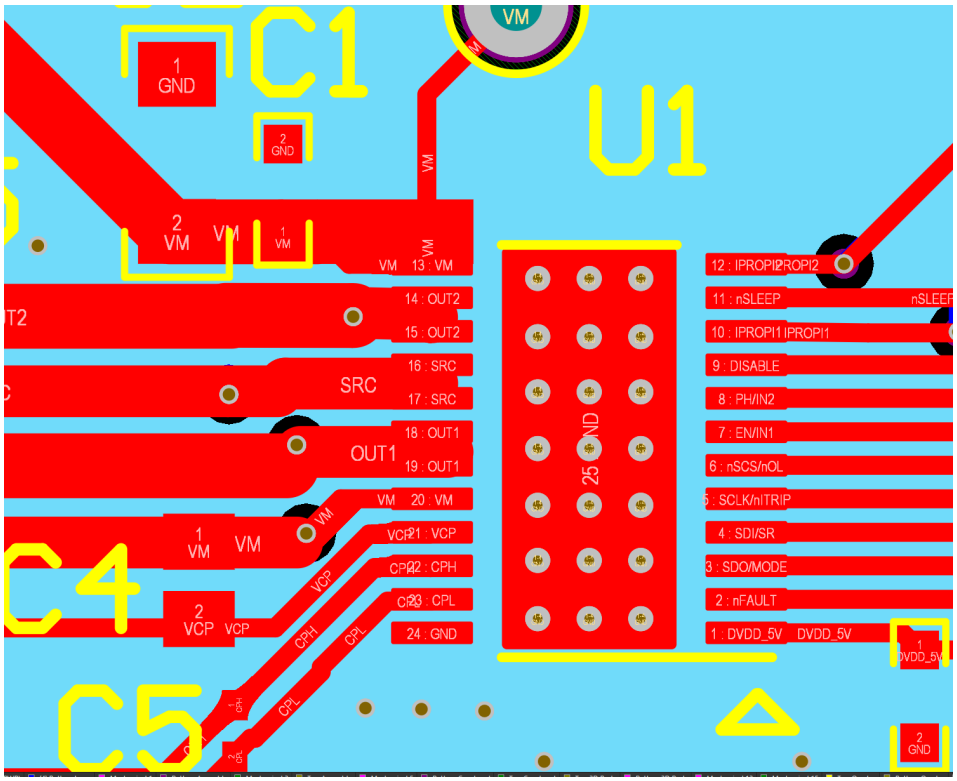
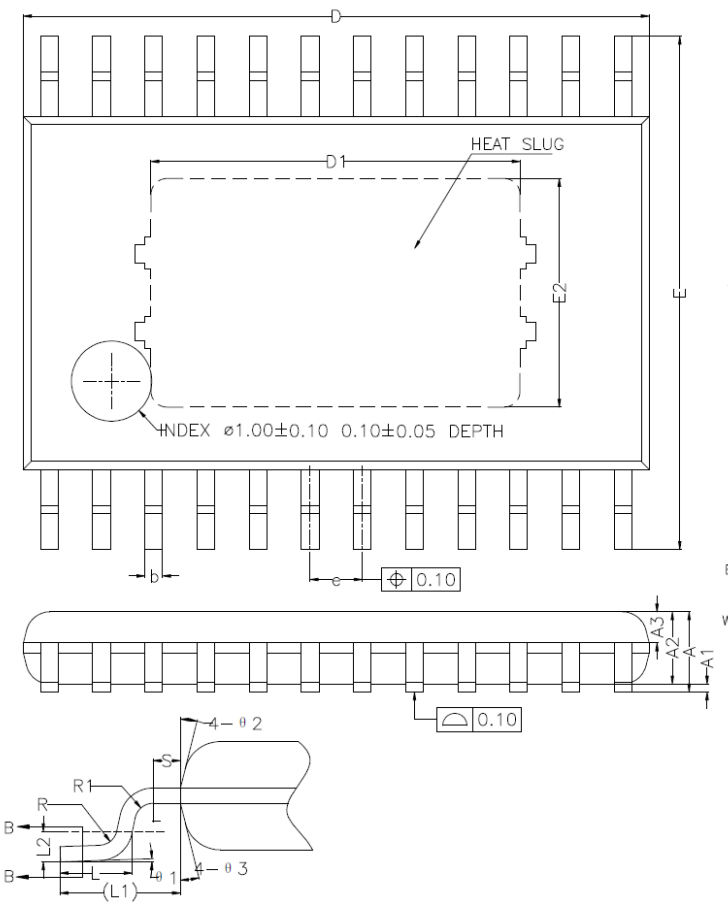


Figure 9.1 Layout Example

10. Package Information

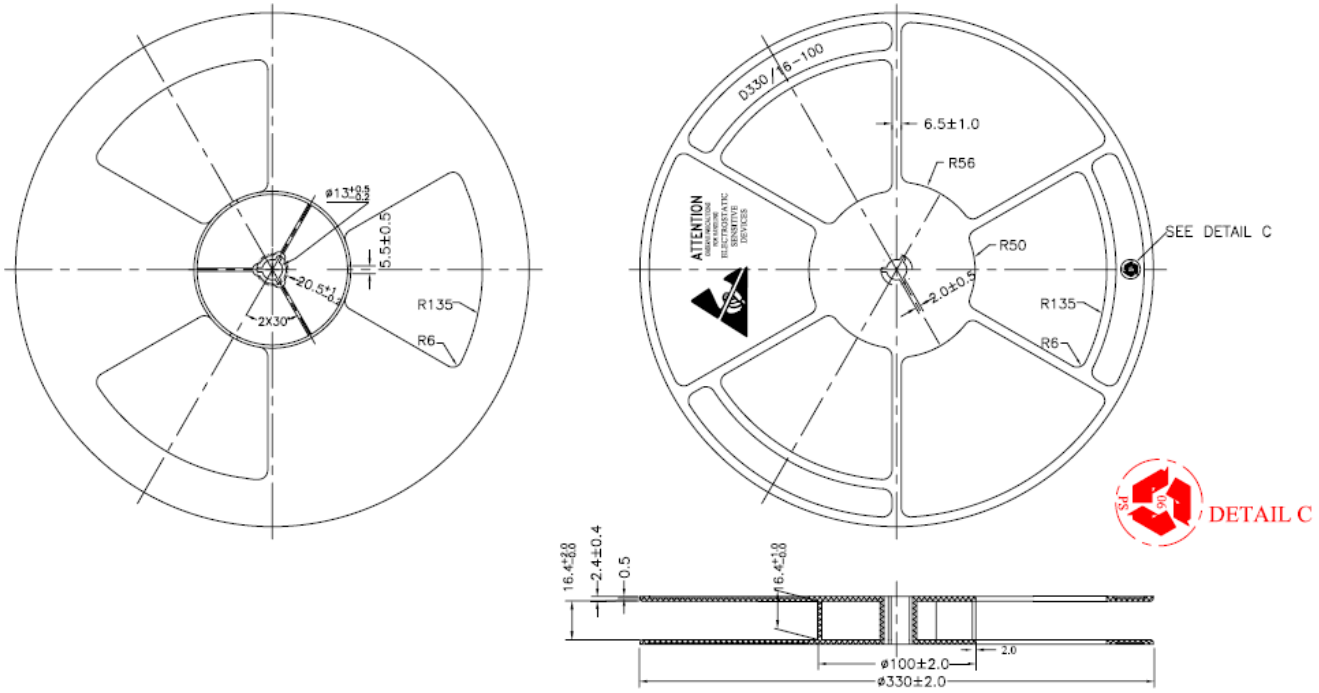


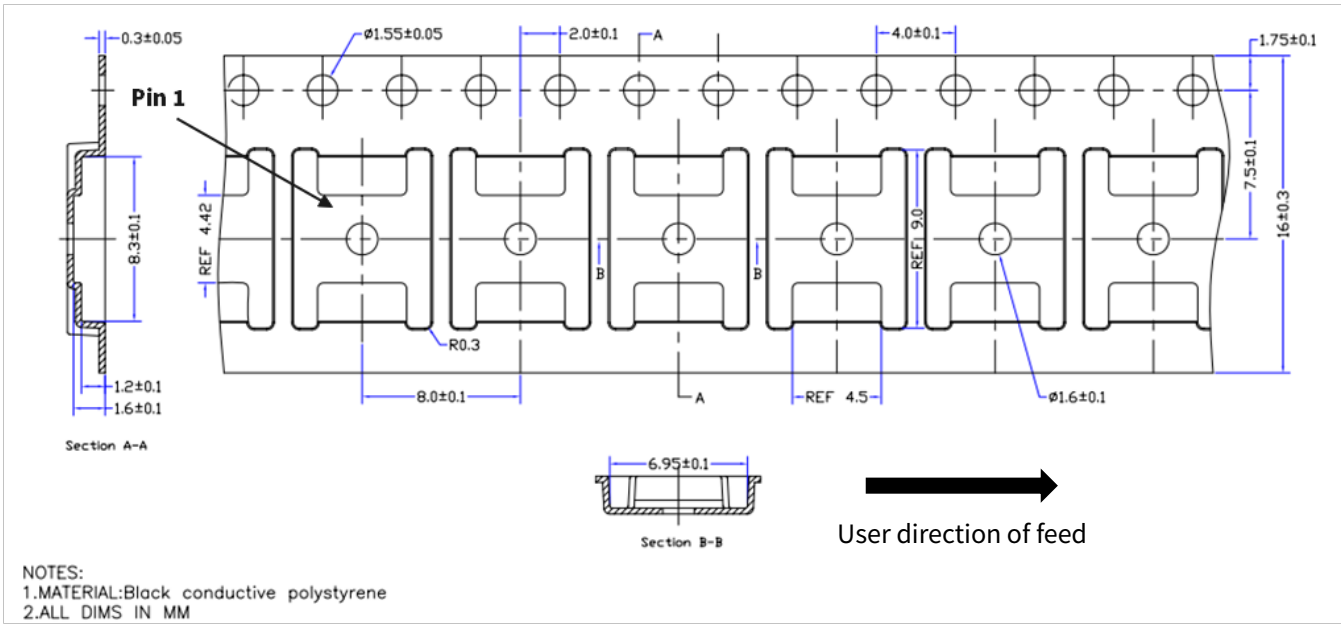
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.15
A1	0.05	–	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.20	–	0.29
b1	0.19	0.22	0.25
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	7.70	7.80	7.90
D1	4.40	4.60	4.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.65	2.85	3.05
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	12°	14°	16°
θ 3	12°	14°	16°

NOTES:
1.ALL DIMENSIONS REFER TO JEDEC STANDARD MO–153 ADT
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. 'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

11. Tape and Reel Information





12. Ordering Information

Part Number	Automotive / Industrial	Temperature	Package Type	MSL	SPQ
NSD7315H-Q1HTSXR	Automotive	-40 to 125℃	HTSSOP24	MSL3	4000
NSD7315S-Q1HTSXR	Automotive	-40 to 125℃	HTSSOP24	MSL3	4000
Note: All packages are RoHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.					

13. Revision History

Revision	Description	Date
1.0	Initial version	2025/5/13

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