NSD7310C
Brushed DC Motor Driver Single H-Bridge

Datasheet (EN) 1.0

NOVOSENSE

Product Overview

The device NSD7310C is a brushed-DC motor H-bridge driver for Industrial market including printer, appliance, robotics or other small machines application. With two inputs (IN1&IN2 and the 4x integrated N-channel MOSFETS, the device can control external motors bidirectionally with up to 3.8A peak current. The device also features sleep mode with low quiescent current when both IN1 and IN2 inputs are low.

The device is integrated with current chopping regulation, depends on VREF input and the voltage of IPROBE pin, which is proportional to the current output of the integrated current mirror of the current flowing through motor and IPROBE output resistor. The current chopping function limits the current during motor start-up or stall condition.

The device is also fully protected from faults including VM undervoltage, overcurrent (output short to battery or short to GND) and overtemperature. When fault condition is removed, the device automatically resumes normal operation.

Applications

- Printers
- Appliances
- Robots
- Industrial Equipment
- Electrical Lock
- Brushed-DC motor actuators

Device Information

Part Number	Package	Body Size
NSD7310C-DHSPR	HSOP8	4.90mm × 3.90mm

Key Features

- Single H-Bridge Motor Driver
- Wide 5V to 36V Operating Voltage
- Full path (HS + LS) RDS(ON) Typical 500mΩ
- 3.8A Peak Current Drive
- PWM Control Interface
- Integrated Current Chopping Regulation with Current Mirror Output
- Low Quiescent Sleep Mode
- Small Package and Footprint
- 8 Pin HSOP8 4.9mm X 3.9mm with exposed PAD
- Integrated Fault Protection Features
- – VM Undervoltage Protection (UV)
- – Overcurrent Protection (OCP)
- – Over Temperature Shutdown (TSD)
- – Fault with Automatically Recovery
- RoHS & REACH Compliance

Functional Block Diagrams

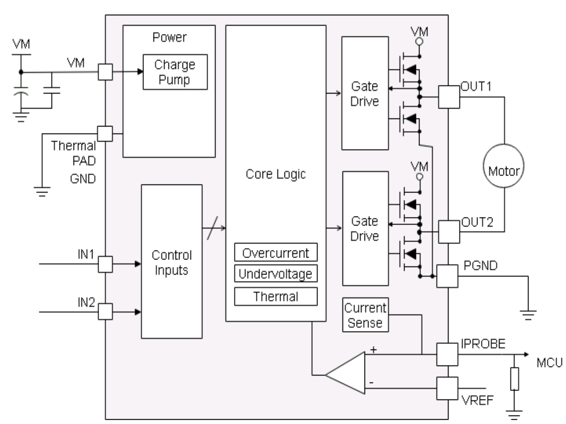

Figure 1. NSD7310C Block Diagram

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1. Pin Configuration and Functions

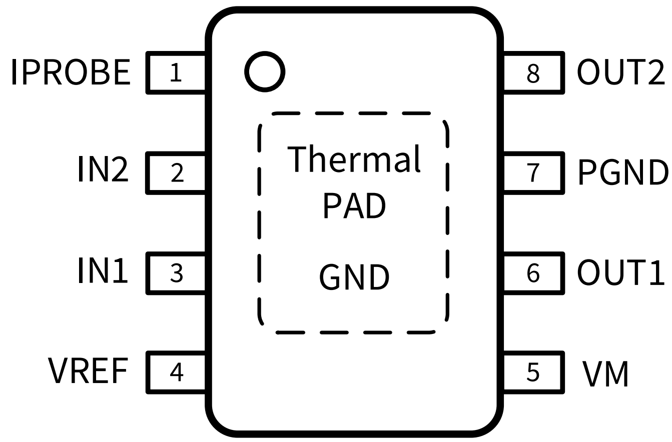


Figure 2. NSD7310C Pinout(TOP VIEW)

Table 1. NSD7310C Pin Configuration and Description

SYMBOL	No	TYPE	DESCRIPTION
IPROBE	1	O	Current feedback output pin, Put external resistor on this pin to ground. See application information section for resistor selection
IN1	3	I	Logic inputs. Controls the H-bridge output. Has internal pull downs.
IN2	2	I	Logic inputs. Controls the H-bridge output. Has internal pull downs.
PGND	7	PWR	High-current ground path. connect directly to board ground.
OUT1	6	O	H-bridge output1 pin. Connect directly to the motor or other inductive load.
OUT2	8	O	H-bridge output2 pin. Connect directly to the motor or other inductive load.
VM	5	PWR	5V to 38V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitor needs to guarantee VM pin voltage in maximum range. Put the 0.1μF and bulk capacitor close to the VM pin.
VREF	4	I	Analog input. Apply a voltage between 0.3 to 3.6 V.
Thermal PAD / GND	—		Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

2. Absolute Maximum Rating

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	40	V
Logic input voltage (IN1, IN2)	–0.3	6	V
VREF input pin (VREF)	–0.3	6	V

Continuous phase node pin voltage (OUT1, OUT2)	–0.7	VM + 0.7	V
Voltage difference between PGND and GND	-0.3	0.3	V
Current feedback output voltage (IPROBE)	–0.3	6	V

3. ESD Ratings

SYMBOL	DESCRIPTION	VALUE	UNIT
VESD	Human Body Model (HBM) (1), per ANSI/ESDA/JEDEC JS-001	±4000	V
	Charged device model (CDM) (1), per JEDEC specification JS-002	±750	V

(1) ± 4000v HBM and ± 750v CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 4000 V HBM & ± 750v CDM may actually have higher performance.

4. Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VM	VM Power supply voltage	5		36	V
VREF	VREF input voltage range	0.3		3.6	V
V_{IN1}, V_{IN2}	Logic input voltage (IN1, IN2)	0		5.5	V
fpwm	Logic input PWM frequency (IN1, IN2)	0		200	kHz
Imax	Max output current (2)	0		3.8	A

(2) When the maximum allowable output load current is considered during application scenario, both power dissipation and thermal condition, including ambient temperature, application board thermal condition etc., shall also be evaluated.

5. Thermal Information

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_a	Ambient operating ambient temperature	-40		125	°C
T_j	Junction temperature	-40		150	°C
T_{stg}	Storage temperature	-65		150	°C
R_{thjc}	Thermal resistance, junction to case		2.7		°C/W
R_{thja}	Thermal resistance, junction to ambient, on 2-layer PCB		62		°C/W
	Thermal resistance, junction to ambient, on 4-layer PCB based on JEDEC standard		35		°C/W

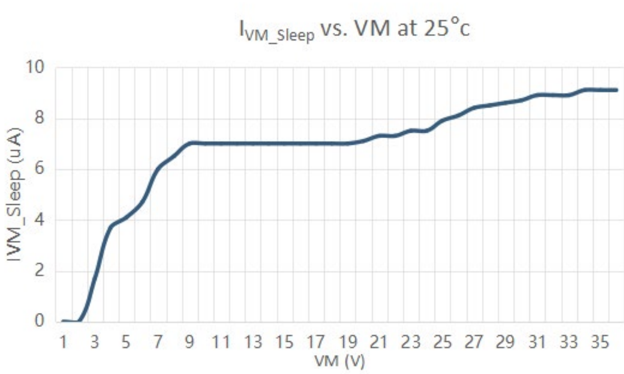
6. Electrical Characteristics

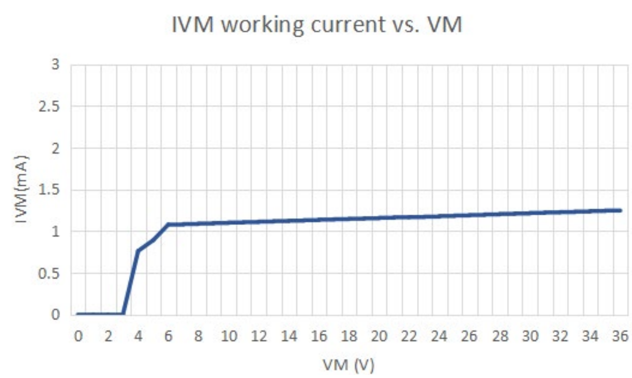
T_j = 25°C, VM=5 to 36V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
VM	VM operating voltage		5		36	V
I_{VM}	VM operating supply current	VM = 12 V		2	5	mA
$I_{VMSLEEP}$	VM sleep current	VM = 12 V		6	10	μA
t_{ON}	Turn-on time	VM > V_{UVLO} with IN1 or IN2 high		23	50	μs
Logic Control Input (IN1, IN2)						
V_{IL}	Input logic low voltage				0.5	V
V_{IH}	Input logic high voltage		1.8			V
V_{HYS}	Input logic hysteresis			0.5		V
I_{IL}	Input logic low current	VIN = 0 V	-1		1	μA
I_{IH}	Input logic high current	VIN = 3.3 V		33	100	μA
R_{PD}	Pulldown resistance	to GND		100		kΩ
t_{PD}	Propagation delay	INx to OUTx change		0.6	1	μs
t_{sleep}	Time to sleep	Inputs low to sleep		1	1.5	ms
H-BRIDGE OUTPUS (OUT1, OUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 12 V, I = 1 A, Ta= 25°c		265		mΩ
$R_{DS(ON)}$	Low-side FET on resistance	VM = 12 V, I = 1 A, Ta= 25°c		235		mΩ
t_{DEAD}	Output dead time			200		ns
V_d	Body diode forward voltage	IOUT = 1 A		0.8	1	V
CURRENT REGULATION						
A_{IPROBE}	Current mirror scaling factor			1.5		mA/A
A_{ERR}	Current mirror scaling error	IOUT < 0.1A	-7.5		7.5	mA
		0.1A ≤ IOUT ≤ 0.15A	7		7	%
		0.15A < IOUT < 0. 5A	-5		5	%
		0.5A ≤ IOUT ≤ 2A	-4		4	%
t_{OFF}	PWM off-time			27		μs
$t_{deglitch}$	regulation deglitch timing			0.8		μs
t_{BLANK}	PWM blanking time			2.5		μs

PROTECTION						
V_{UV}	VM undervoltage protection	VM falls until UV triggers	4.2	4.6		V
		VM rises until operation recovers		4.75	5	V
V_{UV_HYS}	VM undervoltage hysteresis			150		mV
t_{UV}	VM undervoltage deglitch time			10		μs
I_{OCP}	Overcurrent protection threshold		3.8	4.5	6.4	A
t_{OCP}	Overcurrent deglitch time			1.5		μs
t_{RETRY}	Overcurrent retry time			3		ms
T_{SD}	Thermal shutdown temperature		150	165	180	°C
T_{HYS}	Thermal shutdown hysteresis			20		°C

7. Typical Characteristics





8. Functional Description

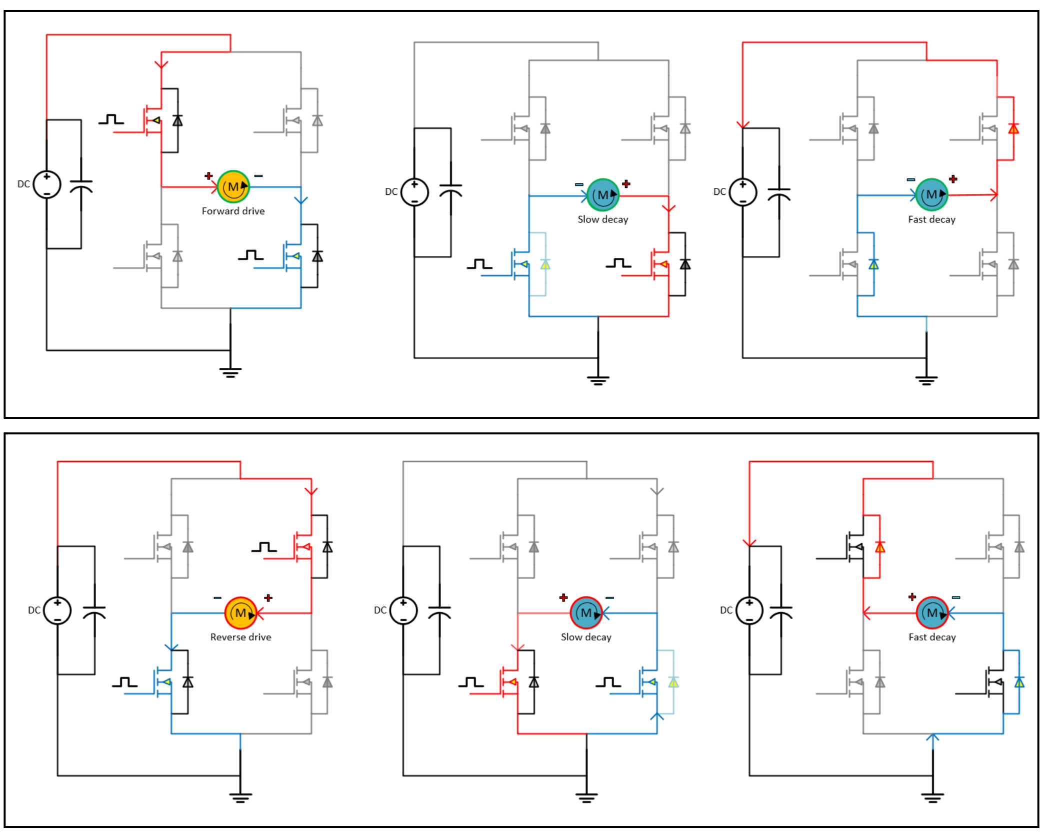
8.1. H-bridge operation

The NSD7310C contains two logic input pins IN1 and IN2, the two pins are internally pulled down and able to receive up to max 200kHz PWM signal, for controlling the internal integrated output stage to support motor operation in different states as below table 2.

Table 2. NSD7310C operation state description

IN1	IN2	V_{IPROBE}> V_{REF}	OUT1	OUT2	Description
1	0	False	HIGH	LOW	Normal driving, forward mode
0	1	False	LOW	HIGH	Normal driving, reverse mode
1	0	True	HIGH/LOW	LOW	Current regulation, forward
0	1	True	LOW	HIGH/LOW	Current regulation, reverse
1	1	x	LOW	LOW	Slow decay
0	0	x	HIZ	HIZ	Fast decay mode. Device move from fast decay to low power sleep mode after both IN1 and IN2 move to 0 for 1ms typ (t_{sleep})

Figure 2. High side/low side activation in forward/reverse/slow decay/fast decay



An internal dead-time t_{DEAD} is implemented between internal high side and low side switching to avoid cross conduction.

8.2. VREF, IPROBE pin and current regulation

The NSD7310C device integrates current sensing, feedback, and regulation functions with VREF pin and IPROBE pin. These features allow the device to sense the output current without external amplifier. The current regulation function allows for the device to limit the output current automatically in the case of motor stall or high load torque events and give detailed feedback to the controller about the output current through a current proportional output in IPROPI pin.

The IPROBE pin is the scaling output of load current measured by internal current mirror. The shunt-less monitoring technique senses the current flowing through low side drain to source, while the current from source to drain of that channel during slow decay or fast decay is considered as zero. For example, if the H-bridge is in forward / reverse / slow decay, the current output of IPROBE pin is proportional to the current in one of the low side MOSFET.

$$I_{IPROBE} = AIPROBE * (I_{LS1} + I_{LS2})$$

The corresponding IPROBE pin voltage can be calculated using I_{IPROBE} and external resistor R_{IPROBE} by

$$V_{IPROBE} = I_{IPROBE} * R_{IPROBE}$$

Together with the external VREF input, the current regulation level I_{TRIP} is set according to the external VREF input vs. VIPROBE.

$$I_{TRIP} = \frac{V_{REF}}{AIPROBE * R_{IPROBE}} = \frac{V_{REF}}{1.5mA/A * R_{IPROBE}(kohm)}$$

Note: VREF input voltage is recommended NOT higher than 3.6V.

The NSD7310C use fixed off-time current regulation. When the load current reaches the setting I_{TRIP}, the internal controller will automatically move the H-Bridge output to slow decay state by two internal low side MOSFET in ON state for fixed t_{OFF}. After t_{OFF} elapses, the H-bridge returns back to driving state according to IN1/IN2 pin states. Additionally, the trigger signal of I_{TRIP} will be ignored at the beginning of PWM transition and filtered after ITRIP exceeded; the two timings, t_{BLANK} and t_{DEG}, avoid false sense overload events due to motors or systems capacitance.

Note: The state change of INx can't interrupt the slow decay state of current regulation. (Figure 6)

Figure 3. Parameter schematic diagram of Current Regulation

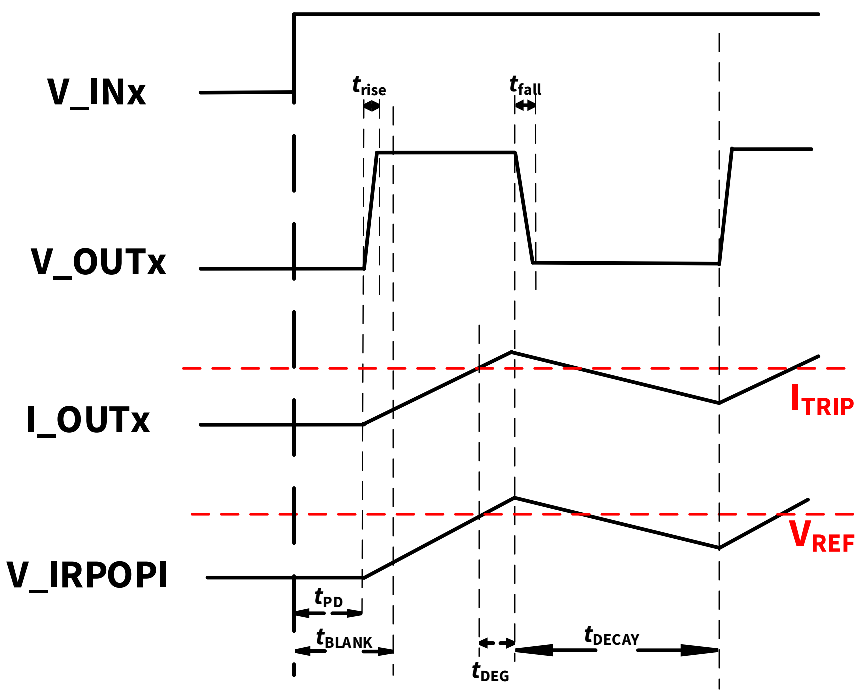
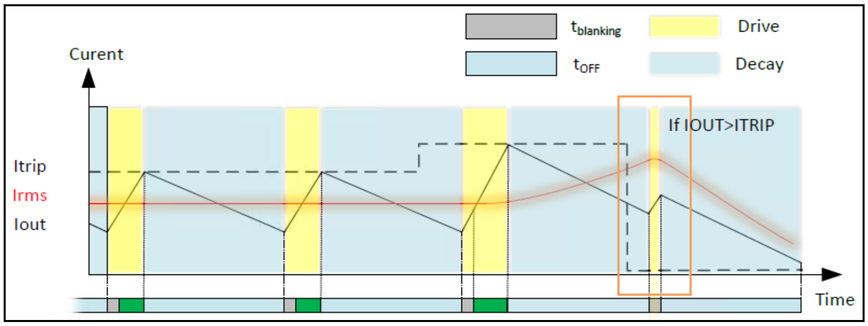


Figure 4. Current chopping regulation schemes



8.3. Low power sleep mode

Low power sleep mode in NSD7310C is active when both IN1 and IN2 keeps for low after 1ms (typ) t_{sleep}. It disables most internal circuits, including charge pump and control logic blocks etc., and reduces device current consumption.

When one of IN1 or IN2 pins state moves to high and remains at least 5μs, the device exits from low power sleep mode. After 23μs (typ) t_{ON} delay timing, OUT1 and OUT2 can be active in normal driving reverse / forward according to IN1 and IN2 inputs.

8.4. Protection function

8.4.1. VM undervoltage protection

When VM power supply pin voltage falls below the undervoltage low threshold (V_{UV}) over 10μs typ. undervoltage deglitch time, OUT1 and OUT2 becomes HIZ and internal power stage MOSFETs are disabled. When VM rise above the $V_{UV(HIGH)}$, the device automatically resumes normal operation according to IN1/IN2 pin status.

8.4.2. Overcurrent protection

The device integrates internal current monitor to against output load short, OUT1 / OUT2 pin short to battery or GND. If one of these faults happens and internal sensed current > OCP threshold I_{OCP} for longer than t_{OCP}, all H-bridge output MOSFET are disabled.

In the meantime, device provides overcurrent protection recovery function by auto-retry mechanism. After H-bridge output MOSFET disabled for the duration t_{RETRY}, it automatically re-enables and works according to the state of IN1/IN2 pins. While OCP fault is still present, the protection and auto retry repeats; otherwise, the device moves to normal operation state.

8.4.3. Overtemperature

If the device internal junction temperature over T_{SD} threshold, the internal MOSFET also automatically disabled. Normal operation will be resumed when internal junction temperature drops below T_{SD}-T_{HYS}

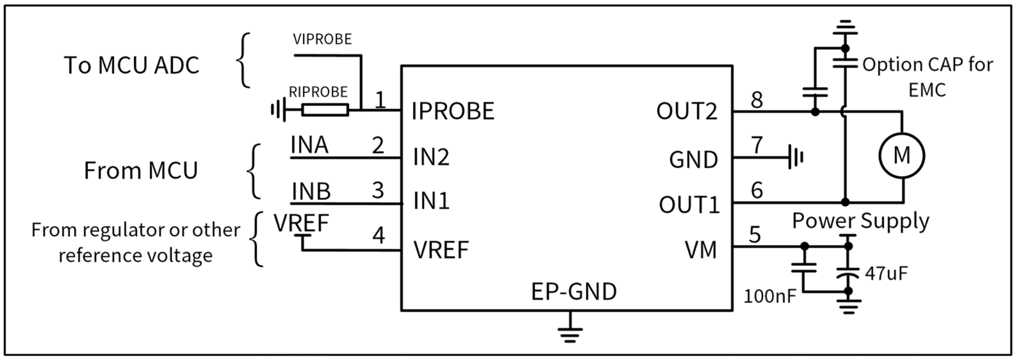
8.4.4. Fault Protection Summary

Fault	Condition	H-Bridge	Recovery procedure
VM undervoltage	VM < $V_{UV\ (LOW)}$	Disabled, HIZ	VM > $V_{UV\ (HIGH)}$
OCP	I > I_{OCP}	Disabled, HIZ	Auto-retry with t_{RETRY} interval
Over temperature	T_J > T_{SD}	Disabled, HIZ	T_J < T_{SD} - T_{HYS}

9. Application Information

9.1. Application diagram

Figure 5. Typical application connection



9.2. Application Curves

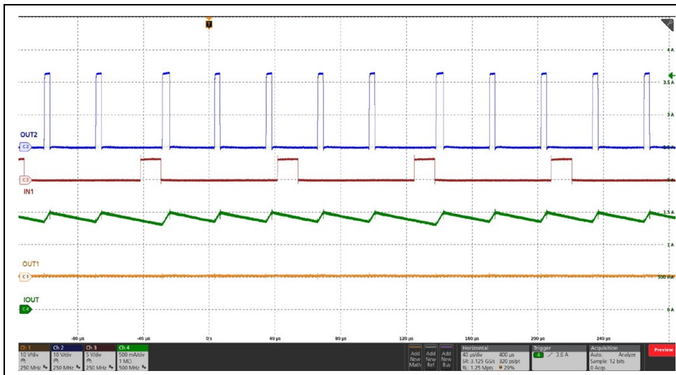


Figure 6. VM=24V; RL Load=1Ω+1mH; Vref=2.25V; R_{IPROPI}=1kΩ. IN2=3.3V; IN1=12kHz;

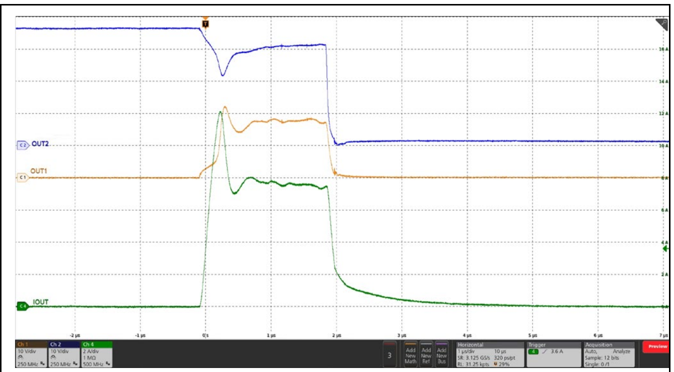


Figure 7. OCP with VM = 36V and Outputs shorted Together; IN2=3.3V; IN1=0V;

9.3. IPROBE pin and external Output resistor selection

An external resistor, R_{IPROBE}, should be put on IPROBE pin in order to generate the proportional voltage V_{IPROBE} with refer to load current. MCU can use ADC to measure the VIPROBE and monitor the load current.

Additional, NSD7310C integrates an internal clamp circuit which limits IPROBE pin max voltage up to VREF input plus one diode. In case of unexpected high load current or R_{IPROBE} loss, the clamp circuit protects both IPROBE pin and MCU ADC pin and easy the external application circuit.

Hence, the resistor value is suggested to be calculated based on AIPROBE scaling factor and maxim load current in the application.

$$R_{IPROBE} \leq \frac{V_{REF}}{A_{IPROBE} * I_{TRIP}}$$

For example, I_{TRIP} = 1.5A, VREF=2.5V and A_{IPROBE} = 1.5 mA/A, then RIPROBE should be chosen around 1.1 kohm / SMT 0603 or 0402 size.

9.4. Device power dissipation and continuous driving current

Total device power dissipation (P_{TOT}) is consisted of three parts: VM supply current and related dissipation (P_{VM}), H-bridge switching loss (P_{SW}) and H-bridge MOSFET ON static power dissipation (P_{ON}).

$$P_{TOT} = P_{VM} + P_{SW} + P_{ON}$$

$$P_{TOT} = VM * I_{VM} + I_{LOAD} * V_M * (t_{rise} + t_{fall}) * f_{PWM} + I_{LOAD}^2 * (R_{DS(ON)_{HS}} + R_{DS(ON)_{LS}})$$

If the input PWM frequency is used below 20kHz, the switching loss P_{SW} is insignificant comparing with P_{ON}, therefore, the power loss of NSD7310C under this condition can be quickly estimated by the formula

$$P_{TOT} \approx I_{RMS}^2 \times (R_{DS(ON)_{HS}} + R_{DS(ON)_{LS}})$$

The device junction temperature calculation is defined as $T_J = T_{amb} + (R_{thja} * P_{TOT})$, for continuous driving, the device internal temperature must be less than Tj max (150°c) for system operating.

9.5. Layout tips

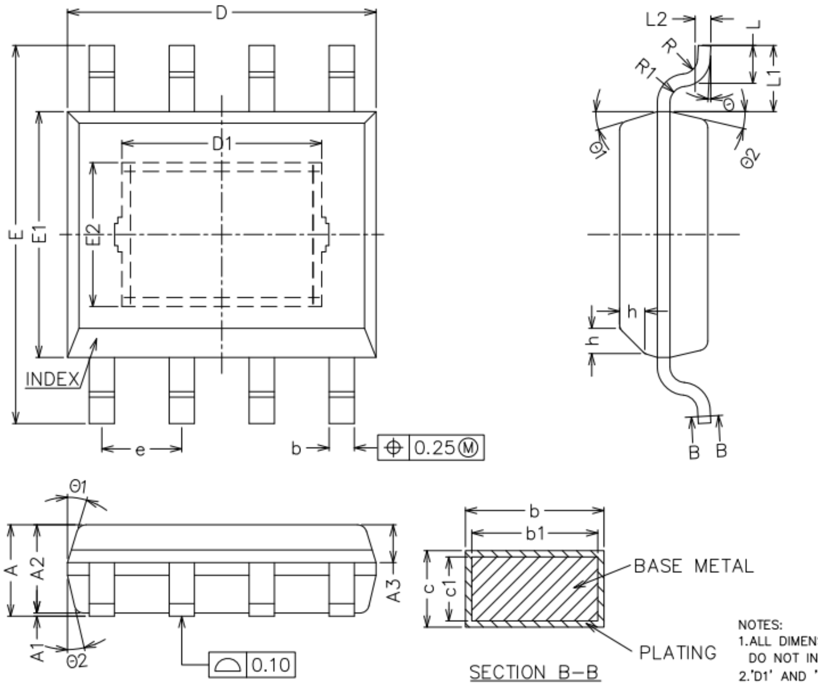
For optimized thermal performance, the NSD7310C exposed pad must be directly soldered to the PCB surface, also multiple vias should be used to transfer the heat to other PCB layers. In the meanwhile, the PCB is recommended to have higher copper coverage and thick ground plane.

For robust and reliable electrical usage, the power supply pin VM should be decoupled with a bulk capacitor (47µF or 100µF) and one low value ceramic capacitor (100nF typical). The placement of two capacitors suggests close to VM pin as much as possible.

The generic option capacitor value on OUT1 & OUT2 for EMC is 10nF. The most appropriated value shall be determined during system-level EMC testing. For layout, put the option EMC capacitor close to output connector is suggested.

10. Package Information

10.1. HSOP8 package information



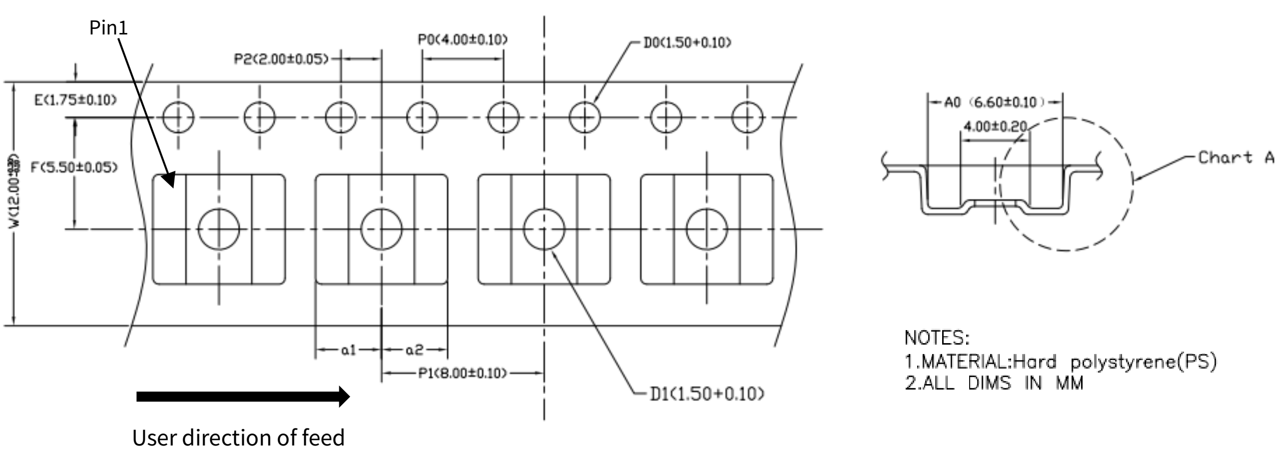
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

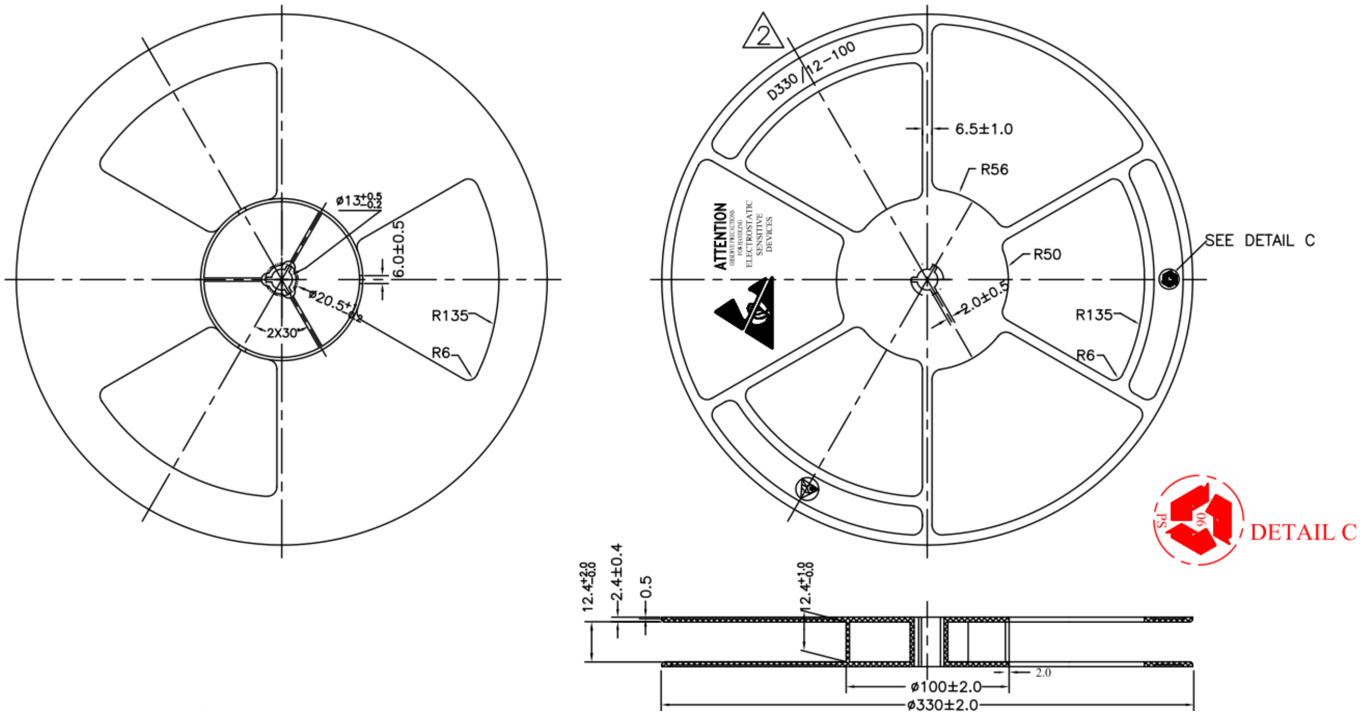
SYMBOL	MIN	NOM	MAX
A	1.35	1.45	1.65
A1	0	–	0.15
A2	1.35	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
D1	3.02	3.17	3.32
	1.98	2.13	2.28
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.13	2.28	2.43
	1.98	2.13	2.28
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
Θ	0°	–	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°

NOTES:
1.ALL DIMENSIONS REFER TO JEDEC STANDARD MS–012 BA DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2.'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

Note: Variation A, D1 (MIN 3.02, TYP 3.17, MAX 3.32) & E2 (MIN 2.13, TYP 2.28, MAX 2.43), is used.

10.2. HSOP8 packaging information





11. Ordering Information

Part Number	Automotive / Industrial	VREF / VTRIP	nFAULT	IPROBE	Package Type	MSL	SPQ
NSD7310C-DHSPR	Industrial	VREF input pin	NO	YES	HSOP8	MSL3	2500
Note: All packages are RoHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.							

12. Revision History

Revision	Description	Date
1.0	Initial version.	2025/9/22

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