NOVOSENSE

NSD56620-Q1
Eight channel Low-side and High-side switches
Datasheet (EN) 1.0

Product Overview

The NSD56620 is an eight channel Low-side and High-side switches, the output stages incorporate two high-side and six auto-configurable high-side or low-side switches, which is specially designed to control relays and LEDs in automotive and industrial applications.

The 16-bit serial peripheral interface (SPI) is utilized to control and diagnose the device and the loads. The SPI interface also provides daisy chain capability.

This device is able to keep its state at low battery voltage ($V_S \geq 4.5$ V).

The NSD56620 is equipped with two input pins that are connected to two outputs. With the Input Mapping it is possible to connect the input pins to different outputs, or assign more outputs to the same input pin. In this case more channels can be controlled with one signal applied to one input pin.

In Limp Home mode (Fail-Safe mode) the input pins are directly routed to channels 2 and 3.

The device provides diagnosis of the load via Open Load at ON state, Open Load at OFF state and short circuit detection. Temperature sensors are available for each channel to protect the device against Over Temperature.

Applications

- Relays
- LEDs and Bulbs
- Solenoids

Device Information

Part Number	Package	Body Size
NSD56620-Q1HTSBR	HTSOP24	8.65mm x 3.9mm

Key Features

- AEC Q-100 (Grade 1) Qualified for automotive: T_A from –40 °C to 125 °C
- 16-bit serial peripheral interface for control and diagnosis
- Daisy Chain capability SPI also compatible with 8-bit SPI devices
- 2 CMOS compatible parallel input pins with Input Mapping functionality
- Cranking capability down to V_S = 4.5 V
- Digital supply voltage range compatible with 3.3V and 5V micro-controllers
- Bulb Inrush Mode (BIM) to drive 2W lamps and electronic loads
- Very low quiescent current
- Limp Home mode
- RoHS & REACH Compliance

Protection and Diagnostic Features

- Short circuit to ground or battery protection
- Over Current latch OFF
- Thermal shutdown latches OFF
- Latched diagnostic information via SPI register
- Over Load detection at ON state
- Open Load detection at OFF state using Output Status Monitor function
- Output Status Monitor
- Input Status Monitor
- Open Load detection at ON state

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1. Pin Configuration and Functions

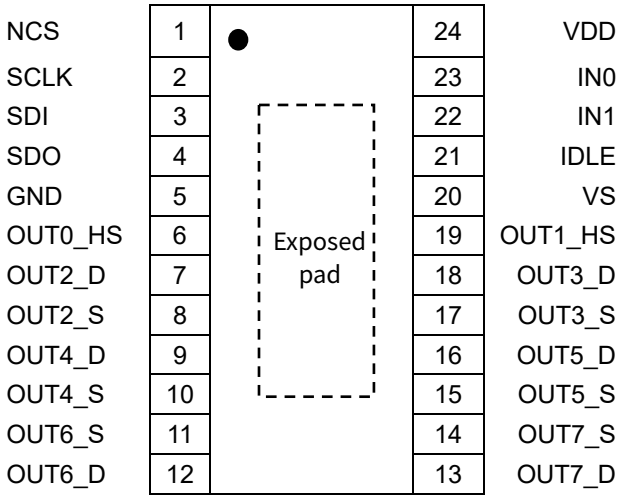


Figure 1.1 NSD56620 Package

Table 1.1 NSD56620 Pin Configuration and Description

NSD56620 Pin No.	Symbol	Type	Function
1	NCS	Input	Chip Select, "low" active, integrated pull-up to VDD
2	SCLK	Input	Serial Clock, "high" active, integrated pull-down to ground
3	SDI	Input	Serial Input, "high" active, integrated pull-down to ground
4	SDO	Output	Serial Output, "Z" (tri-state) when NCS is "high"
5	GND	Ground	Ground connection
6	OUT0_HS	Output	Source of high-side power transistor (channel 0)
7	OUT2_D	Output	Drain of auto configurable power transistor (channel 2)
8	OUT2_S	Output	Source of auto configurable power transistor (channel 2)
9	OUT4_D	Output	Drain of auto configurable power transistor (channel 4)
10	OUT4_S	Output	Source of auto configurable power transistor (channel 4)
11	OUT6_S	Output	Source of auto configurable power transistor (channel 6)
12	OUT6_D	Output	Drain of auto configurable power transistor (channel 6)
13	OUT7_D	Output	Drain of auto configurable power transistor (channel 7)
14	OUT7_S	Output	Source of auto configurable power transistor (channel 7)
15	OUT5_S	Output	Source of auto configurable power transistor (channel 5)
16	OUT5_D	Output	Drain of auto configurable power transistor (channel 5)
17	OUT3_S	Output	Source of auto configurable power transistor (channel 3)

18	OUT3_D	Output	Drain of auto configurable power transistor (channel 3)
19	OUT1_HS	Output	Source of high-side power transistor (channel 1)
20	VS	Power	Power supply VS for power switches gate control, protections and high side (channel 0 and channel 1)
21	IDLE	Input	Idle mode control, “high” activates Idle mode, integrated pull-down to ground
22	IN1	Input	Input pin 1, connected to channel 3 by default and in Limp Home mode, “high” active, integrated pull-down to ground
23	IN0	Input	Input pin 0, connected to channel 2 by default and in Limp Home mode, “high” active, integrated pull-down to ground
24	VDD	Power	Digital supply VDD, supply voltage for SPI with support function to VS
	Exposed pad	Ground	It is recommended to connect it to PCB ground for cooling and EMC - not usable as electrical GND pin. Electrical ground must be provided by pins 5.

2. Block Diagram

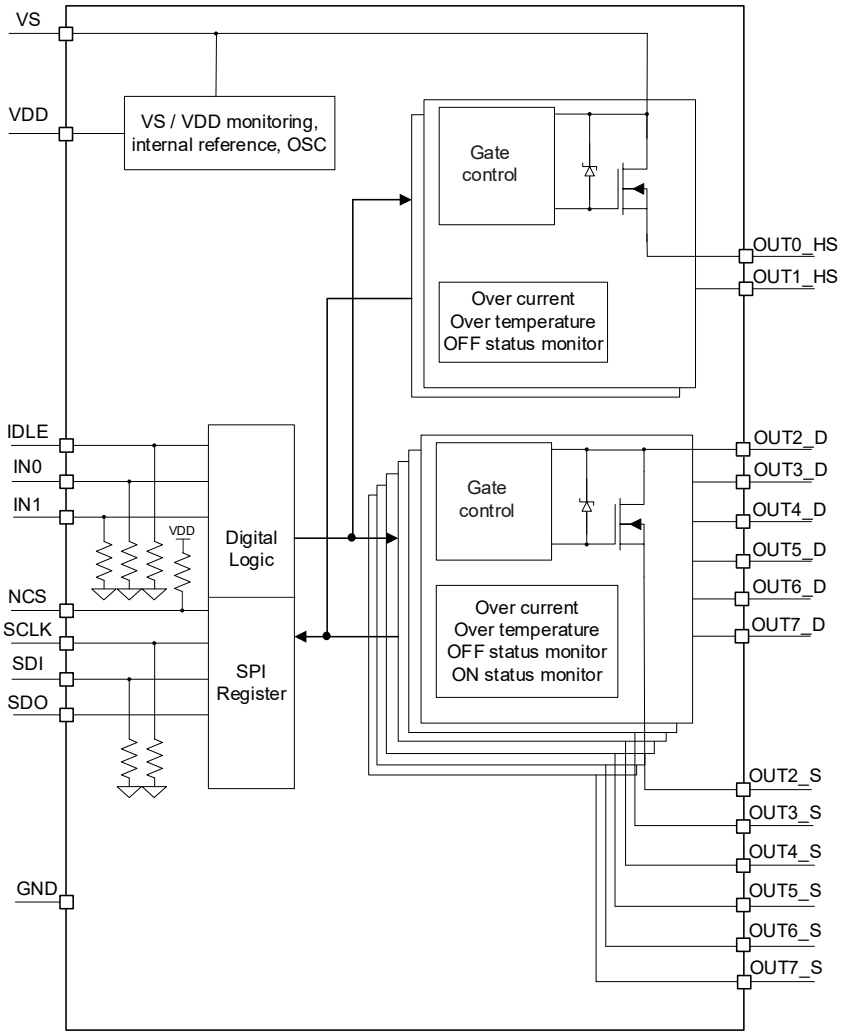


Figure 2.1 Block Diagram of NSD56620

3. Application Information

Note1: Recommended components may depend on the requirements at system levels and shall be confirmed by specific tests on the final application.

Note2: There is no reverse polarity protection function in VS pin and OUTn_D pins of auto configuration as HSD. A reverse protection diode or ideal diode must be added before VS pin and OUTn_D pins of auto configuration as HSD.

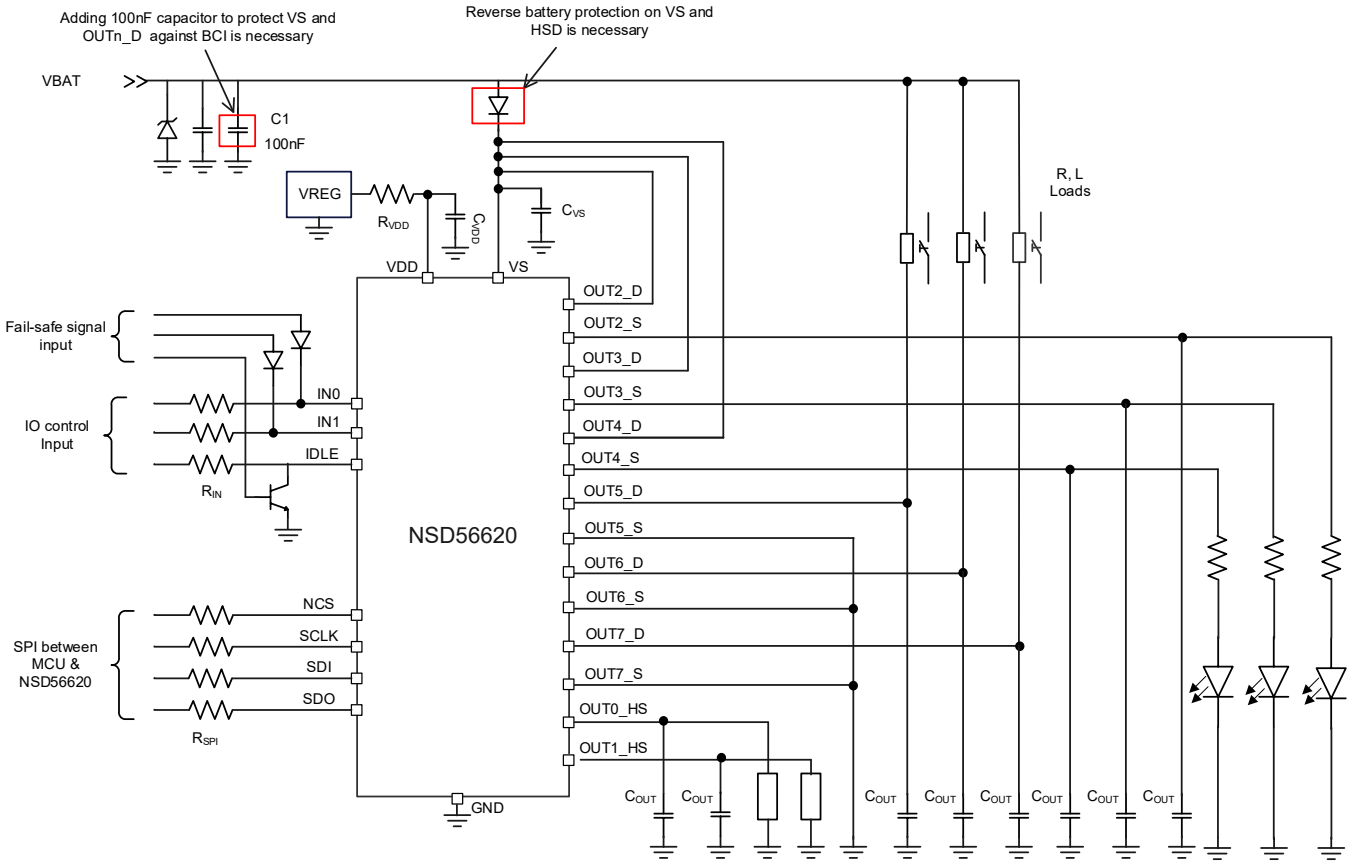


Figure 3.1 NSD56620 Application Diagram

Table 3.1 Suggested Component values

Reference	Value	Purpose
R_{IN}	4.7 kΩ	Protection of the micro-controller during Over Voltage and Reverse Polarity Guarantee NSD56620 channels OFF during Loss of Ground
R_{SPI}	500 Ω	Protection of the micro-controller during Over Voltage and Reverse Polarity
R_{VDD}	100 Ω	Logic supply voltage spikes filtering
C_{VDD}	100 nF	Logic supply voltage spikes filtering
C_{VS}	68 nF	Analog supply voltage spikes filtering
TVS	P6SMB30	Transient voltage suppressor
C_{OUT}	22 nF	Protection of NSD56620 against ESD and BCI
C_1	100 nF	Protection of VS and OUTn_D against BCI

Note: When f_{SCLK} ≥ 2MHz or VDD=3.3V, resistor in SPI line is suggested 100R, and MCU I/O is suggested to set in strong mode.

4. General Product Characteristics

Table 4.1 Product summary

PARAMETER	SYMBOL	VALUES
Analog supply voltage	V_S	4.5 V … 28 V
Digital supply voltage	V_{DD}	3.0 V … 5.5 V
Typical on-state resistance at T_J = 25 °C	$R_{DS(ON)}$	1 Ω
Nominal load current (T_A = 85 °C, all channels)	$I_{L(NOM)}$	330 mA
Maximum Energy dissipation - repetitive	E_{AR}	10 mJ @ $I_{L(EAR)}$ = 220 mA
Minimum Drain to Source clamping voltage	$V_{DS(CL)}$	39 V
Minimum overload switches OFF threshold	$I_{L(OVL1)}$	500 mA
Typical VS quiescent current at T_J ≤ 85 °C	I_{SLEEP}	1 µA
Maximum SPI clock frequency	f_{SCLK}	5 MHz

4.1. Absolute Maximum Ratings

T_J = -40 °C to +150 °C, all voltages with respect to ground.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog Supply voltage	V_S	-0.3		28	V
Digital Supply voltage	V_{DD}	-0.3		5.5	V
Supply voltage for load dump protection	$V_{S(LD)}$			39	V
Voltage at power transistor	V_{DS}	-0.3		39	V
Voltage at IDLE pin	V_{IDLE}	-0.3		5.5	V
Voltage at input pins	V_{IN}	-0.3		5.5	V
Voltage at chip select pin	V_{NCS}	-0.3		5.5	V
Voltage at serial clock pin	V_{SCLK}	-0.3		5.5	V
Voltage at serial input pin	V_{SDI}	-0.3		5.5	V
Voltage at serial output pin SDO	V_{SDO}	-0.3		V_{DD}+0.3	V
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C

4.2. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	±750	V

4.3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	7		18	V
Upper Supply Voltage Range for Extended Operation 1)	$V_{S\ (EXT,\ UP)}$	18		28	V
Lower Supply Voltage Range for Extended Operation 1)	$V_{S\ (EXT,\ LOW)}$	4.5		7	V
Junction Temperature	T_J	-40		150	°C
Logic supply voltage	V_{DD}	3		5.5	V

1) Parameter deviation possible

4.4. Thermal Information

Parameters	Symbol	HTSOP24	Unit
Junction-to-ambient thermal resistance 1)	θ_{JA}	28.4	°C/W
Junction-to-case(bottom) thermal resistance 1)	$\theta_{JC\ (bottom)}$	3.6	°C/W
Junction-to-top characterization parameter 1)	ψ_{JT}	2.1	°C/W

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four-layer board.

1) Not subject to production test, specified by design

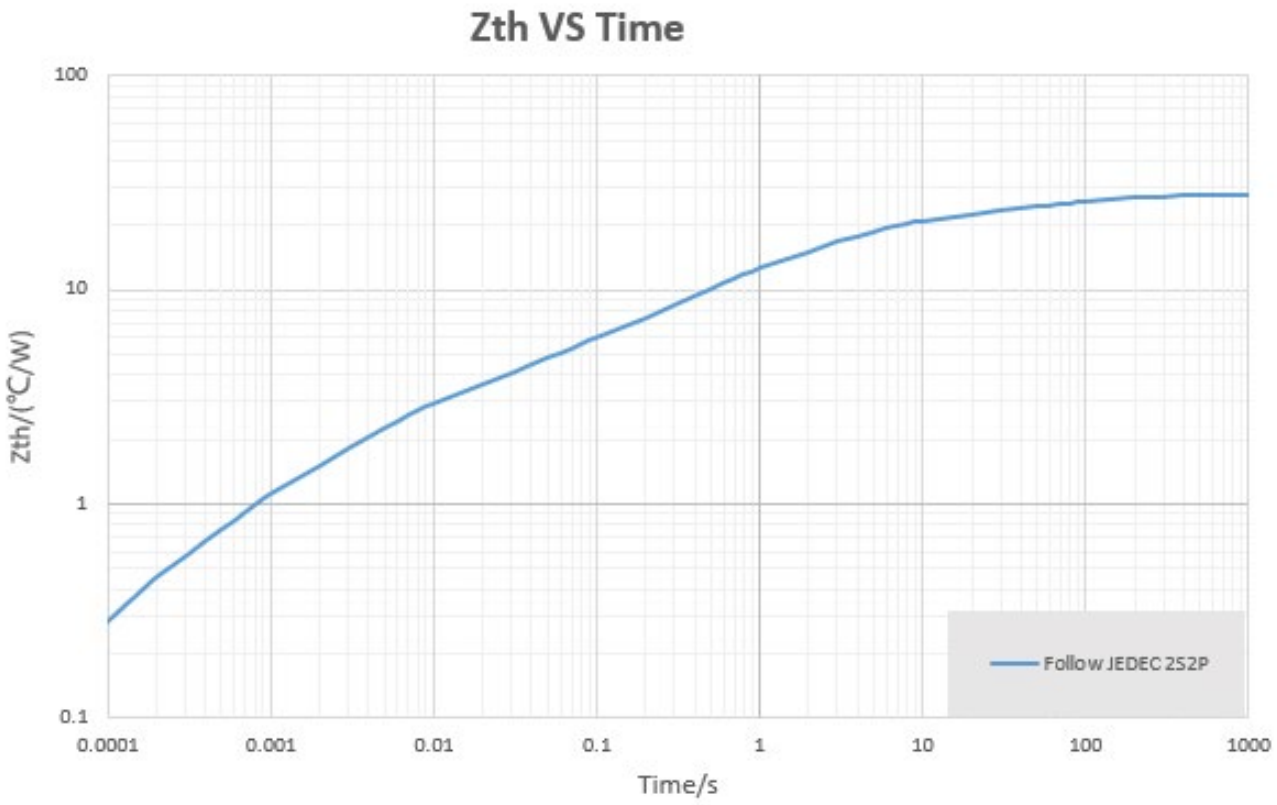


Figure 4.1 Typical Thermal Impedance

5. Power supply

The device is fed by two supply voltages:

• V_S (analog supply voltage used also for the logic)

• V_{DD} (digital supply voltage)

The VS supply line is connected to a battery feed, and outputs Vreg by LDO. Vreg is used, in combination with VDD supply, for the driving circuitry of the power stages. An increased current consumption may be observed at VDD pin when Vreg voltage drops below VDD voltage (for instance during cranking events down to 4.5 V),

VS and VDD supply voltages have an undervoltage detection circuit. Function of the UV circuit is shown in **Table 5.1.**

Figure 5.1 shows a basic interaction between supply pins VS and VDD, the output stage drivers and SDO supply line.

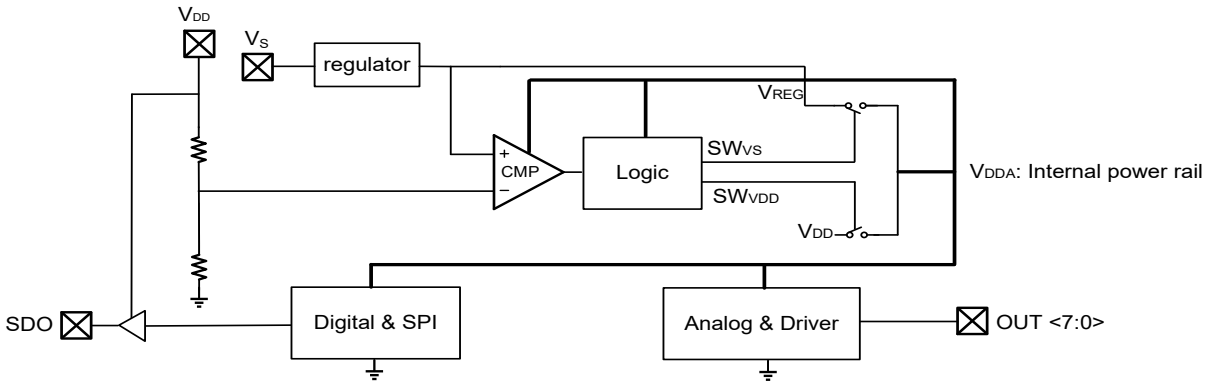


Figure 5.1 NSD56620 Internal Power Supply concept

An overview of channel behavior according to different VS and VDD supply voltages is shown in **Table 5.1** (the table is valid after a successful power-up, see Chapter 5.1.1 for more details).

Table 5.1 Device capability as function of V_S and V_{DD}

	V_{DD} < 3V	**V_{DD} ≥ 3V**
$V_S < V_{S(UV)}$	channels cannot be controlled	channels cannot be controlled
	SPI registers reset	SPI registers available
	SPI communication not available	SPI communication possible (f_{SCLK} = 5 MHz)
	Limp Home mode not available	Limp Home mode not available
$V_S \geq V_{S(UV)}$	channels cannot be controlled by SPI	channels can be switched ON and OFF (SPI control) ($R_{DS(ON)}$ deviations possible)
	SPI registers reset	SPI register available
	SPI communication not available	SPI communication possible (f_{SCLK} = 5 MHz)
	Limp Home mode available ($R_{DS(ON)}$ deviations possible)	Limp Home mode available ($R_{DS(ON)}$ deviations possible)

5.1. Operation Modes

NSD56620 has the following four operation modes: Sleep mode, Idle mode, Active mode and Limp Home mode.

The transition between operation modes is determined according to following levels and states:

• IDLE pin logic level

• INn pins logic level

• **OUT.OUTn** bits state

• **HWCR.ACT** bit state

• **HWCR_PWM.PWM0** and **HWCR_PWM.PWM1** bits state

The operation mode of the NSD56620 can be observed by:

• status of output channels

• status of SPI registers

• current consumption at VDD pin (I_{VDD}) and VS pin (I_{VS})

The state diagram including the possible transitions is shown in **Figure 5.2**

The default operation mode for switching on loads is Active mode. Output turn-on time t_{ON} will be extended due to the mode transition latency.

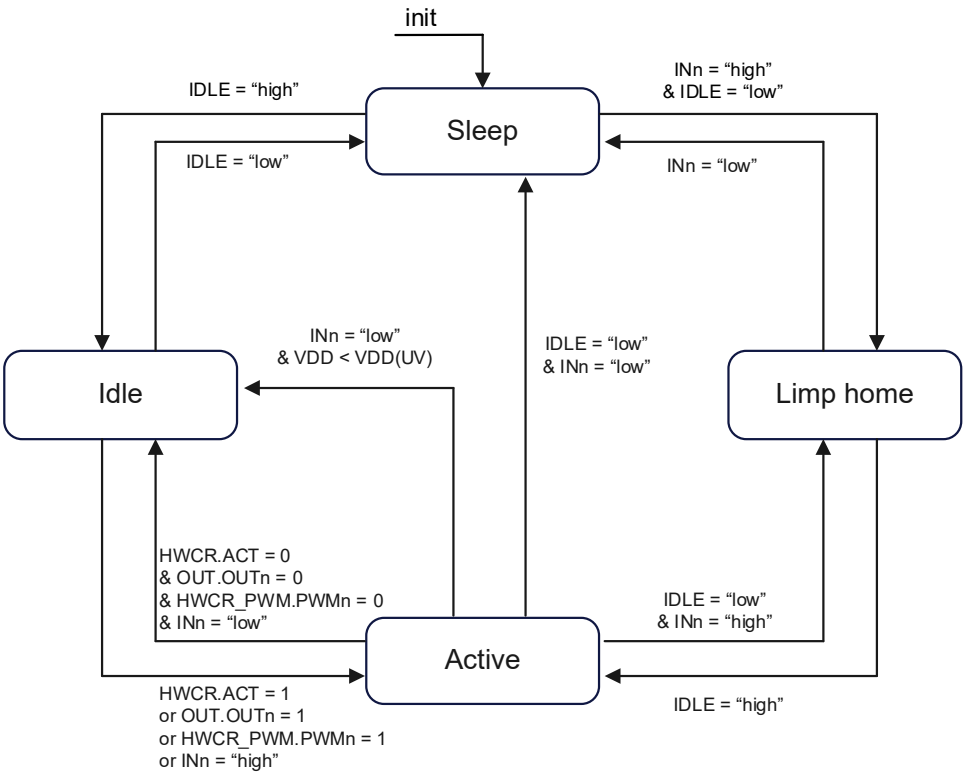


Figure 5.2 Operation Mode state diagram

Table 5.2 shows the correlation between device operation modes, V_S and V_{DD} supply voltages, and state of the important functions (channels operativity, SPI communication and SPI registers).

Table 5.2 Device function in relation to operation modes, V_S and V_{DD} voltages

Operation Mode	Function	Undervoltage condition on V_S V_{DD} < 3V	Undervoltage condition on V_S V_{DD} ≥3V	V_S not in undervoltage V_{DD} < 3V	V_S not in undervoltage V_{DD} ≥3V
Sleep	Channels	not available	not available	not available	not available
	SPI comm.	not available	not available	not available	not available
	SPI registers	reset	reset	reset	reset
Idle	Channels	not available	not available	not available	not available
	SPI comm.	not available	√	not available	√
	SPI registers	reset	√	reset	√
Active	Channels	not available	not available	√ (IN pins only)	√
	SPI comm.	not available	√	not available	√
	SPI registers	reset	√	reset	√
Limp Home	Channels	not available	not available [1)]	√ (IN pins only)	√ (IN pins only)
	SPI comm.	not available	√ (read-only)	not available	√ (read-only)
	SPI registers	reset	√ (read-only)	reset	√ (read-only)

1) IN limp home mode, when VS under voltage detected, the channel will shut off

5.1.1. Power-up

The IC performs Power-up procedure when one of the supply voltages (V_S or V_{DD}) is applied to the device and the INn or IDLE pins are set to “high”.

5.1.2. Sleep mode

In sleep mode, the outputs of the device are OFF and the SPI registers are reset to default values. The current consumption is minimum.

5.1.3. Idle mode

The current consumption of the device can reach the parameter IIDLE in Idle mode. The internal voltage regulator is still working. Diagnosis functions are not available. The output channels are disabled. The SPI registers are working and SPI communication is possible when VDD is available. **ERRn** bits are not cleared for functional safety reasons in Idle mode.

5.1.4. Active mode

Device current consumption is specified with I_{ACTIVE}. When IDLE pin is set to “high” and one of the input pins is set to “high” or one **OUT.OUTn** bit is set to “1” or one **HWCR_PWM.PWMn** bit is set to “1”, the device enters Active mode. The device returns to Idle mode as soon as all inputs pins are set to “low” , OUT.OUTn bits are set to “0” , **HWCR_PWM.PWMn** bits are set to “0” and **HWCR.ACT** is set to “0”. If all input pins are set to “low”, an undervoltage condition on VDD supply brings the device into Idle mode.

5.1.5. Limp Home mode

When IDLE pin is “low” and one of the input pins is set to “high”, the device is brought into Limp Home mode switching ON the channel connected to it. All other channels are OFF.SPI registers can be read but cannot be written. More in detail:

- **VSUV** and **LOPVDD** are set to “1”
- **OLON** and **OLOFF** bits are set to “0”
- **ERRn** bits work normally
- **DIAG_OSM.OUTn** bits can be read and work normally
- MODE bits are set to “01_B” (Limp Home mode)
- **TER** bit is set to “1” on the first SPI command after entering Limp Home mode. Afterwards it works normally
- When the device is in Limp Home mode, all other registers are set to their default value and cannot be programmed.

5.1.6. Power supply modes transition

When the device is in Active mode or in Limp Home mode the channel turn-on time is as defined by parameter t_{ON}. In all other cases, it is necessary to add the transition time required to reach Active mode or Limp Home mode (as shown in **Figure 5.3**).

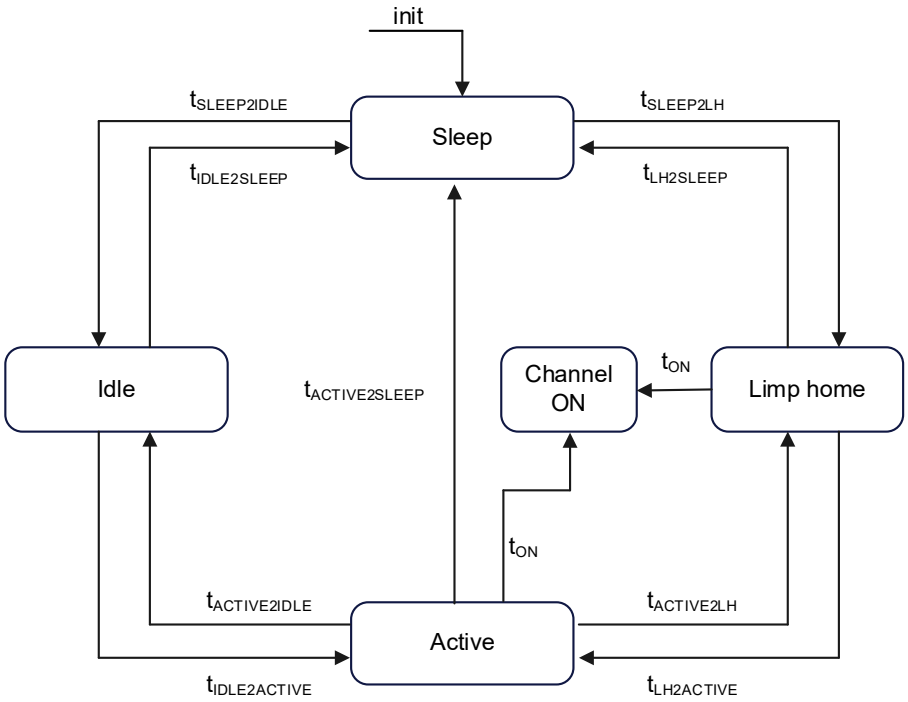


Figure 5.3 Transition Time diagram

5.2. Reset condition

The following 3 conditions reset the SPI registers to the default value:

• VDD is not present or below the undervoltage threshold V_{DDUV}

• IDLE pin is set to “low” (in limp home mode, see Chapter 5.1.5 for more details).

• A reset command (**HWCR.RST** set to “1”) is executed

- **ERRn** bits are not cleared by a reset command (for functional safety)

- **VSUV** and **LOPVDD** bits are cleared by a reset command

If there are no input pin set to “high”, all channels are switched OFF. And the Input Mapping configuration is reset.

5.2.1. Undervoltage on VS

Undervoltage behavior is shown in **Figure 5.4**

Between $V_{S(UV)\_FALL}$ and $V_{S(UV)\_RISE}$ the undervoltage mechanism is triggered. the logic will set the bit **VSUV** to “1” if the device is operative and the supply voltage drops below the undervoltage threshold $V_{S(UV)\_FALL}$. The bit **VSUV** is set to “0” after the first Standard Diagnosis readout as soon as the supply voltage VS is above the minimum voltage operative threshold $V_{S(UV)\_RISE}$.

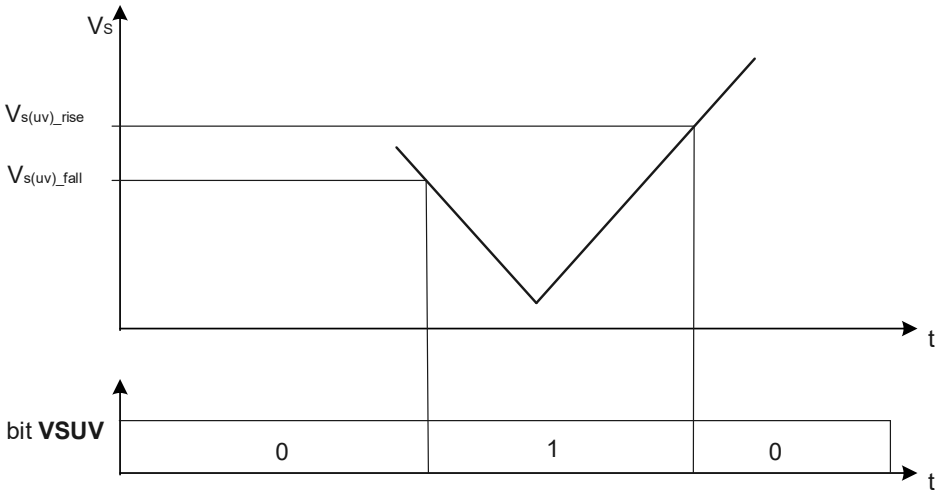


Figure 5.4 VS Undervoltage Behavior

5.2.2. Low operating power on VDD

In VDD rise condition, when $V_{DD} \le V_{DD(LOP)\_RISE}$, the bit **LOPVDD** remains "1", As soon as $V_{DD} > V_{DD(LOP)\_RISE}$ the bit **LOPVDD** is set to "0" after the first Standard Diagnosis readout.

In VDD fall condition, when $V_{DD} > V_{DD(LOP)\_FALL}$, the bit **LOPVDD** remains "0", As soon as $V_{DD} \le V_{DD(LOP)\_FALL}$ the bit **LOPVDD** is set to "1" after the first Standard Diagnosis readout.

5.3. Electrical Characteristics Power Supply

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground.
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VS pin						
$V_{S(UV)\_FALL}$	Analog supply undervoltage shutdown falling	VM falls until **VSUV** triggers	3.6	4	4.3	V
$V_{S(UV)\_RISE}$	Analog supply minimum operative voltage rising	VM rises until operation recovers	4	4.5	4.9	V
$V_{S(HYS)}$	Undervoltage shutdown hysteresis			0.5		V
$I_{VS(SLEEP)}$	Analog supply current consumption in Sleep mode with loads	V_{DD}=V_{NCS}=0V		1	20	μA
VDD pin						
$V_{DD(OP)}$	Logic Supply Operating voltage	f_{SCLK} = 5 MHz	3.0		5.5	V
V_{DDUV_FALL}	Logic supply undervoltage shutdown falling	V_{SDI} = V_{SCLK} = V_{NCS} = 0 V SDO from "low" to "high" impedance	2.5	2.7	2.85	V
V_{DDUV_RISE}	Logic supply minimum operative voltage rising	V_{SDI} = V_{SCLK} = V_{NCS} = 0 V SDO from "high" to "low" impedance	2.6	2.8	2.95	V

V_{DDUV_HYS}	VDD Undervoltage shutdown hysteresis			0.1		V
$V_{DD(LOP)}$	Logic Supply Lower Operating Voltage		3.0		4.5	V
$V_{DD(LOP)\_FALL}$	Logic Supply Lower Operating Voltage falling	**VDDLOP** from “0” to “1”		4		V
$V_{DD(LOP)\_RISE}$	Logic Supply Lower Operating Voltage rising	**VDDLOP** from “1” to “0”		4.2		V
$I_{VDD(SLEEP)}$	Logic supply current in Sleep mode	V_{NCS} =V_{DD}		0.1	10	µA
Overall current consumption						
I_{SLEEP}	Overall current consumption in Sleep mode $I_{VS(SLEEP)}$ +$I_{VDD(SLEEP)}$	V_{NCS} =V_{DD}			30	µA
I_{IDLE}	Overall current consumption in Idle mode $I_{VS(IDLE)}$ +$I_{VDD(IDLE)}$	f_{SCLK} = 0 MHz, **IOL.OUTn** = 0_B V_{NCS} =V_{DD}			2.5	mA
I_{ACTIVE}	Overall current consumption in Active mode $I_{VS(ACTIVE)}$ +$I_{VDD(ACTIVE)}$	f_{SCLK} = 0 MHz, **IOL.OUTn** = 0_B V_{NCS} =V_{DD}			4.5	mA
V_{SDIFF}	Voltage difference between, V_S and V_{DD} supply lines			100		mV
Timings						
$t_{SLEEP2IDLE}$	Sleep to Idle delay [1]	from IDLE pin to **TER** + **ISM** register = 8680_H		280	400	µs
$t_{IDLE2SLEEP}$	Idle to Sleep delay [1]	from IDLE pin to Standard Diagnosis = 0000_H, external pull-down SDO to GND required		100	200	µs
$t_{IDLE2ACTIVE}$	Idle to Active delay [1]	from INn or NCS pins to MODE = 10_B		100	200	µs
$t_{ACTIVE2IDLE}$	Active to Idle delay [1]	from INn or NCS pins to MODE = 11_B		50	200	µs
$t_{SLEEP2LH}$	Sleep to Limp Home delay [1]	from INn pins to V_{DS} = 10% V_S		400+t_{ON}	600+t_{ON}	µs
$t_{LH2SLEEP}$	Limp Home to Sleep delay [1]	from INn pins to Standard Diagnosis = 0000_H, External pull-down SDO to GND required		100+t_{OFF}	400+t_{OFF}	µs
$t_{LH2ACTIVE}$	Limp Home to Active delay [1]	from IDLE pin to MODE = 10_B		50	100	µs
$t_{ACTIVE2LH}$	Active to Limp Home delay [1]	from IDLE pin to TER + ISM register = 8683_H (IN0 = IN1 = “high”) or 8682_H (IN1 = “high”, IN0 = “low”)		50	100	µs

		or 8681_H (IN1 = “low”, IN0 = “high”)				
$t_{ACTIVE2SLEEP}$	Active to Sleep delay[1)]	from IDLE pin to Standard Diagnosis = 0000_H, External pull-down SDO to GND required		80	100	µs

1) Not subject to production test - specified by design

6. Control Pins

The device has three pins (IN0, IN1 and IDLE) to directly control the device operation without using SPI.

6.1. Input pins (IN0, IN1)

The device has two input pins IN0 & IN1. Each input pin is connected to one channel in default (IN0 to channel 2, IN1 to channel 3). In idle & active mode, input mapping registers **MAP_IN0** and **MAP_IN1** can be programmed to connect other channels to the corresponding input pin, as shown in **Figure 6.1**. The signals to drive the channels are generated by an OR combination between OUT control registers, IN0 and IN1.

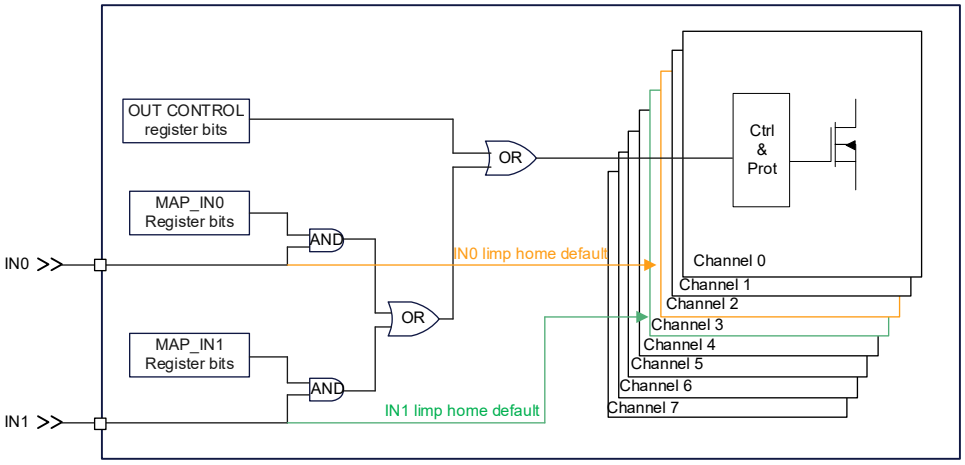


Figure 6.1 Input Mapping

The logic level of the input pins can be monitored via the Input Status Monitor Register (**ISM**). The input status monitor register is also operative and available for SPI read when NSD56620 is in Limp Home mode.

6.2. IDLE pin

The IDLE pin is used to bring the device into Sleep mode or Limp Home mode, depends on the logic combination of IDLE and INx pins. See Chapter 5.1 Operation Modes for further details

To ensure a proper mode transition, IDLE pin must be set for at least $t_{IDLE2SLEEP}$ (IDLE pin transition from “high” to “low”) or $t_{SLEEP2IDLE}$ (IDLE pin transition from “low” to “high”).

After setting the IDLE pin to “low”, the following behavior are as below:

- All registers in the SPI are reset to default values.
- If both inputs IN0 & IN1 are also set to “low”, then:

  V_{DD} and V_S Undervoltage detection circuits are disabled to decrease current consumption.

  SPI communication is not available, SDO pin remains in high impedance state.

6.3. Electrical Characteristics Control Pins

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDLE pin						
$V_{IDLE(L)}$	Low input level		0		0.8	V
$V_{IDLE(H)}$	High input level		2.0		5.5	V
$I_{IDLE(L)}$	Low input current	V_{IDLE} = 0.8 V	5	12	20	μA
$I_{IDLE(H)}$	High input current	V_{IDLE} = 2.0 V	14	28	45	μA
R_{IDLE}	Idle pin input pull-down resistor		50	70	150	kΩ
Input Pins (IN0 & IN1)						
$V_{IN(L)}$	L-input level		0		0.8	V
$V_{IN(H)}$	H-input level		2.0		5.5	V
$I_{IN(L)}$	Low input current	V_{IDLE} = 0.8 V	5	12	20	μA
$I_{IN(H)}$	High input current	V_{IDLE} = 2.0 V	14	28	45	μA

7. Operating Modes

The device is an eight channels low-side and high-side relay switch. The power stages are built by N-channel lateral power MOSFET.

There are six auto-configurable channels which can be used either as low-side or as high-side switches. A charge pump is connected to the output MOSFET gate in auto-configurable channels. Auto-configurable channels adjust the diagnostic and protective functions according their potential at drain and source automatically.

The load is connected between ground and source of the power transistor (pins OUTn_S, n = 2……7) in high-side configuration. The drains of the power transistors (OUTn_D, with “n” equal to the configurable channel number) can be connected to any potential between ground and VS. The channel behaves like a high-side switch when the drain is connected to VS.

In low-side configuration, the source of the power transistors must be connected to GND.

$R_{DS(ON)}$ depends on the supply voltage and junction temperature T_J.

7.1. Operating modes

7.1.1. Switching resistive loads

In the case of resistive loads switching, refer to the following switching times and slew rates.

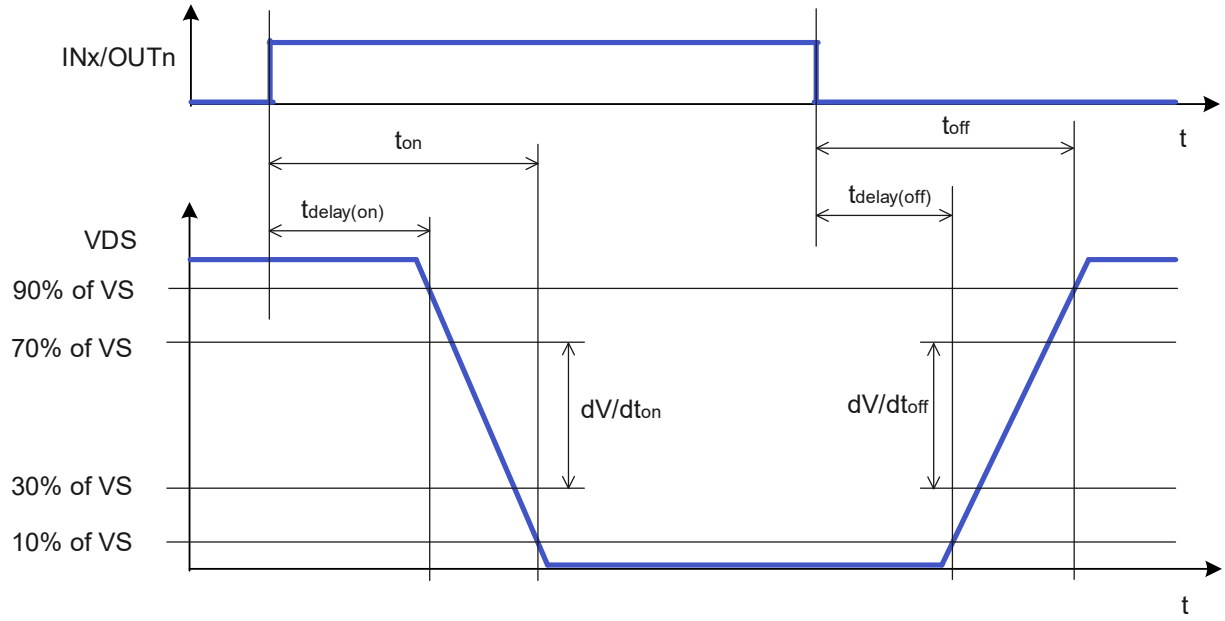


Figure 7.1 Switching ON/OFF timing using resistive Load

7.1.2. Inductive output active clamp

In order to avoid avalanche condition during switching-off an inductive load, the device integrates an internal active clamp, which limits the voltage across the output power switch up to $V_{DS(CL)}$. And The potential at HSD Output pin is not allowed to go below $V_{OUT\_S(CL)}$.

Figure 7.2 shows a concept drawing of the implementation. The clamping structure protects the device in all operative modes (Sleep, Idle, Active, Limp Home).

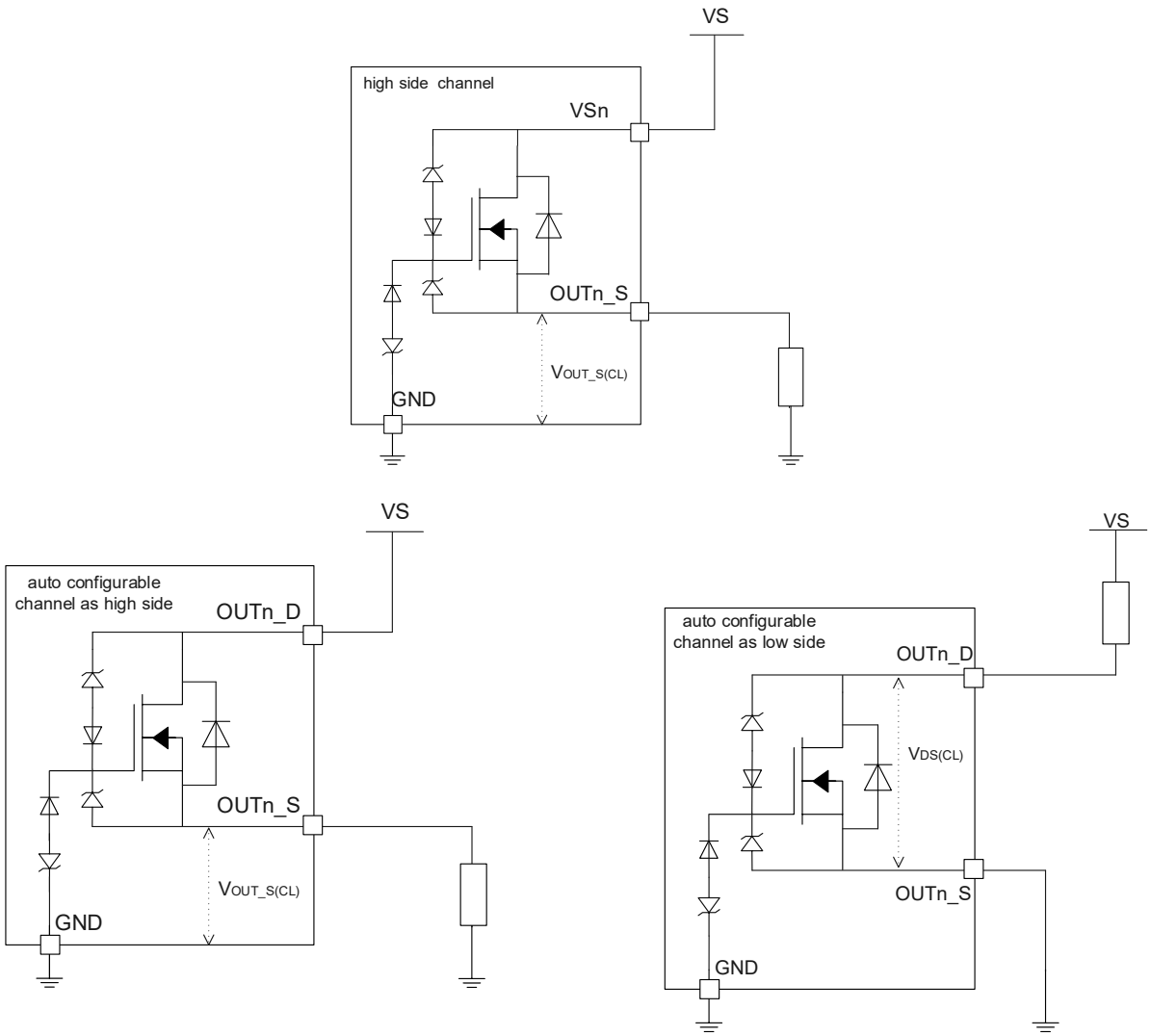


Figure 7.2 Output Clamp concept

7.1.3. Maximum load inductance

During demagnetization of inductive loads, energy has to be dissipated in the NSD56620. Equation below shows how to calculate the energy for low-side switches:

$$E = \int (V_{DS} * ID)dt = \int (C1 * C4)dt$$

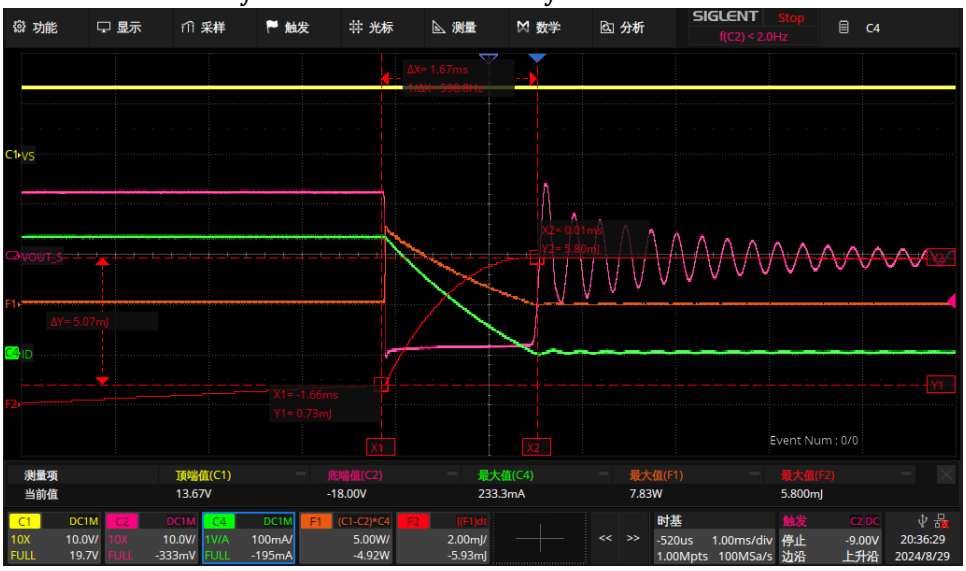
C1: V_{DS} C4: ID

F1: P=C1*C4=V*ID

F2: E=$\int(V_{DS} * ID)dt = \int(C1 * C4)dt$

Equation below shows how to calculate the energy for high-side switches:

$$E = \int[(V_S - V_{OUT\_S}) * ID]dt = \int[(C1 - C2) * C4]dt$$



C1: VS C2: V_{OUT_S} C4: ID

F1: P=(C1-C2) *C4= (VS- V_{OUT_S}) *ID

F2: E=$\int[(V_S - V_{OUT\_S}) * ID]dt = \int[(C1 - C2) * C4]dt$

The maximum energy, which is converted into heat, is limited by the thermal design of the component. When the inductances connected to the outputs are demagnetized at the same time, the E_{AR} value provided in **Table 4.1** assumes that all channels can dissipate the same energy.

7.2. Switching Channels in parallel

During switching channels in parallel application, it may happen that the two channels switch OFF not fully synchronously, therefore bringing an additional thermal stress to the channel that switches OFF last. In order to avoid this condition, NSD56620 provides in the SPI registers (bits **HWCR.PAR**) the parallel operation of two neighbor channels. It is possible to synchronize the following couples of channels:

• channel 0 and channel 2 → HWCR.PAR (0) set to “1”

• channel 1 and channel 3 → HWCR.PAR (1) set to “1”

• channel 4 and channel 6 → HWCR.PAR (2) set to “1”

• channel 5 and channel 7 → HWCR.PAR (3) set to “1”

When operating in this mode, the fastest channel to react to an Over Load or Over Temperature condition will also deactivate the other of parallel group. The inductive energy that two channels can handle once set in parallel is lower than twice the single channel energy.

Note: The synchronization bits only influence how the channels react to Over Load or Over Temperature conditions. Synchronized channels ON/OFF have to be controlled by the micro-controller.

7.3. “Bulb Inrush Mode” (BIM)

Although device is optimized for relays and LED, it may be necessary to use one or more of the outputs as high side switches to drive small lamps or electronic loads with a big input capacitor. In such a case the inrush current trigger the overload diagnostic, switching the channel OFF.

In normal operation in order to re-engage the channels from an overload condition, an SPI command to clear the latches (register **COEL.OUTn**) is needed, to allow the channel turning ON again; for some applications this re-engagement procedure takes too long to transfer enough energy to activate the load.

The IC provides means to overcome this issue by setting **BIM.OUTn** bit to “1”.

Once this feature is enabled, in case the channel reaches the overload current threshold and latches OFF, it restarts automatically after a time t_{INRUSH}, allowing the load to go out of the inrush phase. The automatic reengagement of the faulty channels lasts for a BIM time (t_{BIM}).

Once the t_{BIM} counter is started, it is reset once the t_{BIM} is expired.

A time diagram is shown in **Figure 7.3**. While **BIM.OUTn** bits are set to “1”, **ERRn** bits may be also set to “1” but this doesn’t latch the channel OFF. An internal timer set the bit **BIM.OUTn** back to “0” after 40 ms (parameter t_{BIM}) to prevent an excessive thermal stress to the channel, especially in case of short circuit at the output. The channel configured with BIM option can be either driven by an SPI command (**OUT.OUTn**), PWM command (internal generator) or INn parallel input.

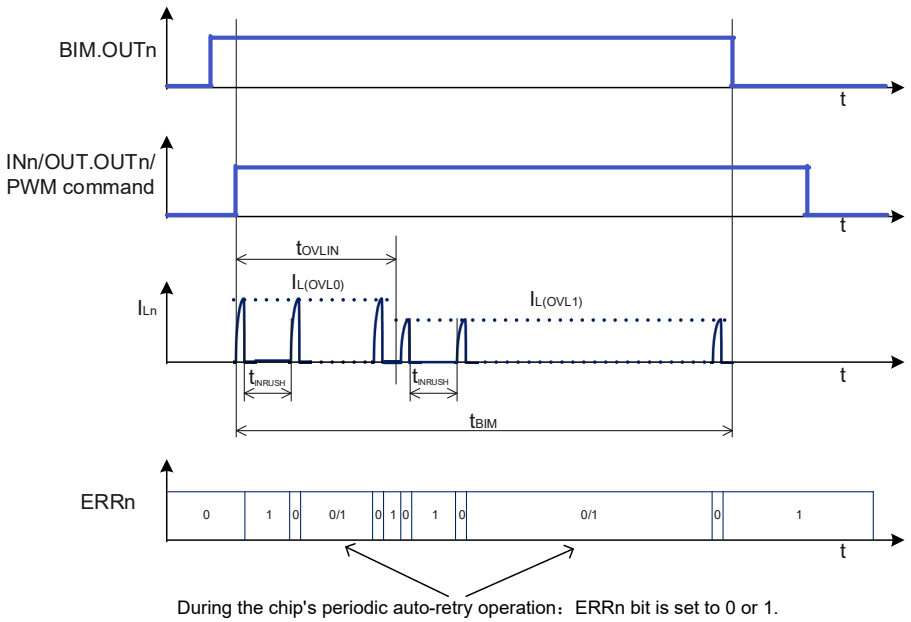


Figure 7.3 Bulb Inrush Mode (BIM) operation

7.4. Automatic PWM Generator

Device has two independents automatic PWM generator implemented. These can be assigned to one or more channels, and can be programmed with a different duty cycle and frequency.

Both refer to a base frequency f_{INT} generated by an internal oscillator. This base frequency can be adjusted using **HWCR_PWM.ADJ** bits as described in Table 7.1.

Table 7.1 HWCR_PWM.ADJ coefficients overview

bit content	absolute delta to f_{INT}
0000_B	(reserved)
0001_B	-37.2%
0010_B	-31.9%
0011_B	-26.9%
0100_B	-21.0%
0101_B	-15.5%
0110_B	-10.9%
0111_B	-5.8%
1000_B	–
1001_B	+4.3%
1010_B	+8.9%
1011_B	+14.0%
1100_B	+19.5%
1101_B	+25.6%
1110_B	+32.4%
1111_B	+40.0%

For each PWM generator four parameters can be set:

• duty cycle (bits **PWM_CR0.DC** for PWM Generator 0)

  – 8 configuration bits are available to achieve 0.39% duty cycle resolution

  – In case the duty cycle is changed, the PWM generator waits until the previous cycle is completed before using the new duty cycle (this happens also when the duty cycle is either 0% or 100% - the new duty cycle is taken with the next PWM cycle)

  – the maximum duty cycle achievable is 99.61% (**PWM_CR0.DC** set to "11111111_B"). It is possible to achieve 100% by setting **PWM_CR0.FREQ** to "11_B"

• frequency (bits **PWM_CR0.FREQ** for PWM Generator 0)

  – with 2 bits is possible to select the divider for f_{INT} to achieve the needed duty cycle

Table 7.2 PWM_CR0.FREQ generator available frequencies

PWM_CR0.FREQ bit content	PWM frequency (when f_{INT} = 102.4 kHz)
00_B	100 Hz
01_B	200 Hz
10_B	400 Hz

• channel output control and mapping registers **PWM_OUT** and **PWM_MAP**)

  – any channel can be mapped to each PWM Generator

  – it is possible to have 4 independent PWM groups of channels together with 2 parallel input

Figure 7.4 expands the concept shown in **Figure 6.1** adding the PWM Generators.

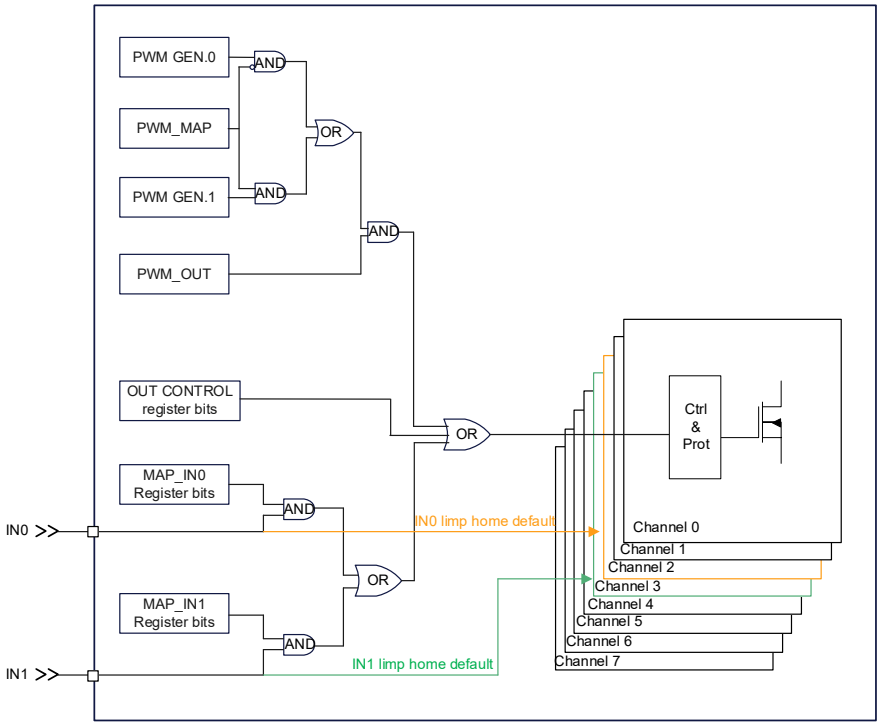


Figure 7.4 PWM Generator Mappings

7.5. Electrical Characteristics Power Stages

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Characteristics						
$R_{DS(ON)}$	On-State Resistance	T_J = 25 °C		1		Ω
$R_{DS(ON)}$	On-State Resistance	T_J = 150 °C $I_L = I_{L(EAR)}$ = 220 mA		1.8	2.2	Ω
$I_{L(NOM)}$	Nominal load current (all channels active) [1]	T_A = 85 °C, $T_J \leq$ 150 °C		330	500	mA
$I_{L(NOM)}$	Nominal load current (all channels active) [1]	T_A = 105 °C, $T_J \leq$ 150 °C		260	500	mA
$I_{L(EAR)}$	Load current for maximum energy dissipation - repetitive (all channels active) [1]	T_A = 85 °C, $T_J \leq$ 150 °C		220		mA
E_{AS}	Maximum energy dissipation single pulse [1]	T_J = 25 °C, I_L = 2 x $I_{L(EAR)}$			50	mJ
E_{AS}	Maximum energy dissipation single pulse [1]	T_J = 150 °C, I_L = 2 x $I_{L(EAR)}$			25	mJ
E_{AR}	Maximum energy dissipation repetitive pulses- $I_{L(EAR)}$ [1]	T_J = 85 °C, $I_L = I_{L(EAR)}$, $2*10^6$ cycles			10	mJ
E_{AR}	Maximum energy dissipation repetitive pulses- $2*I_{L(EAR)}$	T_J = 85 °C $I_L = 2*I_{L(EAR)}$			15	mJ

	(two channels in parallel) [1)]	$2*10^6$ cycles **HWCR.PAR** = "1" for affected channels				
$V_{DS(CL)}$	Drain to Source Output clamping voltage for configurable channels as low side	I_L = 20 mA, V_S = 7 V	39	43	47	V
$V_{OUT\_S(CL)}$	Source to Ground Output clamping voltage for high side or configurable channels as high side	I_L = 20 mA V_S =V_{OUTn_D}= 7 V	-25		-16	V
$I_{L(OFF)}$	Output leakage current (each channel) (Low Side channels)	V_{IN} = 0 V or floating V_{DS} = 18V **OUT.OUTn** = 0		0.1	3	µA
$I_{L(OFF)}$	Output leakage current (each channel) (High Side channels)	V_{IN} = 0 V or floating V_{DS} = 18V V_{OUTn_HS}= 0V V_{OUTn_S}= 0V **OUT.OUTn** = 0		0.1	3	µA
Timings						
$t_{DELAY(ON)}$	Turn-ON delay (from INx pin or bit to V_{OUT} = 90% V_S for low side, and from INx pin or bit to V_{OUT} = 10% V_S for high side)	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	1	6	10	µs
$t_{DELAY(OFF)}$	Turn-OFF delay (from INx pin or bit to V_{OUT} = 10% V_S for low side, and from INx pin or bit to V_{OUT} = 90% V_S for high side)	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	1	10	20	µs
t_{ON}	Turn-ON time (from INx pin or bit to V_{OUT} = 10% V_S for low side, and from INx pin or bit to V_{OUT} = 90% V_S for high side)	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	6	20	40	µs
t_{OFF}	Turn-OFF time, (from INx pin or bit to V_{OUT} = 90% V_S for low side, and from INx pin or bit to V_{OUT} = 10% V_S for high side)	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	6	20	40	µs
t_{ON} - t_{OFF}	Turn-ON/OFF matching	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	-10	0	10	µs
dV/dt_{ON}	Turn-ON slew rate (V_{DS} = 70% to 30% V_S for low side, and V_{DS} = 30% to 70% V_S for high side)	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	0.5	1.3	2.5	V/µs

$-dV/dt_{OFF}$	Turn-OFF slew rate (V_{DS} = 30% to 70% V_S for low side, and V_{DS} = 70% to 30% V_S for high side)	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	0.5	1.3	2.5	V/µs
t_{INRUSH}	Bulb Inrush Mode restart time [1]	Active mode			40	µs
t_{BIM}	Bulb Inrush Mode reset time [1]	Active mode		40		ms
PWM Generator						
f_{INT}	Internal reference frequency	**HWCR_PWM.ADJ** = 1000_B	80	102	125	kHz
$f_{INT(VAR)}$	Internal reference frequency variation [1]		-15		15	%
t_{SYNC}	Internal reference frequency synchronization time [1]	**HWCR_PWM.ADJ** = 1000_B		5	10	µs

1) Not subject to production test - specified by design

8. Protection Functions

8.1. Over Load Protection

The device has two different overload current thresholds that preserve itself in case of overload or short-circuit of the load (see **Figure 8.1**):

- $I_{L(OVL0)}$ between channel switch ON and t_{OVLIN}
- $I_{L(OVL1)}$ after t_{OVLIN}

Every time the channel is switched OFF, the over load current threshold is set back to $I_{L(OVL0)}$

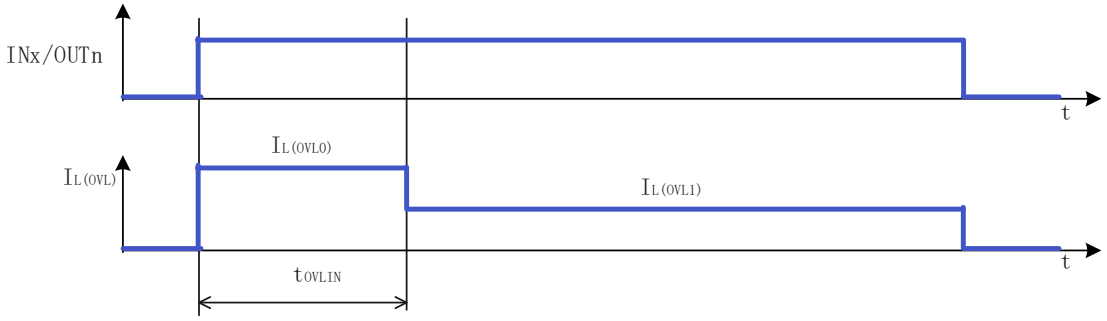


Figure 8.1 Over Load current thresholds

In case the load current is higher than $I_{L(OVL0)}$ or $I_{L(OVL1)}$ and $t_{OFF(OVL)}$ elapsed, the over loaded channel is switched OFF and the corresponding diagnosis bit **ERRn** is set.

After clearing the protection latch by setting the corresponding **COEL.OUTn** bit to “1”, the channel can be switched ON. This bit is automatically set back to “0” internally after clearing latching status of the channel. Please refer to **Figure 8.2** for details.

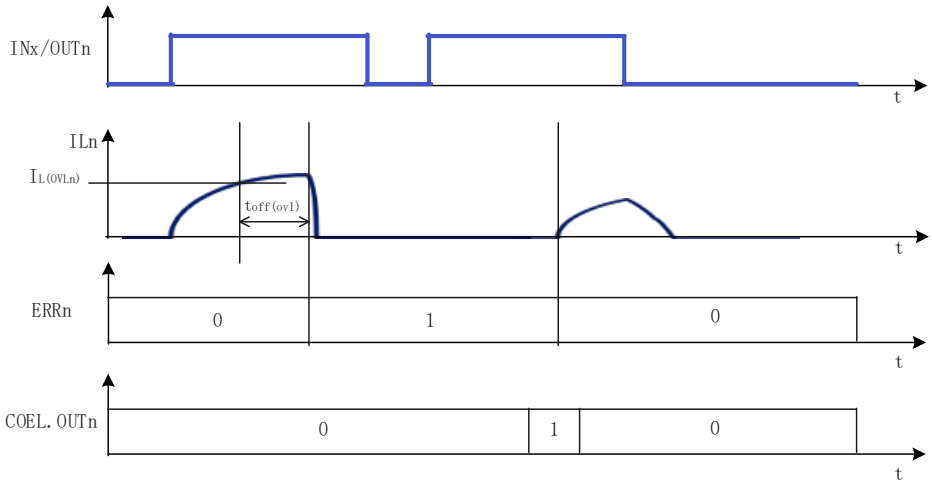


Figure 8.2 Latch OFF at Over Load

8.2. Over temperature Protection

A temperature sensor is integrated for each channel, which switch off the channel in over temperature in order to prevent output stage overheat.

Once the temperature increases above the $T_{J(SC)}$ The according diagnosis bit **ERRn** is set (combined with Over Load protection). The channel can be switched ON after clearing the protection latch by setting the corresponding **COEL.OUTn** bit to “1”. This bit is set back to “0” internally after de-latching the channel.

8.3. Over Temperature and Over Load Protection in Limp Home mode

In limp-home mode, through the input pin IN0 and IN1, the channels 2 and 3 can be switched on. In case of overload, short-circuit or over-temperature the channels are switched off.

In the meanwhile, the device provides auto-retry mechanism If the input pins remain “high” in limp home mode, the channels restart with the following timings (See **Figure 8.3** for details):

• 10 ms (first 8 retries)
• 20 ms (following 8 retries)
• 40 ms (following 8 retries)
• 80 ms (as long as the input pin remains “high” and the error is still present)

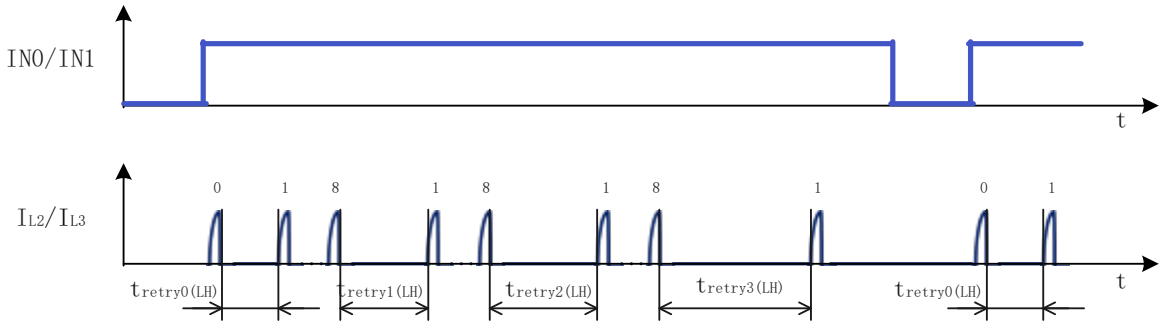


Figure 8.3 Restart timer in Limp Home mode

Note: Every time the input pin is set to “low”, the restart timer is reset. And the timer starts from 10 ms again for the next over temperature / load protection while in Limp Home mode

8.4. Reverse Polarity Protection

There is no reverse polarity protection function in VS pin and OUTn_D pins of auto configuration as HSD. A reverse protection diode or ideal diode must be added before VS pin and OUTn_D pins of auto configuration as HSD.

For auto configuration as low side, the reverse current through the channels is limited by the connected loads, so there is no need to add reverse protection diode or ideal diode before them.

See **Figure 3.1** Application Diagram for details.

8.5. Electrical Characteristics Protection

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Over Load						
$I_{L(OVL0)}$	Over Load detection current		1	1.7	2.5	A
$I_{L(OVL1)}$	Over Load detection current		0.5	0.9	1.5	A
t_{OVLIN}	Over Load threshold switch delay time	Guaranteed by digital SCAN	110	170	260	μs
$t_{OFF(OVL)}$	Over Load shut-down delay time		10	15	20	μs
Over Temperature						
$T_{J(SC)}$	Thermal shut-down temperature [1)]		150	170	190	°C
Timings						
$t_{RETRY0(LH)}$	Restart time in Limp Home mode	Guaranteed by digital SCAN	7	10	13	ms
$t_{RETRY1(LH)}$	Restart time in Limp Home mode	Guaranteed by digital SCAN	14	20	26	ms

$t_{RETRY2(LH)}$	Restart time in Limp Home mode	Guaranteed by digital SCAN	28	40	52	ms
$t_{RETRY3(LH)}$	Restart time in Limp Home mode	Guaranteed by digital SCAN	56	80	104	ms

1) Not subject to production test - specified by design

9. Diagnosis

The SPI communication provides diagnosis information about the device and the load status. Diagnosis information of each channel is independent from other channels. An error condition on one channel has no influence on the diagnostic of other channels in the device (unless two neighbor channels are configured to work in parallel, see Chapter 7.2 for more details).

9.1. Over Load and Over Temperature

When either an Over Load or an Over Temperature occurs on one channel, the diagnosis bit **ERRn** is set accordingly. The channel latches OFF and must be reactivated setting corresponding **COEL.OUTn** bit to “1”.

9.2. Output status Monitor

To monitor the output pin and load status, the device integrates dedicated voltage comparator for each channel. It compares V_{DS} with $V_{DS(OL)}$ (auto-configurable channels used as Low-Side switches) , V_{OUT_S} with $V_{OUT\_S(OL)}$ (auto-configurable channels used as High-Side), V_{OUT} with $V_{OUT(OL)}$ (High-Side channels) and sets the corresponding **DIAG_OSM.OUTn** bits accordingly, based on the below logic.

- $V_{DS} < V_{DS(OL)} \rightarrow$ **DIAG_OSM.OUTn** = “1” (auto-configurable channels as Low-Side)
- $V_{OUT\_S} > V_{OUT\_S(OL)} \rightarrow$ **DIAG_OSM.OUTn** = “1” (auto-configurable channels as High-Side)
- $V_{OUT} > V_{OUT(OL)} \rightarrow$ **DIAG_OSM.OUTn** = “1” (High-Side channels)

The bits are updated every time **DIAG_OSM** register is read.

Additionally, a diagnosis current IOL in parallel to the power switch can be enabled by programming the **IOL.OUTn** bit. With IOL enabled and power switch OFF, open Load in OFF state can be detected when **DIAG_OSM.OUTn** = “1”.

Open load in off state can be detected in the following case:

Channel	Bit IOL.OUTn	Bit DIAG_OSM.OUTn	Bit OLOFF
OFF	1	1	1

Note:

1. If the diagnosis current I_{OL} is enabled or if the channel changes state (ON → OFF or OFF → ON), it is necessary to wait a time t_{OSM} for a reliable diagnosis.

*2. Due to output status monitor checks the voltage level at the outputs in real time, for Open Load in OFF diagnostic, it is necessary to read **DIAG_OSM** register after the channels switch off.*

*3. In Standard Diagnosis the bit **OLOFF** represents the OR combination of all **DIAG_OSM.OUTn** bits for all channels in OFF state which have the corresponding current source IOL activated*

4. Enabling I_{OL} current sources increases the current consumption of the device.

5. Even if an Open Load is detected, the channel is not latched OFF.

Output Status Monitor diagnostic is available when $V_S = V_{S(NOR)}$ and $V_{DD} \geq V_{DD(UV)}$.

See **Figure 9.1** for **DIAG_OSM** timing overview and **Figure 9.2** for **DIAG_OSM** internal structure

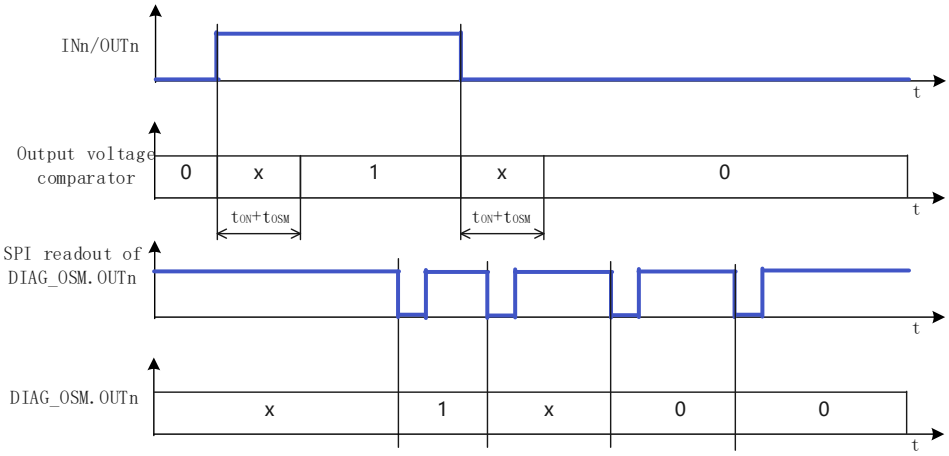


Figure 9.1 Output Status Monitor timing

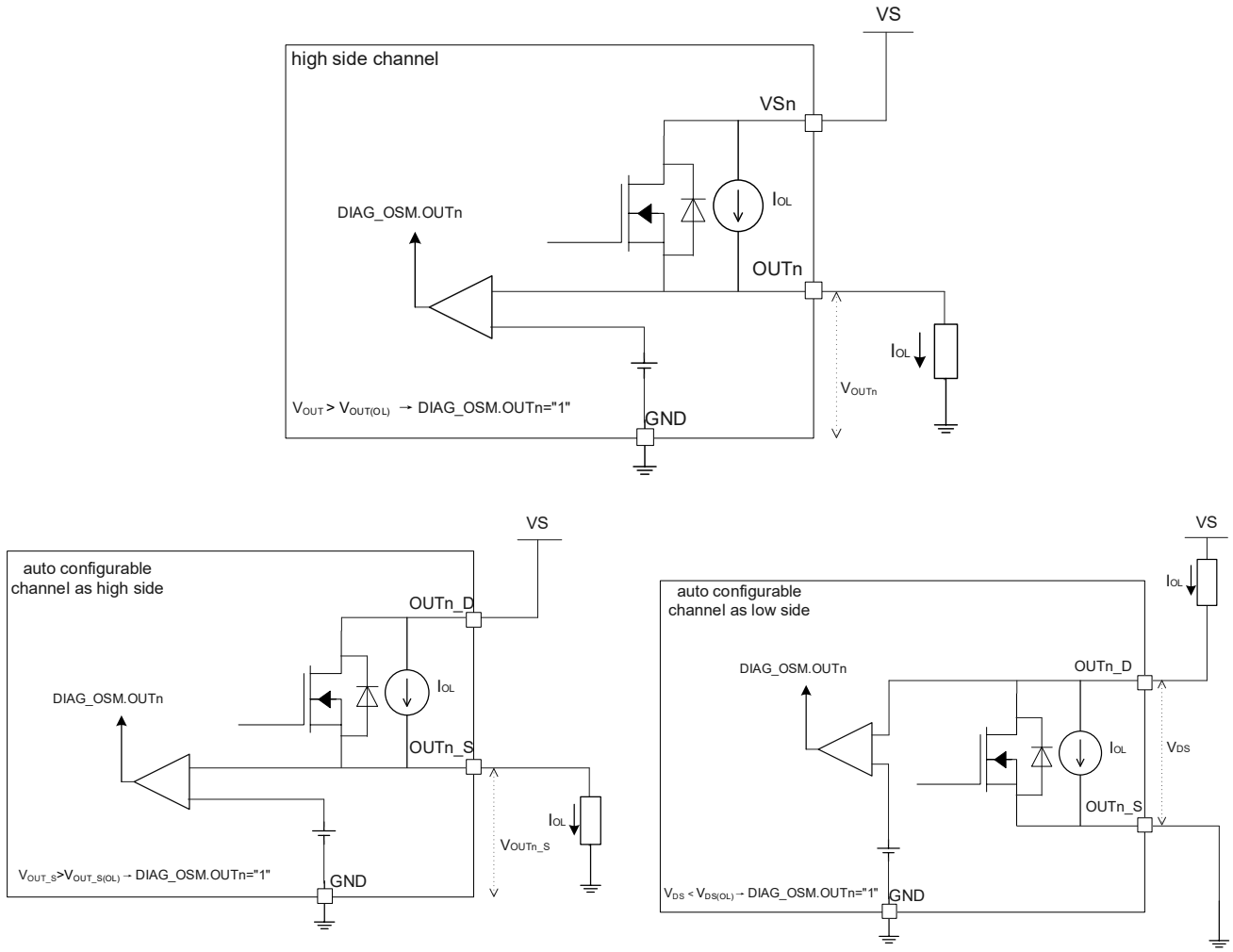


Figure 9.2 Output Status Monitor - concept

9.3. Open Load at ON

On each channel it is possible to request the open load at on diagnosis, the device will ignore the request of the channel is configured as low side. By default, after a reset Open Load at ON diagnosis is not active. The device compares the load current I_{L_Sn} with the open Load detection threshold current $I_{L(OL)}$. The **DIAG_OPL_ON.OUTn** bit is set as follows:

$I_{L\_Sn} < I_{L(OL)} \rightarrow$ **DIAG_OPL_ON. OUTn** = "1" if $V_{OUTn\_S} > V_{OUT\_S(OL)}$

9.3.1. Open Load at ON - direct channel diagnosis

The internal multiplexer checks for Open Load at ON condition on the selected channel when **DIAG_OPL_ONEN.MUX** bits are programmed with a value corresponding to a channel ($0000_B \rightarrow 0111_B$). Before activating the diagnosis, it is recommended that the channel is ON for at least t_{ON}. The corresponding **DIAG_OPL_ON. OUTn** bit for the selected channel is available after a time $t_{OLONSET}$. All the other bits in the **DIAG_OPL_ON** register is set to default ("0_B"). The bits are updated every time the register is read.

The corresponding **DIAG_OPL_ON. OUTn** bit content is mirrored also in the Standard Diagnosis (bit **OLON**), when a channel is selected. The register content is updated at every read request from micro-controller in case of several register readouts in sequence. See **Figure 9.3** for further details.

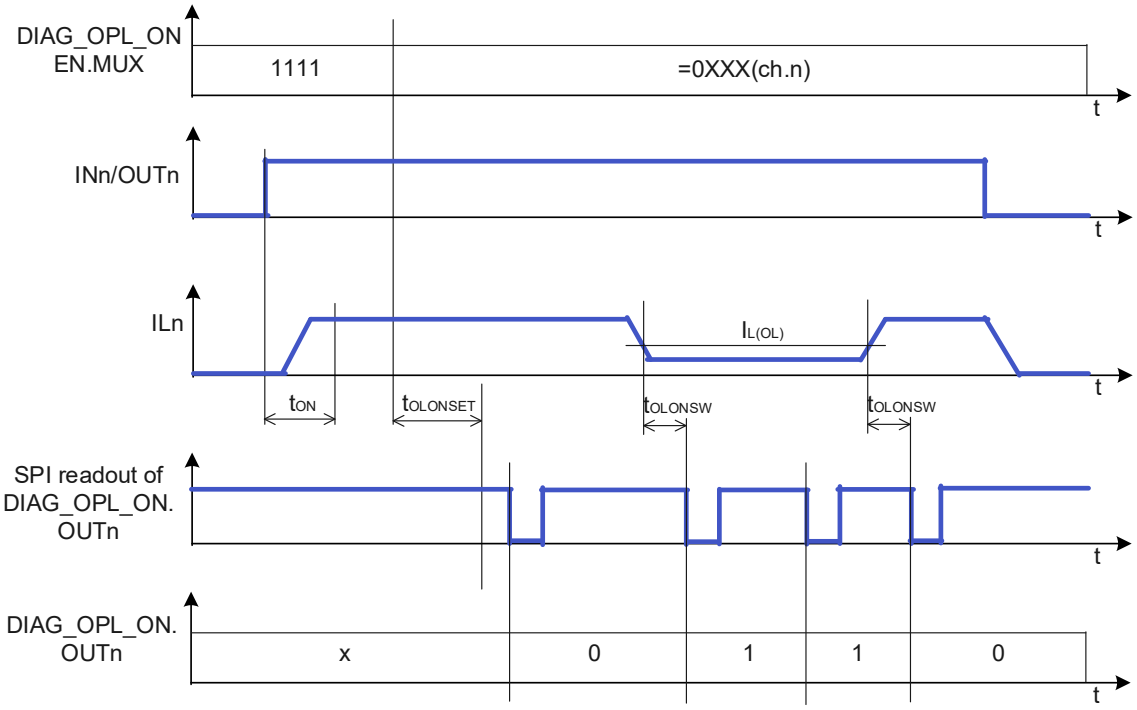


Figure 9.3 Open Load at ON timings (direct channels diagnosis)

9.3.2. Open Load at ON - diagnosis loop

The device starts a diagnosis loop where all high-side switches channels are checked for Open Load at ON when **DIAG_OPL_ONEN.MUX** bits are programmed with the value 1010_B.

First the internal logic checks all channels which are directly driven by MCU（including INx and **OUT.OUTn**） and not configured to be driven by the internal PWM generator.

And then the internal logic checks all channels which are configured to be driven by the internal PWM generator.

• Diagnosis sequence for channels driven directly by MCU

- The first channel to be checked is channel 0. Prior to activating the diagnostic loop, the channel must remain in the ON state for at least t_{ON}.
- The diagnosis for the first channel is completed (**DIAG_OPL_ON.OUTn** bit is updated) after a time $t_{OLONSET}$.
- The internal multiplexer is set to the next channel. After a time t_{OLONSW} the diagnosis is completed (**DIAG_OPL_ON.OUTn** bit is updated) for the currently selected channel. This step is repeated for all other remaining directly driven channels.
- The corresponding **DIAG_OPL_ON. OUTn** is set to "0_B", if one channel is OFF when the diagnosis is performed.

• Diagnosis sequence for channels driven by the internal PWM Generators (see Chapter 7.4)

- These channels are diagnosed after all the channels that are directly driven by the microcontroller have been checked.
- Channels mapped to PWM Generator 0 are diagnosed first
- After a time $t_{OLONSET}$, the channel switch on is the trigger event to perform Open Load at ON diagnosis for the first channel
- The diagnosis for the first channel is completed (**DIAG_OPL_ON.OUTn** bit is updated) after a time $t_{ONMAX} + t_{OLONSW}$
- The internal multiplexer is set to the next channel. The diagnosis is completed (**DIAG_OPL_ON.OUTn** bit is updated) for the currently selected channel after a time t_{OLONSW}. This step is repeated for all remaining PWM generator driven channels.
- If the channel is in OFF state during the PWM period, the internal logic waits until the channel change to the ON state to perform the diagnosis. The diagnostic procedure for the channel is completed after a duration of $t_{ONMAX} + t_{OLONSW}$.
- The minimum ON time for a reliable diagnosis is > $t_{ONMAX} + t_{OLONSW}$. If the ON time is < $t_{ONMAX} + t_{OLONSW}$ the corresponding **DIAG_OPL_ON. OUTn** is set to "0_B".

- If the PWM generator0 or PWM generator1 is actived without configuring the corresponding CR0 or CR1, the diagnostic loop module will wait for corresponding CRX to be configured, and normal diagnosis loop can't take place.
- If the **PWM_MAP** map the channel to PWM generator1 which is not active, the diagnosis will not be able to exit the diagnosis loop.
- When some channels are mapped to PWM generator 0 via **PWM_MAP**, but none of the channels are connected to PWM generator 0 through **PWM_OUT**, there is a possibility that open load at ON cannot be diagnosed in the diagnosis loop
- In summary, if the diagnosis loop function is to be utilized, the recommended initialization configuration is as follows:
  - **PWM_CR0** register :(9300_H)
  - **PWM_CR1** register :(9700_H)
  - **HWCR_PWM** register:($8E83_H$)

When the loop finishes, **DIAG_OPL_ONEN.MUX** bits are set back to 1111_B (default value) and **DIAG_OPL_ON. OUTn** bits store the last diagnosis loop result. It is necessary to start another diagnosis loop to update the register content.

Figure 9.4 shows the timing in case of channels driven directly by micro-controller, while **Figure 9.5** represents the case with channels driven by internal PWM Generators.

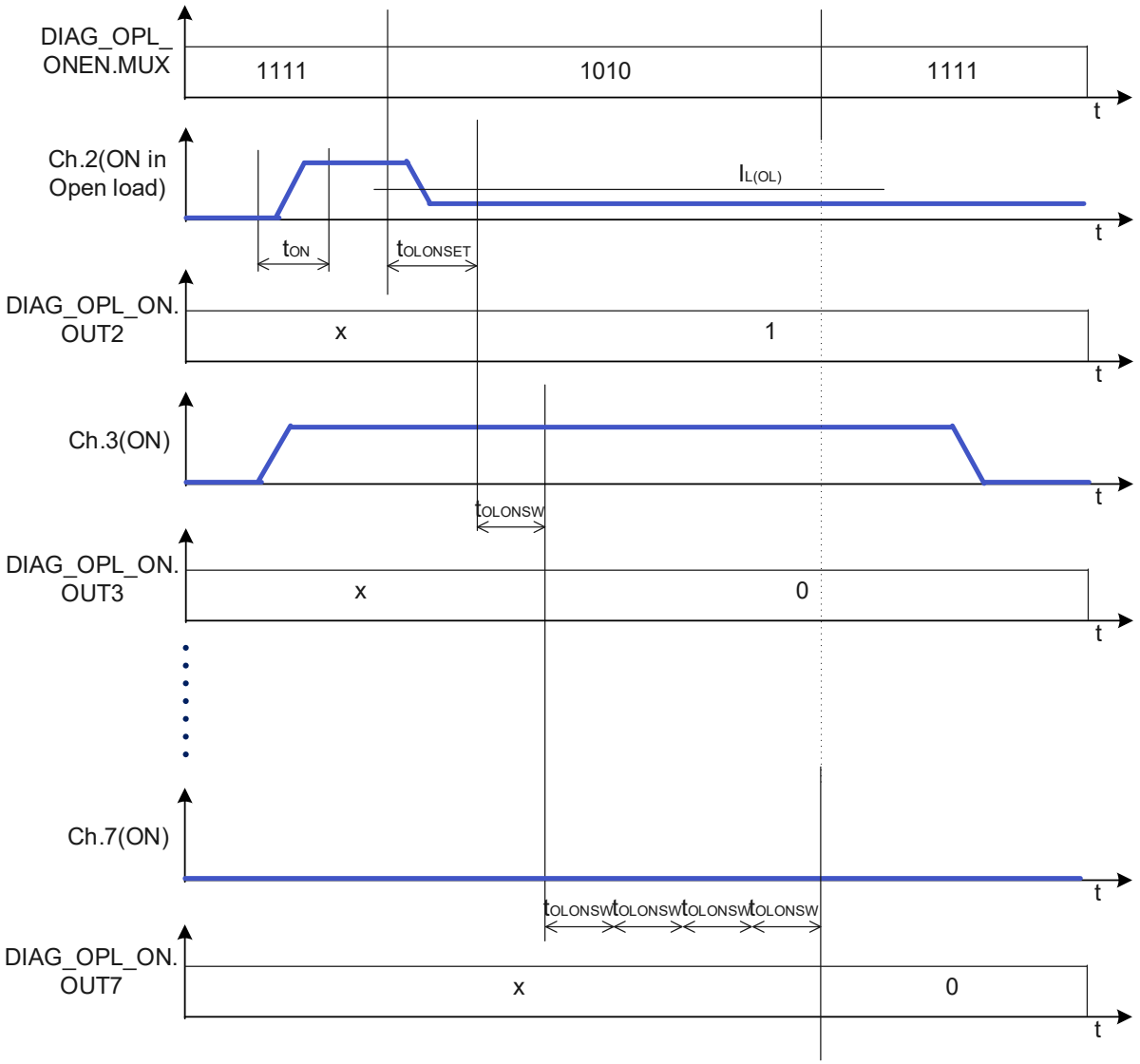
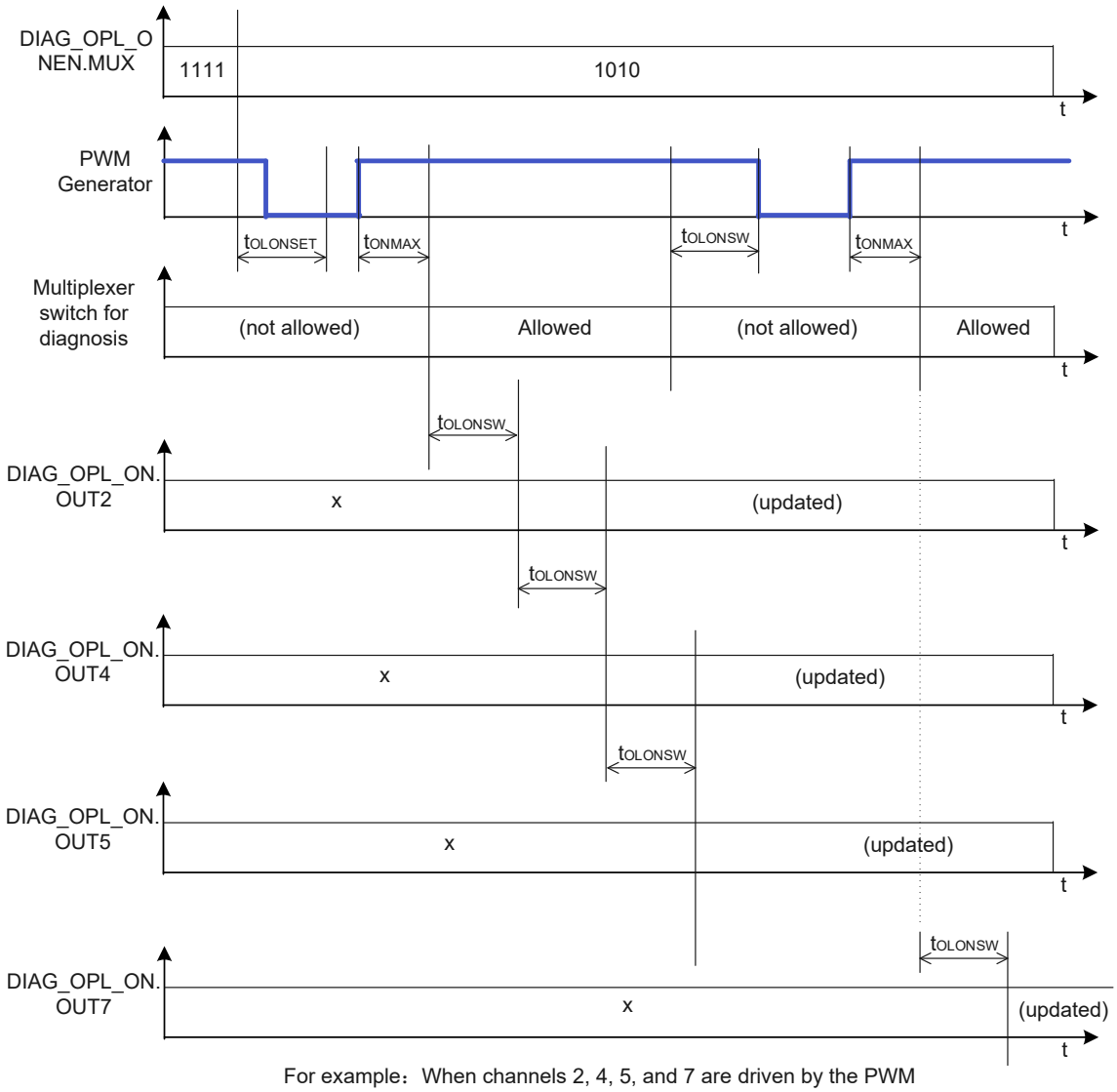


Figure 9.4 Open Load at ON timings (diagnosis loop - channels driven by micro-controller directly)



For example：When channels 2, 4, 5, and 7 are driven by the PWM generator, the sequence of their diagnostic loops is as illustrated in the figure.

Figure 9.5 Open Load at ON timings (diagnosis loop - channels driven by internal PWM Generators)

9.3.3. OLON bit

The **OLON** bit can assume the following values:

• “0” = no Open Load at ON state detected, or the channel is OFF when the diagnosis is performed

• “1” = Open Load at ON state detected

According to the setting of **DIAG_OPL_ONEN.MUX** different information is reported in the Standard Diagnosis.

• **DIAG_OPL_ONEN.MUX** set to $0000_B \rightarrow 0111_B$: The **OLON** bit shows the Open Load at ON state diagnosis performed on the selected channel. The information is updated at every Standard Diagnosis readout.

• **DIAG_OPL_ONEN.MUX** set to 1010_B: the **OLON** bit shows the “OR” combination of all bits in **DIAG_OPL_ON** register. The information is updated while the diagnosis loop is running.

• **DIAG_OPL_ONEN.MUX** set to 1111_B: the **OLON** bit shows the result of the latest diagnosis loop performed. It is necessary to start another diagnosis loop to update the information.

• **DIAG_OPL_ONEN.MUX** set to any other value: The **OLON** bit is set to “0”. These values of **DIAG_OPL_ONEN.MUX** bits are reserved and should not be used in the application.

9.4. Electrical Characteristics Diagnosis

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Status Monitor						
t_{OSM}	Output Status Monitor comparator settling time [1]				20	µs
$V_{DS(OL)}$	Output Status Monitor threshold voltage (auto-configurable channels used as Low-Side switches)		3	3.3	3.6	V
$V_{OUT(OL)}$	Output Status Monitor threshold voltage (High-Side channels)		3	3.3	3.6	V
$V_{OUT\_S(OL)}$	Output Status Monitor threshold voltage (auto-configurable channels used as High-Side switches)		3	3.3	3.6	V
I_{OL}	Output diagnosis current	V_{DS} = 3.3 V	60	85	105	µA
R_{OL}	Open Load equivalent resistance [1]	Application information	28		300	kΩ
Open load at ON						
t_{ONMAX}	Open Load at ON Diagnosis waiting time before mux activation [1]		40	58	76	µs
$t_{OLONSET}$	Open Load at ON Diagnosis settling time [1]			20	40	µs
t_{OLONSW}	Open Load at ON Diagnosis channel switching time [1]			10	20	µs
$I_{L(OL)}$	Open Load detection threshold current		1		15	mA

1) Not subject to production test - specified by design

10. Serial Peripheral Interface (SPI)

The SPI version of the device has full duplex, 4-wire synchronous communication. This section describes the SPI protocol, the command structure, and the control and status registers. The device can be connected with the MCU in the following configurations:

• One slave device

• Multiple slave devices in parallel connection

• Multiple slave devices in series (daisy chain) connection

The falling edge of NCS indicates the beginning of an access. Date is shifted out on line SDO at the first rising edge of SCLK and sampled in on line SDI at first falling edge of SCLK. Each access must be terminated by a rising edge of NCS.

CPOL=0, CPHA=1

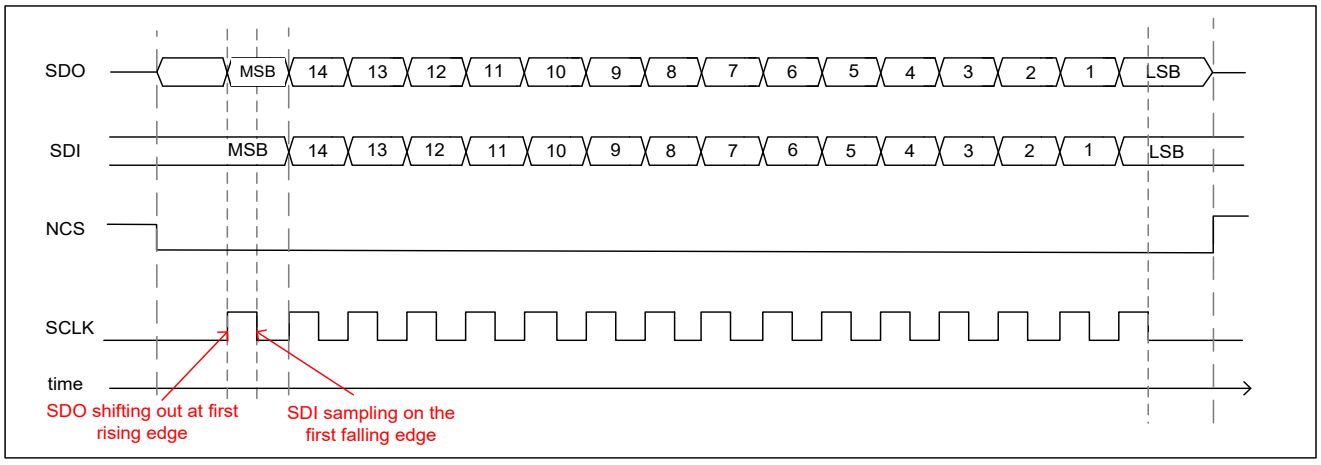


Figure 10.1 Serial Peripheral Interface

A modulo 8/16 counter ensures that data is taken only when a multiple of 8 bits has been transferred after the first 16 bits. Otherwise a **TER** bit is asserted. In this way the interface provides daisy chain capability with 16 bits as well as with 8-bit SPI devices.

10.1. SPI signal description

NCS - Chip Select: Whenever the pin is in “low” state, data transfer can take place. Any signals at the SCLK and SDI pins are ignored when NCS is in "high" state and SDO is forced into a high impedance state.

• NCS “high” to “low” Transition:

- The requested information is transferred into the shift register.
- SDO changes from high impedance state to "high" or “low” state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SDI. This allows to detect a faulty transmission even in daisy chain configuration.
- If the device is in Sleep mode, SDO pin remains in high impedance state and no SPI transmission occurs.

• NCS “low” to "high" Transition：

- Command decoding is only done, when after the falling edge of NCS exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected after the first 16 SCLK pulses. In case of faulty transmission, the transmission error bit (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock: This input pin clocks the internal shift register. The serial input (SDI) transfers data into the shift register on the falling edge of SCLK while the serial output (SDO) shifts date out on the rising edge of the serial clock. It is essential that the SCLK pin is in “low” state whenever chip select NCS makes any transition, otherwise the command may be not accepted.

SDI - Serial Input: Serial input data bits are shift-in at this pin, MSB first. SDI information is read on the falling edge of SCLK.

SDO Serial Output: Data is shifted out serially at this pin, MSB first. SDO is in high impedance state until the NCS pin goes to “low” state. New data appears at the SDO pin following the rising edge of SCLK.

10.2. Parallel and daisy chain capability

SPI communication between micro controller (SPI master) and multiple these devices (slave) can be operated in parallel or in daisy chain. Parallel operation: several slave devices are connected to one SPI channel, which share communication lines SDI, SDO and SCLK, but every slave connects dedicated own NCS.

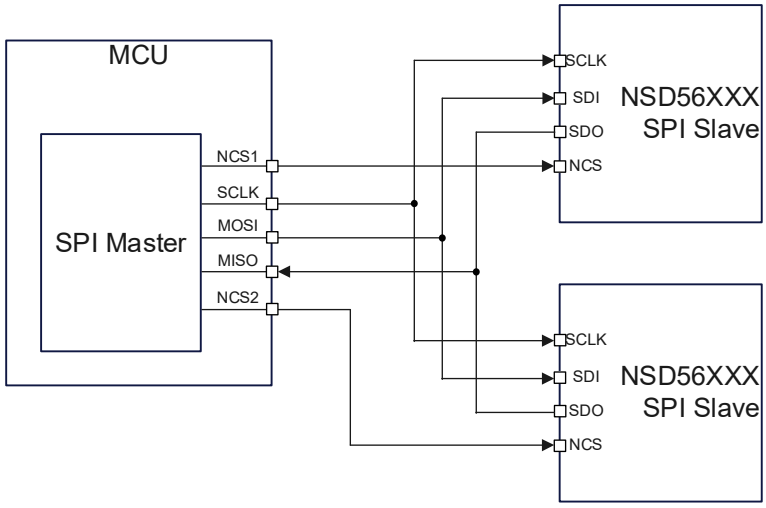


Figure 10.2 Parallel Configuration

Daisy chain operation: multi devices are connected with shared one NCS and SCLK, while each device SDI and SDO are daisy-chain connected. An example of 3 devices in daisy chain as below **Figure 10.3**:

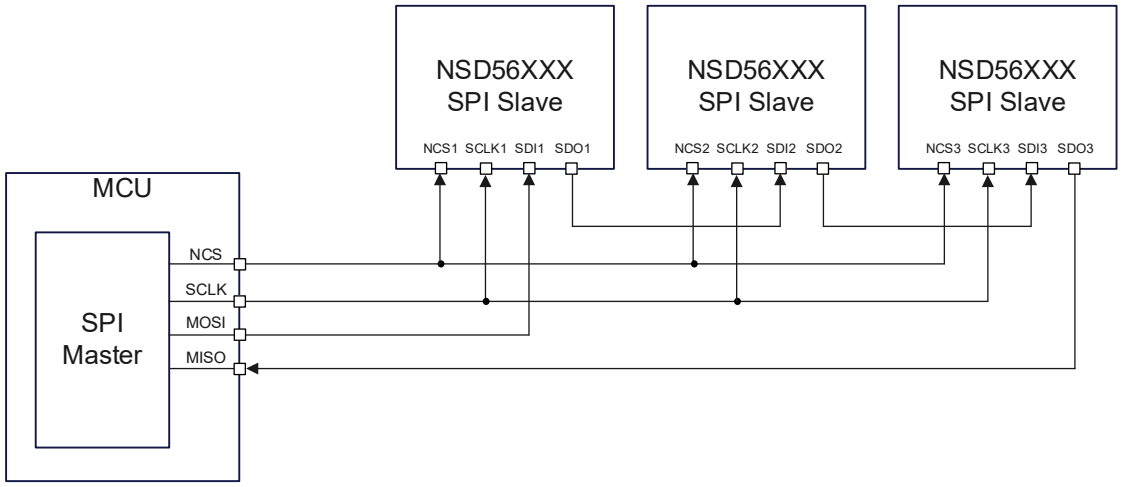


Figure 10.3 Daisy Chain Configuration

The NCS line must turn “high” to make the device acknowledge the transferred data in single chip configuration. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, several multiples of 8 bits have to be shifted through the devices. After that, the NCS line must turn “high”.

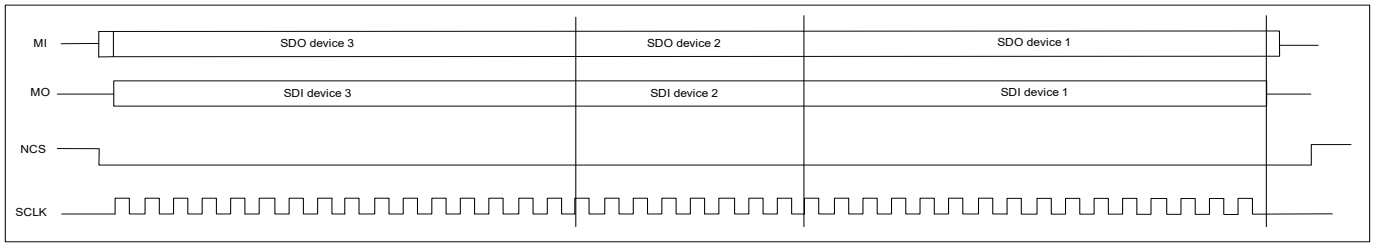


Figure 10.4 Data Transfer in Daisy Chain Configuration

10.3. Timing Diagrams

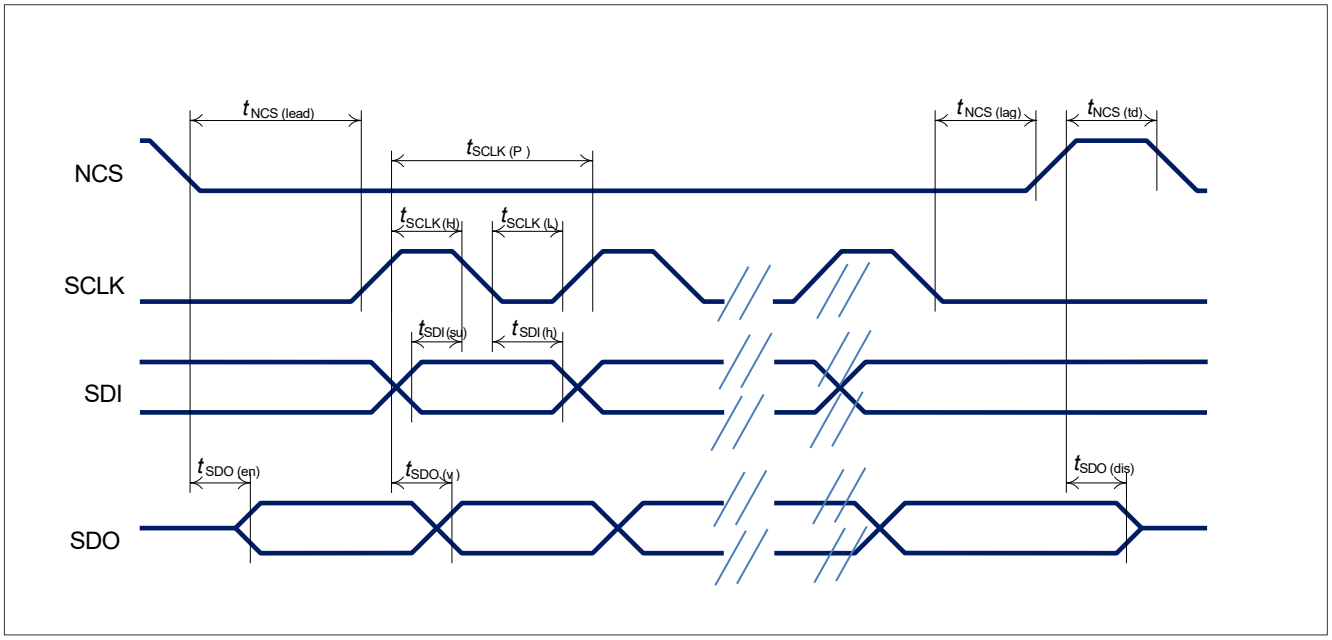


Figure 10.5 Timing Diagram SPI Access

10.4. Electrical Characteristics Serial Peripheral Interface (SPI)

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J= 25 °C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Characteristics (NCS, SCLK, SDI) - "low" level of pin						
$V_{NCS(L)}$	NCS		0		0.8	V
$V_{SCLK(L)}$	SCLK		0		0.8	V
$V_{SDI(L)}$	SDI		0		0.8	V
Input Characteristics (NCS, SCLK, SDI) - "high" level of pin						
$V_{NCS(H)}$	NCS		2		V_{DD}	V
$V_{SCLK(H)}$	SCLK		2		V_{DD}	V
$V_{SDI(H)}$	SDI		2		V_{DD}	V
Output Characteristics (SDO)						
$V_{SDO(L)}$	L level output voltage	I_{SDO} = -1.5 mA	0		0.4	V
$V_{SDO(H)}$	H level output voltage	I_{SDO} = 1.5 mA	V_{DD} - 0.4		V_{DD}	V
Timings						
$t_{NCS(lead)}$	Enable lead time (falling NCS to rising SCLK) [1]	V_{DD} ≥ 3 V	200			ns
$t_{NCS(lag)}$	Enable lag time (falling SCLK to rising NCS) [1]	V_{DD} ≥ 3 V	200			ns
$t_{NCS(td)}$	Transfer delay time (rising NCS to falling NCS) [1]	V_{DD} ≥ 3 V	250			ns
$t_{SDO(en)}$	Output enable time (falling NCS to SDO valid) [1]	V_{DD} ≥ 3 V, C_L = 20 pF at SDO pin			200	ns
$t_{SDO(dis)}$	Output disable time (rising NCS to SDO tristate) [1]	V_{DD} ≥ 3 V, C_L = 20 pF at SDO pin			200	ns
f_{SCLK}	Serial clock frequency[1]	V_{DD} ≥ 3 V			5	MHz
$t_{SCLK(P)}$	Serial clock period[1]	V_{DD} ≥ 3 V	200			ns
$t_{SCLK(H)}$	Serial clock "high" time[1]	V_{DD} ≥ 3 V	75			ns
$t_{SCLK(L)}$	Serial clock "low" time [1]	V_{DD} ≥ 3 V	75			ns
$t_{SDI(su)}$	Data setup time (required time SDI to falling SCLK) [1]	V_{DD} ≥ 3 V	20			ns
$t_{SDI(h)}$	Data hold time (falling SCLK to SDI) [1]	V_{DD} ≥ 3 V	20			ns
$t_{SDO(v)}$	Output data valid time with capacitive load[1]	V_{DD} ≥ 3 V, C_L = 20 pF at SDO pin			100	ns

1) Not subject to production test, specified by design

10.5. SPI Protocol

The relationship between SDI and SDO content during SPI communication is shown in **Figure 10.6**.

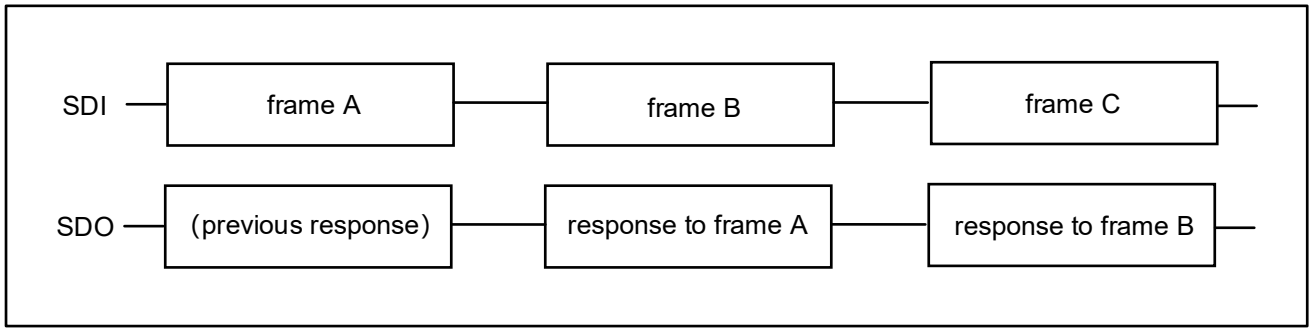


Figure 10.6 Relationship between SDI and SDO during SPI communication

The SPI protocol provides the answer to a command frame only with the next transmission triggered by the MCU.

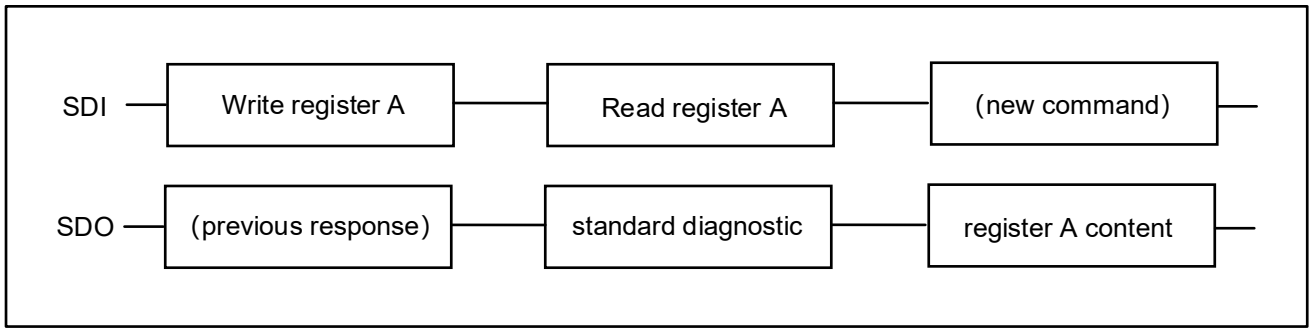


Figure 10.7 Register content sent back to µC

There are 3 special situations where the frame sent back to the µC is not related directly to the previous received frame:

• In case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8 with a minimum of 16 bits), shown in **Figure 10.8**

• When NSD56620 logic supply comes out of Power-On reset condition or after a Software Reset, as shown in **Figure 10.9**

• In case of command syntax errors

- "write" command starting with "11" instead of "10"
- "read" command starting with "00" instead of "01"
- "read" or "write" commands on registers which are "reserved" or "not used"

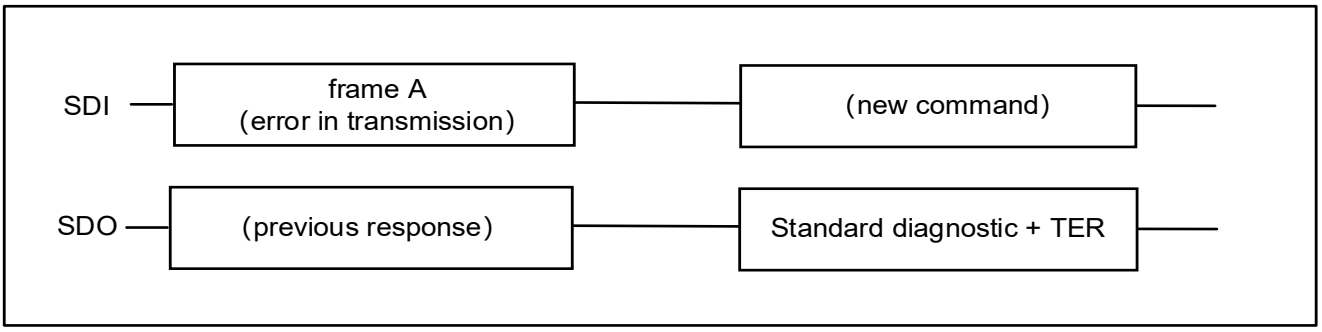


Figure 10.8 NSD56620 response after an error in transmission

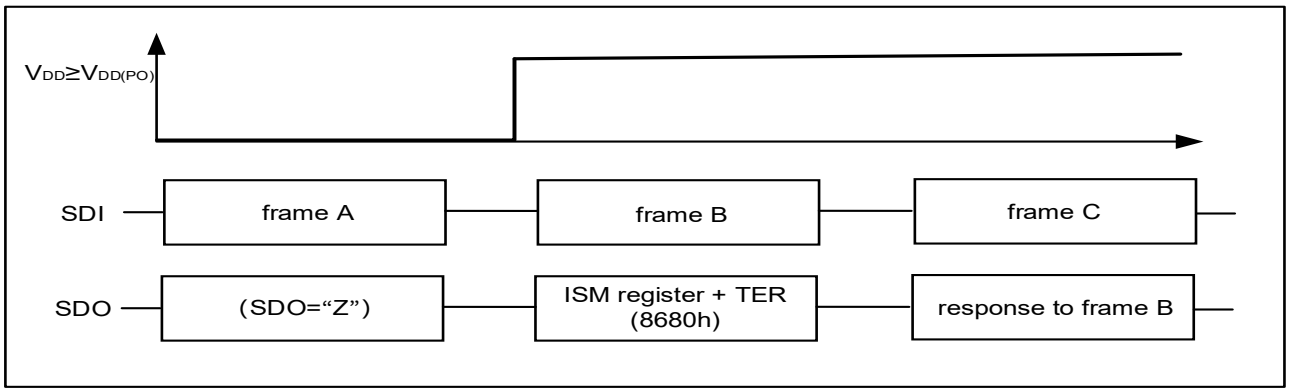


Figure 10.9 NSD56620 response after coming out of Power-On reset at V_{DD}

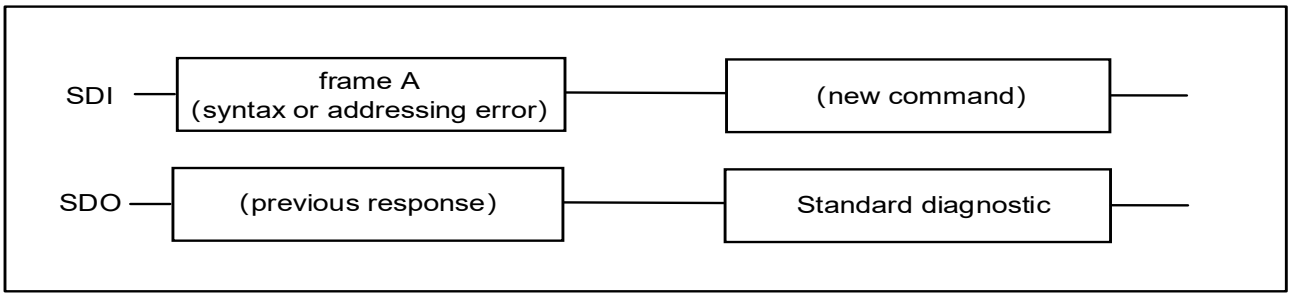


Figure 10.10 NSD56620 response after a command syntax error

A summary of all possible SPI commands is presented in Table 10.1, including the answer that NSD56620 sends back at the next transmission.

Table 10.1 SPI Command summary[1)]

Requested Operation	Frame sent to device (SDI pin)	Frame received from device (SDO pin) with the next command
Read Standard Diagnosis	0xxxxxxxxxxxxx01$_B$ ("xxxxxxxxxxxx$_B$" = don´t care)	0ddddddddddddddd$_B$ (Standard Diagnosis)
Write 10-bit register	10aaaaccccccccc$_B$ where: "aaaa$_B$" = register address ADDR0 "ccccccccc$_B$" = new register content	0ddddddddddddddd$_B$ (Standard Diagnosis)
Read 10-bit registers	01aaaaxxxxxxxx10$_B$ where: "aaaa$_B$" = register address ADDR0 "xxxxxxxx$_B$" = don´t care	10aaaaccccccccc$_B$ where: "aaaa$_B$" = register address ADDR0 "ccccccccc$_B$" = register content
Write 8-bit register	10aaaabbccccccccc$_B$ where: "aaaa$_B$" = register address ADDR0 "bb$_B$" = register address ADDR1 "cccccccc$_B$" = new register content	0ddddddddddddddd$_B$ (Standard Diagnosis)
Read 8-bit registers	01aaaabbxxxxxx10$_B$ where: "aaaa$_B$" = register address ADDR0 "bb$_B$" = register address ADDR1 "xxxxxx$_B$" = don´t care	10aaaabbccccccccc$_B$ where: "aaaa$_B$" = register address ADDR0 "bb$_B$" = register address ADDR1 "cccccccc$_B$" = register content

1) "a" = address bits for ADDR0 field, "b" = address bit for ADDR1 field, "c" = register content, "d" = diagnostic bit

10.6. SPI registers Overview

10.6.1. Standard Diagnosis

Table 10.2 Standard Diagnosis register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field Name	0	VSUV	LOP VDD	MODE		TER	OLON	OLOFF	ERR							
Default	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

1) Default value is 7800_H

Table 10.3 Standard Diagnosis register description

Bit	Field Name	Type	Description
15	Reserved	r	0: reserved (default value)
14	VSUV	r	VS Undervoltage Monitor 0: No undervoltage condition on V_S detected 1: (default) There was at least one V_S Undervoltage condition since last Standard Diagnosis readout
13	LOPVDD	r	VDD Lower Operating Range Monitor 0: V_{DD} is above $V_{DD(LOP)}$ 1: (default) There was at least one "V_{DD} = $V_{DD(LOP)}$" condition since last Standard Diagnosis readout
12:11	MODE	r	Operative Mode Monitor 00: (reserved) 01: Limp Home Mode 10: Active Mode 11: (default) Idle Mode
10	TER	r	Transmission Error 0: Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1: (default) Previous transmission failed The first frame after a reset is **TER** set to "high" and the **ISM** register. The second frame is the Standard Diagnosis with **TER** set to "low" (if there was no fail in the previous transmission).
9	OLON	r	Open Load at ON state Diagnosis 0: (default) No Open Load at ON detected 1: Open Load at ON detected
8	OLOFF	r	Open Load in OFF Diagnosis 0: (default) All channels in OFF state (which have **IOL.OUTn** bit set to "1") have V_{DS} > $V_{DS(OL)}$ 1: At least one channel in OFF state (with **IOL.OUTn** bit set to "1") has V_{DS} < $V_{DS(OL)}$ Channels in ON state are not considered
7	ERR7	r	Over Load / Over Temperature Diagnosis of channel 7 0: (default) No failure detected 1: Over Temperature or Over Load

6	ERR6	r	Over Load / Over Temperature Diagnosis of channel 6 0: (default) No failure detected 1: Over Temperature or Over Load
5	ERR5	r	Over Load / Over Temperature Diagnosis of channel 5 0: (default) No failure detected 1: Over Temperature or Over Load
4	ERR4	r	Over Load / Over Temperature Diagnosis of channel 4 0: (default) No failure detected 1: Over Temperature or Over Load
3	ERR3	r	Over Load / Over Temperature Diagnosis of channel 3 0: (default) No failure detected 1: Over Temperature or Over Load
2	ERR2	r	Over Load / Over Temperature Diagnosis of channel 2 0: (default) No failure detected 1: Over Temperature or Over Load
1	ERR1	r	Over Load / Over Temperature Diagnosis of channel 1 0: (default) No failure detected 1: Over Temperature or Over Load
0	ERR0	r	Over Load / Over Temperature Diagnosis of channel 0 0: (default) No failure detected 1: Over Temperature or Over Load

10.6.2. Register structure

The register structure is as follow:

Table 10.4 Register structure - all registers (with the exclusion of PWM_CR0 and PWM_CR1)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field Name	r = 0 w = 1	r = 1 w = 0	ADDR						DATA							
			ADDR0				ADDR1									

Table 10.5 Register structure - PWM_CR0 and PWM_CR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field Name	r = 0 w = 1	r = 1 w = 0	ADDR0				DATA									

Table 10.6 Power output control register (REG_ADDR = 0x00)-OUT

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	OUT.OUT7	OUT.OUT6	OUT.OUT5	OUT.OUT4	OUT.OUT3	OUT.OUT2	OUT.OUT1	OUT.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.7 Power output control register description

Bit	Field Name	Type	Description
7	OUT.OUT7	r/w	0: (default) Channel 7 output is OFF 1: Channel 7 output is ON
6	OUT.OUT6	r/w	0: (default) Channel 6 output is OFF 1: Channel 6 output is ON
5	OUT.OUT5	r/w	0: (default) Channel 5 output is OFF 1: Channel 5 output is ON
4	OUT.OUT4	r/w	0: (default) Channel 4 output is OFF 1: Channel 4 output is ON
3	OUT.OUT3	r/w	0: (default) Channel 3 output is OFF 1: Channel 3 output is ON
2	OUT.OUT2	r/w	0: (default) Channel 2 output is OFF 1: Channel 2 output is ON
1	OUT.OUT1	r/w	0: (default) Channel 1 output is OFF 1: Channel 1 output is ON
0	OUT.OUT0	r/w	0: (default) Channel 0 output is OFF 1: Channel 0 output is ON

Table 10.8 Bulb Inrush Mode control register (REG_ADDR = 0x01)-BIM

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	BIM.OUT7	BIM.OUT6	BIM.OUT5	BIM.OUT4	BIM.OUT3	BIM.OUT2	BIM.OUT1	BIM.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.9 Bulb Inrush Mode register description

Bit	Field Name	Type	Description
7	BIM.OUT7	r/w	0: (default) Channel 7 output latches OFF in case of errors 1: Channel7 output restarts automatically in case of errors
6	BIM.OUT6	r/w	0: (default) Channel 6 output latches OFF in case of errors 1: Channel6 output restarts automatically in case of errors
5	BIM.OUT5	r/w	0: (default) Channel 5 output latches OFF in case of errors 1: Channel5 output restarts automatically in case of errors
4	BIM.OUT4	r/w	0: (default) Channel 4 output latches OFF in case of errors 1: Channel4 output restarts automatically in case of errors
3	BIM.OUT3	r/w	0: (default) Channel 3 output latches OFF in case of errors 1: Channel3 output restarts automatically in case of errors
2	BIM.OUT2	r/w	0: (default) Channel 2 output latches OFF in case of errors 1: Channel2 output restarts automatically in case of errors
1	BIM.OUT1	r/w	0: (default) Channel 1 output latches OFF in case of errors

			1: Channel1 output restarts automatically in case of errors
0	BIM.OUT0	r/w	0: (default) Channel 0 output latches OFF in case of errors 1: Channel0 output restarts automatically in case of errors

Table 10.10 Input Mapping (Input Pin 0) register (REG_ADDR = 0x04)-MAPIN0

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	MAPIN0. OUT7	MAPIN0. OUT6	MAPIN0. OUT5	MAPIN0. OUT4	MAPIN0. OUT3	MAPIN0. OUT2	MAPIN0. OUT1	MAPIN0. OUT0
Default	0	0	0	0	0	1	0	0

Table 10.11 Input Mapping (Input Pin 0) register description

Bit	Field Name	Type	Description
7	MAPIN0.OUT7	r/w	0: (default) Channel 7 output is not connected to the IN0 1: Channel 7 output is connected to the IN0
6	MAPIN0.OUT6	r/w	0: (default) Channel 6 output is not connected to the IN0 1: Channel 6 output is connected to the IN0
5	MAPIN0.OUT5	r/w	0: (default) Channel 5 output is not connected to the IN0 1: Channel 5 output is connected to the IN0
4	MAPIN0.OUT4	r/w	0: (default) Channel 4 output is not connected to the IN0 1: Channel 4 output is connected to the IN0
3	MAPIN0.OUT3	r/w	0: (default) Channel 3 output is not connected to the IN0 1: Channel 3 output is connected to the IN0
2	MAPIN0.OUT2	r/w	0: Channel 2 output is not connected to the IN0 1: (default) Channel 2 output is connected to the IN0
1	MAPIN0.OUT1	r/w	0: (default) Channel 1 output is not connected to the IN0 1: Channel 1 output is connected to the IN0
0	MAPIN0.OUT0	r/w	0: (default) Channel 0 output is not connected to the IN0 1: Channel 0 output is connected to the IN0

Table 10.12 Input Mapping (Input Pin 1) register (REG_ADDR = 0x05) -MAPIN1

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	MAPIN1. OUT7	MAPIN1. OUT6	MAPIN1. OUT5	MAPIN1. OUT4	MAPIN1. OUT3	MAPIN1. OUT2	MAPIN1. OUT1	MAPIN1. OUT0
Default	0	0	0	0	1	0	0	0

Table 10.13 Input Mapping (Input Pin 1) register description

Bit	Field Name	Type	Description
7	MAPIN1.OUT7	r/w	0: (default) Channel 7 output is not connected to the IN1 1: Channel 7 output is connected to the IN1
6	MAPIN1.OUT6	r/w	0: (default) Channel 6 output is not connected to the IN1 1: Channel 6 output is connected to the IN1
5	MAPIN1.OUT5	r/w	0: (default) Channel 5 output is not connected to the IN1 1: Channel 5 output is connected to the IN1

4	MAPIN1.OUT4	r/w	0: (default) Channel 4 output is not connected to the IN1 1: Channel 4 output is connected to the IN1
3	MAPIN1.OUT3	r/w	0: Channel 3 output is not connected to the IN1 1: (default) Channel 3 output is connected to the IN1
2	MAPIN1.OUT2	r/w	0: (default) Channel 2 output is not connected to the IN1 1: Channel 2 output is connected to the IN1
1	MAPIN1.OUT1	r/w	0: (default) Channel 1 output is not connected to the IN1 1: Channel 1 output is connected to the IN1
0	MAPIN1.OUT0	r/w	0: (default) Channel 0 output is not connected to the IN1 1: Channel 0 output is connected to the IN1

Table 10.14 Input Status Monitor register (REG_ADDR = 0x06)-ISM

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TER	reserved	reserved	reserved	reserved	reserved	IN1	IN0
Default	1	0	0	0	0	0	0	0

Table 10.15 Input Status Monitor register description

Bit	Field Name	Type	Description
7	TER	r	0: Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1: (default) Previous transmission failed
6	reserved	r	0: reserved (default value)
5	reserved	r	0: reserved (default value)
4	reserved	r	0: reserved (default value)
3	reserved	r	0: reserved (default value)
2	reserved	r	0: reserved (default value)
1	IN1	r	0: (default) The input pin is set to “low” 1: The input pin is set to “high”
0	IN0	r	0: (default) The input pin is set to “low” 1: The input pin is set to “high”

Table 10.16 Open Load diagnostic current control register (REG_ADDR = 0x08) -DIAG_IOL

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	IOL.OUT7	IOL.OUT6	IOL.OUT5	IOL.OUT4	IOL.OUT3	IOL.OUT2	IOL.OUT1	IOL.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.17 Open Load diagnostic current control register description

Bit	Field Name	Type	Description
7	IOL.OUT7	r/w	0: (default) Channel 7 diagnosis current not enabled

			1: Channel 7 diagnosis current enabled
6	IOL.OUT6	r/w	0: (default) Channel 6 diagnosis current not enabled 1: Channel 6 diagnosis current enabled
5	IOL.OUT5	r/w	0: (default) Channel 5 diagnosis current not enabled 1: Channel 5 diagnosis current enabled
4	IOL.OUT4	r/w	0: (default) Channel 4 diagnosis current not enabled 1: Channel 4 diagnosis current enabled
3	IOL.OUT3	r/w	0: (default) Channel 3 diagnosis current not enabled 1: Channel 3 diagnosis current enabled
2	IOL.OUT2	r/w	0: (default) Channel 2 diagnosis current not enabled 1: Channel 2 diagnosis current enabled
1	IOL.OUT1	r/w	0: (default) Channel 1 diagnosis current not enabled 1: Channel 1 diagnosis current enabled
0	IOL.OUT0	r/w	0: (default) Channel 0 diagnosis current not enabled 1: Channel 0 diagnosis current enabled

Table 10.18 Output Status Monitor register (REG_ADDR = 0x09) -DIAG_OSM

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DIAG_OSM.OUT7	DIAG_OSM.OUT6	DIAG_OSM.OUT5	DIAG_OSM.OUT4	DIAG_OSM.OUT3	DIAG_OSM.OUT2	DIAG_OSM.OUT1	DIAG_OSM.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.19 Output Status Monitor register description

Bit	Field Name	Type	Description
7	DIAG_OSM.OUT7	r	0: (default) Channel 7 VDS > VDS(OL) 1: Channel 7 VDS < VDS(OL)
6	DIAG_OSM.OUT6	r	0: (default) Channel 6 VDS > VDS(OL) 1: Channel 6 VDS < VDS(OL)
5	DIAG_OSM.OUT5	r	0: (default) Channel 5 VDS > VDS(OL) 1: Channel 5 VDS < VDS(OL)
4	DIAG_OSM.OUT4	r	0: (default) Channel 4 VDS > VDS(OL) 1: Channel 4 VDS < VDS(OL)
3	DIAG_OSM.OUT3	r	0: (default) Channel 3 VDS > VDS(OL) 1: Channel 3 VDS < VDS(OL)
2	DIAG_OSM.OUT2	r	0: (default) Channel 2 VDS > VDS(OL) 1: Channel 2 VDS < VDS(OL)
1	DIAG_OSM.OUT1	r	0: (default) Channel 1 VDS > VDS(OL) 1: Channel 1 VDS < VDS(OL)
0	DIAG_OSM.OUT0	r	0: (default) Channel 0 VDS > VDS(OL) 1: Channel 0 VDS < VDS(OL)

Table 10.20 Open Load at ON Monitor register (REG_ADDR = 0x0A) - DIAG_OPL_ON

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DIAG_OPL_ON.OUT7	DIAG_OPL_ON.OUT6	DIAG_OPL_ON.OUT5	DIAG_OPL_ON.OUT4	DIAG_OPL_ON.OUT3	DIAG_OPL_ON.OUT2	DIAG_OPL_ON.OUT1	DIAG_OPL_ON.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.21 Open Load at ON Monitor register description

This feature is active only on High-Side channels and auto configurable channels used as High-Side switches

Bit	Field Name	Type	Description
7	DIAG_OPL_ON.OUT7	r	0: (default) Channel 7 normal operation or diagnosis performed on channel 7 OFF 1: Channel 7 Open Load at ON detected
6	DIAG_OPL_ON.OUT6	r	0: (default) Channel 6 normal operation or diagnosis performed on channel 6 OFF 1: Channel 6 Open Load at ON detected
5	DIAG_OPL_ON.OUT5	r	0: (default) Channel 5 normal operation or diagnosis performed on channel 5 OFF 1: Channel 5 Open Load at ON detected
4	DIAG_OPL_ON.OUT4	r	0: (default) Channel 4 normal operation or diagnosis performed on channel 4 OFF 1: Channel 4 Open Load at ON detected
3	DIAG_OPL_ON.OUT3	r	0: (default) Channel 3 normal operation or diagnosis performed on channel 3 OFF 1: Channel 3 Open Load at ON detected
2	DIAG_OPL_ON.OUT2	r	0: (default) Channel 2 normal operation or diagnosis performed on channel 2 OFF 1: Channel 2 Open Load at ON detected
1	DIAG_OPL_ON.OUT1	r	0: (default) Channel 1 normal operation or diagnosis performed on channel 1 OFF 1: Channel 1 Open Load at ON detected
0	DIAG_OPL_ON.OUT0	r	0: (default) Channel 0 normal operation or diagnosis performed on channel 0 OFF 1: Channel 0 Open Load at ON detected

Table 10.22 Open Load at ON diagnostic control register (REG_ADDR = 0x0B) - DIAG_OPL_ONEN

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	reserved	reserved	reserved	reserved	DIAG_OPL_ONEN.MUX			
Default	0	0	0	0	1	1	1	1

Table 10.23 Open Load at ON diagnostic control register description

This feature is active only on High-Side channels and auto configurable channels used as High-Side switches

Bit	Field Name	Type	Description
7	reserved	r/w	reserved
6	reserved	r/w	reserved
5	reserved	r/w	reserved
4	reserved	r/w	reserved
3:0	DIAG_OPL_ONEN.MUX	r/w	0000_B Open Load at ON diagnostic active on channel 0 0001_B Open Load at ON diagnostic active on channel 1 0010_B Open Load at ON diagnostic active on channel 2 0011_B Open Load at ON diagnostic active on channel 3 0100_B Open Load at ON diagnostic active on channel 4 0101_B Open Load at ON diagnostic active on channel 5 0110_B Open Load at ON diagnostic active on channel 6 0111_B Open Load at ON diagnostic active on channel 7 1000_B (reserved) 1001_B (reserved) 1010_B Open Load at ON diagnosis loop start 1011_B (reserved) 1100_B (reserved) 1101_B (reserved) 1110_B (reserved) 1111_B (default) Open Load at ON diagnostic not active

Table 10.24 Hardware Configuration Register (REG_ADDR = 0x0C) -HWCR

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	ACT	RST	reserved	reserved	PAR3	PAR2	PAR1	PAR0
Default	0	0	0	0	0	0	0	0

Table 10.25 Hardware Configuration Register description

Bit	Field Name	Type	Description
7	ACT	r/w	0: (default) Normal operation or device leaves Active Mode 1: Device enters Active Mode
6	RST	r/w	0: (default) Normal operation 1: Execute Reset command (self-clearing)
5	reserved	r/w	0: reserved (default value)
4	reserved	r/w	0: reserved (default value)
3	PAR3	r/w	0: (default) Channel 7 and channel 5 Normal operation 1: Channel 7 and channel 5 have Over Load and Over Temperature synchronized
2	PAR2	r/w	0: (default) Channel 6 and channel 4 Normal operation 1: Channel 6 and channel 4 have Over Load and Over Temperature synchronized

1	PAR1	r/w	0: (default) Channel 3 and channel 1 Normal operation 1: Channel 3 and channel 1 have Over Load and Over Temperature synchronized
0	PAR0	r/w	0: (default) Channel 2 and channel 0 Normal operation 1: Channel 2 and channel 0 have Over Load and Over Temperature synchronized

Table 10.26 Clear Output Error Latch Register (REG_ADDR = 0x0D) -COEL

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	COEL.OUT7	COEL.OUT6	COEL.OUT5	COEL.OUT4	COEL.OUT3	COEL.OUT2	COEL.OUT1	COEL.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.27 Clear Output Error Latch Register description

Bit	Field Name	Type	Description
7	COEL.OUT7	r/w	0: (default) Channel 7 Normal operation 1: Clear the error latch for the channel 7
6	COEL.OUT6	r/w	0: (default) Channel 6 Normal operation 1: Clear the error latch for the channel 6
5	COEL.OUT5	r/w	0: (default) Channel 5 Normal operation 1: Clear the error latch for the channel 5
4	COEL.OUT4	r/w	0: (default) Channel 4 Normal operation 1: Clear the error latch for the channel 4
3	COEL.OUT3	r/w	0: (default) Channel 3 Normal operation 1: Clear the error latch for the channel 3
2	COEL.OUT2	r/w	0: (default) Channel 2 Normal operation 1: Clear the error latch for the channel 2
1	COEL.OUT1	r/w	0: (default) Channel 1 Normal operation 1: Clear the error latch for the channel 1
0	COEL.OUT0	r/w	0: (default) Channel 0 Normal operation 1: Clear the error latch for the channel 0

Table 10.28 PWM Configuration Register (REG_ADDR = 0x0E) – HWCR_PWM

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	HWCR_PWM.ADJ				reserved	reserved	HWCR_PWM.PWM1	HWCR_PWM.PWM0
Default	1	0	0	0	0	0	0	0

Table 10.29 PWM Configuration Register description

This feature is active only on auto-configuration channels used as high side switches.

Bit	Field Name	Type	Description
7:4	HWCR_PWM.ADJ	r/w	0000_B (reserved) 0001_B base frequency f_{INT} - 37.2% 0010_B base frequency f_{INT} - 31.9% 0011_B base frequency f_{INT} - 26.9% 0100_B base frequency f_{INT} - 21.0% 0101_B base frequency f_{INT} - 15.5% 0110_B base frequency f_{INT} - 10.9% 0111_B base frequency f_{INT} - 5.8% 1000_B (default) base frequency f_{INT} 1001_B base frequency f_{INT} + 4.3% 1010_B base frequency f_{INT} + 8.9% 1011_B base frequency f_{INT} + 14.0% 1100_B base frequency f_{INT} + 19.5% 1101_B base frequency f_{INT} + 25.6% 1110_B base frequency f_{INT} + 32.4% 1111_B base frequency f_{INT} + 40.0%
3	reserved	r/w	reserved
2	reserved	r/w	reserved
1	HWCR_PWM.PWM1	r/w	0: (default) PWM Generator 1 not active 1: PWM Generator 1 active
0	HWCR_PWM.PWM0	r/w	0: (default) PWM Generator 0 not active 1: PWM Generator 0 active

Table 10.30 PWM Generator Configuration 0 Register (REG_ADDR0 = $0x0100_B$)- PWM_CR0

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM_CR0.FREQ		PWM_CR0.DC							
Default	0	0	0	0	0	0	0	0	0	0

Table 10.31 PWM Generator Configuration 0 Register

Bit	Field Name	Type	Description
9:8	PWM_CR0.FREQ	r/w	00_B (default) internal clock divided by 1024 01_B internal clock divided by 512 10_B internal clock divided by 256 11_B 100% duty cycle
7:0	PWM_CR0.DC	r/w	(resolution: 0.39%) 00000000_B, PWM generator is OFF 11111111_B, PWM generator is ON (99.61% duty cycle)

Table 10.32 PWM Generator Configuration 1 Register (REG_ADDR0 = $0x0101_B$)- PWM_CR1

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM_CR1.FREQ		PWM_CR1.DC							
Default	0	0	0	0	0	0	0	0	0	0

Table 10.33 PWM Generator Configuration 1 Register

Bit	Field Name	Type	Description
9:8	PWM_CR1.FREQ	r/w	00_B (default) internal clock divided by 1024 01_B internal clock divided by 512 10_B internal clock divided by 256 11_B 100% duty cycle
7:0	PWM_CR1.DC	r/w	(resolution: 0.39%) 00000000_B, PWM generator is OFF 11111111_B, PWM generator is ON (99.61% duty cycle)

Table 10.34 PWM Generator Output Control Register (REG_ADDR = 0x24) - PWM_OUT

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM_OUT.OUT7	PWM_OUT.OUT6	PWM_OUT.OUT5	PWM_OUT.OUT4	PWM_OUT.OUT3	PWM_OUT.OUT2	PWM_OUT.OUT1	PWM_OUT.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.35 PWM Generator Output Control Register description

Bit	Field Name	Type	Description
7	PWM_OUT.OUT7	r/w	0: (default) channel 7 is not driven by one of the two PWM Generators 1: channel 7 is connected to a PWM Generator
6	PWM_OUT.OUT6	r/w	0: (default) channel 6 is not driven by one of the two PWM Generators 1: channel 6 is connected to a PWM Generator
5	PWM_OUT.OUT5	r/w	0: (default) channel 5 is not driven by one of the two PWM Generators 1: channel 5 is connected to a PWM Generator
4	PWM_OUT.OUT4	r/w	0: (default) channel 4 is not driven by one of the two PWM Generators 1: channel 4 is connected to a PWM Generator
3	PWM_OUT.OUT3	r/w	0: (default) channel 3 is not driven by one of the two PWM Generators 1: channel 3 is connected to a PWM Generator
2	PWM_OUT.OUT2	r/w	0: (default) channel 2 is not driven by one of the two PWM Generators 1: channel 2 is connected to a PWM Generator
1	PWM_OUT.OUT1	r/w	0: (default) channel 1 is not driven by one of the two PWM Generators 1: channel 1 is connected to a PWM Generator
0	PWM_OUT.OUT0	r/w	0: (default) channel 0 is not driven by one of the two PWM Generators 1: channel 0 is connected to a PWM Generator

Table 10.36 PWM Generator Output Mapping Register (REG_ADDR = 0x25) - PWM_MAP

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM_MAP.OUT7	PWM_MAP.OUT6	PWM_MAP.OUT5	PWM_MAP.OUT4	PWM_MAP.OUT3	PWM_MAP.OUT2	PWM_MAP.OUT1	PWM_MAP.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.37 PWM Generator Output Mapping Register description

Bit	Field Name	Type	Description
7	PWM_MAP.OUT7	r/w	0: (default) The selected output is connected to PWM Generator 0 1: The selected output is connected to PWM Generator 1
6	PWM_MAP.OUT6	r/w	0: (default) The selected output is connected to PWM Generator 0 1: The selected output is connected to PWM Generator 1
5	PWM_MAP.OUT5	r/w	0: (default) The selected output is connected to PWM Generator 0 1: The selected output is connected to PWM Generator 1
4	PWM_MAP.OUT4	r/w	0: (default) The selected output is connected to PWM Generator 0 1: The selected output is connected to PWM Generator 1
3	PWM_MAP.OUT3	r/w	0: (default) The selected output is connected to PWM Generator 0 1: The selected output is connected to PWM Generator 1
2	PWM_MAP.OUT2	r/w	0: (default) The selected output is connected to PWM Generator 0 1: The selected output is connected to PWM Generator 1
1	PWM_MAP.OUT1	r/w	0: (default) The selected output is connected to PWM Generator 0 1: The selected output is connected to PWM Generator 1
0	PWM_MAP.OUT0	r/w	0: (default) The selected output is connected to PWM Generator 0 1: The selected output is connected to PWM Generator 1

10.6.3. SPI command quick list

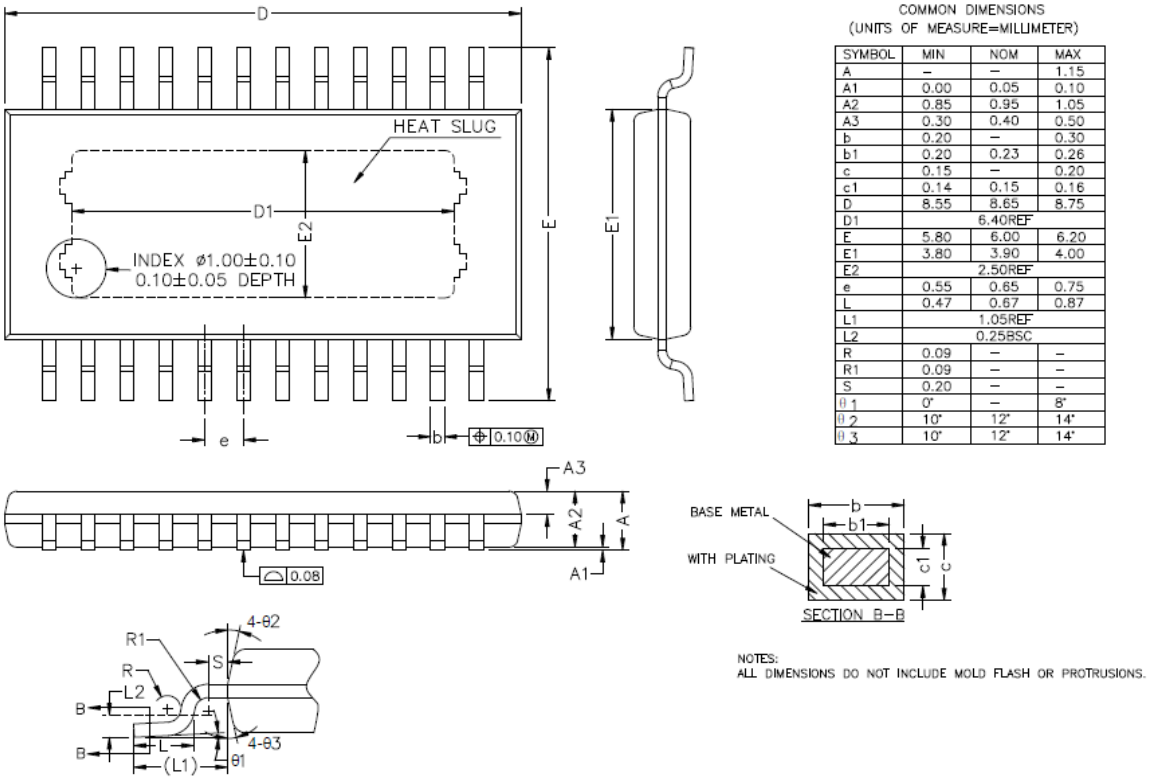
A summary of the most used SPI commands (read and write operations on all registers) is shown in **Table 10.38**

Table 10.38 SPI command quick list

Register	“read” command	“write” command	content written
OUT	4002_H	$80XX_H$	XX_H = xxxxxxxx$_B$
BIM	4102_H	$81XX_H$	XX_H = xxxxxxxx$_B$
MAPIN0	4402_H	$84XX_H$	XX_H = xxxxxxxx$_B$
MAPIN1	4502_H	$85XX_H$	XX_H = xxxxxxxx$_B$
ISM	4602_H	n.a. (read-only)	–
DIAG_IOL	4802_H	$88XX_H$	XX_H = xxxxxxxx$_B$
DIAG_OSM	4902_H	n.a. (read-only)	–
DIAG_OPL_ON	$4A02_H$	n.a. (read-only)	–
DIAG_OPL_ONEN	$4B02_H$	$8BXX_H$	XX_H = xxxxxxxx$_B$

HWCR	$4C02_H$	$8CXX_H$	XX_H = $xxxxxxxx_B$
COEL	$4D02_H$	$8DXX_H$	XX_H = $xxxxxxxx_B$
HWCR_PWM	$4E02_H$	$8EXX_H$	XX_H = $xxxxxxxx_B$
PWM_CR0	5002_H	$90XX_H$	$0XX_H$ = $00xxxxxxx_B$
		$91XX_H$	$1XX_H$ = $01xxxxxxx_B$
		$92XX_H$	$2XX_H$ = $10xxxxxxx_B$
		$93XX_H$	$3XX_H$ = $11xxxxxxx_B$
PWM_CR1	5402_H	$94XX_H$	$0XX_H$ = $00xxxxxxx_B$
		$95XX_H$	$1XX_H$ = $01xxxxxxx_B$
		$96XX_H$	$2XX_H$ = $10xxxxxxx_B$
		$97XX_H$	$3XX_H$ = $11xxxxxxx_B$
PWM_OUT	6402_H	$A4XX_H$	XX_H = $xxxxxxxx_B$
PWM_MAP	6502_H	$A5XX_H$	XX_H = $xxxxxxxx_B$

11. Package Information

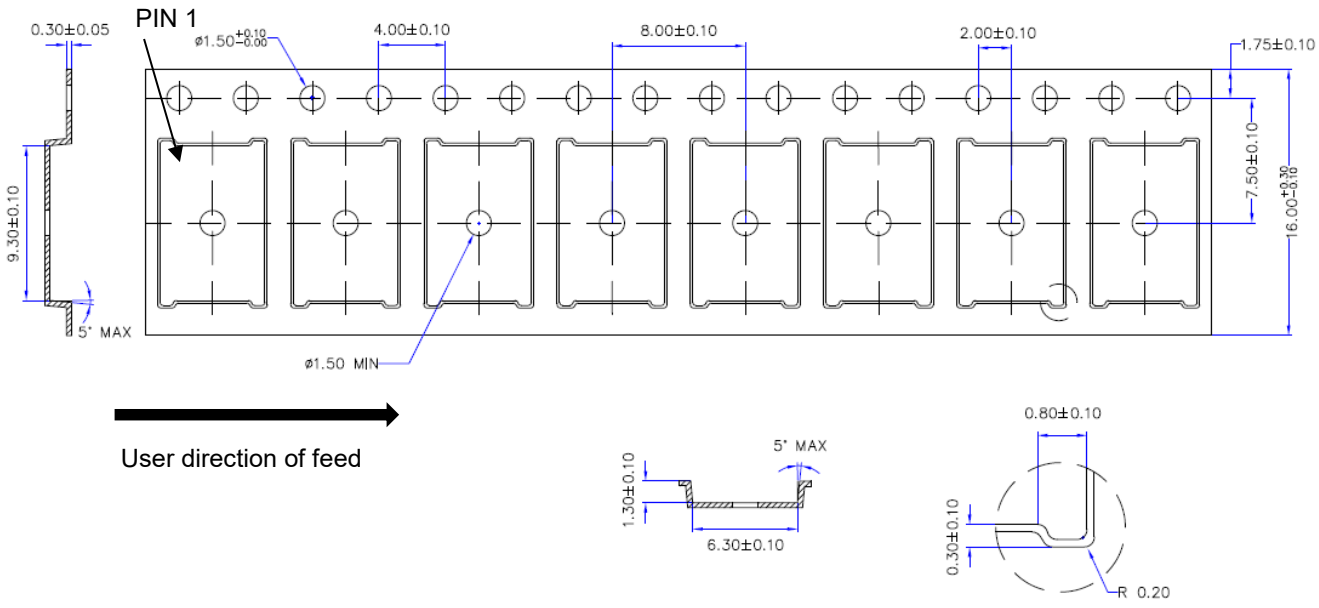


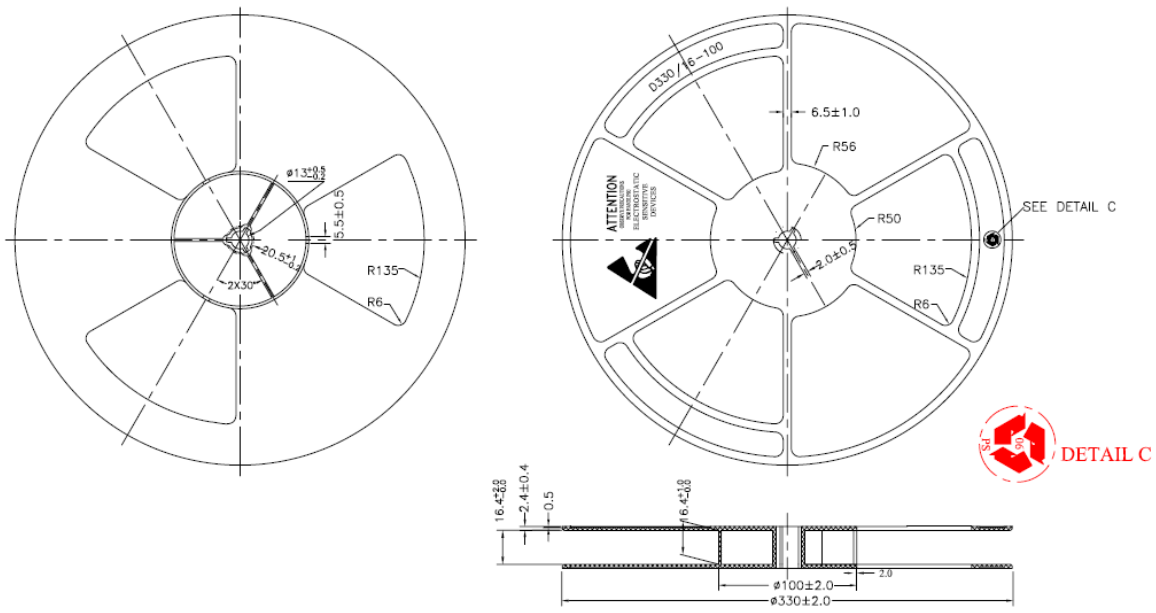
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.15
A1	0.00	0.05	0.10
A2	0.85	0.95	1.05
A3	0.30	0.40	0.50
b	0.20	–	0.30
b1	0.20	0.23	0.26
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	8.55	8.65	8.75
D1		6.40REF	
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2		2.50REF	
e	0.55	0.65	0.75
L	0.47	0.67	0.87
L1		1.05REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

12. Tape and Reel Information

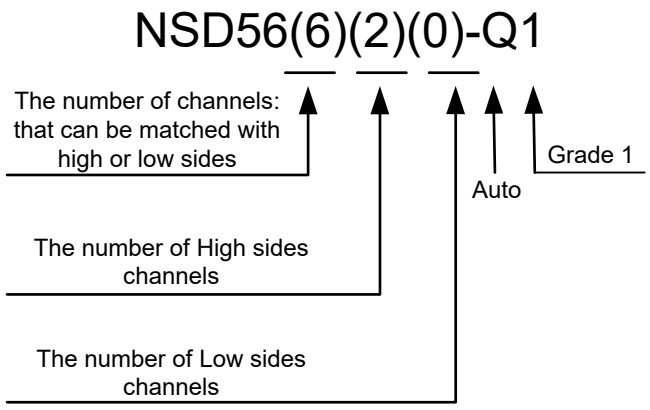



ø13*0.5
5.5±0.5
20.5*1
2X30°
R135
R6
D330/6-100
6.5±1.0
R56
R50
SEE DETAIL C
2.0±0.5
R135
R6
ATTENTION
DETAIL C
16.4+2.0 -0.0
2.4±0.4
0.5
16.4+1.0 -0.0
2.0
ø100±2.0
ø330±2.0

13. Ordering Information

Part Number	Package Type	Temperature	Output State	MSL	SPQ
NSD56620-Q1HTSBR	HTSOP24	-40 to 125°C	2 HSD + 6 auto-configurable HSD/LSD	3	4000
Note: All packages are RoHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature					

Part Number Rule:



14. Revision History

Revision	Description	Date
1.0	Initial version	2025/9/17

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