

Product Overview

The NSD3661/NSD3662 is a 3*N-channel MOSFET driver which targets driving MOSFETs used in phase-isolation application, but also can be used as a high/low side MOSFET driver. The device integrates three independent floating gate drivers to turn on/off MOSFETs even when the phase voltage slew rate is high. A two-stage charge pump in the device provides stable voltage for gate drivers over full supply voltage range.

In NSD3661 three independent gate drives are controlled by three input signals independently when device is supplied correctly (NSD3661 has no sleep mode). In NSD3662 three independent gate drives are controlled to turn on/off at the same time after the device enters normal mode.

The device has undervoltage monitors for PVDD, VCP and VGS to ensure MOSFETs in safe conducting state. (VGS UV and VCP UV only for NSD3662)

Key Features

- AEC Q-100 Grade 1 Qualified
- 3 floating gate drivers for N-channel MOSFET:
 - Fixed turn on/off current and timing
 - 4.5V to 50V operating range
- Integrated 2-stage charge-pump with spread spectrum
 - Support 0% to 100% PWM operation
 - Reverse protection MOSFET driver output
- Low current consumption in sleep mode (only for NSD3662)
- Protection and diagnostic:
 - Supply voltage monitor
 - Charge pump voltage monitor (VCP UV only for NSD3662)
 - Gate driver monitor (VGS UV Fault only for NSD3662)

- RoHS & REACH Compliance

Applications

- Electric power steering (EPS)
- Electric braking
- 3-phase solid-state relay driver
- 3-high/low side MOSFET driver

Device Information

Part Number	Package	Body Size
NSD3661-Q1HTSPR	HTSSOP16	5.00 × 4.40mm
NSD3662-Q1HTSPR	HTSSOP16	5.00 × 4.40mm

Functional Block Diagrams

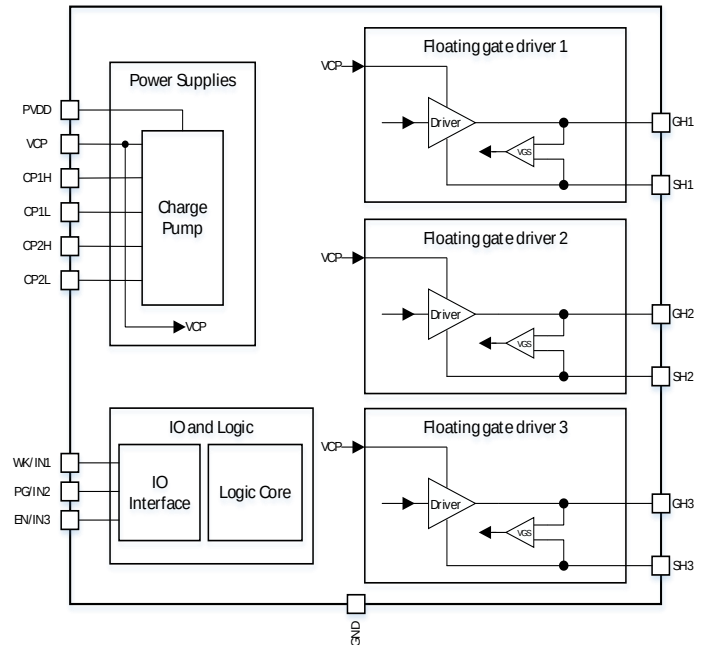


Figure 1 NSD3661/NSD3662 Block Diagram

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1. Pin Configuration and Functions

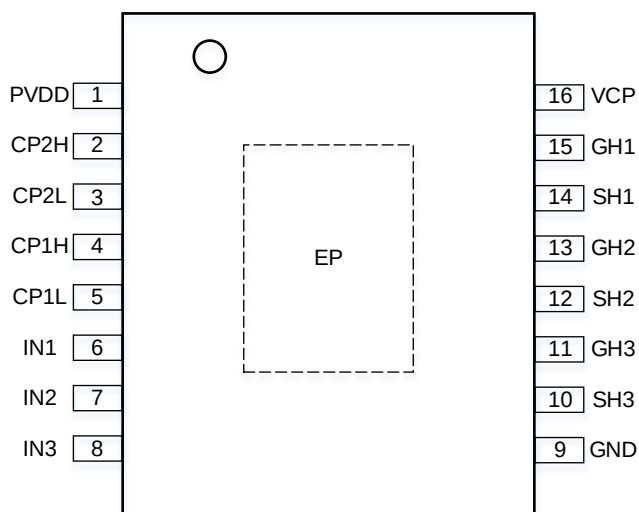


Figure 1.1 NSD3661 Pin-out

Table 1.1 NSD3661 Pin Configuration and Description

PIN NO.	Symbol	Function
1	PVDD	Device supply
2	CP2H	Positive connection for charge pump2
3	CP2L	Negative connection for charge pump2
4	CP1H	Positive connection for charge pump1
5	CP1L	Negative connection for charge pump1
6	IN1	Digital control input for floating gate driver1
7	IN2	Digital control input for floating gate driver2
8	IN3	Digital control input for floating gate driver3
9	GND	Device ground
10	SH3	Source terminal for floating gate driver3
11	GH3	Gate terminal for floating gate driver3
12	SH2	Source terminal for floating gate driver2
13	GH2	Gate terminal for floating gate driver2
14	SH1	Source terminal for floating gate driver1
15	GH1	Gate terminal for floating gate driver1
16	VCP	Charge pump output
	EP	Exposed pad, suggest connecting to GND for better EMC and thermal performance

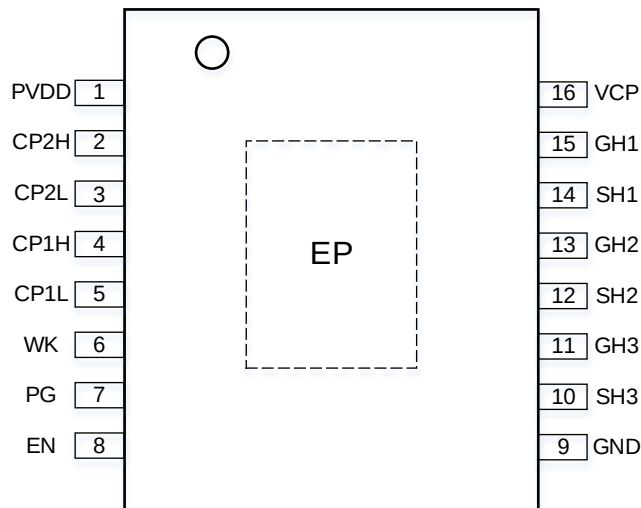


Figure 1.2 NSD3662 Pin-out

Table 1.2 NSD3662 Pin Configuration and Description

PIN NO.	Symbol	Function
1	PVDD	Device supply
2	CP2H	Positive connection for charge pump2
3	CP2L	Negative connection for charge pump2
4	CP1H	Positive connection for charge pump1
5	CP1L	Negative connection for charge pump1
6	WK	Digital control input for device activation, suggest being ignition/wake up input
7	PG	Digital control input for device activation, suggest being system supply OK input
8	EN	Digital control input for floating gate driver enables, also as fault indication pin by internal open drain structure
9	GND	Device ground
10	SH3	Source terminal for floating gate driver3
11	GH3	Gate terminal for floating gate driver3
12	SH2	Source terminal for floating gate driver2
13	GH2	Gate terminal for floating gate driver2
14	SH1	Source terminal for floating gate driver1
15	GH1	Gate terminal for floating gate driver1
16	VCP	Charge pump output
	EP	Exposed pad, suggest connecting to GND for better EMC and thermal performance

2. Absolute Maximum Ratings

Parameters	Symbol		Min	Typ	Max	Unit	Note
Gate driver power supply pin voltage (PVDD)	VPVDD		-0.3	-	50	V	
Charge pump output pin voltage (VCP)	VVCP		VPVDD-0.3	-	VPVDD+15	V	
Charge pump1 positive pin voltage (CP1H)	VCP1H		VPVDD-0.3	-	VVCP+0.6	V	
Charge pump2 positive pin voltage (CP2H)	VCP2H		VPVDD-0.6	-	VVCP+0.3	V	
Charge pump negative pin voltage (CP1L, CP2L)	VCP1L, VCP2L		-0.3	-	VPVDD+0.3	V	
Digital input pin voltage (IN1,IN2,IN3,WK,PG)	VINx		-0.3	-	50	V	
Digital input pin voltage (EN)	VEN		-0.3	-	50	V	<=1mA
Gate terminal voltage (GHx)	VGHx		-8	-	62	V	
Transient 1us voltage (GHx)			-14	-	62	V	
Voltage difference between GHx and SHx	VGHx-VSHx		-0.3	-	13.5	V	<=350mA
PVDD Voltage with respect to SH range	VPVDD-VSHx		-50		50	V	
VCP Voltage with respect to SH range	VCP-VSHx		-50		65	V	
Source terminal voltage (SHx)	VSHx		-8	-	50	V	
Transient 1us voltage (GHx)			-14	-	50	V	
Junction temperature	TJ		-40	-	150	°C	
Storage temperature	Tstg		-55	-	150	°C	

⁽¹⁾ All ratings are referenced to GND and valid in the absence of additional circuit operating constraints. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

3. ESD Ratings

<i>Parameters</i>	<i>Symbol</i>	<i>Note or Test Condition</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
Human Body Model(HBM), PVDD & SHx pins to GND ANSI/ESDA/JEDEC JS-001	VESDHBM1	HBM	-4	-	4	kV
Human Body Model(HBM), other pins per ANSI/ESDA/JEDEC JS-001	VESDHBM3	HBM	-2	-	-2	kV
Charged device model(CDM), Corner pin, per JEDEC specification JS-002	VESDCDM1	CDM	-750	-	750	V
Charged device model(CDM), other pins, per JEDEC specification JS-002	VESDCDM2	CDM	-500	-	500	V

4. Recommended Operating Conditions

<i>Parameters</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
Gate driver supply range for normal operation	VPVDD_nor	4.5		50	V
Gate driver extended Supply range; parameter deviations possible	VPVDD_ext	VPVDD_UV_H		50	V
Digital input range (IN1, IN2, IN3/WK, PG, EN)	VDIN_nor	0		50	V
Junction temperature range	TJ_nor	-40		150	°C

5. Thermal Information

<i>Parameters</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
IC Junction-to-Air Thermal Resistance	θ_{JA}		34		°C/W
Junction-to-case Thermal Resistance	θ_{JC}		2		°C/W

6. Specifications

6.1. Supply Voltage and Current Electrical Characteristics

4.5V ≤ VPVDD ≤ 50V, -40°C ≤ TJ ≤ 150°C, all voltages with respect to ground, positive current if flowing into pin.

Parameters	Symbol	Min	Typ	Max	Unit	Note or Test Condition
PVDD current in normal mode	IPVDD_Q			10	μA	VPVDD=12V (only in NSD3662)
	IPVDD1		6	9	mA	Gate drivers inactive, VPVDD=12V
	IPVDD2		11	15	mA	Gate drivers active, VPVDD=12V
	IPVDD3		50	75	mA	Gate drivers active, VPVDD=12V, ICP =12mA load
PVDD undervoltage threshold	VPVDD_UV_H	3.6	3.8	4	V	VPVDD rising threshold
	VPVDD_UV_L	3.4	3.6	3.8	V	VPVDD falling threshold
PVDD undervoltage hysteresis	VPVDD_UV_HYS		200		mV	
PVDD undervoltage delay time	tPVDD_UV	5	13	25	μs	The time delay from PVDD_UV to close drivers
Charge pump frequency without spread spectrum	fCP ⁽²⁾		400		kHz	
Charge pump voltage with respect to PVDD	VVCP-VPVDD	11	12	12.5	V	VPVDD >9V, ICP ≤1mA load
		10.5	11.5	12	V	6V < VPVDD ≤9V, ICP ≤1mA load
		7.5	8.5	9	V	4.5V ≤ VPVDD ≤6V, ICP ≤1mA load ⁽¹⁾
Spread spectrum modulation amplitude	fCP_MOD_RA ⁽³⁾		±10		%	
Charge pump undervoltage threshold respect to PVDD(for turn off driver)	VVCP_UV_H	6.4	6.7	7	V	Rising threshold
	VVCP_UV_L	6.3	6.5	6.9	V	Falling threshold
Charge pump undervoltage triggers EN fault threshold respect to PVDD(Only for NSD3662)	VVCP_UV_EN_H	7.3	7.8	8.3	V	Rising threshold
	VVCP_UV_EN_L	7	7.6	8	V	Falling threshold ⁽¹⁾
Charge pump undervoltage threshold hysteresis	VVCP_UV_HYS		200		mV	
Charge pump undervoltage filter time	tVCP_UV		12.5		μs	
Charge pump startup time	tVCP_up		300		μs	VCP-PVDD from 0% to 75%
Charge pump UV recover blanking time	tVCP_blank		100		μs	

Parameters	Symbol	Min	Typ	Max	Unit	Note or Test Condition
Device internal blocks startup time	twake			400	μs	The time taken to transition from Sleep Mode to Normal Mode

⁽¹⁾ In NSD3662, there is a possibility of reporting VGS_UV and VCP_UV, since VCP is close to VVCP_UV_EN_L threshold at PVDD=4.5V.

⁽²⁾ Not test covered, guaranteed by characterization.

⁽³⁾ Not test covered, guaranteed by design.

6.2. Input and Output Electrical Characteristics

4.5V ≤ VPVDD ≤ 50V, -40°C ≤ TJ ≤ 150°C, all voltages with respect to ground, positive current if flowing into pin.

Parameters	Symbol	Min	Typ	Max	Unit	Note or Test Condition
Input logic low voltage	VIL			0.8	V	IN1, IN2, IN3(NSD3661)/ WK, PG(NSD3662)
Input logic high voltage	VIH	2.0			V	IN1, IN2, IN3(NSD3661)/ WK, PG(NSD3662)
Input hysteresis	VIHYS	0.1			V	IN1, IN2, IN3(NSD3661)/ WK, PG(NSD3662)
EN, Input logic low voltage	VIL			0.4	V	EN(NSD3662)
EN, Input logic high voltage	VIH	0.7			V	EN(NSD3662)
EN Input hysteresis	VIHYS	0.1	0.2		V	EN(NSD3662)
EN regulated voltage	Vfault	0.9	1.0	1.1	V	I _{EN} =20uA~500uA
Internal pull down resistance	RPD		100		kΩ	IN1, IN2, IN3/WK, PG, EN(RPD1+RPD2)

6.3. Gate Driver Electrical Characteristics

4.5V ≤ VPVDD ≤ 50V, -40°C ≤ TJ ≤ 150°C, all voltages with respect to ground, positive current if flowing into pin.

Parameters	Symbol	Min	Typ	Max	Unit	Note or Test Condition
GHx output voltage low level	VGHx_L	0		0.3	V	Gate driver Active off, IGHx=1mA, VGHx-VSHx
GHx output voltage high level	VGHx_H	9	11	12.5	V	Gate driver Active on, VPVDD > 9V, VGHx-VSHx
		9	10.5	11.5	V	Gate driver Active on, 9V ≥ VPVDD > 6V, VGHx-VSHx
		7.2	7.8	9	V	Gate driver Active on, 6V ≥ VPVDD ≥ 4.5V, VGHx-VSHx
ISOURCE current	ISOURCE	8.5	10	12	mA	VGHx-VSHx=7V
IHOLD current	IHOLD		0.4		mA	VGHx-VSHx=7V
ISTRONG on resistance	ISTRONG		10		Ω	Tj=25°C, IGHx=10mA
			15		Ω	Tj=150°C, IGHx=10mA
Passive discharge path on resistance	Rpassive		950		kΩ	VGHx-VSHx=0.5V
			100		Ω	VGHx-VSHx=1.8V
Leakage current on SHx	ISHx	-2		2	μA	Gate driver x in passive off state, SHx ≤ PVDD
		-250		0	μA	Gate driver x in active off state, SHx ≤ PVDD
		-600		0	μA	Gate driver x in active on state, SHx ≤ PVDD
VGS comparator threshold for VGS UV fault	VGS_TH	6	7	8	V	Rising threshold
		5.5	6.5	7.5	V	Falling threshold ⁽¹⁾
VGS UV fault filter time	tGS_UV	3.7		18	μs	
Input propagation delay for turn on	tPD_rise			3	μs	ENx rising to GHx-SHx 20%
Input propagation delay for turn off	tPD_fall			2.25	μs	ENx falling to GHx-SHx 80%
TDRIVE time	TDRIVE	16	26	36	μs	
Internal system clock	fosc		14.4		MHz	

⁽¹⁾ In NSD3662, there is a possibility of reporting VGS_UV and VCP_UV, since VCP is close to VVCP_UV_EN_L threshold at PVDD=4.5V.

7. Function description

7.1. Power Supply

7.1.1.General Description

PVDD serves as a single supply for the device, it supplies internal voltage regulators for logic blocks, also charge pump for floating gate drivers.

It is recommended to put ceramic capacitors connected close to PVDD and ground plane.

VPVDD is monitored for under voltage.

7.1.2.Detailed Description

Vpdd Undervoltage Monitor

When $VPVDD < VPVDD_UV_L$ for longer than $tPVDD_UV$, device detects a PVDD undervoltage fault, then device will do following things:

- All gate drivers move to passive off state
 - Device move to sleep mode(NSD3662)/low power mode(NSD3661)
- After the fault is gone ($VPVDD > VPVDD_UV_H$ for longer than $tPVDD_UV$), two versions have different behavior:
- In NSD3661,
- Device moves to normal mode
 - Re-start charge pump
 - All gate drivers will re-work following current INx control input after $VVCP > VVCP_UV_H$ and $tvcp_blank$ delay
- In NSD3662,
- Device will still be in the sleep mode (after WK and PG both high, device will move to normal mode)

7.2. Charge Pump

7.2.1.General Description

The two-stage charge pump provides a stable voltage (VVCP) above VPVDD for gate drivers, external reverse protection circuit and so on. With stable voltage above VPVDD gate drivers can drive external N-channel MOSFET properly across a wide supply voltage range.

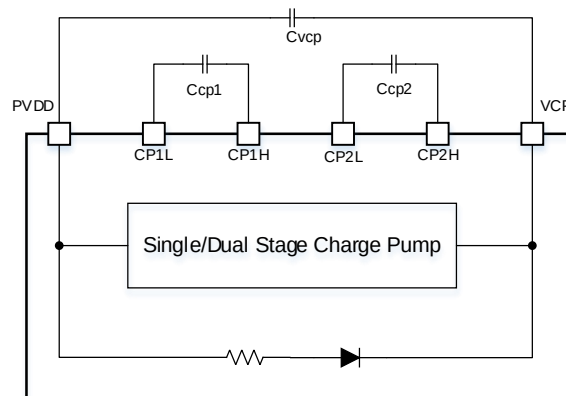


Figure 7.1 Charge Pump Block Diagram

7.2.2.Detailed Description

Frequency Modulation

The Charge pump clock has spread spectrum solution used to reduce the emission. The modulation has a $\pm 10\%$ range of fcp.

7.2.3.Vcp Undervoltage Monitor

- In NSD3661,
 - When $V_{VCP} < V_{VCP_UV_L}$ for longer than t_{VCP_UV} , device detects a VCP undervoltage fault.

After the fault happens, device will do following things:

 - All gate drivers move to passive off state
 - The charge pump keeps running

after $V_{VCP} > V_{VCP_UV_H}$ for longer than t_{VCP_UV} , device will do following things:

 - All gate drivers will re-work following current INx control input after tvcp_blank delay
 - In NSD3662,
 - When $V_{VCP} < V_{VCP_UV_EN_L}$, EN pin will be pulled to Vfault.

After $V_{VCP} > V_{VCP_UV_EN_H}$, device will release open drain structure in EN pin (EN pin voltage will set by external signal) after tvcp_blank delay.
 - When $V_{VCP} < V_{VCP_UV_L}$ for longer than t_{VCP_UV} , device detects a VCP undervoltage fault.

After the fault happens, device will do following things:

 - All gate drivers move to passive off state
 - EN pin will be pulled to Vfault
 - The charge pump keeps running

after $V_{VCP} > V_{VCP_UV_H}$ for longer than t_{VCP_UV} , device will do following things:

 - All gate drivers will re-work following current EN control input after tvcp_blank delay
- Note: During powerup after VCP UV not present, all gate drivers will follow control input after tvcp_blank.

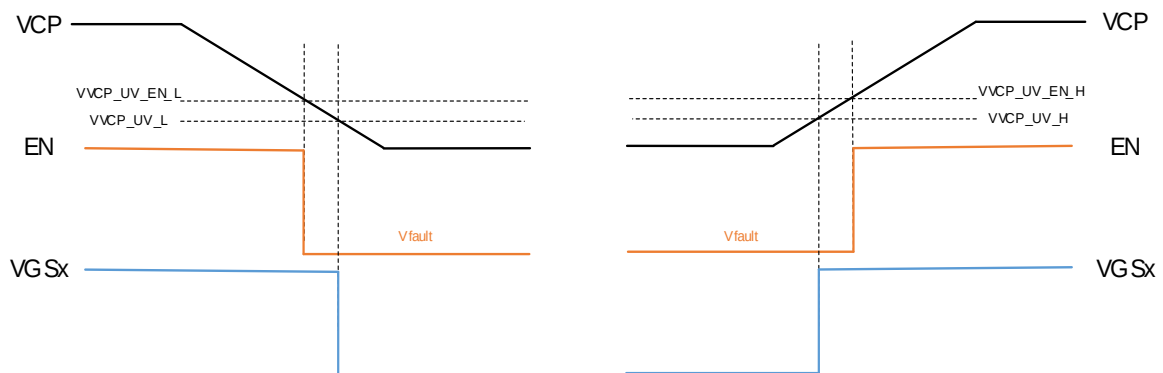


Figure 7.2 VCP undervoltage monitor (NSD3662)

Vcp Supplied By External Power

To improve VCP voltage robustness, device provide the possibility for external power to supply VCP, external VCP supply should also follow VCP pin AMR parameter ($VPVDD-0.3V \sim VPVDD+15V$), to limit current resistor in series is suggested.

7.3. Input and Output pins

7.3.1. Detailed Description

In1/Wk, In2/Pg

There is logic input IN1 and IN2 for NSD3661, WK and PG for NSD3662, also there is internal pull-down resistor RPD.

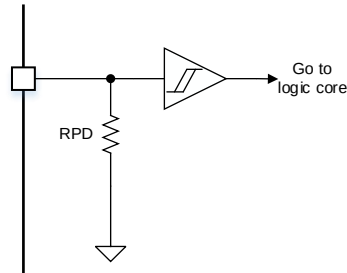


Figure 7.3 IN1/WK, IN2/PG Block Diagram

■ In NSD3661,

After the PVDD UV event is gone, device will start up and move to normal mode, in normal mode IN1 and IN2 will control floating gate driver1 and gate driver2.

■ In NSD3662,

Device will keep in sleep mode when WK or PG input is logic low, when WK and PG input are both logic high, device will start up and move to normal mode.

In3/En

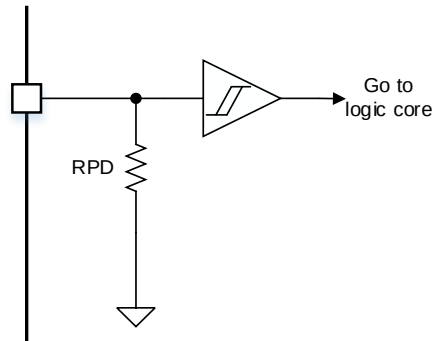


Figure 7.4 IN3 Block Diagram (NSD3661)

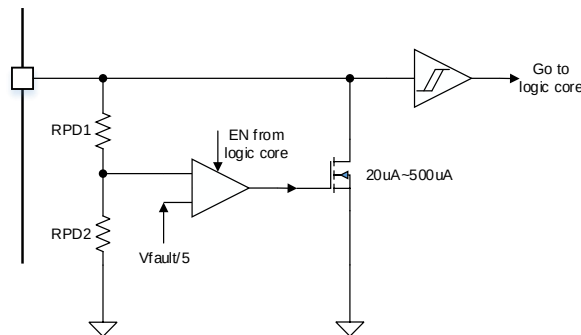


Figure 7.5 EN Block Diagram (NSD3662)

There is logic input IN3 for NSD3661 with internal pull-down resistor RPD, analog pin EN for NSD3662 with internal pull-down resistor RPD1 and RPD2.

■ In NSD3661,

- After the PVDD UV event is gone, device will start up and move to normal mode, in normal mode IN3 will control floating gate driver3.
- In NSD3662,
- In normal mode, EN pin will control all floating gate drivers together.
- The open-drain structure is only for fault conditions. The EN pin will be pulled to VFAULT when an error occurs.

Note: The EN pin should be pulled up with a pull-up resistor, the pull-up resistor should be set so that the current input to the EN pin is between 20uA-500uA, so that the EN pin is properly regulated to the Vfault voltage by the internal current source in the event of a fault.

7.4. Operation Mode

7.4.1. General Description

Device has three stable operation mode:

- Sleep mode, during sleep mode, all internal blocks will be in off state, gate drivers are in passive off state (only NSD3662 have sleep mode)
- Low power mode, external enabled signal present, but PVDD in under voltage state, only few internal blocks are active
- Normal mode, during normal mode, all blocks are in active state

- In NSD3661:

After the PVDD UV event is gone, device will start up and move to normal mode with twake delay (during twake device is starting up). When device meet PVDD UV event, device will move to low power mode directly.

Note: after device move to normal mode, gate driver will follow input logic to drive gate after tvcp_blank and VCP no UV.

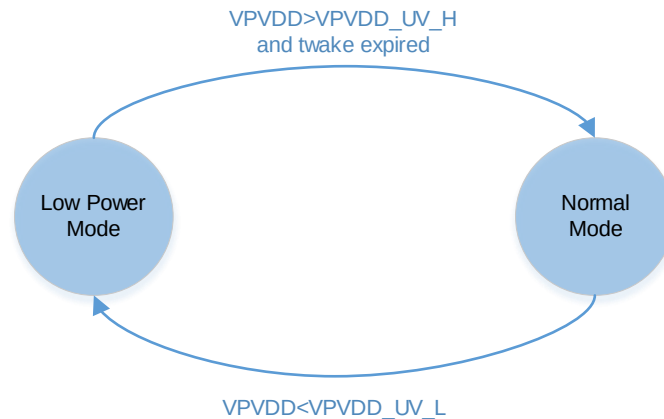


Figure 7.6 NSD3661 Operation Mode

- In NSD3662:

Device will keep in sleep mode when WK or PG input is logic low, when WK and PG both are logic high also PVDD UV event is gone, device will start up and move to normal mode with twake delay (during twake device is starting up).

If WK=PG is logic high, but device meet PVDD under voltage, device will move to low power mode with only few internal blocks are active.

Note: after device move to normal mode, gate driver will follow input logic to drive gate after tvcp_blank and VCP no UV.

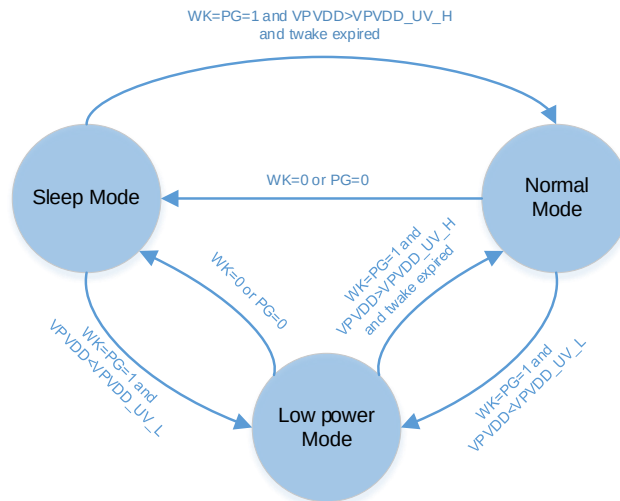


Figure 7.7 NSD3662 Operation Mode

7.5. Gate Driver

7.5.1.General Description

Gate driver block provides gate driver function and diagnostic.

Gate driver function:

- MOS turn on/off timing is fixed as below:

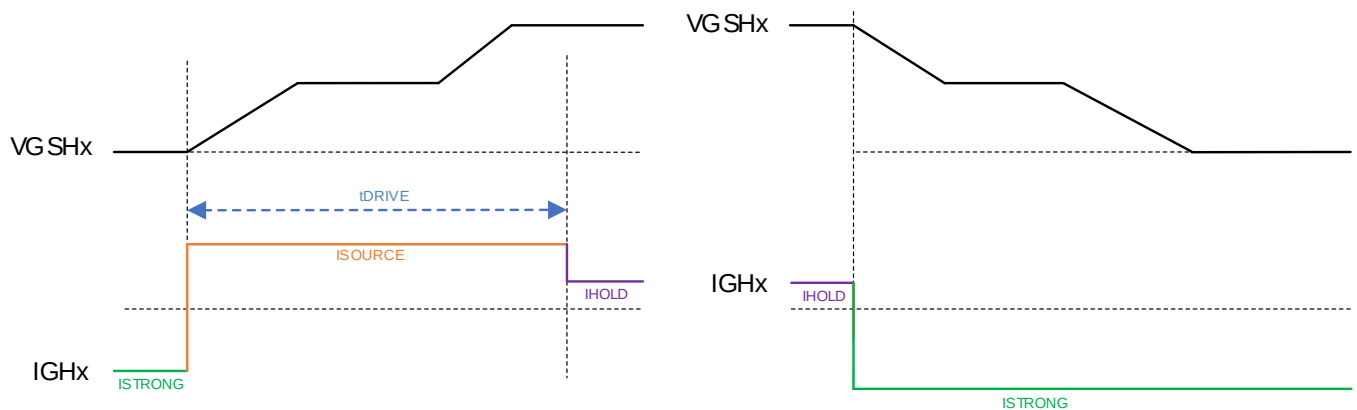


Figure 7.8 Driver Timing

Diagnostic:

- VGS monitors to detect VGS UV fault(Only for NSD3662, refer to 6.5.1.1)

7.5.2. Block Description

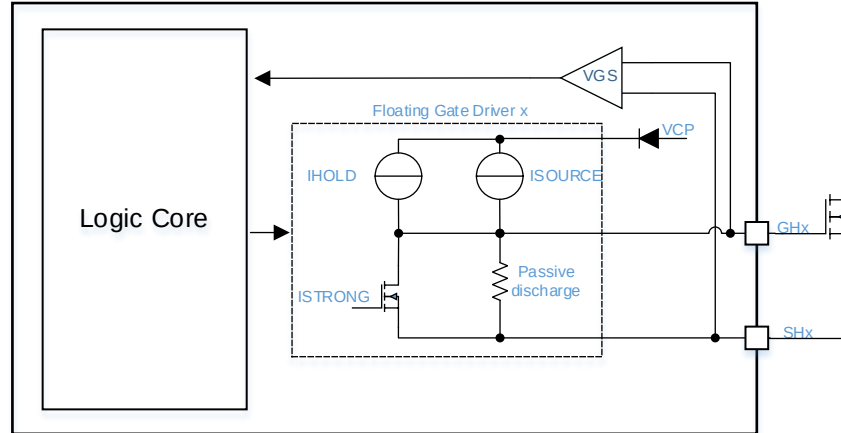


Figure 7.9 Gate Driver Block Diagram

- ISOURCE is current source to turn on external MOSFET.
- IHOLD is current source to maintain external MOSFET in on state after ISOURCE phase, this state called active on state.
- ISTRONG is internal switch to turn off external MOSFET, this state called active off state
- Passive discharge is passive discharge path to keep external MOSFET off when device in sleep mode or unsupplied, this state called passive off state
- VGS comparator to check VGS status compared to threshold to check whether VGS voltage in valid range with filter time after tDRIVE (VGS fault monitor).
- Below table is summary for static operation state of different blocks

Table 7.1 NSD3661 Gate Driver Internal Blocks Operation State Table

Mode	INx	IHOLD in gate driver x	ISTRONG in gate driver x	Passive Discharge in gate driver x	VGS Comparator in gate driver x	States
Low power mode	X	OFF	OFF	Active	OFF	Passive off
Normal mode	0	OFF	Active	OFF	OFF	Active off
Normal mode	1	Active	OFF	OFF	Active	Active on

Table 7.2 NSD3662 Gate Driver Internal Blocks Operation State Table

Mode	PVDD_UV	WK and PG	EN	IHOLD in all gate drivers	ISTRONG in all gate drivers	Passive Discharge in all gate drivers	VGS Comparator in all gate drivers	States
Low power mode	1	1	X	OFF	OFF	Active	OFF	Passive off
Sleep mode	X	0	X	OFF	OFF	Active	OFF	Passive off
Normal mode	0	1	0	OFF	Active	OFF	OFF	Active off
Normal mode	0	1	1	Active	OFF	OFF	Active	Active on

7.5.3.Diagnostic Description

Vgs Uv Monitor

After MOSFET is turned on (during TDRIVE VGS comparator output is ignored), if VGS of MOSFET is lower than VGS_TH for longer than tGS_UV during MOSFET is active on, device will detect VGS UV fault, the fault reaction as below.

- In NSD3661, the VGS UV fault does not change the driver output status.
- In NSD3662,

After the fault happens, device will do following things:

- EN pin will be pulled to Vfault
- All gate drivers and charge pump keep running

After VGS of MOSFET higher than VGS_TH for longer than tGS_UV again, device will do following things:

- Release open drain structure in EN pin (EN pin voltage will set by external signal)

7.6. Internal Oscillator

7.6.1.General Description

There is main oscillation to generate system clock with fosc frequency.

7.7. Protection and diagnostic

7.7.1.Protection And Diagnostic Overview

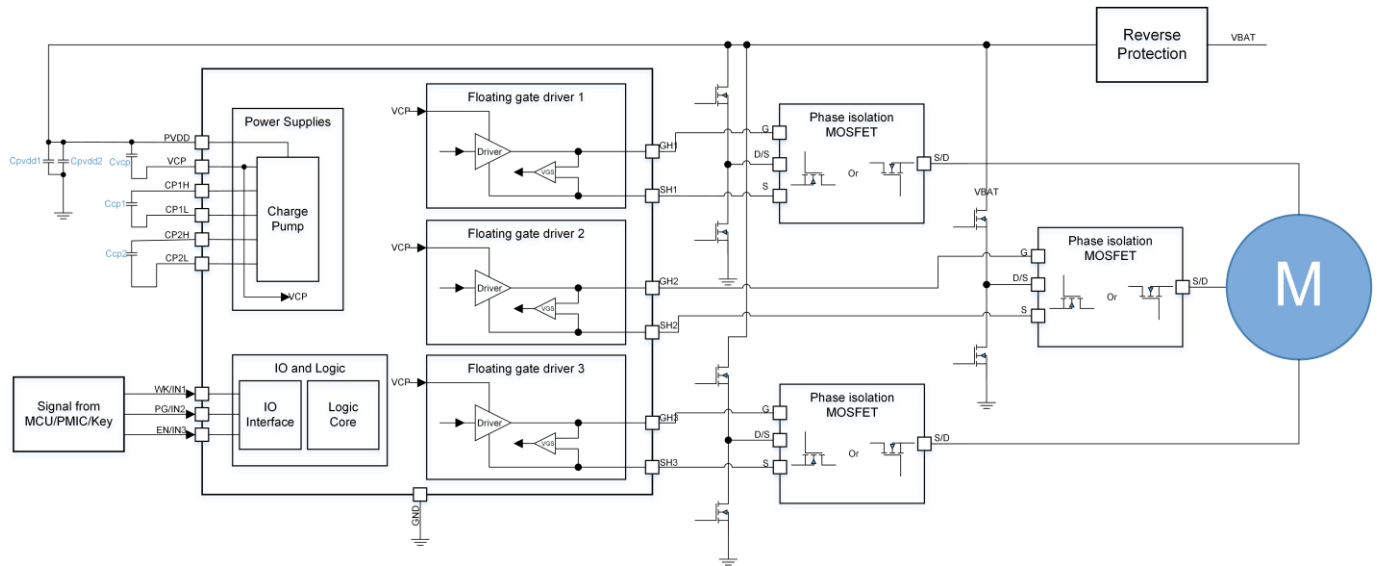
Table 7.3 NSD3661 Protection and diagnostic status table

Name	Logic core	Charge pump	Gate drivers
POR by PVDD UV	Reset	Restart	Restart
VCP_UV	Not affect	Not affect	Passive off
VGS_UV during on state	Not affect	Not affect	Not affect

Table 7.4 NSD3662 Protection and diagnostic status table

Name	Logic core	Charge pump	Gate drivers	EN open drain structure
POR by WK or PG	Reset	Restart	Restart	OFF
POR by PVDD UV	Reset	Restart	Restart	OFF
VCP_UV	Not affect	Not affect	Passive off	Active
VGS_UV during on state	Not affect	Not affect	Not affect	Active

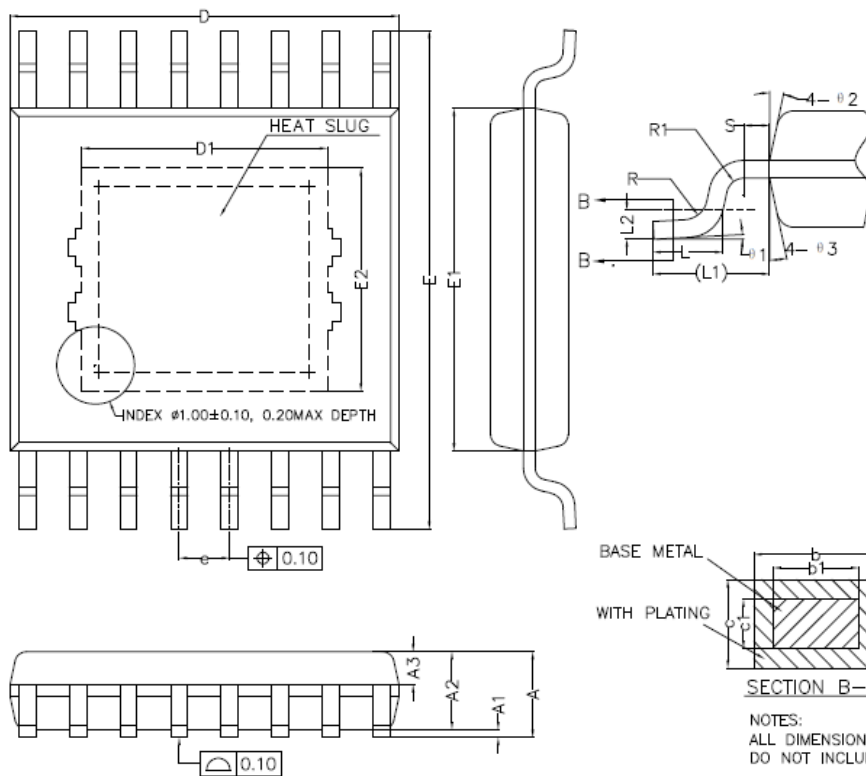
8. Application information



Notes:

Designator	Value
Cvcp	1 μ F
Ccp1, Ccp2	330nF
Cpvdd1	100nF
Cpvdd2	1 μ F~10 μ F

9. Package information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.32	0.42	0.52
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.15	—	0.20
c1	0.14	0.15	0.16
D	4.90	5.00	5.10
D1	3.16REF		
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.86REF		
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	—	—
R1	0.09	—	—
S	0.20	—	—
$\varnothing 1$	0"	—	8"
$\varnothing 2$	10"	12"	14"
$\varnothing 3$	10"	12"	14"

10. Ordering Information

Part Number	Package Type	Marking	MSL	SPQ	MPQ	Operating Temp
NSD3661-Q1HTSPR	HTSSOP16	NSD36 61Q	3	4000	4000	-40 to 125°C
NSD3662-Q1HTSPR	HTSSOP16	NSD36 62Q	3	4000	4000	-40 to 125°C

Note: All packages are RoHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.

Technical drawing of a circular electronic component, showing top, front, and side views with dimensions in mm.

Top View (Left):

- Overall diameter: $\phi 330 \pm 2.00$
- Inner circle diameter: $\phi 133 \pm 0.5$
- Radial dimension: 6.0 ± 0.5
- Angle: $2 \times 30^\circ$
- Radius: $R135$, $R6$

Top View (Right):

- Overall diameter: $\phi 330 \pm 2.00$
- Inner circle diameter: $\phi 100 \pm 2.0$
- Radial dimension: 6.5 ± 1.0
- Radius: $R56$, $R50$, $R135$, $R6$
- Angle: $2 \times 0 \pm 0.5$
- Warning label: **ATTENTION** (ELECTROSTATIC SENSITIVE DEVICE)
- Reference: SEE DETAIL C

Front View (Bottom):

- Overall width: $W(12.00 \pm 0.30)$
- Overall height: $E(1.75 \pm 0.10)$
- Pin 1 location: $Pin1$
- Dimensions: $T(0.35 \pm 0.05)$, $P0(4.00 \pm 0.10)$, $P2(2.00 \pm 0.05)$, $P1(8.00 \pm 0.10)$, $D0(1.50 \pm 0.10)$, $D1(1.50 \pm 0.10)$, $F(5.50 \pm 0.05)$

Side View (Bottom Right):

- Overall width: $W(12.00 \pm 0.30)$
- Overall height: $E(1.75 \pm 0.10)$
- Dimensions: $K0(1.60 \pm 0.10)$, $K1(1.30 \pm 0.10)$, $A0(6.85 \pm 0.10)$, $MAX5^\circ$, 0.3000

Notes:

- ALL DIMS IN MM

NOTES:
1. ALL DIMS IN MM
2. MATERIAL: BLACK CONDUCTIVE PS
3. The other tolerance not indicated are $\pm 0.1\text{mm}$

12. Revision history

Revision	Description	Date
1.0	Initial release	2026/6/15

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