NOVOSENSE

NSD3602
Automotive Two-Channel Half Bridge Gate Drivers
Datasheet (EN) 1.0

Product Overview

NSD3602 is a highly integrated device which includes two half bridge gate drivers and a current sense amplifier.

Gate drivers provide advanced functions like slew rate control and VGS handshaking. Current sense amplifier supports high common mode voltage input. A 16-bit SPI is used to configure parameters, control device, and read out status registers for diagnostics. Device offers an array of diagnostic features to ensure robust operation. These features include supply voltage monitor, charge pump voltage monitor, VDS overvoltage monitor, VGS voltage monitor and thermal monitor (warning and shutdown protection).

Key Features

- Multiple interface versions available
  - SPI interface version (NSD3602S): Flexible configuration and diagnostics
  - Hardware interface version (NSD3602H): Simplified control and fewer MCU pins
- AEC-Q100 Grade1 qualified
- Two channel half bridge gate drivers
  - 4.9V to 37V operating range
  - Four control modes target for different application
- Configurable charge/discharge current driver for improving EMC performance
  - NSD3602S support two phases for MOSFET turn on/off (NSD3602H only support one phase)
  - 0.25mA to 64mA source/sink current for different phases
- Integrated charge-pump with spread spectrum
  - Support 0% to 100% PWM operation
  - Reverse protection MOSFET driver output
- One wide common mode current sense amplifier (CSA)
  - Support high side, low side and inline topology
  - Configurable gain (10/20/40/80V/V)
  - Configurable over current threshold, filter time and fault reaction (only for NSD3602S)
- Low current consumption in sleep mode
- 16-bit, max 10MHz SPI interface
- Protection and diagnostic (limited in NSD3602H since no SPI interface)
  - Supply and regulator voltage monitor (DVDD, AREF and VCP UV, PVDD OV and UV)
  - Gate driver monitor (VGS Fault and VDS OV)
  - Support off state diagnostic
  - Thermal warning and shutdown
  - Window watchdog timer
  - Support brake function in sleep mode and normal mode
  - Dedicated fault interrupt pin (nFLT)
- RoHS & REACH Compliance

Applications

- Automotive brushed DC motor applications (Seat, Power lift gate, Window lifters…)
- Automotive body control functions (Door locks, Latches…)

Device Information

Part Number	Function Description	Package	Body Size
NSD3602S-Q1QDAR	SPI version	VQFN32	5.00 × 5.00mm
NSD3602H-Q1QDAR	Hardware version	VQFN32	5.00 × 5.00mm

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1. Pin Configuration and Functions

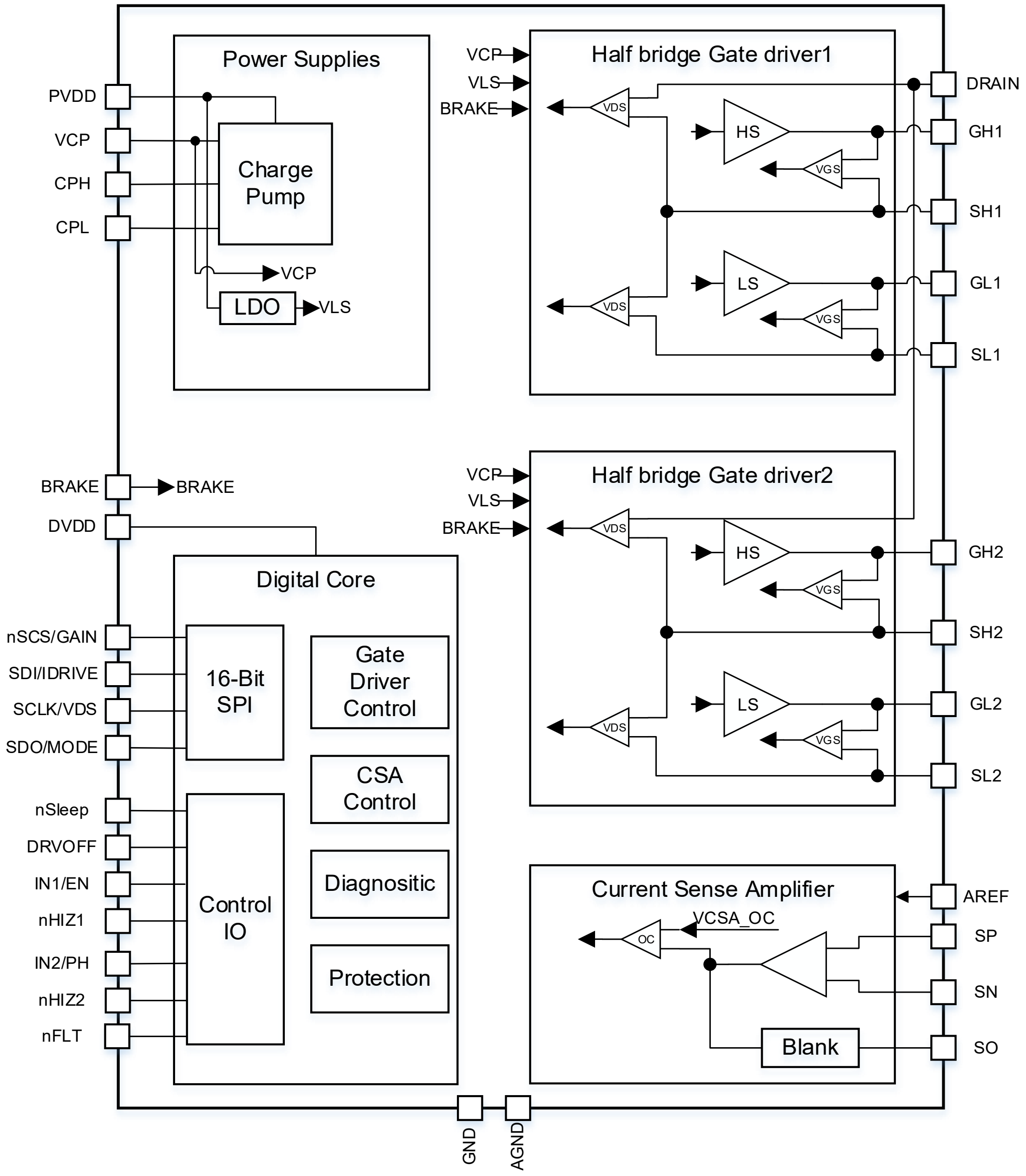
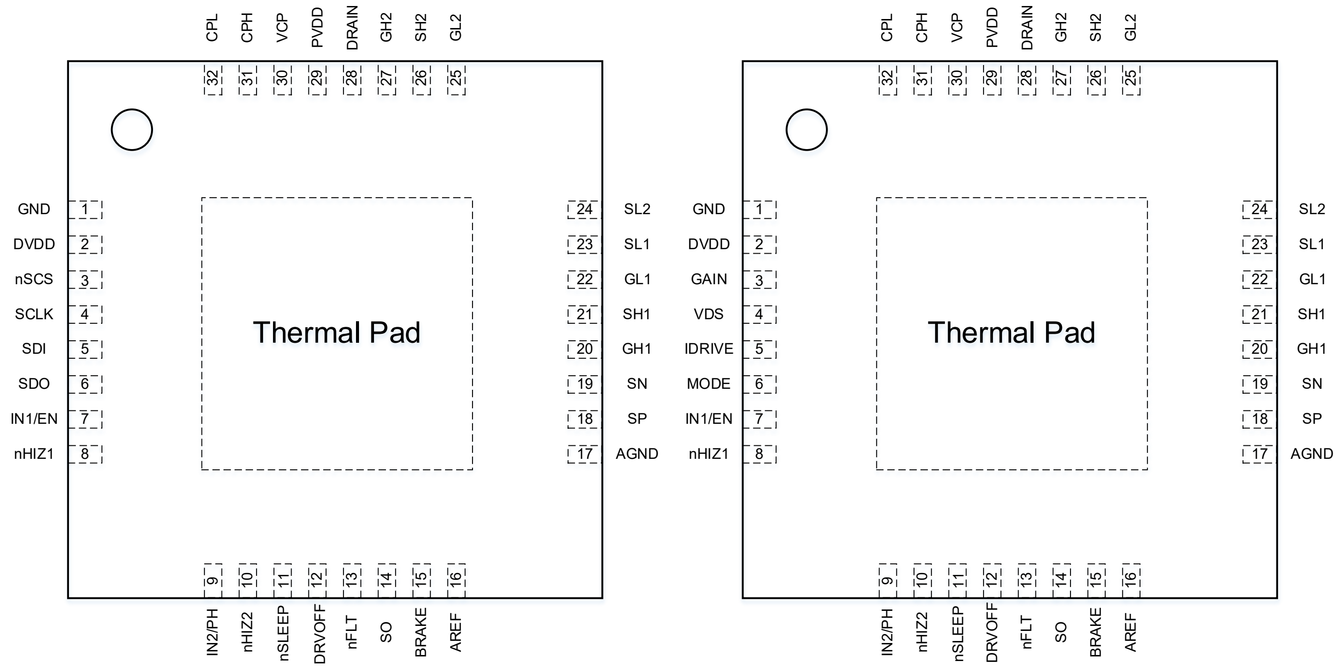


Figure 1.1 NSD3602 block diagram



NSD3602S VQFN32-Pin package NSD3602H VQFN32-Pin package

Figure 1.2 NSD3602 VQFN32 package

Table 1.1 NSD3602 Pin Configuration and Description

PIN NO	***Symbol***		***I/O***	***Type***	***Description***
	NSD3602S	**NSD3602H**			
1	GND		-	Power	Device ground (for digital core and charge pump)
2	DVDD		-	Power	Device digital core and IO supply
3	nSCS	—	I	Digital	Serial chip selection, internal pull up by resistor
	—	GAIN	I	Analog	Current sense amplifier gain setting input, internal pull up and down by resistor
4	SCLK	—	I	Digital	Serial clock input, internal pull down by resistor
	—	VDS	I	Analog	VDS monitor threshold setting input, internal pull up and down by resistor
5	SDI	—	I	Digital	Serial data input, internal pull down by resistor
	—	IDRIVE	I	Analog	Gate driver charge/discharge current setting input, internal pull up and down by resistor
6	SDO	—	O	Digital	Serial data output, internal push pull output
	—	MODE	I	Analog	Control mode setting input, internal pull up and down by resistor
7	IN1/EN		I	Digital	Half bridge control input, internal pull down by resistor
8	nHIZ1		I	Digital	Half bridge control input, internal pull down by resistor
9	IN2/PH		I	Digital	Half bridge control input, internal pull down by resistor
10	nHIZ2		I	Digital	Half bridge control input, internal pull down by resistor
11	nSLEEP		I	Digital	Device enable pin, internal pull down by resistor

12	DRVOFF	I	Digital	Driver shutdown pin, internal pull down by resistor
13	nFLT	O	Digital	Fault indicator output, open drain output
14	SO	O	Analog	Current sense amplifier (CSA) output
15	BRAKE	I	Digital	Brake function control pin, internal pull down by resistor
16	AREF	-	Power	External voltage reference and power supply for CSA
17	AGND	-	Power	Device ground for current sense amplifier
18	SP	I	Analog	Current sense amplifier positive input
19	SN	I	Analog	Current sense amplifier negative input
20	GH1	I/O	Analog	High side1 gate to turn on/off high side1 MOSFET, also VGS monitor input
21	SH1	I/O	Analog	High side1 source to turn on/off high side1 MOSFET, also is sense input for multi-function in half bridge 1(VGS monitor, VDS monitor)
22	GL1	I/O	Analog	Low side1 gate to turn on/off low side1 MOSFET, also VGS monitor input
23	SL1	I/O	Analog	Source for low side1 and sense input for VDS monitor and VGS monitor
24	SL2	I/O	Analog	Source for low side2 and sense input for VDS monitor and VGS monitor
25	GL2	I/O	Analog	Low side2 gate to turn on/off low side2 MOSFET, also VGS monitor input
26	SH2	I/O	Analog	High side2 source to turn on/off high side2 MOSFET, also is sense input for multi-function in half bridge 2(VGS monitor, VDS monitor)
27	GH2	I/O	Analog	High side2 gate to turn on/off high side2 MOSFET, also VGS monitor input
28	DRAIN	I	Analog	High side MOSFET drain sense input for both half bridge
29	PVDD	-	Power	Device supply for charge pump
30	VCP	-	Power	Charge pump output
31	CPH	-	Power	Positive connection for charge pump
32	CPL	-	Power	Negative connection for charge pump
	Thermal Pad			Exposed pad, left floating or better connected to GND plane for better EMC and thermal performance

Note: AGND and GND should be connected together and close to device

2. Absolute Maximum Ratings

All voltages with respect to ground, positive current if flowing into pin.

Parameters	***Symbol***	***Min***	***Typ***	***Max***	***Unit***	***Comments***
Gate driver power supply pin voltage (PVDD)	V_{PVDD}	-0.3		40	V	
Drain sense input pin voltage (DRAIN)	V_{DRAIN}	-0.3		40	V	
Digital power supply pin voltage (DVDD)	V_{DVDD}	-0.3		5.75	V	
CSA power supply and reference pin voltage (AREF)	V_{AREF}	-0.3		5.75	V	
Voltage difference between ground pins (AGND, GND)	V_{GND} - V_{AGND}	-0.3		0.3	V	
Charge pump output pin voltage (VCP)	V_{VCP}	-0.3		55	V	
Voltage difference between VCP and PVDD	V_{VCP} - V_{PVDD}	-0.3		32	V	
Charge pump positive pin voltage (CPH)	V_{CPH}	V_{PVDD}-0.3		V_{VCP}+0.3	V	
Charge pump negative pin voltage (CPL)	V_{CPL}	-0.3		V_{PVDD}+0.3	V	
Input pin voltage (nSLEEP, IN1/EN, IN2/PH, nHIZx, DRVOFF, SDI, nSCS, SCLK, GAIN, VDS, IDRIVE, MODE, nFLT)	V_{nSLEEP}, $V_{IN1/EN}$, $V_{IN2/PH}$, V_{nHIZx}, V_{DRVOFF}, V_{SDI}, V_{nSCS}, V_{SCLK}, V_{GAIN}, V_{VDS}, V_{IDRIVE}, V_{MODE}, V_{nFLT}	-0.3		5.75	V	
Digital output pin voltage (SDO)	V_{SDO}	-0.3		V_{DVDD}+0.3	V	|I|<10mA
Brake pin voltage (BRAKE)	V_{BRAKE}	-0.3		40	V	
High side gate driver pin voltage (GHx)	V_{GHx}	-2		V_{VCP}+0.3	V	
Transient 1µs High side gate driver pin voltage (GHx)		-5		V_{VCP}+0.3	V	
Voltage difference between GHx and SHx	V_{GHx} - V_{SHx}	-0.3		16	V	
High side source pin voltage (SHx)	V_{SHx}	-2		40	V	
Transient 1µs high side source pin voltage (SHx)		-5		40	V	
Voltage difference between VCP and SHx	V_{VCP} - V_{SHx}	-0.3		55	V	
Low side gate driver pin voltage (GLx), normal mode	V_{GLx}	-2		13.5	V	
Transient 1µs low side gate driver pin voltage (GLx), normal mode		-3		13.5	V	
Low side gate driver pin voltage (GLx), sleep mode	V_{GLx}	-2		15	V	
Transient 1µs low side gate driver pin voltage (GLx), sleep mode		-3		15	V	
Voltage difference between GLx and SLx	V_{GLx} - V_{SLx}	-0.3		16	V	
Voltage difference between PVDD and	V_{PVDD} - V_{GLx}	-0.3		40	V	

GLx						
Half bridge driver GND (SL1/SL2)	V_{SLx}	-2		2	V	
Transient 1μs Half bridge driver GND (SL1/SL2)		-3		3	V	
CSA input pin voltage (SN, SP)	V_{SN}, V_{SP}	-2		40	V	
Transient 1μs CSA input pin voltage (SN, SP)		-5		40	V	
CSA input pin differential voltage (SN, SP)	V_{SP} - V_{SN}	-5		5	V	
CSA output pin voltage (SO)	V_{SO}	-0.3		V_{AREF}+0.3	V	|I|<10mA
Junction temperature	T_J	-40		150	℃	
Storage temperature	T_{STG}	-55		150	℃	

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD		
	● All pins	±2.0	kV
	● PVDD, DRAIN & SHx pins to GND	±4.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB		
	● All pins	±750	V

4. Recommended Operating Conditions

All voltages with respect to ground, positive current if flowing into pin.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Gate driver supply range for normal operation (PVDD)	V_{PVDD_nor}	4.9		37	V	
Gate driver extended supply range, parameter deviations possible (PVDD)	V_{PVDD_ext}	$V_{PVDD\_UV\_H}$		40	V	
Digital supply range for normal operation (DVDD)	V_{DVDD_nor}	3		5.5	V	
Digital extended supply range, parameter deviations possible (DVDD)	V_{DVDD_ext}	$V_{DVDD\_POR\_H}$		5.75	V	
CSA supply and reference input range (AREF)	V_{AREF_nor}	3		5.5	V	
Pin input voltage range	V_{IN_nor}	0		V_{DVDD}	V	
Digital output current (SDO)	I_{DOUT_nor}	-5		5	mA	
Open drain pullup voltage (nFLT)	V_{OD_nor}	0		5.5	V	
Open drain current (nFLT)	I_{OD_nor}	0		5	mA	
Brake input normal range (BRAKE)	V_{BRAKE_nor}	0		V_{PVDD}	V	
CSA output current (SO)	I_{SO_nor}	-1		1	mA	
Junction temperature range	T_{J_nor}	-40		150	℃	

5. Thermal Information

Parameters	*Symbol*	*MIN*	*TYP*	*MAX*	*Unit*
Junction-to-ambient thermal resistance	θ_{JA}		32.3		℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$		25.2		℃/W
Junction-to-case (bottom) thermal resistance	$\theta_{JC(bot)}$		4.53		℃/W
Junction-to-board thermal resistance	θ_{JB}		11.9		℃/W

6. Specifications

6.1. Power Supply Electrical Characteristics

4.9V ≤ V_{PVDD} ≤ 37V, 3V ≤ V_{DVDD}/V_{AREF} ≤ 5.5V, -40℃ ≤ T_J ≤ 150℃, all voltages with respect to ground, positive current if flowing into pin.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{PVDD_Q}	PVDD current in sleep mode	V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP}, V_{BRAKE} = 0V, V_{DVDD}, V_{AREF} = 5V, -40℃≤ T_J ≤ 25℃		3	6	µA
		V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP}, V_{BRAKE} = 0V, V_{DVDD}, V_{AREF} = 5V, T_J = 125℃		4	9	µA
$I_{PVDD\_Q\_BRAKE}$		V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP} = 0V, V_{BRAKE} = 5V, V_{DVDD}, V_{AREF} = 5V, -40℃≤ T_J ≤125℃		75	350	µA
I_{DVDD_Q}	DVDD current in sleep mode	V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP} = 0V, V_{DVDD}, V_{AREF} = 5V, -40℃≤ T_J ≤125℃		0.1	3	µA
I_{DRAIN_Q}	DRAIN current in sleep mode	V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP} = 0V, V_{DVDD}, V_{AREF} = 5V, -40℃≤ T_J ≤125℃		0.1	2	µA
I_{AREF_Q}	AREF current in sleep mode	V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP} = 0V, V_{DVDD}, V_{AREF} = 5V, -40℃≤ T_J ≤125℃		0.1	1.5	µA
I_{PVDD1}	PVDD current in normal mode	V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP}, V_{DVDD}, V_{AREF} = 5V, I_{CP} = 0mA, DRV_EN = 0b for NSD3602S		2.5	5	mA
I_{PVDD2}		V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP}, V_{DVDD}, V_{AREF} = 5V, I_{CP} = 0mA, DRV_EN = 1b for NSD3602S, or NSD3602H		3	8	mA
I_{PVDD3}		V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP}, V_{DVDD}, V_{AREF} = 5V, I_{CP} = 15mA, DRV_EN = 1b for NSD3602S, or NSD3602H		40	50	mA
I_{DVDD}	DVDD current in normal mode	V_{DVDD} = 3.3V/5V, SPI not active for NSD3602S, or NSD3602H		3.5	5.5	mA
I_{DRAIN}	DRAIN current in normal mode	V_{PVDD}, V_{DRAIN} = 13.5V, V_{nSLEEP}, V_{DVDD}, V_{AREF} = 5V, V_{DS_TH} ≤ 500mV, off state pull up/down current source disabled		0.5	2	mA
I_{AREF}	AREF current in normal mode	V_{AREF} = 3.3V/5V while SO floating, CSA enabled		0.5	1.8	mA
$V_{PVDD\_UV\_H}$	PVDD undervoltage threshold	V_{PVDD} rising	4.3	4.6	4.9	V
$V_{PVDD\_UV\_L}$		V_{PVDD} falling	4.2	4.5	4.8	V
$V_{PVDD\_UV\_HYS}$	PVDD undervoltage hysteresis			100		mV
t_{PVDD_UV}	PVDD		8	10	12.75	µs

	undervoltage filter time					
$V_{PVDD\_OV\_H}$	PVDD overvoltage threshold	V_{PVDD} rising, PVDD_OV_TH = 0b	21	22.5	24	V
		V_{PVDD} rising, PVDD_OV_TH = 1b	27	28.5	30	V
$V_{PVDD\_OV\_L}$		V_{PVDD} falling, PVDD_OV_TH = 0b	19	21.5	23	V
		V_{PVDD} falling, PVDD_OV_TH = 1b	25	27.5	29	V
$V_{PVDD\_OV\_HYS}$	PVDD overvoltage hysteresis			1		V
t_{PVDD_OV}	PVDD overvoltage filter time	PVDD_OV_TFILTER = 00b	0.75	1	1.5	µs
		PVDD_OV_TFILTER = 01b	1.5	2	2.5	µs
		PVDD_OV_TFILTER = 10b	3.25	4	4.75	µs
		PVDD_OV_TFILTER = 11b	7	8	9	µs
$V_{DVDD\_POR\_H}$	DVDD POR threshold	V_{DVDD} rising	2.6	2.8	3	V
$V_{DVDD\_POR\_L}$		V_{DVDD} falling	2.5	2.7	2.9	V
$V_{DVDD\_POR\_HYS}$	DVDD POR hysteresis			100		mV
t_{DVDD_POR}	DVDD POR filter time	1)		8		µs
t_{FLT_OFF}	Active turn off time for faults			20		µs
$V_{AREF\_UV\_H}$	AREF undervoltage threshold	V_{AREF} rising	2.6	2.8	3	V
$V_{AREF\_UV\_L}$		V_{AREF} falling	2.5	2.7	2.9	V
$V_{AREF\_UV\ \_HYS}$	AREF undervoltage hysteresis			100		mV
t_{AREF_UV}	AREF undervoltage filter time		12	16	20	µs

1) Not subject to production test, guaranteed by design

6.2. Charge Pump Electrical Characteristics

4.9V ≤ V_{PVDD} ≤ 37V, 3V ≤ V_{DVDD}/V_{AREF} ≤ 5.5V, -40℃ ≤ T_J ≤ 150℃, all voltages with respect to ground, positive current if flowing into pin.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{VCP}	Charge pump frequency without spread spectrum			400		kHz
$V_{VCP\text{-}PVDD}$	Charge pump voltage with respect to	V_{PVDD} ≥ 13V, I_{CP} ≥ -15mA	10	12	13	V
		V_{PVDD} = 11V, I_{CP} ≥ -15mA	8.4	10	11.5	V

	PVDD	V_{PVDD} = 9V, I_{CP} ≥ -11mA	7	8	9	V
		V_{PVDD} = 7V, I_{CP} ≥ -7.5mA	5.5	6	7	V
		V_{PVDD} = 5.5V, I_{CP} ≥ -5mA	4.5	5	5.5	V
$f_{VCP\_MOD\_S}$	Spread spectrum modulation frequency	CP_SS_CONFIG = 0b, NSD3602H		16.5		kHz
		CP_SS_CONFIG = 1b		33		kHz
$f_{VCP\_MOD\_RA}$	Spread spectrum modulation amplitude			±10		%
$V_{VCP\_UV\_H}$	Charge pump undervoltage threshold	VCP_UV_TH = 0b, VCP_UV_TH_M = 0b, NSD3602H	2.5	3	3.5	V
		VCP_UV_TH = 1b, VCP_UV_TH_M = 0b	4.5	5.5	6.5	V
		VCP_UV_TH = 0b, VCP_UV_TH_M = 1b	6	6.75	7.5	V
		VCP_UV_TH = 1b, VCP_UV_TH_M = 1b	7.5	8	8.5	V
$V_{VCP\_UV\_L}$		VCP_UV_TH = 0b, VCP_UV_TH_M = 0b, NSD3602H	2	2.5	3	V
		VCP_UV_TH = 1b, VCP_UV_TH_M = 0b	4	5	6	V
		VCP_UV_TH = 0b, VCP_UV_TH_M = 1b	5.5	6.25	7	V
		VCP_UV_TH = 1b, VCP_UV_TH_M = 1b	7	7.5	8	V
$V_{VCP\_UV\_HYS}$	Charge pump undervoltage threshold hysteresis			500		mV
t_{VCP_UV}	Charge pump undervoltage filter time		8	10	13	μs
t_{VCP_blank}	Charge pump startup blanking time		400	500	600	μs

6.3. Input and Output Electrical Characteristics

4.9V ≤ V_{PVDD} ≤ 37V, 3V ≤ V_{DVDD}/V_{AREF} ≤ 5.5V, -40℃ ≤ T_J ≤ 150℃, all voltages with respect to ground, positive current if flowing into pin.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input logic low voltage	nSLEEP, IN1/EN, IN2/PH, DRVOFF, nSCS, SCLK, SDI, nHIZx	0		0.3×V_{DVDD}	V

		BRAKE	0		0.6	V
V_{IH}	Input logic high voltage	nSLEEP, IN1/EN, IN2/PH, DRVOFF, nSCS, SCLK, SDI, nHIZx	0.7×V_{DVDD}		5.5	V
		BRAKE	1.8		5.5	V
V_{HYS}	Input hysteresis	nSLEEP, IN1/EN, IN2/PH, DRVOFF, nSCS, SCLK, SDI, nHIZx		0.1×V_{DVDD}		V
		BRAKE		0.5		V
I_{IL}	Input logic low current	V_{DIN} = 0V, nSLEEP, IN1/EN, IN2/PH, DRVOFF, SCLK, SDI, nHIZx, BRAKE	-5		5	μA
		V_{DIN} = 0V, V_{DVDD} = 5V, nSCS	-100	-50		μA
I_{IH}	Input logic high current	V_{DIN} = 5V, nSLEEP, IN1/EN, IN2/PH, DRVOFF, SCLK, SDI, nHIZx		50	100	μA
		V_{DIN} = 5V, V_{DVDD} = 5V, nSCS	-5		5	μA
		V_{DIN} = 5V, nSLEEP = 0V, BRAKE		5	10	μA
		V_{DIN} = 5V, nSLEEP = 5V, BRAKE_DIS = 0b, BRAKE		35	100	μA
R_{PD}	Internal pulldown resistance	nSLEEP, IN1/EN, IN2/PH, DRVOFF, SCLK, SDI, nHIZx to GND	50	100	150	kΩ
		BRAKE to GND, V_{BRAKE} ≤ 2V, 4.9V ≤ V_{PVDD} ≤ V_{POB_OV}, sleep mode or BRAKE_DIS = 0b for NSD3602S, or NSD3602H	500	1000	1500	kΩ
		BRAKE to GND, V_{BRAKE} ≤ 2V, 4.9V ≤ V_{PVDD} ≤ V_{POB_OV}, BRAKE_DIS = 1b (normal mode) for NSD3602S	50	136	200	kΩ
R_{PU}	Internal pullup resistance	nSCS to DVDD	50	100	150	kΩ
$R_{PD\_GAIN\_MODE}$	Internal pulldown resistance	GAIN, MODE to GND in NSD3602H		100		kΩ
$R_{PU\_GAIN\_MODE}$	Internal pullup resistance	GAIN, MODE to DVDD in NSD3602H		100		kΩ
V_{TH1_GAIN}, V_{TH1_MODE}	Internal threshold 1	GAIN, MODE threshold for NSD3602H	0.15×V_{DVDD}	0.2×V_{DVDD}	0.25×V_{DVDD}	V
R_{LEVEL2_GAIN}, R_{LEVEL2_MODE}	External pulldown resistance	GAIN, MODE resistor to GND to set level 2 for NSD3602H	44.65	47	49.35	kΩ
V_{TH2_GAIN}, V_{TH2_MODE}	Internal threshold 2	GAIN, MODE threshold for NSD3602H	0.35×V_{DVDD}	0.4×V_{DVDD}	0.45×V_{DVDD}	V
R_{LEVEL3_GAIN}, R_{LEVEL3_MODE}	External pulldown resistance	GAIN, MODE resistor to GND to set level 3 for NSD3602H	500	HiZ		kΩ
V_{TH3_GAIN}, V_{TH3_MODE}	Internal threshold 3	GAIN, MODE threshold for NSD3602H	0.75×V_{DVDD}	0.8×V_{DVDD}	0.85×V_{DVDD}	V

$R_{PD\_VDS\_IDRIVE}$	Internal pulldown resistance	VDS, IDRIVE to GND in NSD3602H		100		kΩ
$R_{PU\_VDS\_IDRIVE}$	Internal pullup resistance	VDS, IDRIVE to DVDD in NSD3602H		69		kΩ
V_{TH1_VDS}, V_{TH1_IDRIVE}	Internal threshold 1	VDS, IDRIVE threshold for NSD3602H	0.18×V_{DVDD}	0.2×V_{DVDD}	0.22×V_{DVDD}	V
R_{LEVEL2_VDS}, R_{LEVEL2_IDRIVE}	External pulldown resistance	VDS, IDRIVE resistor to GND to set level 2 for NSD3602H	28.5	30	31.5	kΩ
V_{TH2_VDS}, V_{TH2_IDRIVE}	Internal threshold 2	VDS, IDRIVE threshold for NSD3602H	0.28×V_{DVDD}	0.3×V_{DVDD}	0.32×V_{DVDD}	V
R_{LEVEL3_VDS}, R_{LEVEL3_IDRIVE}	External pulldown resistance	VDS, IDRIVE resistor to GND to set level 3 for NSD3602H	95	100	105	kΩ
V_{TH3_VDS}, V_{TH3_IDRIVE}	Internal threshold 3	VDS, IDRIVE threshold for NSD3602H	0.48×V_{DVDD}	0.5×V_{DVDD}	0.52×V_{DVDD}	V
R_{LEVEL4_VDS}, R_{LEVEL4_IDRIVE}	External pulldown resistance	VDS, IDRIVE resistor to GND to set level 4 for NSD3602H	500	HiZ		kΩ
V_{TH4_VDS}, V_{TH4_IDRIVE}	Internal threshold 4	VDS, IDRIVE threshold for NSD3602H	0.68×V_{DVDD}	0.7×V_{DVDD}	0.72×V_{DVDD}	V
R_{LEVEL5_VDS}, R_{LEVEL5_IDRIVE}	External pullup resistance	VDS, IDRIVE resistor to DVDD to set level 5 for NSD3602H	58.9	62	65.1	kΩ
V_{TH5_VDS}, V_{TH5_IDRIVE}	Internal threshold 5	VDS, IDRIVE threshold for NSD3602H	0.78×V_{DVDD}	0.8×V_{DVDD}	0.82×V_{DVDD}	V
t_{nSLEEP_FLT}				10	20	µs
t_{dsleep}	Sleep mode delay		t_{FLT_OFF}+3			µs
t_{wake}		NSD3602S and NSD3602H			200	µs
t_{DRVOFF}				1.5	3	µs
V_{OL}	Output logic low voltage	I_{DOUT} = 5mA, SDO			0.6	V
V_{OH}	Output logic high voltage	I_{DOUT} = -5mA, SDO	0.8×V_{DVDD}			V
I_{SDO}	Leakage current for tri-state		-10		10	µA
I_{ODZ_nFLT}	Open drain pin logic high current	V_{nFLT} = 5V, nFLT open drain not active, nSLEEP = 5V	-10		10	µA
R_{OD_nFLT}	Open drain resistance	nFLT, 1mA			150	Ω
Brake function						

I_{POB_P}	Charge current for brake function	$V_{GS} \leq 7V$		-15		mA
I_{POB_N}	Discharge current for brake function	$V_{GS} \geq 3V$		27		mA
V_{GS_POB}	VGS voltage during brake	$V_{PVDD} \geq 8V$, $I_{GLx} = -1mA$	5.5		15	V
t_{POB_on}	Turn on time for brake			10		μs
t_{POB_off}	Turn off time for brake			20		μs
V_{POB_VDS}	VDS OV threshold for brake		250	350	450	mV
t_{POB_VDS}	VDS OV filter time for both rising and falling		2.5	4	5.75	μs
$V_{POB\_OV\_H}$	PVDD OV threshold for brake	Rising	27.5	31	34.5	V
$V_{POB\_OV\_L}$		Falling	24.5	29	32.5	V
$V_{POB\_OV\_HYS}$	PVDD OV hysteresis for brake			2		V
t_{brake_on}	Brake pin input and PVDD OV filter for brake function activation			17.5		μs
t_{brake_off}	Brake pin input and PVDD OV filter for brake function deactivation			27.5		μs

6.4. Gate Driver Electrical Characteristics

$4.9V \leq V_{PVDD} \leq 37V$, $3V \leq V_{DVDD}/V_{AREF} \leq 5.5V$, $-40℃ \leq T_J \leq 150℃$, all voltages with respect to ground, positive current if flowing into pin.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{GHx_L}	GHx output voltage low level	Gate driver active off, $I_{GHx} = 1mA$, $V_{GHx} - V_{SHx}$			0.25	V
V_{GLx_L}	GLx output voltage low level	Gate driver active off, $I_{GLx} = 1mA$, $V_{GLx} - V_{SLx}$			0.25	V
V_{GHx_H}	GHx output voltage high	Gate driver active on, $R_{load} = 10kΩ$, $V_{PVDD} \geq 13V$, $I_{CP} = 0mA$, $V_{GHx} - V_{SHx}$	V_{CP}-0.25	11	12	V

	level	Gate driver active on, R_{load} = 10kΩ, V_{PVDD} ≥ 5.5V, I_{CP} = 0mA, V_{GHx} - V_{SHx}	V_{CP}-0.25	11	12	V
V_{GLx_H}	GLx output voltage high level	Gate driver active on, R_{load} = 10kΩ, V_{PVDD} ≥ 10.5V, V_{GLx}-V_{SLx}	V_{PVDD}-0.25	11.5	13.5	V
		Gate driver active on, R_{load} = 10kΩ, 10.5V ≥ V_{PVDD} ≥ 4.9V, V_{GLx}-V_{SLx}	V_{PVDD}-0.25	V_{PVDD}	V_{PVDD}	V
I_{SOURCE}	Charge current for I_{PRE_CHR}, I_{DRVP}, I_{PST_CHR}	ISOURCE = 0000b, V_{GSx} = 7V	0.1	0.25	0.4	mA
		ISOURCE = 0001b, V_{GSx} = 7V (V_{IDRIVE} < V_{TH1_IDRIVE} for NSD3602H)	0.5	1	1.5	mA
		ISOURCE = 0010b, V_{GSx} = 7V	1.3	2	2.7	mA
		ISOURCE = 0011b, V_{GSx} = 7V	2.1	3	3.9	mA
		ISOURCE = 0100b, V_{GSx} = 7V (V_{TH1_IDRIVE} < V_{IDRIVE} < V_{TH2_IDRIVE} for NSD3602H)	2.8	4	5.2	mA
		ISOURCE = 0101b, V_{GSx} = 7V	4.3	6	7.7	mA
		ISOURCE = 0110b, V_{GSx} = 7V (V_{TH2_IDRIVE} < V_{IDRIVE} < V_{TH3_IDRIVE} for NSD3602H)	5	8	11	mA
		ISOURCE = 0111b, V_{GSx} = 7V	9	12	15	mA
		ISOURCE = 1000b, V_{GSx} = 7V (V_{TH3_IDRIVE} < V_{IDRIVE} < V_{TH4_IDRIVE} for NSD3602H)	12	16	20	mA
		ISOURCE = 1001b, V_{GSx} = 7V	15	20	25	mA
		ISOURCE = 1010b, V_{GSx} = 7V	18	24	30	mA
		ISOURCE = 1011b, V_{GSx} = 7V	21	28	35	mA
		ISOURCE = 1100b, V_{GSx} = 7V (V_{TH4_IDRIVE} < V_{IDRIVE} < V_{TH5_IDRIVE} for NSD3602H)	24	32	39	mA
		ISOURCE = 1101b, V_{GSx} = 7V	27	40	50	mA
		ISOURCE = 1110b, V_{GSx} = 7V	28	48	60	mA
		ISOURCE = 1111b, V_{GSx} = 7V (V_{TH5_IDRIVE} < V_{IDRIVE} for NSD3602H)	46	64	78	mA
	Offset charge current for $I_{PRE\_CHR\_HS/LS}$, $I_{DRVP\_HS/LS}$	ISOURCE_L = 00b, V_{GSx} = 7V, NSD3602H		0		mA
		ISOURCE_L = 01b, V_{GSx} = 7V		0.25		mA
		ISOURCE_L = 10b, V_{GSx} = 7V		0.5		mA
		ISOURCE_L = 11b, V_{GSx} = 7V		0.75		mA
I_{SINK}	Discharge current for $I_{PRE\_DCHR\_HS/LS}$,	ISINK = 0000b, V_{GSx} = 3V	0.1	0.25	0.4	mA
		ISINK = 0001b, V_{GSx} = 3V	0.35	1	1.65	mA

	$I_{DRVN\_HS/LS}$, $I_{PST\_DCHR\_HS/LS}$	($V_{IDRIVE} < V_{TH1\_IDRIVE}$ for NSD3602H)				
		ISINK = 0010b, V_{GSx} = 3V	1.2	2	2.8	mA
		ISINK = 0011b, V_{GSx} = 3V	1.4	3	4.6	mA
		ISINK = 0100b, V_{GSx} = 3V ($V_{TH1\_IDRIVE} < V_{IDRIVE} < V_{TH2\_IDRIVE}$ for NSD3602H)	2.1	4	5.9	mA
		ISINK = 0101b, V_{GSx} = 3V	3.5	6	8.5	mA
		ISINK = 0110b, V_{GSx} = 3V ($V_{TH2\_IDRIVE} < V_{IDRIVE} < V_{TH3\_IDRIVE}$ for NSD3602H)	5	8	11	mA
		ISINK = 0111b, V_{GSx} = 3V	8	12	16	mA
		ISINK = 1000b, V_{GSx} = 3V ($V_{TH3\_IDRIVE} < V_{IDRIVE} < V_{TH4\_IDRIVE}$ for NSD3602H)	12	16	20	mA
		ISINK = 1001b, V_{GSx} = 3V	15	20	25	mA
		ISINK = 1010b, V_{GSx} = 3V	18	24	30	mA
		ISINK = 1011b, V_{GSx} = 3V	21	28	35	mA
		ISINK = 1100b, V_{GSx} = 3V ($V_{TH4\_IDRIVE} < V_{IDRIVE} < V_{TH5\_IDRIVE}$ for NSD3602H)	24	32	39	mA
		ISINK = 1101b, V_{GSx} = 3V	30	40	52	mA
		ISINK = 1110b, V_{GSx} = 3V	36	48	62	mA
		ISINK = 1111b, V_{GSx} = 3V ($V_{TH5\_IDRIVE} < V_{IDRIVE}$ for NSD3602H)	46	64	78	mA
	Offset charge current for I_{PRE_DCHR}, I_{DRVN}, I_{PST_DCHR}	ISINK_L = 00b, V_{GSx} = 3V, NSD3602H		0		mA
		ISINK_L = 01b, V_{GSx} = 3V		0.25		mA
		ISINK_L = 10b, V_{GSx} = 3V		0.5		mA
		ISINK_L = 11b, V_{GSx} = 3V		0.75		mA
I_{HOLD}	Gate pull up hold current	V_{GSx}= 7V	5	16	30	mA
I_{STRONG}	Gate pull down strong current	V_{GSx} = 3V, I_{SOURCE_HS}, $I_{SOURCE\_LS} < 16mA$	30	62	90	mA
		V_{GSx} = 3V, I_{SOURCE_HS} or $I_{SOURCE\_LS} \geq 16mA$	45	128	205	mA
I_{OFF_PU}	Pull up current for off state diagnostic	13.5V drop	-5	-3.3	-2	mA
		3V drop	-2	-1.6	-0.5	mA
		1V drop	-0.3		0	mA
I_{OFF_PD}	Pull down current for off state diagnostic	13.5V drop	2	3.3	5	mA
		3V drop	1	1.6	4	mA
		1V drop	0		0.8	mA

$I_{passive}$	Passive discharge path current capability	V_{GSx} = 2V	1	2	5	mA
R_{PD_HS}	Passive gate pulldown resistor for HS	GHx to SHx		150		kΩ
I_{SHx}	Leakage current on SHx when half bridge is turned off (active off or passive off)	SHx, DRAIN ≤ 37V, nSLEEP = 0V	-5	0	5	μA
		SHx, DRAIN ≤ 37V, nSLEEP = 5V, HBx in off state, V_{DS_TH} ≤ 1.4V	-250	-75	0	μA
V_{GS_TH}	VGS comparator threshold for VGS fault, GS handshaking and CCPD	VGS_TH = 0b, NSD3602H	1.1	1.4	1.7	V
		VGS_TH = 1b	0.8	1	1.2	V
t_{GS_FLT}	VGS UV fault filter time		1.5	2	2.75	μs
t_{GS_HS}	Filter for VGS handshaking			210		ns
V_{DS_TH}	VDS comparator threshold	$V_{DS\_TH\_HBx}$ = 0000b ($V_{VDS} < V_{TH1\_VDS}$ for NSD3602H)	0.03	0.06	0.09	V
		$V_{DS\_TH\_HBx}$ = 0001b	0.05	0.08	0.11	V
		$V_{DS\_TH\_HBx}$ = 0010b ($V_{TH1\_VDS} < V_{VDS} < V_{TH2\_VDS}$ for NSD3602H)	0.07	0.1	0.13	V
		$V_{DS\_TH\_HBx}$ = 0011b	0.085	0.12	0.155	V
		$V_{DS\_TH\_HBx}$ = 0100b	0.105	0.14	0.175	V
		$V_{DS\_TH\_HBx}$ = 0101b	0.125	0.16	0.195	V
		$V_{DS\_TH\_HBx}$ = 0110b	0.14	0.18	0.22	V
		$V_{DS\_TH\_HBx}$ = 0111b ($V_{TH2\_VDS} < V_{VDS} < V_{TH3\_VDS}$ for NSD3602H)	0.15	0.2	0.25	V
		$V_{DS\_TH\_HBx}$ = 1000b	0.24	0.3	0.36	V
		$V_{DS\_TH\_HBx}$ = 1001b	0.32	0.4	0.48	V
		$V_{DS\_TH\_HBx}$ = 1010b ($V_{TH3\_VDS} < V_{VDS} < V_{TH4\_VDS}$ for NSD3602H)	0.4	0.5	0.6	V
		$V_{DS\_TH\_HBx}$ = 1011b	0.5	0.6	0.7	V
		$V_{DS\_TH\_HBx}$ = 1100b	0.58	0.7	0.82	V
		$V_{DS\_TH\_HBx}$ = 1101b ($V_{TH4\_VDS} < V_{VDS} < V_{TH5\_VDS}$ for	0.8	1	1.2	V

		NSD3602H)				
		$V_{DS\_TH\_HBx}$ = 1110b	1.1	1.4	1.7	V
		$V_{DS\_TH\_HBx}$ = 1111b	1.6	2	2.4	V
t_{DS_OV}	Filter time for VDS OV fault	TFILTER_DS = 00b	0.75	1	1.25	μs
		TFILTER_DS = 01b	1.5	2	2.5	μs
		TFILTER_DS = 10b, NSD3602H	3.3	4	4.7	μs
		TFILTER_DS = 11b	7	8	8.4	μs
t_{PD_IO}	Input pins propagation delay	IN1/EN, IN2/PH, nHIZx input edge to Gxx edge		500	850	ns
t_{PD_SPI}	SPI command propagation delay	nSCS rising edge to Gxx edge		1	2	μs
$t_{PRE\_CHG\_HS/LS}$	Pre-charge duration for HS/LS	TPCHG_HS/LS = 00b		70		ns
		TPCHG_HS/LS = 01b		140		ns
		TPCHG_HS/LS = 10b		280		ns
		TPCHG_HS/LS = 11b		560		ns
$t_{PRE\_DCHG\_HS/LS}$	Pre-discharge duration for HS/LS	TPDCHG_HS/LS = 00b		140		ns
		TPDCHG_HS/LS = 01b		280		ns
		TPDCHG_HS/LS = 10b		560		ns
		TPDCHG_HS/LS = 11b		980		ns
t_{DRIVE}	Blanking time for MOSFET turn on	TDRIVE=00b, TDRIVE_M = 00b		96		ns
		TDRIVE=01b, TDRIVE_M = 00b		2		μs
		TDRIVE=10b, TDRIVE_M = 00b, NSD3602H		4		μs
		TDRIVE=11b, TDRIVE_M = 00b		8		μs
		TDRIVE=00b, TDRIVE_M = 01b		0.5		μs
		TDRIVE=01b, TDRIVE_M = 01b		1		μs
		TDRIVE=10b, TDRIVE_M = 01b		1.5		μs
		TDRIVE=11b, TDRIVE_M = 01b		2.5		μs
		TDRIVE=00b, TDRIVE_M = 10b		3		μs
		TDRIVE=01b, TDRIVE_M = 10b		6		μs
		TDRIVE=10b, TDRIVE_M = 10b		10		μs
		TDRIVE=11b, TDRIVE_M = 10b		12		μs
		TDRIVE=00b, TDRIVE_M = 11b		16		μs
		TDRIVE=01b, TDRIVE_M = 11b		20		μs
		TDRIVE=10b, TDRIVE_M = 11b		24		μs

		TDRIVE=11b, TDRIVE_M = 11b		32		µs
t_{DEAD}	Digital dead time setting	TDEAD = 000b, TDEAD_M = 0b, NSD3602H		0		µs
		TDEAD = 001b, TDEAD_M = 0b		0.25		µs
		TDEAD = 010b, TDEAD_M = 0b		0.5		µs
		TDEAD = 011b, TDEAD_M = 0b		0.75		µs
		TDEAD = 100b, TDEAD_M = 0b		1		µs
		TDEAD = 101b, TDEAD_M = 0b		2		µs
		TDEAD = 110b, TDEAD_M = 0b		4		µs
		TDEAD = 111b, TDEAD_M = 0b		8		µs
		TDEAD = 000b, TDEAD_M = 1b		3		µs
		TDEAD = 001b, TDEAD_M = 1b		6		µs
		TDEAD = 010b, TDEAD_M = 1b		10		µs
		TDEAD = 011b, TDEAD_M = 1b		12		µs
		TDEAD = 100b, TDEAD_M = 1b		16		µs
		TDEAD = 101b, TDEAD_M = 1b		20		µs
		TDEAD = 110b, TDEAD_M = 1b		32		µs
		TDEAD = 111b, TDEAD_M = 1b		96		µs
t_{DRIVE_LS}	Blanking time for LS MOS turns on	TDRIVE_LS = 0000b		0.5		µs
		TDRIVE_LS = 0001b		1		µs
		TDRIVE_LS = 0010b		1.5		µs
		TDRIVE_LS = 0011b		2		µs
		TDRIVE_LS = 0100b		2.5		µs
		TDRIVE_LS = 0101b		3		µs
		TDRIVE_LS = 0110b		4		µs
		TDRIVE_LS = 0111b		6		µs
		TDRIVE_LS = 1000b		8		µs
		TDRIVE_LS = 1001b		10		µs
		TDRIVE_LS = 1010b		12		µs
		TDRIVE_LS = 1011b		16		µs
		TDRIVE_LS = 1100b		20		µs
		TDRIVE_LS = 1101b		24		µs
		TDRIVE_LS = 1110b		32		µs
		TDRIVE_LS = 1111b		96		µs
t_{DEAD_LS}	Dead time for	TDEAD_LS = 0000b		0		µs

	LS MOS turns off	TDEAD_LS = 0001b		0.25		μs
		TDEAD_LS = 0010b		0.5		μs
		TDEAD_LS = 0011b		0.75		μs
		TDEAD_LS = 0100b		1		μs
		TDEAD_LS = 0101b		2		μs
		TDEAD_LS = 0110b		3		μs
		TDEAD_LS = 0111b		4		μs
		TDEAD_LS = 1000b		6		μs
		TDEAD_LS = 1001b		8		μs
		TDEAD_LS = 1010b		10		μs
		TDEAD_LS = 1011b		12		μs
		TDEAD_LS = 1100b		16		μs
		TDEAD_LS = 1101b		20		μs
		TDEAD_LS = 1110b		32		μs
		TDEAD_LS = 1111b		96		μs

6.5. CSA Electrical Characteristics

4.9V ≤ V_{PVDD} ≤ 37V, 3V ≤ V_{DVDD}/V_{AREF} ≤ 5.5V, -40℃ ≤ T_J ≤ 150℃, all voltages with respect to ground, positive current if flowing into pin.

Symbol	***Parameter***	***Test Conditions***	***Min***	***Typ***	***Max***	***Unit***
V_{com}	CSA input common mode voltage range		-2		VPVDD +2	V
Gain_CSA	CSA gain	CSA_GAIN = 00b ($V_{GAIN} < V_{TH1\_GAIN}$ for NSD3602H)	9.85	10	10.15	V/V
		CSA_GAIN = 01b ($V_{TH1\_GAIN} < V_{GAIN} < V_{TH2\_GAIN}$ for NSD3602H)	19.7	20	20.3	V/V
		CSA_GAIN = 10b ($V_{TH2\_GAIN} < V_{GAIN} < V_{TH3\_GAIN}$ for NSD3602H)	39.4	40	40.6	V/V
		CSA_GAIN = 11b ($V_{TH3\_GAIN} < V_{GAIN}$ for NSD3602H)	78.8	80	81.2	V/V
Gain_DRIFT	Gain temperature drift		-0.5		0.5	%
t_{SET}	Setting time for CSA output step to ±1% target voltage	V_{SO_step} = 1.5V, Gain_CSA = 10V/V Cso = 60pF		2.2		μs
		V_{SO_step} = 1.5V, Gain_CSA = 20V/V		2.2		μs

		Cso = 60pF				
		V_{SO_step} = 1.5V, Gain_CSA = 40V/V Cso = 60pF		2.2		µs
		V_{SO_step} = 1.5V, Gain_CSA = 80V/V Cso = 60pF		3		µs
t_{SET_GAIN}	Setting time for CSA to ±1% target voltage after gain change	After CSN rising edge, Cso = 60pF$^{1)}$			6	µs
t_{slew}	CSA output slew rate	Cso = 60pF		2.5		V/µs
t_{BLK}	CSA blanking switch blank time	CSA_BLANK_SEL = 000b, % of t_{DRIVE}		0		%
		CSA_BLANK_SEL = 001b, % of t_{DRIVE}		25		%
		CSA_BLANK_SEL = 010b, % of t_{DRIVE}		37.5		%
		CSA_BLANK_SEL = 011b, % of t_{DRIVE}		50		%
		CSA_BLANK_SEL = 100b, % of t_{DRIVE}		62.5		%
		CSA_BLANK_SEL = 101b, % of t_{DRIVE}		75		%
		CSA_BLANK_SEL = 110b, % of t_{DRIVE}		87.5		%
		CSA_BLANK_SEL = 111b, % of t_{DRIVE}		100		%
V_{CSA_OFF}	CSA output offset	V_{SP} = V_{SN}, CSA_OFFSET = 0b, NSD3602H		$V_{AREF}/2$		V
		V_{SP} = V_{SN}, CSA_OFFSET = 1b		$V_{AREF}/8$		V
V_{LINEAR}	CSA output linear voltage range	V_{AREF} = 3.3V or 5V	0.25		V_{AREF}-0.25	V
Vin_off	CSA input offset voltage	T_J = 25℃	-1		1	mV
Vin_off_d	CSA input offset voltage drift			±10	±25	µV/℃
Ibias	CSA input bias current	-2V ≤ V_{SP} = V_{SN} ≤ 37V			100	µA
Ibias_off	CSA input bias current mismatching	I_{SP} - I_{SN}, -2V ≤ V_{SP} = V_{SN} ≤ 37V	-1		1	µA
CMRR	Common mode rejection ratio	DC, -40℃≤ T_J ≤125℃	72	90		dB
		DC, -40℃≤ T_J ≤150℃	69	90		dB
		20kHz$^{1)}$		80		dB
PSRR	Power supply rejection ratio$^{1)}$	PVDD to SO, DC		100		dB
		PVDD to SO, 20kHz		90		dB

		PVDD to SO, 400kHz		70		dB
V_{CSA_OC}	CSA OC threshold offset to VCSA_OFF	CSA_OC_TH = 000b CSA_OFFSET = 1b	-0.05	V_{AREF}/8+2*V_{AREF}/24	0.05	V
		CSA_OC_TH = 000b CSA_OFFSET = 0b	-0.05	V_{AREF}/2+1*V_{AREF}/24	0.05	V
			-0.05	V_{AREF}/2-1*V_{AREF}/24	0.05	V
		CSA_OC_TH = 001b CSA_OFFSET = 1b	-0.05	V_{AREF}/8+4*V_{AREF}/24	0.05	V
		CSA_OC_TH = 001b CSA_OFFSET = 0b	-0.05	V_{AREF}/2+2*V_{AREF}/24	0.05	V
			-0.05	V_{AREF}/2-2*V_{AREF}/24	0.05	V
		CSA_OC_TH = 010b CSA_OFFSET = 1b	-0.05	V_{AREF}/8+6*V_{AREF}/24	0.05	V
		CSA_OC_TH = 010b CSA_OFFSET = 0b	-0.05	V_{AREF}/2+3*V_{AREF}/24	0.05	V
			-0.05	V_{AREF}/2-3*V_{AREF}/24	0.05	V
		CSA_OC_TH = 011b CSA_OFFSET = 1b	-0.05	V_{AREF}/8+8*V_{AREF}/24	0.05	V
		CSA_OC_TH = 011b CSA_OFFSET = 0b	-0.05	V_{AREF}/2+4*V_{AREF}/24	0.05	V
			-0.05	V_{AREF}/2-4*V_{AREF}/24	0.05	V
		CSA_OC_TH = 100b CSA_OFFSET = 1b	-0.05	V_{AREF}/8+10*V_{AREF}/24	0.05	V
		CSA_OC_TH = 100b CSA_OFFSET = 0b	-0.05	V_{AREF}/2+5*V_{AREF}/24	0.05	V
			-0.05	V_{AREF}/2-5*V_{AREF}/24	0.05	V
		CSA_OC_TH = 101b CSA_OFFSET = 1b	-0.05	V_{AREF}/8+12*V_{AREF}/24	0.05	V
		CSA_OC_TH = 101b CSA_OFFSET = 0b	-0.05	V_{AREF}/2+6*V_{AREF}/24	0.05	V
			-0.05	V_{AREF}/2-6*V_{AREF}/24	0.05	V
		CSA_OC_TH = 110b CSA_OFFSET = 1b	-0.05	V_{AREF}/8+14*V_{AREF}/24	0.05	V
		CSA_OC_TH = 110b CSA_OFFSET = 0b	-0.05	V_{AREF}/2+7*V_{AREF}/24	0.05	V
			-0.05	V_{AREF}/2-	0.05	V

				$7*V_{AREF}/24$		
		CSA_OC_TH = 111b CSA_OFFSET = 1b	-0.05	$V_{AREF}/8+16*V_{AREF}/24$	0.05	V
		CSA_OC_TH = 111b CSA_OFFSET = 0b	-0.05	$V_{AREF}/2+8*V_{AREF}/24$	0.05	V
			-0.05	$V_{AREF}/2-8*V_{AREF}/24$	0.05	V
t_{CSA_OC}	CSA OC filter time	CSA_OC_TFLT = 000b		1		μs
		CSA_OC_TFLT = 001b		2		μs
		CSA_OC_TFLT = 010b		4		μs
		CSA_OC_TFLT = 011b		6		μs
		CSA_OC_TFLT = 100b		8		μs
		CSA_OC_TFLT = 101b		10		μs
		CSA_OC_TFLT = 110b		50		μs
		CSA_OC_TFLT = 111b		100		μs

1) Not subject to production test, guaranteed by design

6.6. Internal Oscillator Electrical Characteristics

$4.9V \le V_{PVDD} \le 37V$, $3V \le V_{DVDD}/V_{AREF} \le 5.5V$, $-40℃ \le T_J \le 150℃$, all voltages with respect to ground, positive current if flowing into pin.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
fosc	Internal system clock		12.825	14.25$^{1)}$	15.675	MHz

1) In datasheet, if a filter/time parameter does not specify its min or max value, the min and max value follow tolerance of fosc. Also, if fosc modulation is enabled, all filter/time will add this range as additional tolerance

6.7. WD and Thermal Electrical Characteristics

$4.9V \le V_{PVDD} \le 37V$, $3V \le V_{DVDD}/V_{AREF} \le 5.5V$, $-40℃ \le T_J \le 150℃$, all voltages with respect to ground, positive current if flowing into pin.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{WD}	WD timer period	WD_TIMER = 0b	36	40	44	ms
		WD_TIMER = 1b	90	100	110	ms
T_{OTW}	Thermal warning temperature	$^{1)}$	120	140	160	℃
T_{OTSD}	Thermal shutdown temperature	$^{1)}$	150	170	190	℃
T_{HYS}	Thermal hysteresis	$^{1)}$		15		℃
t_{OTW}		$^{1)}$	7	10	13	μs
t_{OTSD}		$^{1)}$	7	10	13	μs

1) Not subject to production test, guaranteed by design

6.8. SPI Timing Requirement and Electrical Characteristics

Symbol	*Parameter*	*Test Conditions*	*Min*	*Typ*	*Max*	*Unit*
t_{SCLK}	SCLK minimum period	1)	100			ns
t_{SCLKH}	SCLK minimum high time	1)	37			ns
t_{SCLKL}	SCLK minimum low time	1)	37			ns
t_{SU_SDI}	SDI input data setup time	1)	25			ns
t_{H_SDI}	SDI input data hold time	1)	25			ns
t_{D_SDO}	SDO output data delay time, CL=20pF	1)			30	ns
t_{SU_nSCS}	nSCS input setup time	1)	25			ns
t_{H_nSCS}	nSCS input hold time	1)	25			ns
t_{HI_nSCS}	nSCS minimum high time	1)	450			ns
t_{D_nSCS}	Enable delay time, nSCS low to SDO active	1)			50	ns
t_{DIS_nSCS}	Disable delay time, nSCS high to SDO tri-state	1)			50	ns

1) Not subject to production test, guaranteed by design

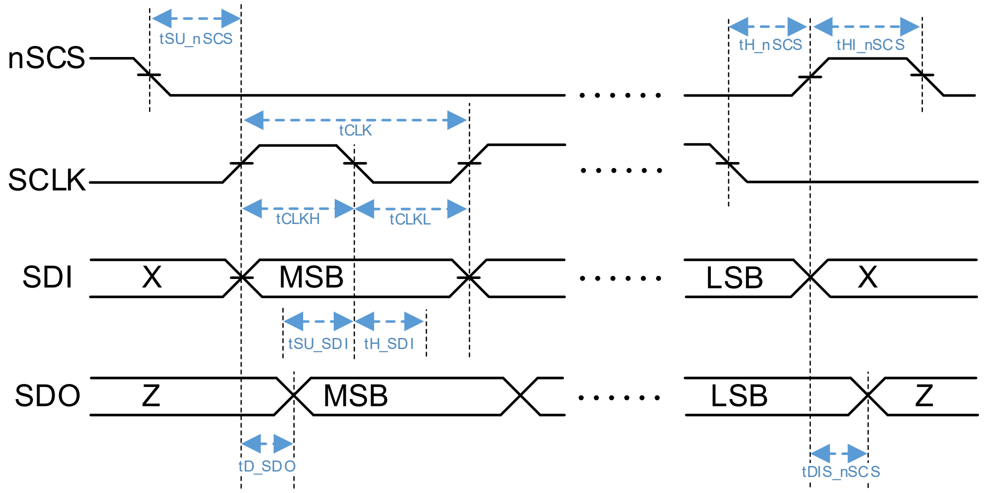


Figure 6.1 SPI Timing Diagram

7. Function Description

7.1. Power Supply

7.1.1. General Description

Device requires three power supplies: V_{PVDD}, V_{DVDD} and V_{AREF}. V_{PVDD} supplies charge pump for gate drivers and CSA input stage. V_{DVDD} supplies digital I/O ports, internal voltage regulator and digital logic. V_{AREF} supplies CSA output stage.

It is recommended to put ceramic capacitors connected close to these supplies and ground planes.

V_{PVDD}, V_{DVDD} and V_{AREF} are monitored for supply faults, V_{PVDD} is monitored for undervoltage and overvoltage faults while V_{DVDD} and V_{AREF} are monitored for undervoltage fault.

7.1.2. Detailed Description

7.1.2.1. VPVDD Undervoltage Monitor

When V_{PVDD} falls below $V_{PVDD\_UV\_L}$ for longer than t_{PVDD_UV}, NSD3602S/H detects a PVDD undervoltage fault, in NSD3602S fault reaction can be set by PVDD_UV_MODE register bit.

In NSD3602H, fault reaction is the same as NSD3602S while PVDD_UV_MODE = 1b.

- ■ PVDD_UV_MODE = 0b, PVDD undervoltage fault is set as latch fault (by default)

  After fault happens, device will do following things:

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to passive discharge state
  - Set FAULT and PVDD_VCP_UV_OR bit in GEN_STA_1 register, nFLT pin will also be activated
  - Set PVDD_UV bit in GEN_STA_2
  - Disable charge pump (pay attention that VCP undervoltage will not be detected after charge pump is disabled)
  - Disable CSA (SO will be in high impedance state)

  After fault ends (V_{PVDD} exceeds $V_{PVDD\_UV\_H}$ for longer than t_{PVDD_UV}), device has no reaction till SPI send clear fault command (write DIAG_CLR = 1b), after clear fault command, device will do following things:

  - Clear FAULT, PVDD_VCP_UV_OR and PVDD_UV bits, release nFLT pin
  - Re-start charge pump
  - All gate drivers and CSA will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$

- ■ PVDD_UV_MODE = 1b, PVDD undervoltage fault is set as auto recover fault

  After fault happens, device will do following things:

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to passive discharge state
  - Set FAULT and PVDD_VCP_UV_OR bit in GEN_STA_1 register, nFLT pin will also be activated
  - Set PVDD_UV bit in GEN_STA_2
  - Disable charge pump (pay attention that VCP undervoltage will not be detected after charge pump is disabled)
  - Disable CSA (SO will be in high impedance state)

  After fault ends (V_{PVDD} exceeds $V_{PVDD\_UV\_H}$ for longer than t_{PVDD_UV}), device will do following things:

  - Clear FAULT bit, release nFLT pin
  - Re-start charge pump
  - All gate drivers and CSA will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$
  - PVDD_VCP_UV_OR and PVDD_UV will keep status till SPI send clear fault command (write DIAG_CLR = 1b)

7.1.2.2. VPVDD Overvoltage Monitor

When V_{PVDD} exceeds $V_{PVDD\_OV\_H}$ for longer than t_{PVDD_OV}, NSD3602S detects a PVDD overvoltage fault, the fault reaction can be set by PVDD_OV_MODE bits, overvoltage threshold and filter time are configurable by PVDD_OV_TH and PVDD_OV_TFILTER bits.

In NSD3602H, there is no PVDD overvoltage monitor.

- ■ PVDD_OV_MODE = 00b, PVDD overvoltage fault is set as latch fault (by default)

  After fault happens, device will do following things:

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to passive discharge state if CP_DIS_PVDD_OV = 1b. If CP_DIS_PVDD_OV = 0b, after t_{FLT_OFF}, gate drivers move to active off by I_{STRONG} discharge current
  - Set FAULT and OV bit in GEN_STA_1 register, nFLT pin also be activated
  - Set PVDD_OV bit in GEN_STA_2
  - Disable charge pump after t_{FLT_OFF} if CP_DIS_PVDD_OV = 1b. If CP_DIS_PVDD_OV = 0b, charge pump will keep running during PVDD overvoltage
  - Disable CSA (SO will be in high impedance) if CP_DIS_PVDD_OV = 1b. If CP_DIS_PVDD_OV = 0b, CSA will keep running during PVDD overvoltage

  After fault ends (V_{PVDD} falls below $V_{PVDD\_OV\_L}$ for longer than t_{PVDD_OV}), device has no reaction till SPI send clear fault command (write DIAG_CLR = 1b), after clear fault command, device will do following things:

  - Clear FAULT, OV and PVDD_OV bits, release nFLT pin
  - Re-start charge pump if disabled previously
  - All gate drivers will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$
  - CSA will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$ if disabled previously

- PVDD_OV_MODE = 01b, PVDD overvoltage fault is set as auto recover fault

  After fault happens, device will do following things:

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to passive discharge sate if CP_DIS_PVDD_OV = 1b. If CP_DIS_PVDD_OV = 0b, after t_{FLT_OFF}, gate drivers move to active off by I_{STRONG} discharge current
  - Set FAULT and OV bits in GEN_STA_1 register, nFLT pin also be activated
  - Set PVDD_OV bit in GEN_STA_2
  - Disable charge pump after t_{FLT_OFF} if CP_DIS_PVDD_OV = 1b. If CP_DIS_PVDD_OV = 0b, charge pump will keep running during PVDD overvoltage
  - Disable CSA (SO will be in high impedance) if CP_DIS_PVDD_OV = 1b. If CP_DIS_PVDD_OV = 0b, CSA will keep running during PVDD overvoltage

  After fault ends (V_{PVDD} falls below $V_{PVDD\_OV\_L}$ for longer than t_{PVDD_OV}), device will do following things:

  - Clear FAULT bit, release nFLT pin
  - Re-start charge pump if disabled previously
  - All gate drivers will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$
  - CSA will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$ if disabled previously
  - OV and PVDD_OV will keep status till SPI send clear fault command (write DIAG_CLR = 1b)

- PVDD_OV_MODE = 10b, PVDD overvoltage fault is set as warning fault

  After fault happens, device will do following things:

  - Set WARN and OV bits in GEN_STA_1 register
  - Set PVDD_OV bit in GEN_STA_2 register
  - After fault ends (V_{PVDD} falls below $V_{PVDD\_OV\_L}$ for longer than t_{PVDD_OV}), WARN, OV and PVDD_OV will keep status till SPI send clear fault command (write DIAG_CLR = 1b)

- PVDD_OV_MODE = 11b, PVDD overvoltage fault is set as no fault

  After fault happens, device will do nothing

7.1.2.3. VDVDD Undervoltage Monitor

When V_{DVDD} falls below $V_{DVDD\_POR\_L}$ for longer than t_{DVDD_POR}, NSD3602S/H will enter sleep mode with all function disabled, gate driver will move to passive discharge state. After V_{DVDD} exceeds $V_{DVDD\_POR\_H}$, device will power on reset (POR), after POR successfully all register bits will be set with default values, POR bit in GEN_STA_1 will be 1 until SPI send clear fault command.

Note:

1. After POR there is delay (t_{wake}) before device enter normal mode
2. If V_{DVDD} drops to 0V too fast, device will enter sleep mode directly without t_{DVDD_POR} filter time

7.1.2.4. VAREF Undervoltage Monitor

When V_{AREF} falls below $V_{AREF\_UV\_L}$ for longer than t_{AREF_UV}, NSD3602S detects an AREF undervoltage fault, device will set AREF_UV and OT_WD_CSA_OR bits, after V_{AREF} exceeds $V_{AREF\_UV\_H}$ for longer than t_{AREF_UV}, AREF_UV and OT_WD_CSA_OR bits can be cleared by sending SPI clear fault command (write DIAG_CLR = 1b).

In NSD3602H there is no AREF undervoltage monitor.

7.2. Charge Pump

7.2.1. General Description

The single stage charge pump provides a stable voltage (V_{VCP}) above V_{PVDD} for high side gate drivers, external reverse protection circuit and so on. With stable voltage above V_{PVDD}, high side gate drivers can drive external N-channel MOSFETs properly across a wide supply voltage range. Some faults will lead charge pump disabled, otherwise charge pump will keep running while nSLEEP is high, during running Charge pump provides few configuration options.

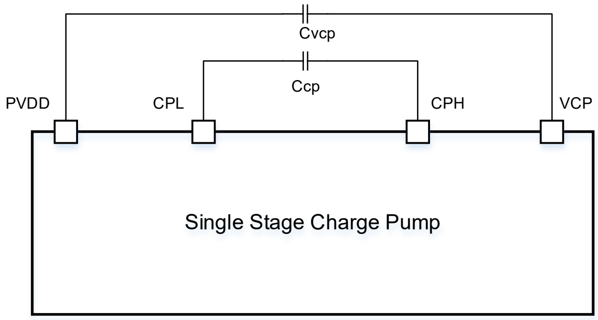


Figure 7.1 Charge Pump Block Diagram

7.2.2. Detailed Description

7.2.2.1. Frequency Modulation

The Charge pump clock has spread spectrum solution used to reduce emission. In NSD3602S CP_SS_DIS bit can be used to enable or disable spread spectrum function.

In NSD3602H spread spectrum function is always enabled with 16.5kHz modulation frequency.

- CP_SS_DIS = 0b: spread spectrum enabled (modulation frequency can be 33kHz/16.5kHz depend on CP_SS_CONFIG bit).
- CP_SS_DIS = 1b: spread spectrum disabled, charge pump working frequency is always fcp.

7.2.2.2. VCP Undervoltage Monitor

When V_{VCP} falls below $V_{VCP\_UV\_L}$ for longer than t_{VCP_UV}, NSD3602S/H detects a VCP undervoltage fault, in NSD3602S the fault reaction can be set by VCP_UV_MODE bit, undervoltage threshold $V_{VCP\_UV\_L}$ can be configured by VCP_UV_TH and VCP_UV_TH_M bits.

In NSD3602H, undervoltage reaction and threshold is the same with NSD3602S while VCP_UV_MODE = 1b, VCP_UV_TH = 0b and VCP_UV_TH_M = 0b.

- VCP_UV_MODE = 0b, VCP undervoltage fault is set as latch fault (by default)

After fault happens, device will do following things:

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to passive discharge state
  - Set FAULT and PVDD_VCP_UV_OR bits in GEN_STA_1 register, nFLT pin also be activated
  - Set VCP_UV bit in GEN_STA_2
  - Disable charge pump
  - Disable CSA (SO will be in high impedance state)

Device keeps previous status till SPI send clear fault command (write DIAG_CLR = 1b), after clear fault command, device will do following things:

  - Re-start charge pump
  - Clear FAULT, PVDD_VCP_UV_OR and VCP_UV bits, release nFLT pin
  - All gate drivers and CSA will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$

- VCP_UV_MODE = 1b, VCP undervoltage fault is set as auto recover fault

After fault happens, device will do following things:

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to passive discharge state
  - Set FAULT and PVDD_VCP_UV_OR bits in GEN_STA_1 register, nFLT pin also be activated
  - Set VCP_UV bit in GEN_STA_2
  - Disable CSA (SO will be in high impedance state)
  - Charge pump keeps running

After V_{VCP} exceeds $V_{VCP\_UV\_H}$ for longer than t_{VCP_UV}, device will do following things:

  - Clear FAULT bit, release nFLT pin
  - All gate drivers and CSA will re-work following current configuration in registers
  - PVDD_VCP_UV_OR and VCP_UV will keep status till SPI send clear fault command (write DIAG_CLR = 1b)

7.3. Input and Output Pins

7.3.1. General Description

NSD3602S and NSD3602H have different interface, some IOs are only presented in NSD3602S or NSD3602H

7.3.2. Detailed Description

7.3.2.1. nSLEEP

nSLEEP pin has same function and structure in NSD3602S and NSD3602H. It has internal pulldown resistor RPD and t_{nSLEEP_FLT} filter time.

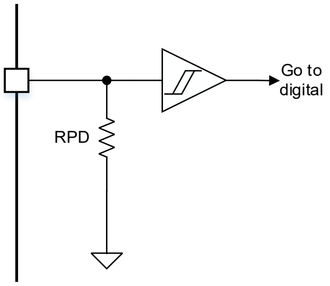


Figure 7.2 nSLEEP Pin Diagram

After nSLEEP turns high, device will enter normal mode and set POR = 1b with t_{wake} delay. Device enters sleep mode by setting nSLEEP pin to low, after nSLEEP turns low, device will enter sleep mode with t_{dsleep} delay, within t_{dsleep} device will turn off external MOSFETS by discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to passive discharge state, if nSLEEP is set to high within t_{dsleep}, device will still finish turn off sequence and reset firstly, then move to normal mode again.

7.3.2.2. DRVOFF

DRVOFF pin has same function and structure in NSD3602S and NSD3602H. It has internal pulldown resistor RPD and t_{DRVOFF} filter time.

DRVOFF pin provides a direct switch off input signal, after DRVOFF turns high, device will turn off all external MOSFETs directly by discharge current set by ISINK_FLT bits for t_{FLT_OFF} then move to active off state while ignoring SPI command, IN1/EN, IN2/PH and nHIZx pin voltages.

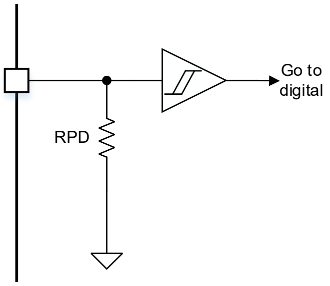


Figure 7.3 DRVOFF Pin Diagram

7.3.2.3. nFLT

nFLT pin has same function and structure in NSD3602S and NSD3602H. nFLT pin works as an open drain fault interrupt for MCU, if device meets fault the open drain structure will active, nFLT pin only have leakage if not active.

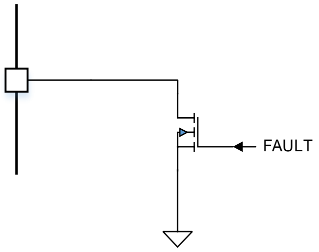


Figure 7.4 nFLT Pin Diagram

7.3.2.4. IN1/EN, IN2/PH, nHIZx

NSD3602 provides 4 input pins (IN1/EN, IN2/PH, nHIZ1 and nHIZ2) with deglitch time and pulldown resistor, these pins are used to control half bridge gate drivers. The control logic can be configured or modified by DRV_MODE register bits for NSD3602S and MODE pin input voltage for NSD3602H.

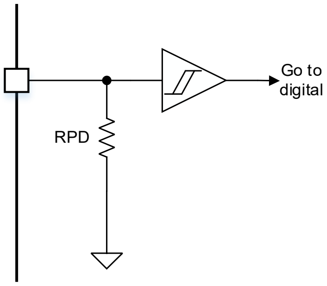


Figure 7.5 IN1/EN, IN2/PH and nHIZx Pin Diagram

Detailed control logic is described below:

- Half bridge control logic

  Half bridge control logic can be entered by setting DRV_MODE = 00b (NSD3602S) or $V_{MODE} < V_{TH1\_MODE}$ (NSD3602H).

  In half bridge control mode, each half bridge (HBx) can be controlled by INx (IN1/EN, IN2/PH), nHIZx and SPI bits independently (SPI bits only for NSD3602S, in NSD3602H half bridge control logic is the same as NSD3602S while DRV_EN = 1b, INx_MODE = 0b, SPI_HIZx = 0b and SPI_INx = 0b).

Table 7.1 NSD3602S and NSD3602H half bridge control logic

Brake function	DRV_EN	!nHIZx or SPI_HIZx	INx	SPI_INx	INx_MODE	GHx	GLx
Off	0	x	x	x	x	Passive off	Passive off
Active	0	x	x	x	x	Passive off	Brake on
Off	1	1	x	x	x	Active off	Active off
Off	1	0	0	x	0	Active off	Active on
Off	1	0	1	x	0	Active on	Active off
Off	1	0	x	0	1	Active off	Active on
Off	1	0	x	1	1	Active on	Active off

Note:

Passive off means external MOSFET is kept off by passive discharge block

Active off means external MOSFET is kept off by ISTRONG block

Active on means external MOSFET is kept on by IHOLD block

Brake on means external MOSFET is kept on by brake block

- H-bridge EN/PH control logic

  H-bridge EN/PH control logic can be entered by setting DRV_MODE = 01b (NSD3602S) or $V_{TH2\_MODE} > V_{MODE} > V_{TH1\_MODE}$ (NSD3602H).

  In H-bridge EN/PH control mode, both half bridges are controlled by IN1/EN, IN2/PH and DRV_FW bit (SPI bit only for NSD3602S, in NSD3602H the H-bridge EN/PH control logic is same with NSD3602S while DRV_EN = 1b and DRV_FW = 0b)

Table 7.2 NSD3602S and NSD3602H H-bridge EN/PH control logic

Brake function	*DRV_EN*	*IN1/EN*	*IN2/PH*	*DRV_FW*	*GH1*	*GL1*	*GH2*	*GL2*
Off	0	x	x	x	Passive off			
Active	0	x	x	x	Passive off	Brake on	Passive off	Brake on
Off	1	0	x	0	Active off	Active on	Active off	Active on
Off	1	0	x	1	Active on	Active off	Active on	Active off
Off	1	1	0	x	Active off	Active on	Active on	Active off
Off	1	1	1	x	Active on	Active off	Active off	Active on

- H-bridge PWM control logic

  H-bridge PWM control logic can be entered by setting DRV_MODE = 10b (NSD3602S) or $V_{TH3\_MODE} > V_{MODE} > V_{TH2\_MODE}$ (NSD3602H).

  In H-bridge PWM control mode, both half bridges are controlled by INx (IN1/EN, IN2/PH) and DRV_FW bit (SPI bit only for NSD3602S, in NSD3602H the H-bridge PWM control logic is same with NSD3602S while DRV_EN = 1b and DRV_FW = 0b)

Table 7.3 NSD3602S and NSD3602H H-bridge PWM control logic

Brake function	*DRV_EN*	*IN1/EN*	*IN2/PH*	*DRV_FW*	*GH1*	*GL1*	*GH2*	*GL2*
Off	0	x	x	x	Passive off			
Active	0	x	x	x	Passive off	Brake on	Passive off	Brake on
Off	1	0	0	x	Active off			
Off	1	0	1	x	Active off	Active on	Active on	Active off
Off	1	1	0	x	Active on	Active off	Active off	Active on
Off	1	1	1	0	Active off	Active on	Active off	Active on
Off	1	1	1	1	Active on	Active off	Active on	Active off

- Split control logic

  Split control logic can be entered by setting DRV_MODE = 11b (NSD3602S) or $V_{MODE} > V_{TH3\_MODE}$ (NSD3602H).

  In split control mode, only HS1 and LS2 can be turned on, HS2 and LS1 are kept off, nHIZx, SPI_HIZx bit are disabled (SPI bit only for NSD3602S, in NSD3602H the split control logic is same with NSD3602S while DRV_EN = 1b)

Table 7.4 NSD3602S and NSD3602H split control logic

Brake function	*DRV_EN*	*IN1/EN*	*IN2/PH*	*DRV_FW*	*GH1*	*GL1*	*GH2*	*GL2*
Off	0	x	x	x	Passive off			
Active	0	x	x	x	Passive off	Brake on	Passive off	Brake on

Off	1	0	0	x	Active off			
Off	1	1	0	x	Active on	Active off	Active off	Active off
Off	1	0	1	x	Active off	Active off	Active off	Active on
Off	1	1	1	x	Active on	Active off	Active off	Active on

7.3.2.5. nSCS/GAIN

Internal structure of nSCS/GAIN input pin is different in NSD3602S and NSD3602H, please refer to diagram below. In NSD3602S nSCS/GAIN work as nSCS pin for SPI function (refer to SPI interface part). In NSD3602H nSCS/GAIN work as GAIN pin, different external connection of GAIN (pull up/down by external resistor or floating) will lead different internal digital signal by three internal comparator, digital core will latch these signals after POR and use these signals to set GAIN of CSA, please refer to CSA part for GAIN mapping.

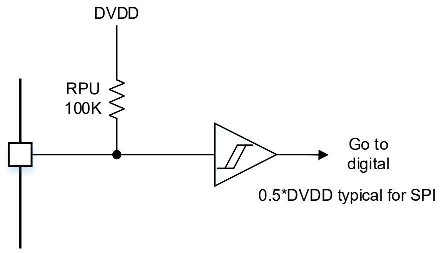


Figure 7.6 nSCS Pin Diagram in NSD3602S

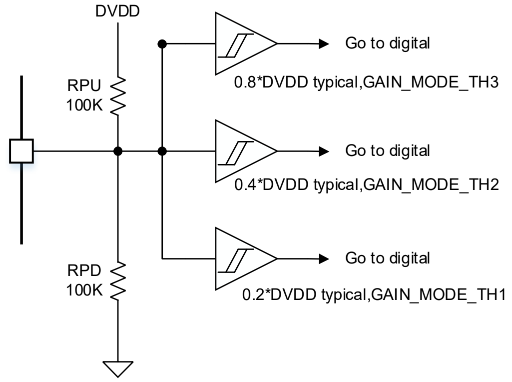


Figure 7.7 GAIN Pin Diagram in NSD3602H

7.3.2.6. SDI/IDRIVE, SCLK/VDS

Internal structure of SDI/IDRIVE and SCLK/VDS input pin are different in NSD3602S and NSD3602H, please refer to diagram below.

In NSD3602S SDI/IDRIVE and SCLK/VDS work as SDI and SCLK pin for SPI function (refer to SPI interface part).

In NSD3602H SDI/IDRIVE and SCLK/VDS work as IDRIVE and VDS pin, different external connection of IDRIVE/VDS (pull up/down by external resistor or floating) will lead different internal digital signal by five internal comparators, digital core will latch these signals after POR and use these signals to set charge/discharge current and VDS OV threshold, detailed mapping is in Gate driver part.

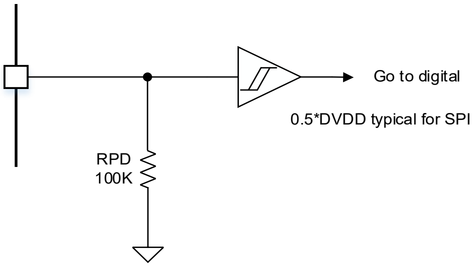


Figure 7.8 SDI and SCLK Pin Diagram in NSD3602S

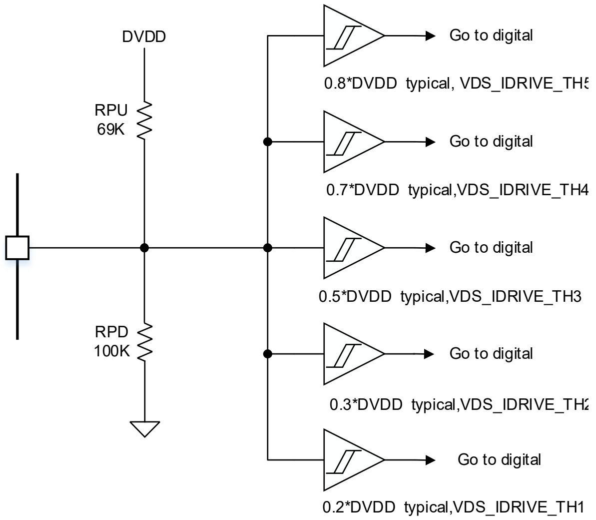


Figure 7.9 IDRIVE and VDS Pin Diagram in NSD3602H

7.3.2.7. SDO/MODE

Internal structure of SDO/MODE input pin is different in NSD3602S and NSD3602H, please refer to diagram below.

In NSD3602S SDO/MODE work as SDO pin for SPI function (refer to SPI interface part).

In NSD3602H SDO/MODE work as MODE pin, different external connection of MODE (pull up/down by external resistor or floating) will lead different internal digital signal by three internal comparators, digital core will latch these signal after POR and use these signal to set HBx control logic, please refer to 7.3.2.4 for details.

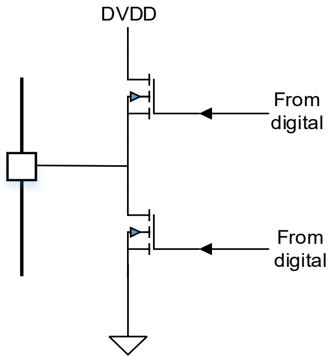


Figure 7.10 SDO Pin Diagram in NSD3602S

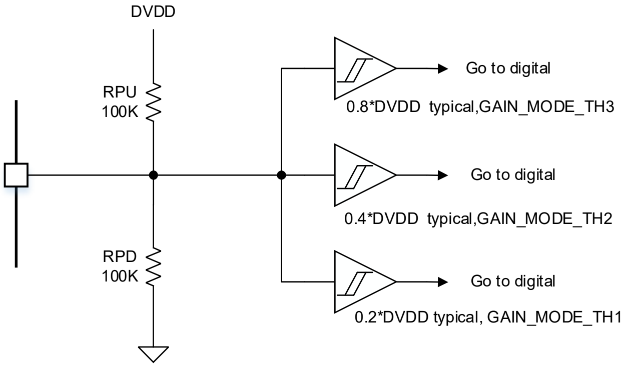


Figure 7.11 MODE Pin Diagram in NSD3602H

7.3.2.8. BRAKE

NSD3602S/H provide brake function to turn on both low side gate driver in sleep and normal mode (normal mode only for NSD3602S, there is no brake function in NSD3602H while NSD3602H in normal mode), the turn on/off current and duration are fixed, also during turn on there is dedicated VDS OV monitor for short protection with fixed threshold and filter time.

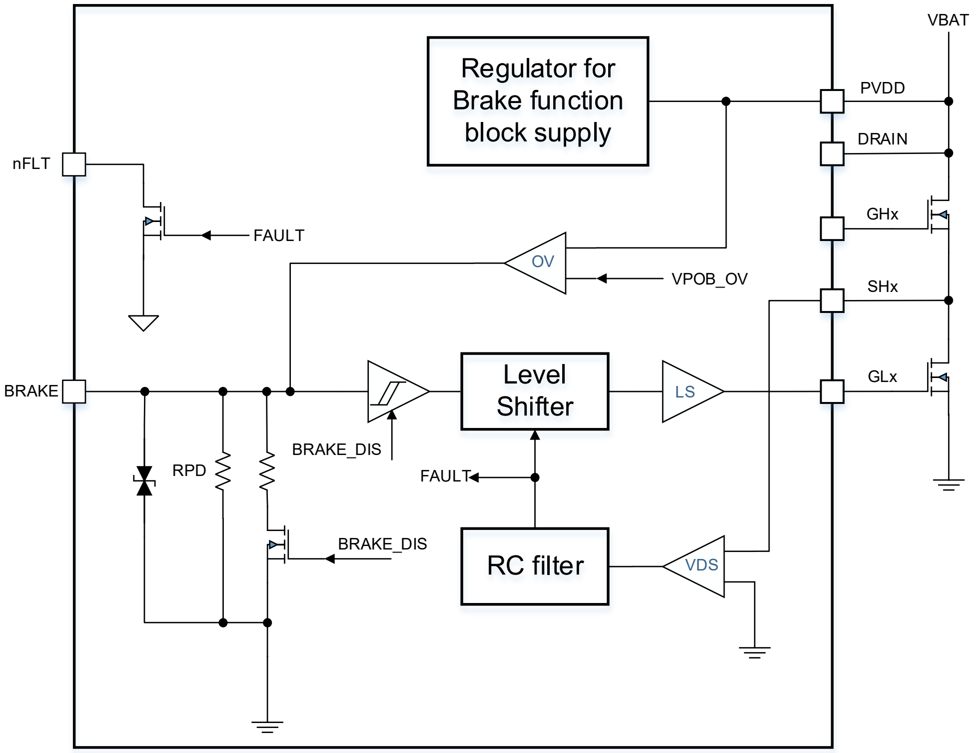


Figure 7.12 Brake Function Block Diagram

- Brake function can be disabled by 2 options
  - Option1: In sleep mode or normal mode, BRAKE pin pulled to GND can disable brake function (if BRAKE pin is floating, PVDD overvoltage still can trigger Brake function)
  - Option2: In normal mode, set BRAKE_DIS = 1b will disable brake function (SPI bit only for NSD3602S, in NSD3602H there is no brake function in normal mode)
- Brake function can be activated by 2 options if disable options above are not present
  - Option1: Internal PVDD overvoltage detection, when V_{PVDD} exceeds $V_{POB\_OV\_H}$ for longer than t_{brake_on}, low side gate drivers will source I_{POB_P} to turn on external MOSFETS and keep this source current to keep MOSFETS on, after t_{POB_ON} VDS OV monitor will start.

    When V_{PVDD} falls below $V_{POB\_OV\_L}$ for t_{brake_off}, low side gate drivers will sink I_{POB_N} to turn off external MOSFETS for t_{POB_OFF} time, after t_{POB_OFF} low side gate drivers will enter passive discharge state
  - Option2: Brake pin is pulled to high, after t_{brake_on} filter time low side gate drivers will source I_{POB_P} to turn on external MOSFETS and keep this source current to keep MOSFETS on, after t_{POB_ON} VDS OV monitor will start.

    When brake pin is pulled low, after t_{brake_off} filter time, low side gate drivers will sink I_{POB_N} to turn off external MOSFETS for t_{POB_OFF} time, after t_{POB_OFF} low side gate drivers will enter passive discharge state
- VDS OV monitor in brake function

  After brake function is activated, VDS OV monitor will start working after t_{POB_ON} with t_{POB_VDS} filter, if VDS of any low side MOSFET exceeds V_{POB_VDS} for longer than t_{POB_VDS}, device will do following things
  - The low side gate driver which meet VDS OV will keep sink I_{POB_N} to turn off external MOSFET
  - If nSLEEP is low nFLT pin will be activated, if nSLEEP is high and BRAKE_DIS = 0b, nFLT pin also will be activated and FAULT bit will be set, VDS OV will also set dedicated bits in VGS_VDS_STA register (VDS_VGS_FLT_OR also will be set)

  When VDS of the affected low side falls below V_{POB_VDS} for longer than t_{POB_VDS}, device will do following things:
  - The affected low side will be turned on again (VDS OV monitor will start working immediately without t_{POB_ON} blanking time)
  - FAULT will be cleared and nFLT pin released if activated previously
  - Other register bits will keep till SPI send clear fault command (write DIAG_CLR = 1b)

Table 7.5 Brake Function Status Overview

nSLEEP	BRAKE_DIS	Brake Pin	PVDD OV	LS1~LS2	nFLT OD
0	X	0	X	Passive off (brake function disabled)	Released
0	X	1	X	Active on by brake function	Active if VDS OV
0	X	HIZ	1	Active on by brake function	Active if VDS OV
1	0	0	X	Follow SPI (brake function disabled)	Active by fault
1	0	1	X	Active on by brake function (better MCU turn off HS1~HS2 before enable brake function)	Can active by VDS OV
1	0	HIZ	1	Active on by brake function (better MCU turn off HS1~HS2 before enable brake function)	Can active by VDS OV
1	1	X	X	Follow SPI (brake function disabled)	Active by fault

Notes:

1. In NSD3602H, brake function is only available when nSLEEP is low
2. In NSD3602S, if user wants to enable brake function in normal mode, DRV_EN = 0b needs to be set before BRAKE_DIS = 0b is set. When DRV_EN = 1b and BRAKE_DIS = 0b occur at the same time, NSD3602S will do logic as DRV_EN = 0b and BRAKE_DIS = 1b

7.3.2.9. SPI Interface

7.3.2.9.1. GENERAL DESCRIPTION

NSD3602S has a SPI interface to set device configurations, operating parameters and read out diagnostic information. The SPI interface consists of four wires:

- The nSCS pin is selection input, falling edge of nSCS starts SPI communication, nSCS has internal pullup resistor RPU.
- The SDI pin is data input, SDI has internal pulldown resistor RPD
- The SDO pin is data output, SDO internal is push pull structure
- The SCLK pin is clock input, SDI data will be shifted in on falling edge of SCLK, data will be shifted out on rising edge of SCLK, SCLK has internal pulldown resistor RPD

7.3.2.9.2. TIMING DESCRIPTION

To have successful communication, below condition should be meet:

- The most significant bit (MSB) is shifted in/out firstly
- SCLK should be low at nSCS edge
- nSCS should be high between two frames
- SCLK and SDI input will be ignored while nSCS is high
- SDO is in HIZ mode while nSCS is high
- For master (MCU), SDI data is shift out at SCLK rising edge, SDO data is captured at SCLK falling edge
- For slave (NSD3602S), SDI data is captured at SCLK falling edge, SDO data is shift out at SCLK rising edge

Detailed timing please refer to Figure 6.1

7.3.2.9.3. SPI FORMAT

The SPI input data (SDI) frame consists of 16 bits: 8 bits command (A1 byte below) and 8 bits data (D1 byte below). The SPI output data (SDO) frame consists of global status indication bits (S1 byte below) and register data (R1 byte below) being accessed by current read command or write command.

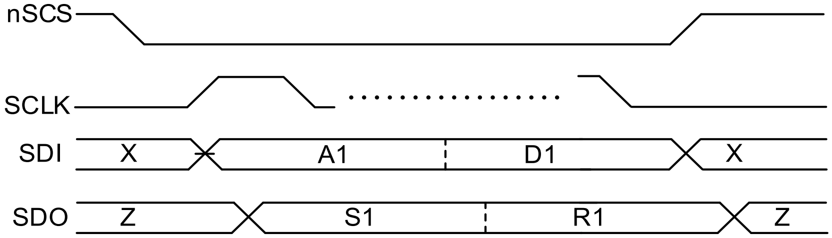


Figure 7.13 SPI Format Overview Diagram

Detailed format as below:

Table 7.6 SDI Input Data Format

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 7.7 SDO Output Data Format

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	FAULT	WARN	VDS_VGS_FLT_OR	PVDD_VCP_UV_OR	OV	OT_WD_CSA_OR/nSPI_OK	D7	D6	D5	D4	D3	D2	D1	D0

SDI input data:

- B15: fixed 0b
- B14: W0=1b means read command, W0=0b means write command
- B8~B13: 6 address bits A0~A5
- B0~B7: 8 data bits

SDO output data:

- B13: FAULT same value with FAULT in GEN_STA_1(0x00)
- B12: WARN same value with WARN in GEN_STA_1(0x00)
- B11: VDS_VGS_FLT_OR same value with VDS_VGS_FLT_OR in GEN_STA_1(0x00)
- B10: PVDD_VCP_UV_OR same value with PVDD_VCP_UV_OR in GEN_STA_1(0x00)
- B9: OV same value with OV in GEN_STA_1(0x00)
- B8: OT_WD_CSA_OR/nSPI_OK is logic OR from OT_WD_CSA_OR bit in GEN_STA_1(0x00) and nSPI_OK which inverted from SPI_OK in GEN_STA_1(0x00)
- B0~B7: 8 data bits

7.3.2.9.4. SPI CLOCK MONITOR

If number of SCLK pulses received during nSCS=low is not multiple of 16(also include SCLK=1 during nSCS falling), device will detect SPI clock error, device will do things below:

- Error frame is ignored
- SPI_OK bit cleared and SPI_CLK_FLT bit is set, these two bits can only be recovered (SPI_OK = 1b, SPI_CLK_FLT = 0b) by SPI clear command

Note: if number of SCLK pulses during nSCS=low equals to 0, device will not detect a SPI clock error

7.3.2.9.5. SPI ADDRESS MONITOR

If address of SPI frame is higher than 0x16, device will detect SPI address error, device will do things below:

- Error frame is ignored
- SPI_OK bit cleared and SPI_ADDR_FLT bit is set, these two bits can only be recovered (SPI_OK = 1b, SPI_ADDR_FLT = 0b) by SPI clear command

7.3.2.9.6. SPI DEDICATED COMMAND

- SPI clear fault command, write command with DIAG_CLR = 1b will clear error bits if corresponding fault already not present

- SPI lock/unlock register command, write command to GEN_CTRL_1 register(0x04) with LOCK bits = 110b, then all control registers except LOCK bits in GEN_CTRL_1 register(0x04) cannot be written but can be read, write command to GEN_CTRL_1 register(0x04) with LOCK bits = 011b, then all control registers can be written again

7.3.2.9.7. SPI SUPPORTED OPERATION FOR MULTIPLE DEVICES

- Without Daisy chain

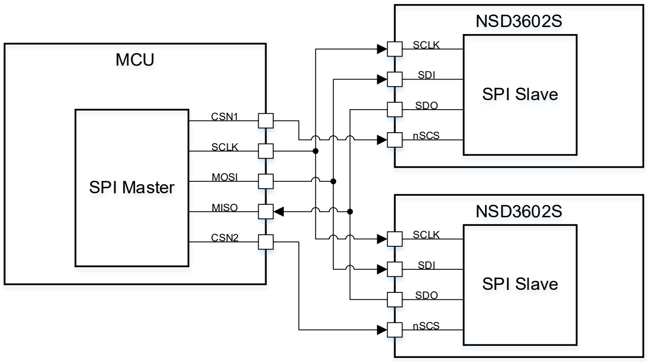


Figure 7.14 Without Daisy Chain Operation Diagram

- With Daisy chain

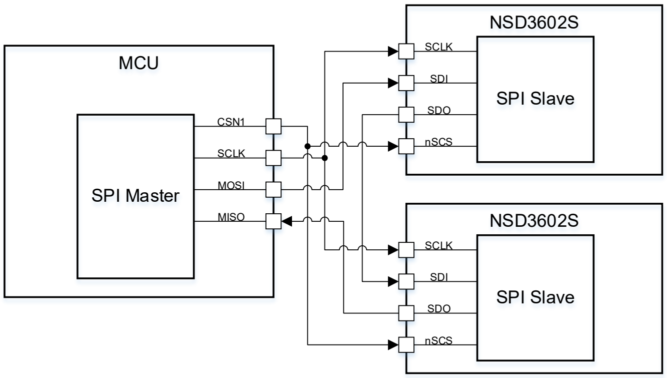


Figure 7.15 Daisy Chain Operation Diagram

Detailed daisy chain topology for 3 devices as below:

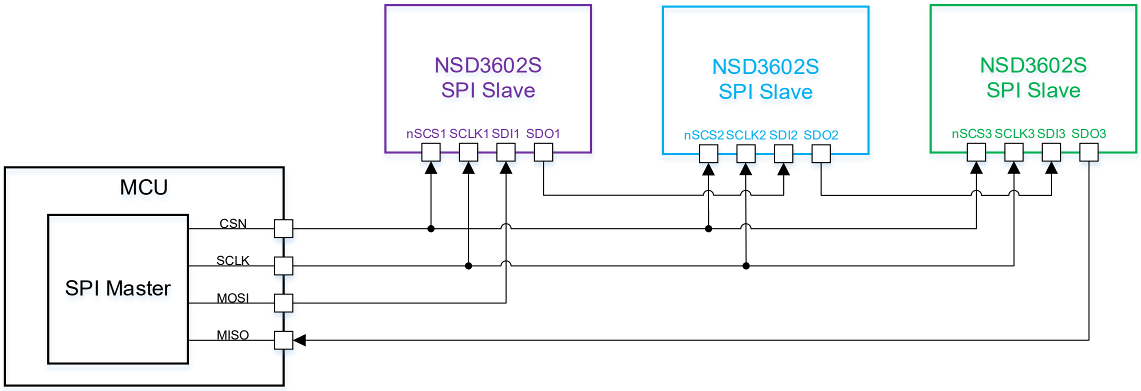
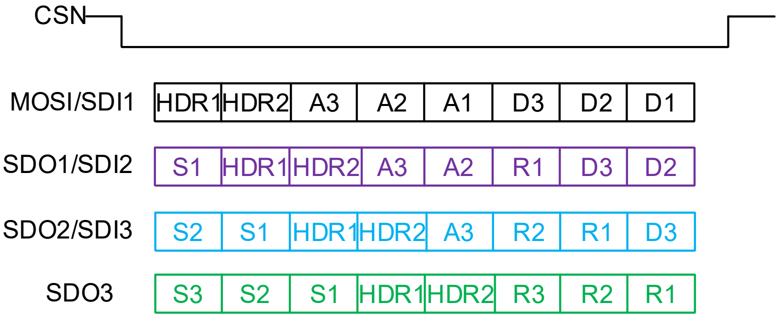


Figure 7.16 Daisy Chain Operation for 3 Devices

Detailed SPI format for daisy chain SPI operation as below, A1~A3, D1~D3, S1~S3 and R1~R3 have same meaning/definition with single device operation described in 7.3.2.9.3



MOSI/SDI1	HDR1	HDR2	A3	A2	A1	D3	D2	D1
SDO1/SDI2	S1	HDR1	HDR2	A3	A2	R1	D3	D2
SDO2/SDI3	S2	S1	HDR1	HDR2	A3	R2	R1	D3
SDO3	S3	S2	S1	HDR1	HDR2	R3	R2	R1

Figure 7.17 SPI Format for 3 Devices Daisy Chain

There are two header bytes dedicated for daisy chain operation

- HDR1 byte contain information of the number of devices connected in the chain by N0~N5 bits, so device support up to 63 devices, other bits are fixed
- HDR2 byte contain CLR bit which can trigger SPI clear command for all device in daisy chain, other bits are fixed (bit7 and bit6) or not care(bit0~bit4)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HDR1	1	0	N5	N4	N3	N2	N1	N0

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HDR2	1	0	CLR	X	X	X	X	X

Figure 7.18 Daisy Chain Header Bytes Format

Note: Internal logic will count number of status bytes it receives before HDR1 and HDR2 to know the position of itself in the chain, also by HDR1 it knows how many devices in the chain, so it only loads the relevant address and data byte in its buffer and bypass the other bytes

7.4. Operation Mode

NSD3602S/H has two stable operation mode:

- Sleep mode. If nSLEEP turns low, device will enter sleep mode with t_{dsleep} delay, or if V_{DVDD} falls below $V_{DVDD\_POR\_L}$ for longer than t_{DVDD_POR} device will enter sleep mode directly (if DVDD drops too fast, device will enter sleep mode without t_{DVDD_POR}). During sleep mode, all internal blocks will be in off state except brake function block, gate drivers will be in passive off state
- Normal mode. If nSLEEP is high and V_{DVDD} exceeds $V_{DVDD\_POR\_H}$ device will enter normal mode with t_{wake} delay (during t_{wake} device is starting up), during normal mode, all blocks can work in two states
  - No fault state: when there is no fault present, all blocks work following SPI command or IO
  - Fault state: when there is fault present, all blocks work following fault reaction configuration

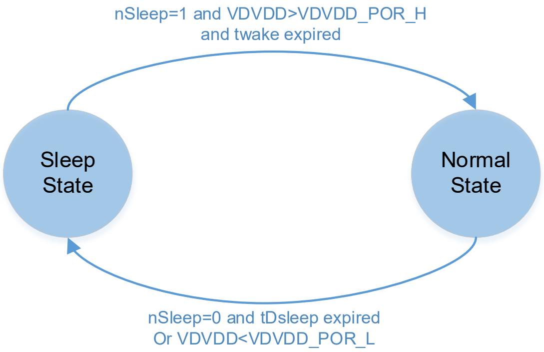


Figure 7.19 Device Operation State Diagram

7.5. Gate Driver

7.5.1. General Description

In NSD3602S/H gate driver block provides gate driver function and diagnostic for 2 half bridges.

- Gate driver function: device provides two kinds of driver, traditional current driver and configurable charge/discharge current profile driver (CCPD)
    - Traditional current driver (available in NSD3602S and NSD3602H): MOSFET turn on/off process only has one phase, duration and current for this phase are configurable, detailed timing as below:

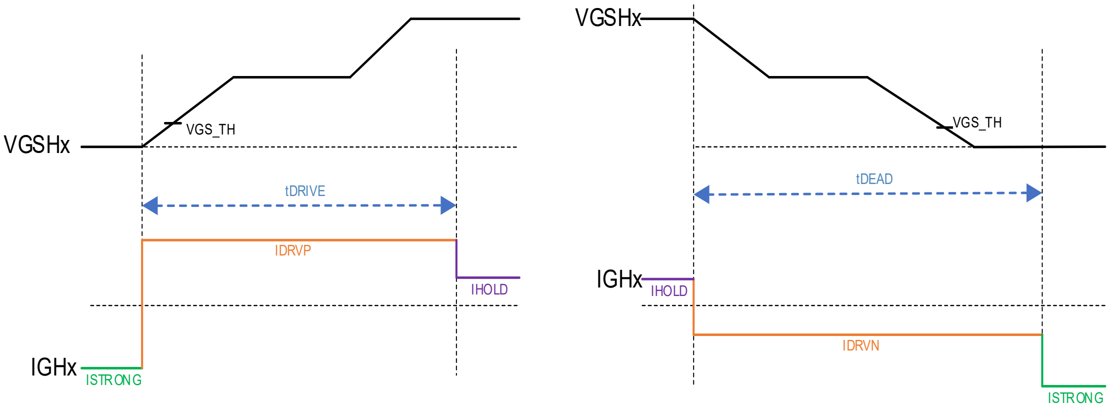


Figure 7.20 Traditional Current Driver Timing in NSD3602S and NSD3602H

- Configurable charge/discharge current profile driver (only available in NSD3602S): MOSFET turn on/off process is divided to two phases (turn off can be three phases if VGS_TH_EN = 1b): pre-charge/discharge phase, charge/discharge phase, post-discharge phase, duration and current for these phases are configurable, detailed timing as below:

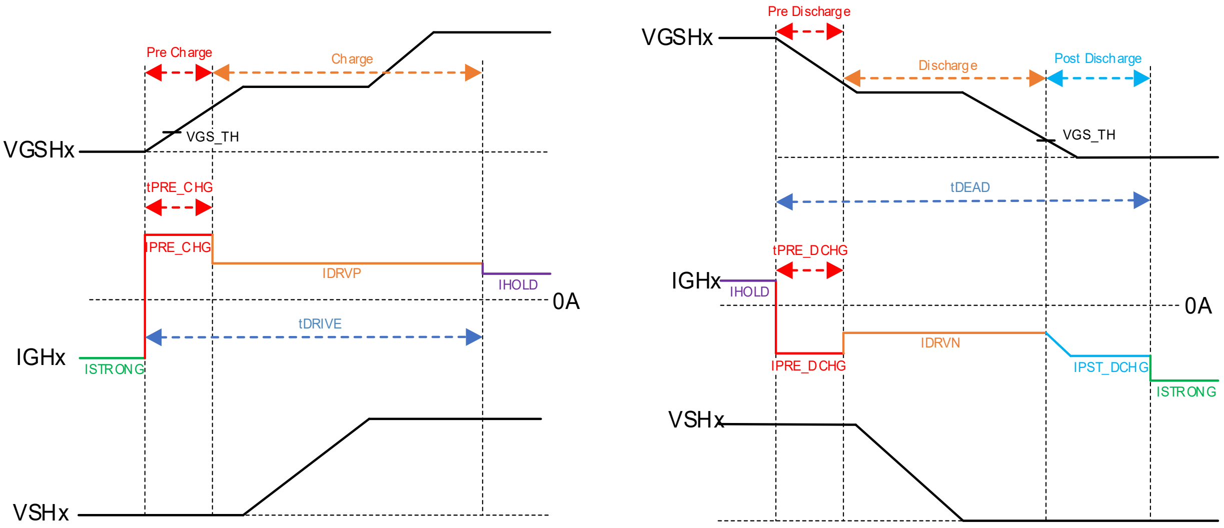


Figure 7.21 CCPD Timing in NSD3602S

- Diagnostic:
    - VDS and VGS monitors to detect VDS OV and VGS faults
    - Voltage status on SHx can be monitored by VDS monitor (only for NSD3602S)

7.5.2. Block Description

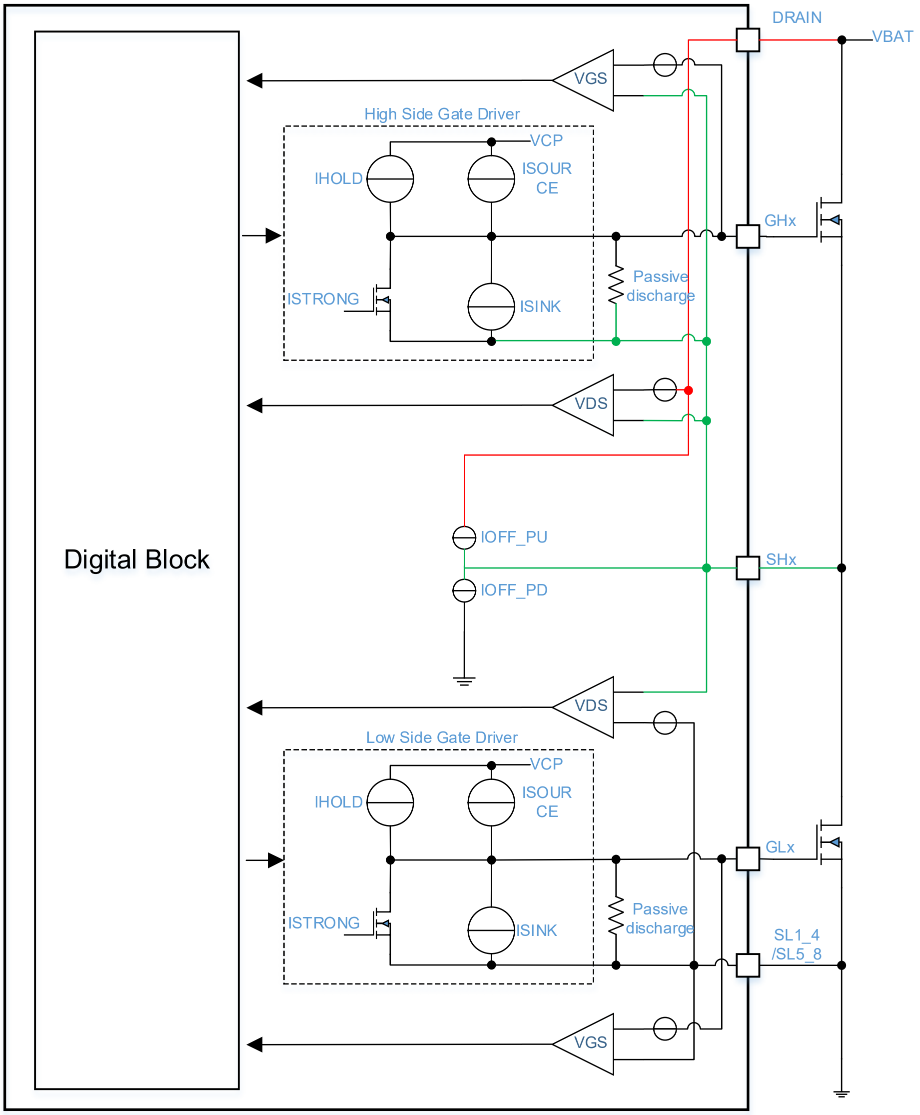


Figure 7.22 Gate Driver Internal Block Diagram

- I_{SOURCE} and I_{SINK} are current sources which can be configured within 0.25mA to 64mA to provide different current in different phases. The function of I_{SOURCE} and I_{SINK} is to achieve desired turn on and turn off timing for external MOSFETs
- I_{HOLD} is fixed current source to maintain external MOSFETs in on state after turn on process, this state is called active on state
- I_{STRONG} is internal switch with current limitation to maintain external MOSFETs in off state after turn off process, this state is called active off state
- Passive discharge is passive discharge path to keep external MOSFETs off when device is unsupplied or in sleep mode or in normal mode while DRV_EN = 0b, this state is called passive off state
- VGS comparator compares the voltage on V_{GS} to the threshold defined by VGS_TH bit, to check VGS status. The status can be used to end pre-charge and enter post-discharge if enabled by VGS_TH_EN bit (there is no pre/post phase in NSD3602H) and VGS handshaking if enabled by VGS_TDEAD_SEL bit (VGS handshaking is always enabled in NSD3602H), the status is also used to check whether V_{GS} voltage is in valid range with blanking time and filter time (VGS fault monitor)
- VDS comparator compares the voltage on V_{DS} to the threshold defined by VDS_TH_HS/LS bits or VDS pin, to check VDS status. The status can be used to check whether there is high current going through MOSFETs with blanking time and filter time, it also works for VSHx status monitor
- I_{OFF_PU} and I_{OFF_PD} are current sources used for off state diagnostic, MCU can use OFF_PU_EN_HBx and OFF_PD_EN_HBx bits to turn on and turn off these current sources after device enter normal mode (only available in NSD3602S)

Below table is summary for static operation state of different blocks

Table 7.8 Gate Driver Internal Blocks Operation State Table

nSLEEP	***DRV_EN***	***Control logic***	***IHOLD/ISTRONG***	***Passive Discharge***	***VGS Comparator***	***VDS Comparator***	***IOFF_PU/IOFF_PD***
0	X	X	OFF	Active	OFF	OFF	OFF
1	0	X	OFF	Active	Active	Active	Control by SPI
1	1	Turn off HSx/LSx	ISTRONG Active	OFF			
1	1	Turn on HSx/LSx	IHOLD Active	OFF			

Note: From logic point view DRV_EN = 1b in NSD3602H

7.5.3. Gate Driver Control Mode

Device support different control modes, refer 7.3.2.4 for details.

7.5.4. Traditional Current Driver Description

7.5.4.1. General Description

NSD3602 uses traditional current driver to drive the two half bridges by default, with a constant current source applied during the charging and discharging of the MOSFETs.

7.5.4.2. Timing Description

Based on control logic, internal digital core will output HSx and LSx turn on/off command to driver stage

- Only HSx MOSFET turns on/off while LSx MOSFET keeps off, timing example as below

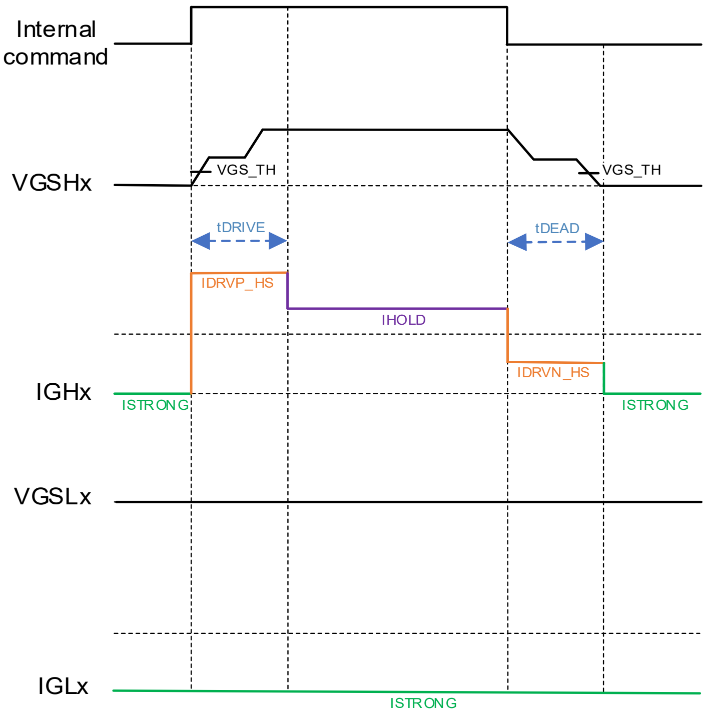


Figure 7.23 Only HSx Turn On and Turn Off Timing

- Only LSx MOSFET turns on/off while HSx MOSFET keeps off, timing example as below

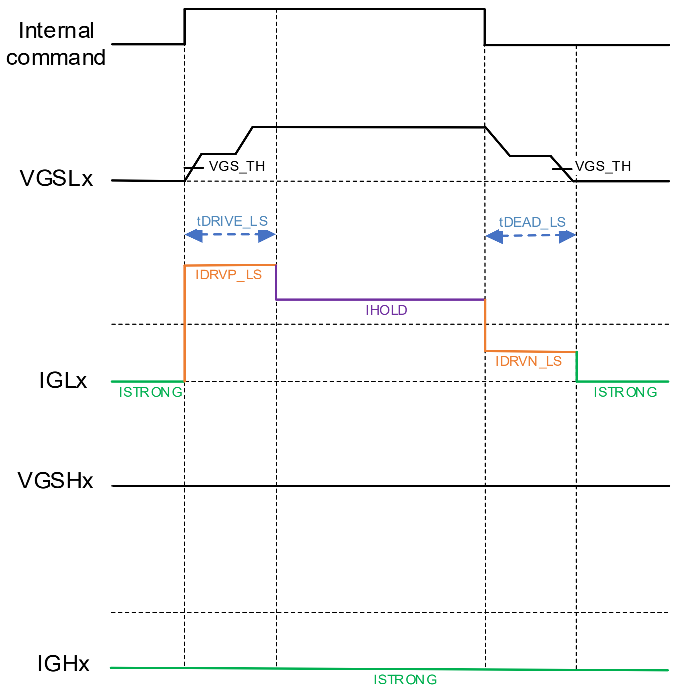


Figure 7.24 Only LSx Turn On and Turn Off Timing

- ■ Complementary operation, HSx/LSx turns on and LSx/HSx turns off, timing example as below

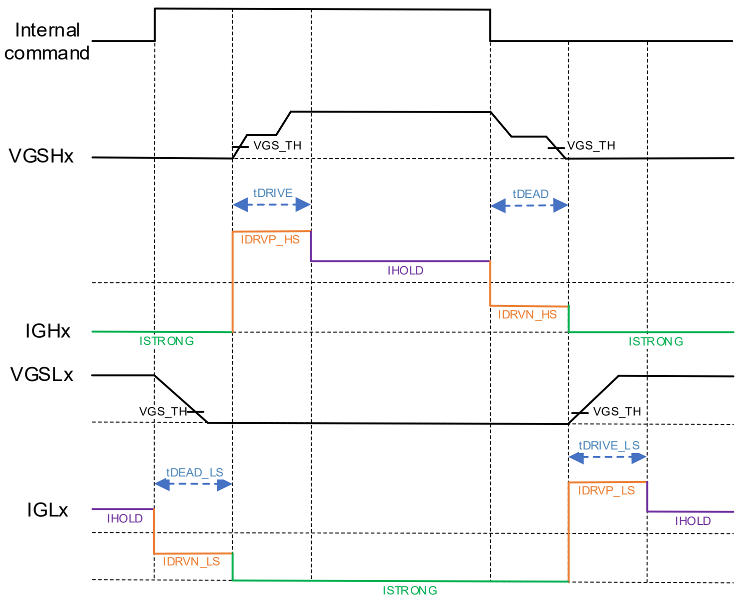


Figure 7.25 Complementary Switching Timing

- I_{DRVP_HS} current set by ISOURCE_HS and ISOURCE_L_HS bits
- I_{DRVN_HS} current set by ISINK_HS and ISINK_L_HS bits
- I_{DRVP_LS} current set by ISOURCE_LS and ISOURCE_L_LS bits
- I_{DRVN_LS} current set by ISINK_LS and ISINK_L_LS bits
- I_{STRONG} current depends on ISOURCE_HS and ISOURCE_LS bits

- I_{HOLD} current fixed at I_{HOLD}
- t_{DRIVE} duration set by TDRIVE and TDRIVE_M bits
- t_{DEAD} duration set by TDEAD, TDEAD_M and VGS_TDEAD_SEL bits
- t_{DRIVE_LS} duration set by TDRIVE, TDRIVE_M, LS_TIME_EN and TDRIVE_LS bits
- t_{DEAD_LS} duration set by TDEAD, TDEAD_M, VGS_TDEAD_SEL, LS_TIME_EN and TDEAD_LS bits
- V_{GS_TH} threshold set by VGS_TH bit
- For NSD3602H, I_{DRVP_HS}, I_{DRVN_HS}, I_{DRVP_LS} and I_{DRVN_LS} are set by IDRIVE pin input refer to table below

Table 7.9 Primary source current & Primary sink current Table

	NSD3602S	NSD3602H
Primary source current Primary sink current	ISOURCE_xx/ISINK_xx bits	IDRIVE pin input
0.25mA	0000b	
1mA	0001b	$V_{IDRIVE} < V_{TH1\_IDRIVE}$
2mA	0010b	
3mA	0011b	
4mA	0100b	$V_{TH1\_IDRIVE} < V_{IDRIVE} < V_{TH2\_IDRIVE}$
6mA	0101b	
8mA	0110b	$V_{TH2\_IDRIVE} < V_{IDRIVE} < V_{TH3\_IDRIVE}$
12mA	0111b	
16mA	1000b	$V_{TH3\_IDRIVE} < V_{IDRIVE} < V_{TH4\_IDRIVE}$
20mA	1001b	
24mA	1010b	
28mA	1011b	
31mA	1100b	$V_{TH4\_IDRIVE} < V_{IDRIVE} < V_{TH5\_IDRIVE}$
40mA	1101b	
48mA	1110b	
64mA	1111b	$V_{TH5\_IDRIVE} < V_{IDRIVE}$

Table 7.10 Offset source current & Offset sink current Table

	NSD3602S	NSD3602H
Offset source current Offset sink current	ISOURCE_L_xx/ISINK_L_xx bits	N/A
0mA	00b	Fixed
0.25mA	01b	N/A
0.5mA	10b	N/A
0.75mA	11b	N/A

7.5.5. Configurable Current Profile Driver (CCPD)

7.5.5.1. General Description

Based on traditional current driver, CCPD can be configured by below SPI bits (CCPD is only available in NSD3602S)

- PRE_EN, if PRE_EN = 1b, CCPD will be enabled, then HSx/LSx turn on and turn off process will have two phases (pre-charge/discharge, charge/discharge)
- VGS_TH_EN, if VGS_TH_EN = 1b, additional to PRE_EN = 1b, HSx/LSx turn off process will have three phases (pre-discharge, discharge, post-discharge) while turn on process still has two phases (pre-charge, charge), but $V_{GS} > V_{GS\_TH}$ can end pre-charge phase

7.5.5.2. Timing description

- Timing example for high side MOSFETs turn on and low side MOSFETs turn off while external power half bridge drive inductive load to GND

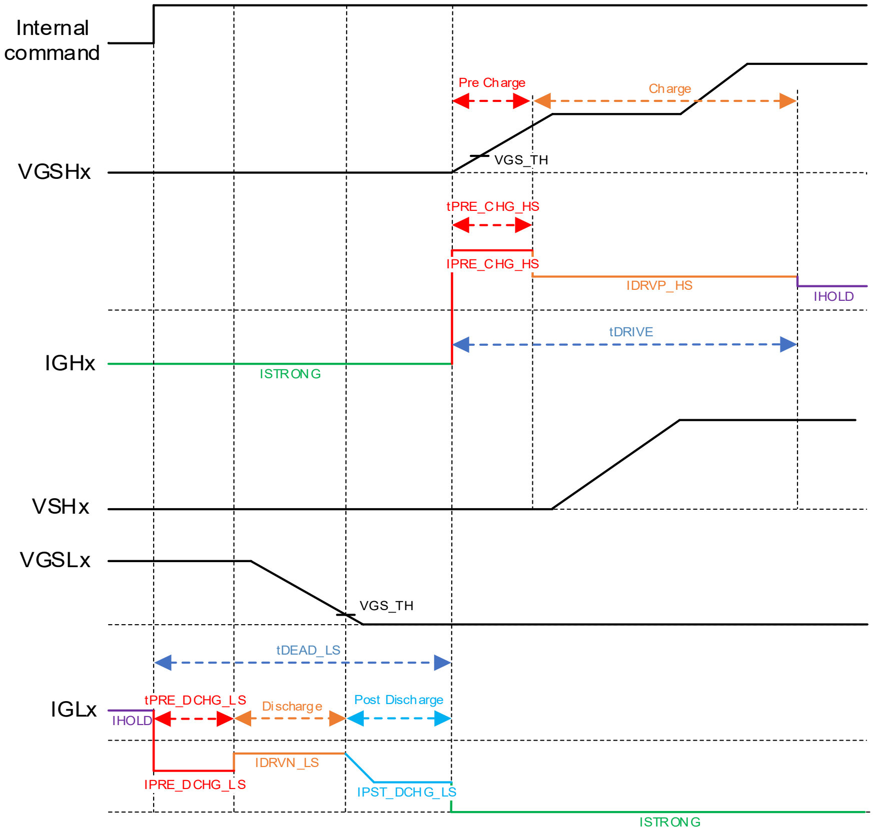


Figure 7.26 CCPD Timing for LSx Turn Off and HSx Turn On

- $I_{PRE\_CHG\_HS}$ current set by IPCHG_HS and ISOURCE_L_HS bits
- I_{DRVP_HS} current set by ISOURCE_HS and ISOURCE_L_HS bits
- $I_{PRE\_DCHG\_LS}$ current set by IPDCHG_LS and ISINK_L_LS bits
- I_{DRVN_LS} current set by ISINK_LS and ISINK_L_LS bits
- $I_{PST\_DCHG\_LS}$ current ramp up from IDRVN_LS to max current (64mA) with one step increased every system clock (if VGS_TH_EN = 0, there will be no post discharge)
- I_{STRONG} current depends on ISOURCE_HS and ISOURCE_LS bits
- I_{HOLD} current fixed at I_{HOLD}
- $t_{PRE\_CHG\_HS}$ duration set by TPCHG_HS and VGS_TH_EN bits
- $t_{PRE\_DCHG\_LS}$ duration set by TPDCHG_LS bits
- t_{DRIVE} duration set by TDRIVE and TDRIVE_M bits

- t_{DEAD_LS} duration set by TDEAD, TDEAD_M, VGS_TDEAD_SEL, LS_TIME_EN and TDEAD_LS bits
- V_{GS_TH} threshold controlled by VGS_TH bits

■ Timing example for high side MOSFETs turn off and low side MOSFETs turn on while external power half bridge drive inductive load to GND

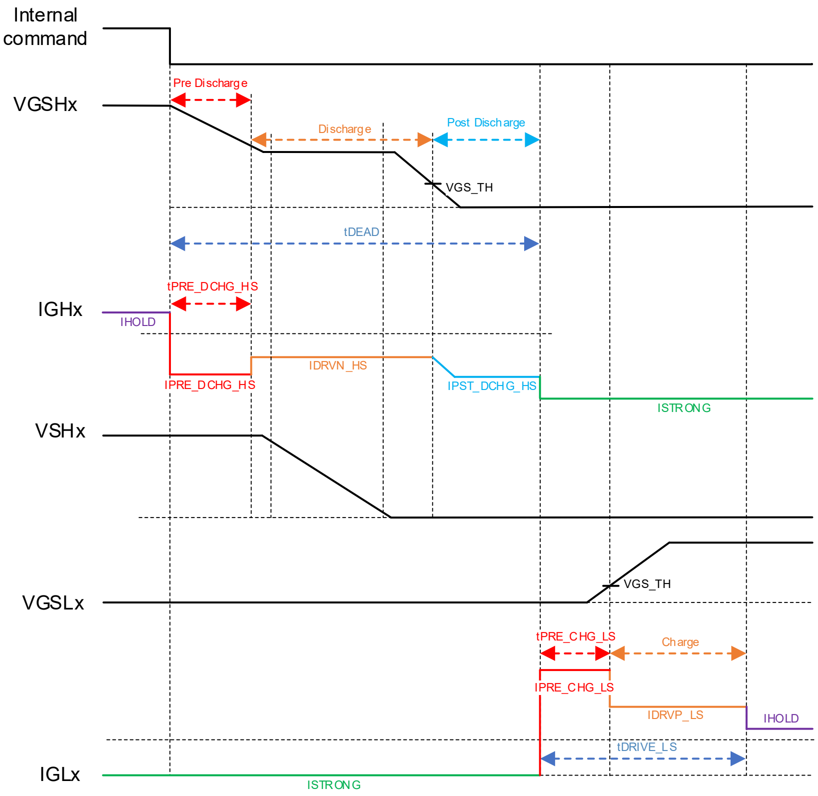


Figure 7.27 CCPD Timing for HSx Turn Off and LSx Turn On

- $I_{PRE\_DCHG\_HS}$ current controlled by IPDCHG_HS and ISINK_L_HS bits
- I_{DRVN_HS} current controlled by ISINK_HS and ISINK_L_HS bits
- $I_{PST\_DCHG\_HS}$ current ramp up from IDRVN_HS to max current (64mA) with one step increased every system clock (if VGS_TH_EN = 0, there will be no post discharge)
- $I_{PRE\_CHG\_LS}$ current controlled by IPCHG_LS and ISOURCE_L_LS bits
- I_{DRVP_LS} current controlled by ISOURCE_LS and ISOURCE_L_LS bits
- I_{STRONG} current depends on ISOURCE_HS and ISOURCE_LS bits
- I_{HOLD} current fixed at I_{HOLD}
- $t_{PRE\_DCHG\_HS}$ duration controlled by TPDCHG_HS
- t_{DEAD} duration controlled by TDEAD, TDEAD_M and VGS_TDEAD_SEL bits
- $t_{PRE\_CHG\_LS}$ duration controlled by TPCHG_LS and VGS_TH_EN bits
- t_{DRIVE_LS} duration controlled by TDRIVE, TDRIVE_M, LS_TIME_EN and TDRIVE_LS bits
- V_{GS_TH} threshold controlled by VGS_TH and bits

7.5.6. Diagnostic Description

7.5.6.1. VDS OV Monitor

VDS OV monitor is based on VDS comparator, the input of VDS comparators for HSx/LSx are different, for HSx MOSFETs NSD3602S/H will use DRAIN as drain sense while SHx as source sense, for LSx MOSFETs NSD3602S/H will use SHx as drain sense while SLx as source sense.

After MOSFET is turned on (during t_{DRIVE}/ t_{DRIVE_LS} VDS comparator output is ignored), if VDS of MOSFET is higher than V_{DS_TH} (set by VDS_TH_HS/LS bit in NSD3602S, VDS pin input in NSD3602H) for longer than t_{DS_OV} (set by TFILTER_DS bit in NSD3602S, fixed at 4µs in NSD3602H), NSD3602S/H will detect VDS OV fault, in NSD3602S the fault reaction can be set by VDS_OV_MODE bit. In NSD3602H the fault reaction is same with NSD3602S while VDS_OV_MODE = 01b or 11b depend on VDS pin input.

- VDS_OV_MODE = 00b, VDS OV fault is set as latch fault

  After fault happens, device will do following things

  - Gate drivers defined by VDS_OV_IND bits generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to active off state (other gate drivers not defined by VDS_OV_IND still can be controlled by SPI or IO inputs)
  - Set FAULT and VDS_VGS_FLT_OR bits in GEN_STA_1 register, nFLT pin also be activated
  - Set VDS_HS_HBx/VDS_LS_HBx bit in VGS_VDS_STA

  After fault ends, device has no reaction till SPI send clear fault command (write DIAG_CLR = 1b), after clear fault command, device will do following things:

  - Clear FAULT, VDS_VGS_FLT_OR and VDS_HS_HBx/VDS_LS_HBx bits, release nFLT pin
  - Gate drivers will re-work following current configuration in registers and IO inputs

- VDS_OV_MODE = 01b, VDS OV fault is set as cycle by cycle fault ($V_{TH5\_VDS} > V_{VDS}$ for NSD3602H)

  After fault happens, device will do following things

  - Gate drivers defined by VDS_OV_IND bits generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to active off state (other gate drivers not defined by VDS_OV_IND still can be controlled by SPI or IO inputs)
  - Set FAULT and VDS_VGS_FLT_OR bit in GEN_STA_1 register, nFLT also be activated
  - Set VDS_HS_HBx/VDS_LS_HBx in VGS_VDS_STA

  When fault gate driver which report VDS_HS_HBx/VDS_LS_HBx is turned off by SPI or IO inputs, device will do following things:

  - Clear FAULT bit, release nFLT pin
  - Gate drivers will re-work following current configuration in registers (fault driver can be re-opened by SPI command or IO inputs)
  - VDS_VGS_FLT_OR and VDS_HS_HBx/VDS_LS_HBx bits will keep till SPI send clear fault command (write DIAG_CLR=1)

  In NSD3602H, VDS_OV_IND logic depends on MODE pin input, VDS_OV_IND = 1b when $V_{MODE} < V_{TH1\_MODE}$ or $V_{MODE} > V_{TH3\_MODE}$, otherwise VDS_OV_IND = 0b

- VDS_OV_MODE = 10b, VDS OV fault is set as warning fault

  After fault happens, device will do following things

  - Set WARN and VDS_VGS_FLT_OR bit in GEN_STA_1 register
  - Set VDS_HS_HBx/VDS_LS_HBx in VGS_VDS_STA

  WARN, VDS_VGS_FLT_OR and VDS_HS_HBx/VDS_LS_HBx will keep till SPI send clear fault command (write DIAG_CLR = 1b) after fault event gone

- VDS_OV_MODE = 11b ($V_{TH5\_VDS} < V_{VDS}$ for NSD3602H), VDS OV fault is set as no fault, after fault happens, device will do nothing

7.5.6.2. VGS Fault Monitor

After MOSFET is turned on/off (during t_{DRIVE}/t_{DRIVE_LS} or t_{DEAD}/t_{DEAD_LS} VGS comparator output is ignored), if V_{GS} of MOSFET is lower than V_{GS_TH} for longer than t_{GS_FLT} during MOSFET is active on, or V_{GS} of MOSFET is higher than V_{GS_TH} for longer than t_{GS_FLT} during MOSFET is active off, NSD3602S/H will detect VGS fault, in NSD3602S the fault reaction can be set by VGS_FLT_MODE bit.

In NSD3602H the fault reaction is same with NSD3602S while VGS_FLT_MODE = 01b or 11b depend on VDS pin input.

- VGS_FLT_MODE = 00b, VGS fault is set as latch fault

  After fault happens, device will do following things

  - Gate drivers defined by VGS_FLT_IND bits generate discharge current defined by ISINK_FLT for tFLT_OFF, then gate drivers move to active off by ISTRONG (other gate drivers not defined by VGS_FLT_IND still can be controlled by SPI or input pins)
  - Set FAULT and VDS_VGS_FLT_OR bit in GEN_STA_1 register, nFLT also be activated
  - Set VGS_HS_HBx/VGS_LS_HBx in VGS_VDS_STA

After fault ends, device has no reaction till SPI send clear fault command (write DIAG_CLR = 1b), after clear fault command, device will do following things:

  - Clear FAULT, VDS_VGS_FLT_OR and VGS_HS_HBx/VGS_LS_HBx bits, release nFLT pin
  - Gate drivers will re-work following current configuration in registers and IO inputs

- VGS_FLT_MODE = 01b, VGS fault is set as cycle by cycle fault ($V_{TH5\_VDS} > V_{VDS}$ for NSD3602H)

  After fault happens, device will do following things

  - Gate drivers defined by VGS_FLT_IND bits generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to active off by I_{STRONG} (other gate drivers not defined by VGS_FLT_IND still can be controlled by SPI or input pins)
  - Set FAULT and VDS_VGS_FLT_OR bit in GEN_STA_1 register, nFLT also be activated
  - Set VGS_HS_HBx/VGS_LS_HBx in VGS_VDS_STA

  When fault gate driver which report VGS_HS_HBx/VGS_LS_HBx is turned off by SPI command or IO inputs, device will do following things:

  - Clear FAULT bit, release nFLT pin
  - Gate drivers will re-work following current configuration in registers and IO inputs (fault driver can be re-turn on by SPI command or input pins)

  VDS_VGS_FLT_OR and VGS_HS_HBx/VGS_LS_HBx will keep till SPI send clear fault command (write DIAG_CLR=1b)

  In NSD3602H, VGS_FLT_IND logic depends on MODE pin input, VGS_FLT_IND = 1b when $V_{MODE} < V_{TH1\_MODE}$ or $V_{MODE} > V_{TH3\_MODE}$, otherwise VGS_FLT_IND = 0b

- VGS_FLT_MODE = 10b, VGS fault is set as warning fault

  After fault happens, device will do following things

  - Set WARN and VDS_VGS_FLT_OR bit in GEN_STA_1 register
  - Set VGS_HS_HBx/VGS_LS_HBx in VGS_VDS_STA

  WARN, VDS_VGS_FLT_OR and VGS_HS_HBx/VGS_LS_HBx will keep till SPI send clear fault command (write DIAG_CLR = 1b) after fault event gone

- VGS_FLT_MODE = 11b ($V_{TH5\_VDS} < V_{VDS}$ for NSD3602H), VGS fault is set as no fault

  After fault happens, device will do nothing

7.5.6.3. VSHx Status Monitor

In NSD3602S SHx voltage status can be monitored by two ways:

- Set OFF_DIAG_EN = 1b, VDS_HS_HBx/VDS_LS_HBx bits will be set as VDS comparator output without blanking and filter time, VDS comparator threshold still follows VDS_TH_HS/LS bits, MCU can know SHx status by SPI, when OFF_DIAG_EN = 1b, VDS_HS_HBx/VDS_LS_HBx bits will not set FAULT and VDS_VGS_FLT_OR bits or active nFLT, when OFF_DIAG_EN change from 1b to 0b, device will clear VDS_HS_HBx/VDS_LS_HBx bits once
- During normal mode, HBx_STA bit in GEN_STA_4 register is HSx VDS comparator output without blanking and filter time, HSx VDS comparator threshold still follows VDS_TH_HS/LS bits, MCU can know SHx status by SPI no matter half bridges are in on state or off state

There is no SHx voltage status monitor in NSD3602H

7.5.6.4. Off State Diagnostic

NSD3602S provides pull-up current source (IOFF_PU) and pull-down current source (IOFF_PD), these two current sources can be controlled by OFF_PU_EN_HBx and OFF_PD_EN_HBx bits, MCU can use these bits and VSHx status monitor function to do off state diagnostic

There is no off state diagnostic function in NSD3602H

7.6. Current Sense Amplifier (CSA)

7.6.1. General Description

NSD3602S/H has one high performance current sense amplifier (CSA) to monitor current by measuring the differential voltage drop on external shunt resistor, CSA support wide common and bi-direction input.

CSA block is shown below, stage1 amplifier is supplied by charge pump so when charge pump is disabled CSA will be turned off, stage2 amplifier, REF amplifier and overcurrent comparator are supplied by AREF. The gain of CSA can be configured by CSA_GAIN bits (GAIN pin input for NSD3602H), offset of CSA output can be configured by CSA_OFFSET bit (offset is fixed for NSD3602H), CSA can be disabled by CSA_DIS bit (CSA is always enabled in NSD3602H). Additionally, CSA has blanking function and sample/hold function (refer to 7.6.2.1~7.6.2.2 for details)

NSD3602S also has one monitor to check AREF undervoltage (refer to 7.1.2.4 for details)

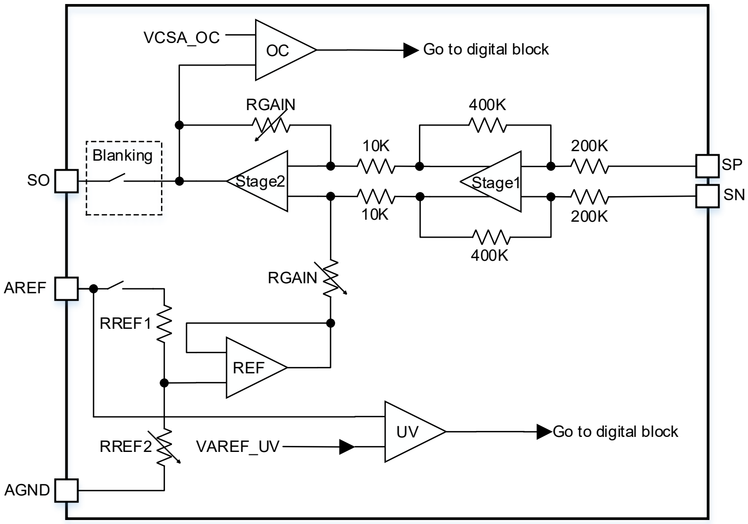


Figure 7.28 CSA Internal Block Diagram

7.6.2. Detailed Description

7.6.2.1. Blanking Function (only for NSD3602S)

CSA has a blanking switch which can be turned off (SO in HIZ mode) for duration set by CSA_BLANK_SEL when half bridge defined by CSA_BLANK_SOURCE is turning on/off, detailed timing is shown below

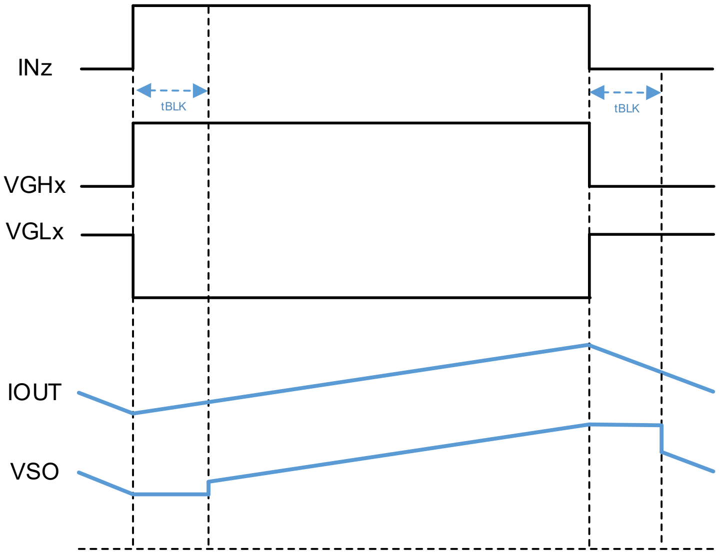


Figure 7.29 Blanking Function Timing

Note: Register only set which HBx to trigger CSA blanking function, the final source is both edge of HSx and LSx in HBx (HSx/LSx turn on/off will both trigger blanking function), but during two MOS switch sequence, blanking will only end by the second MOS turn on/off

7.6.2.2. Sample and Hold Function (only for NSD3602S)

Sample and hold function enabled by CSA_SH_EN bit, if enabled, the blanking switch will be turned off (SO in HIZ mode) when both HSx turn on or both LSx turn on, otherwise blanking switch will be turned on again. Sample and hold function triggered by both LSx turn on timing is shown below.

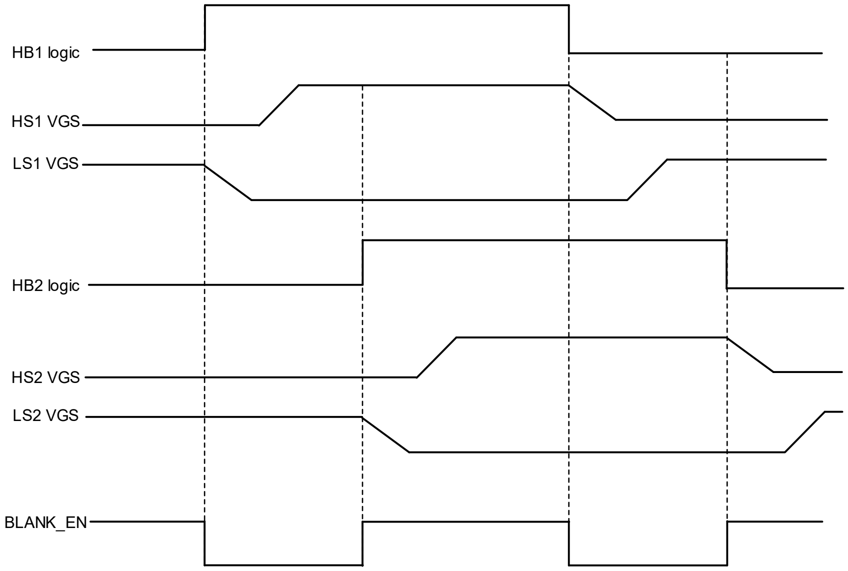


Figure 7.30 Sample and hold function Timing with blanking function disabled

7.6.2.3. Overcurrent Diagnosis

In NSD3602S there is an OC comparator for OC fault detection, when stage2 amplifier output higher than threshold defined by CSA_OC_TH bits for longer than t_{CSA_OC} defined by CSA_OC_TFLT, device detects CSA OC fault, the reaction is set by CSA_OC_FLT_MODE bits

In NSD3602H there is no OC comparator.

- CSA_OC_FLT_MODE = 00b (default), CSA OC fault is set as no fault, device will do nothing
- CSA_OC_FLT_MODE = 01b, CSA OC fault is set as latch fault

  After fault happens, device will do following things

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to active off by I_{STRONG}
  - Set FAULT and OT_WD_CSA_OR bits in GEN_STA_1 register, nFLT also be activated
  - Set CSA_OC in GEN_STA_3

  Device has no reaction till SPI send clear fault command (write DIAG_CLR = 1b) after OC event gone with t_{CSA_OC} filter, after clear fault command, device will do following things:

  - Clear FAULT, OT_WD_CSA_OR and CSA_OC bits, release nFLT pin
  - Gate drivers will re-work following current configuration in registers
- CSA_OC_FLT_MODE = 10b, CSA OC fault is set as warning fault

  After fault happens, device will do following things

  - Set WARN and OT_WD_CSA_OR bits in GEN_STA_1 register
  - Set CSA_OC in GEN_STA_3

  WARN, OT_WD_CSA_OR and CSA_OC bits will keep till SPI send clear fault command (write DIAG_CLR = 1b) after OC event gone with t_{CSA_OC} filter
- CSA_OC_FLT_MODE = 11b, CSA OC fault is set as cycle by cycle fault

  After fault happens, device will do following things

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to active off by I_{STRONG}
  - Set FAULT and OT_WD_CSA_OR bit in GEN_STA_1 register, nFLT also be activated
  - Set CSA_OC in GEN_STA_3

  When there is turn off edge of any HS or LS, device will do following things:

- Clear FAULT bit, release nFLT pin
- Gate drivers will re-work following current configuration in registers

OT_WD_CSA_OR and CSA_OC bits will keep status till SPI send clear fault command (write DIAG_CLR = 1b) after OC event gone with t_{CSA_OC} filter

7.7. Internal Oscillator

There is a main oscillator to generate system clock with fosc frequency, also there is a frequency modulation for system clock to reduce emission of main clock, the modulation function can be disabled/enabled by SYS_CLK_MOD bit, the modulation range can be configured by SYS_CLK_MOD_RAN bit

7.8. Protection and Diagnostic

7.8.1. Protection and diagnostic overview

Table 7.11 NSD3602S Protection and Diagnostic Overview

Name	***Fault mode***	***SPI BIT***	***Digital logic***	***Charge pump***	***Gate drivers***	***CSA***	***Reference***
Disable driver by DRV_EN	n/a	n/a	Not affect	Not affect	pull down sequence2	Not affect	7.3.2.4
Disable driver by DRVOFF	n/a	n/a	Not affect	Not affect	pull down sequence3	Not affect	7.3.2.2
Brake function active	n/a	n/a	Not affect	Not affect	LSx turn on, HSx passive off	Not affect	7.3.2.8
VDS OV in during brake	n/a	FAULT and VDS_LS_HBx (during normal mode)	Not affect	Not affect	LSx turn off by brake block, HSx passive off	Not affect	7.3.2.8
POR by nSLEEP	n/a	POR	Reset	Restart	pull down sequence2	Restart	7.3.2.1
POR by DVDD UV	n/a	POR	Reset	Restart	pull down sequence1	Restart	7.1.2.3
PVDD UV	Latch	FAULT, PVDD_VCP_UV_OR, PVDD_UV	Not affect	Disabled	pull down sequence2	Disabled	7.1.2.1
	Auto Recover	FAULT, PVDD_VCP_UV_OR, PVDD_UV					
PVDD OV	Latch	FAULT, OV, PVDD_OV	Not affect	Not effect (CP_DIS_PVDD_OV=0) Disable (CP_DIS_PVDD_OV=1)	pull down sequence3 (CP_DIS_PVDD_OV=0) pull down sequence2 (CP_DIS_PVDD_OV=1)	Not effect (CP_DIS_PVDD_OV=0) Disable (CP_DIS_PVDD_OV=1)	7.1.2.2
	Auto Recover	FAULT, OV, PVDD_OV					
	Warning	WARN, OV, PVDD_OV	Not affect				
	No Fault	n/a					

VCP UV	Latch	FAULT, PVDD_VCP_UV_OR, VCP_UV	Not affect	Disabled	pull down sequence2	Disabled	7.2.2.2
	Auto Recover			Not affect			
VDS OV	Latch	FAULT, VDS_VGS_FLT_OR, VDS_FLT_STA_x	Not affect		pull down sequence3	Not affect	7.5.6.1
	Cycle						
	Warning	WARN, VDS_VGS_FLT_OR, VDS_FLT_STA_x	Not affect				
	No Fault	n/a					
VGS Fault	Latch	FAULT, VDS_VGS_FLT_OR, VGS_FLT_STA_x	Not affect		pull down sequence3	Not affect	7.5.6.2
	Cycle						
	Warning	WARN, VDS_VGS_FLT_OR, VGS_FLT_STA_x	Not affect				
	No Fault	n/a					
CSA OC	No Fault	n/a	Not affect				7.6.2.3
	Latch	FAULT, OT_WD_CSA_OR, CSA_OC	Not affect		pull down sequence3	Not affect	
	Warning	WARN, OT_WD_CSA_OR, CSA_OC	Not affect				
	Cycle	FAULT, OT_WD_CSA_OR, CSA_OC	Not affect		pull down sequence3	Not affect	
AREF UV	n/a	OT_WD_CSA_OR AREF_UV	Not affect				7.1.2.4
Thermal warning	n/a	WARN, OT_WD_CSA_OR, OTW	Not affect				7.8.3
Thermal shutdown	n/a	FAULT, OT_WD_CSA_OR, OTSD	Not affect	Disabled	pull down sequence2	Disabled	
Off state diagnostic	n/a	VDS_FLT_STA_x or HB_STA	Not affect				7.5.6.4

WD fault	Latch	FAULT, OT_WD_CSA_OR, WD_FLT	Not affect	pull down sequence3	Not affect	7.8.2
	Warning	WARN, OT_WD_CSA_OR, WD_FLT	Not affect			
SPI clock fault	n/a	SCLK_FLT, SPI_OK	Not affect			7.3.2.9.4

Table 7.12 NSD3602H Protection and Diagnostic Overview

Name	***Fault mode***	***Digital logic***	***Charge pump***	***Gate drivers***	***CSA***	***Reference***
Disable driver by DRVOFF	n/a	Not affect	Not affect	pull down sequence3	Not affect	7.3.2.2
Brake function active	n/a	Not affect	Not affect	LSx turn on, HSx passive off	Not affect	7.3.2.8
VDS OV in during brake	n/a	Not affect	Not affect	LSx turn off by brake block, HSx passive off	Not affect	7.3.2.8
POR by nSLEEP	n/a	Reset	Restart	pull down sequence2	Restart	7.3.2.1
POR by DVDD UV	n/a	Reset	Restart	pull down sequence1	Restart	7.1.2.3
PVDD UV	Auto Recover	Not affect	Disabled	pull down sequence2	Disabled	7.1.2.1
VCP UV	Auto Recover	Not affect	Not affect	pull down sequence2	Disabled	7.2.2.2
VDS OV	Cycle	Not affect		pull down sequence3	Not affect	7.5.6.1
	No Fault	Not affect				
VGS Fault	Cycle	Not affect		pull down sequence3	Not affect	7.5.6.2
	No Fault	Not affect				
Thermal shutdown	n/a	Not affect	Disabled	pull down sequence2	Disabled	7.8.3

Table 7.13 Turn Off Sequence Table

Gate driver pull down sequence	***Description***
Pull down sequence1	Directly go to passive off by passive discharge
Pull down sequence2	All Gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF} (20µs typical), then gate drivers move to passive off by passive discharge

Pull down sequence3	All Gate drivers or gate drivers by VDS_OV_IND or VGS_FLT_IND setting generate discharge current defined by ISINK_FLT for t_{FLT_OFF} (20µs typical), then gate drivers move to active off by Istrong discharge
Pull down sequence4 (only for brake function ending)	LSx Gate drivers generate discharge by brake function for 20µs typical, then gate drivers move to passive off by passive discharge

7.8.2. Watchdog (WD)

NSD3602S has a window WD (open window = 10%~100%) to ensure MCU works correctly, WD can be enabled or disabled by WD_EN bit, WD period is set by WD_TIMER bit, if WD is enabled by WD_EN = 1b, within fixed window MCU need to invert WD_RST bit (WD_RST = 0b by default), otherwise device will detect WD fault, the reaction can be configured by WD_FLT_MODE.

In NSD3602H there is no WD.

- WD_FLT_MODE = 0b, WD fault is set as warning fault

  After fault happens, device will do following things

  - Set WARN and OT_WD_CSA_OR bit in GEN_STA_1 register
  - Set WD_FLT bit in GEN_STA_2 register
  - Stop WD

  OT_WD_CSA_OR and WD_FLT will keep status till SPI send clear fault command (write DIAG_CLR = 1b)

  WD can be restarted by inverting WD_RST bit (turn off WD and re-turn on WD by WD_EN will also restart WD)

- WD_FLT_MODE = 1b, WD fault is set as latch fault

  After fault happens, device will do following things

  - All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to active off by I_{strong} discharge current
  - Set FAULT and OT_WD_CSA_OR bit in GEN_STA_1 register, nFLT also be activated
  - Set WD_FLT bit in GEN_STA_2 register
  - Stop WD

  Device has no reaction till SPI send clear fault command (write DIAG_CLR = 1b), after clear fault command, device will do following things:

  - Clear FAULT, OT_WD_CSA_OR and WD_FLT bits, release nFLT pin
  - All gate drivers will re-work following current configuration in registers after

  WD can be restarted by inverting WD_RST (turn off WD and re-turn on WD by WD_EN will also restart WD)

Note: WD fault does not change WD_RST bit

7.8.3. Thermal Monitor

NSD3602S has internal thermal monitor for thermal warning and thermal shutdown protection, NSD3602H only has thermal shutdown protection.

7.8.3.1. Thermal Warning

In NSD3602S if junction temperature T_J exceeds T_{OTW} for longer than t_{OTW}, a thermal warning will be detected, device will do following things

- Set WARN and OT_WD_CSA_OR bits in GEN_STA_1 register
- Set OTW bit in GEN_STA_2 register

After T_J recovers (T_J falls below T_{OTW} - T_{HYS} for longer than t_{OTW}) and SPI send clear fault command (write DIAG_CLR = 1b), device will do following things

- Clear WARN, OT_WD_CSA_OR and OTW bits

7.8.3.2. Thermal Shutdown Protection

In NSD3602S/H if junction temperature T_J exceeds T_{OTSD} for longer than t_{OTSD}, device will detect thermal shutdown, device will do following things

- All gate drivers generate discharge current defined by ISINK_FLT for t_{FLT_OFF}, then gate drivers move to passive discharge
- Set FAULT and OT_WD_CSA_OR bit in GEN_STA_1 register, nFLT also be activated
- Set OTSD bit in GEN_STA_2 register
- Disable charge pump
- Disable CSA (SO will be in high impedance state)
- Disable Brake function while not care BRAKE_DIS bit

In NSD3602S after T_J recovers (T_J falls below T_{OTSD} - T_{HYS} for longer than t_{OTSD}) and SPI send clear fault command (write DIAG_CLR = 1b), device will do following things

- Clear FAULT, OT_WD_CSA_OR and OTSD bits, release nFLT pin
- Brake function enable or disable following BRAKE_DIS bit (also there is 20us delay if BRAKE_DIS = 0)
- Re-start charge pump
- All gate drivers and CSA will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$

In NSD3602H, after T_J recovers (T_J falls below T_{OTSD} - T_{HYS} for longer than t_{OTSD}), device will do following things

- Release nFLT pin
- Re-start charge pump
- All gate drivers and CSA will re-work following current configuration in registers after V_{VCP} exceeds $V_{VCP\_UV\_H}$
- OT_WD_CSA_OR and OTSD bits will keep till SPI clear command

8. Register Description

8.1. Overview

Tables below shows the register map of NSD3602S, the registers not listed in tables below should not be accessed.

Table 8.1 Status Registers

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
GEN_STA1	0x00	SPI_OK	POR	FAULT	WARN	VDS_VGS_FLT_OR	PVDD_VCP_UV_OR	OV	OT_WD_CSA_OR
VDS_VGS_STA	0x01	VGS_HS_HB1	VGS_LS_HB1	VGS_HS_HB2	VGS_LS_HB2	VDS_HS_HB1	VDS_LS_HB1	VDS_HS_HB2	VDS_LS_HB2
GEN_STA2	0x02	PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	WD_FLT	SPI_CLK_FLT	SPI_ADDR_FLT
GEN_STA3	0x03	Reserved	AREF_UV	Reserved	CSA_OC	Device_ID			
GEN_STA4	0x16	Reserved						HB2_STA	HB1_STA

Table 8.2 Control Registers

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL1	0x04	DRV_EN	CP_SS_DIS	IN1_MODE	IN2_MODE	LOCK			DIAG_CLR
DRV_CTRL2	0x05	VGS_TDEAD_SEL	DRV_MODE		DRV_FW	SPI_IN1	SPI_IN2	SPI_HIZ1	SPI_HIZ2
DRV_CTRL3	0x06	ISOURCE_HS				ISINK_HS			
DRV_CTRL4	0x07	ISOURCE_LS				ISINK_LS			
DRV_CTRL5	0x08	VGS_FLT_MODE		TDRIVE		TDEAD			VGS_FLT_IND
DRV_CTRL6	0x09	VDS_OV_MODE		TFILTER_DS		ISINK_FLT		VGS_TH	VDS_OV_IND
DRV_CTRL7	0x0A	VDS_TH_HS				VDS_TH_LS			
DRV_CTRL8	0x0B	SYS_CLK_MOD_RAN		CP_EMI_MODE	OFF_DIAG_EN	OFF_PU_EN_HB1	OFF_PD_EN_HB1	OFF_PU_EN_HB2	OFF_PD_EN_HB2
DRV_CTRL9	0x0C	PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_TFILTER		PVDD_OV_TH	VCP_UV_MODE	VCP_UV_TH
DRV_CTRL10	0x0D	CSA_SH_EN	CSA_BLANK_SOURCE	CSA_BLANK_SEL			CSA_OFFSET	CSA_GAIN	
DRV_CTRL11	0x0E	SYS_CLK_MOD	CP_SS_CONFIG	CP_DIS_PVDD_OV	VCP_UV_TH_M	WD_EN	WD_FLT_MODE	WD_TIMER	WD_RST
DRV_CTRL12	0x0F	CSA_OC_TH			CSA_OC_TFLT			CSA_OC_FLT_MODE	
DRV_CTRL13	0x10	PRE_EN	TDEAD_M	TDRIVE_M		VGS_TH_EN	LS_TIME_EN	BRAKE_DIS	CSA_DIS
DRV_CTRL14	0x11	IPCHG_HS				IPDCHG_HS			
DRV_CTRL15	0x12	TPCHG_HS		TPDCHG_HS		TPCHG_LS		TPDCHG_LS	
DRV_CTRL16	0x13	IPCHG_LS				IPDCHG_LS			
DRV_CTRL17	0x14	ISOURCE_L_HS		ISINK_L_HS		ISOURCE_L_LS		ISINK_L_LS	
DRV_CTRL18	0x15	TDEAD_LS				TDRIVE_LS			

8.2. Detailed Description

8.2.1. GEN_STA1

Table 8.3 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
GEN_STA1	0x00	SPI_OK	POR	FAULT	WARN	VDS_VGS_FLT_OR	PVDD_VCP_UV_OR	OV	OT_WD_CSA_OR
Operation Type		R	R	R	R	R	R	R	R

Table 8.4 Register Description

Bit	Field Name	Operation Type	Reset Value	Description

7	SPI_OK	R	0x1	0b: One or more SPI protocol error in prior frames is detected 1b: No SPI protocol error is detected
6	POR	R	0x1	0b: No POR 1b: POR due to DVDD UV or nSLEEP = 0
5	FAULT	R	0x0	0b: No fault detected 1b: Fault detected
4	WARN	R	0x0	0b: No warning detected 1b: Warning detected
3	VDS_VGS_FLT_OR	R	0x0	0b: No VDS and VGS fault detected 1b: VDS or VGS fault detected in at least one of power stages
2	PVDD_VCP_UV_OR	R	0x0	0b: No PVDD and VCP undervoltage detected 1b: PVDD or VCP undervoltage detected
1	OV	R	0x0	0b: No PVDD overvoltage detected 1b: PVDD overvoltage detected
0	OT_WD_CSA_OR	R	0x0	0b: No over temperature warning / shutdown, watchdog error, AREF UV and CSA OC detected 1b: Over temperature warning / shutdown or watchdog error, AREF UV or CSA OC detected

8.2.2. VDS_VGS_STA

Table 8.5 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
VDS_VGS_STA	0x01	VGS_HS_HB1	VGS_LS_HB1	VGS_HS_HB2	VGS_LS_HB2	VDS_HS_HB1	VDS_LS_HB1	VDS_HS_HB2	VDS_LS_HB2
Operation Type		R	R	R	R	R	R	R	R

Table 8.6 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	VGS_HS_HB1	R	0x0	0b: No VGS fault in HB1 high side external MOSFET detected 1b: VGS fault detected in HB1 high side external MOSFET.
6	VGS_LS_HB1	R	0x0	0b: No VGS fault in HB1 low side external MOSFET detected 1b: VGS fault detected in HB1 low side external MOSFET.
5	VGS_HS_HB2	R	0x0	0b: No VGS fault in HB2 high side external MOSFET detected 1b: VGS fault detected in HB2 high side external MOSFET.
4	VGS_LS_HB2	R	0x0	0b: No VGS fault in HB2 low side external MOSFET detected 1b: VGS fault detected in HB2 low side external MOSFET.
3	VDS_HS_HB1	R	0x0	0b: No VDS OV in HB1 high side external MOSFET detected 1b: VDS OV detected in HB3 high side external MOSFET.
2	VDS_LS_HB1	R	0x0	0b: No VDS OV in HB1 low side external MOSFET detected 1b: VDS OV detected in HB3 low side external MOSFET.
1	VDS_HS_HB2	R	0x0	0b: No VDS OV in HB2 high side external MOSFET detected 1b: VDS OV detected in HB4 high side external MOSFET.
0	VDS_LS_HB2	R	0x0	0b: No VDS OV in HB2 low side external MOSFET detected 1b: VDS OV detected in HB4 low side external MOSFET.

8.2.3. GEN_STA2

Table 8.7 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
GEN_STA2	0x02	PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	WD_FLT	SPI_CLK_FLT	SPI_ADDR_FLT
Operation Type		R	R	R	R	R	R	R	R

Table 8.8 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	PVDD_UV	R	0x0	0b: No PVDD undervoltage detected 1b: PVDD undervoltage detected
6	PVDD_OV	R	0x0	0b: No PVDD overvoltage detected 1b: PVDD overvoltage detected
5	VCP_UV	R	0x0	0b: No charge pump undervoltage detected 1b: charge pump undervoltage detected.
4	OTW	R	0x0	0b: No over temperature warning detected 1b: over temperature warning detected.
3	OTSD	R	0x0	0b: No over temperature shut down detected 1b: over temperature shut down detected
2	WD_FLT	R	0x0	0b: No watchdog fault detected 1b: watchdog fault detected.
1	SPI_CLK_FLT	R	0x0	0b: No SPI clock fault detected 1b: SPI clock fault detected
0	SPI_ADDR_FLT	R	0x0	0b: No SPI address fault detected 1b: SPI address fault detected

8.2.4. GEN_STA3

Table 8.9 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
GEN_STA3	0x03	Reserved	AREF_UV	Reserved	CSA_OC	Device_ID			
Operation Type		R	R	R	R	R			

Table 8.10 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	Reserved	R	0x0	Reserved
6	AREF_UV	R	0x0	0b: AREF UV not detected 1b: AREF UV detected
5	Reserved	R	0x0	Reserved
4	CSA_OC	R	0x0	0b: No CSA overcurrent detected 1b: CSA overcurrent detected
3	Device_ID	R	0x1	1101b: NSD3602S
2		R	0x1	
1		R	0x0	
0		R	0x1	

8.2.5. GEN_STA4

Table 8.11 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
GEN_STA4	0x16	Reserved						HB2_STA	HB1_STA
Operation Type		R	R	R	R	R	R	R	R

Table 8.12 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	Reserved	R	0x0	Reserved
6		R	0x0	
5		R	0x0	
4		R	0x0	
3		R	0x0	
2		R	0x0	
1	HB2_STA	R	0x0	HS2 VDS comparator output when HB2 in off state and OFF_DIAG_EN = 0
0	HB1_STA	R	0x0	HS1 VDS comparator output when HB1 in off state and OFF_DIAG_EN = 0

8.2.6. DRV_CTRL1

Table 8.13 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL1	0x04	DRV_EN	CP_SS_DIS	IN1_MODE	IN2_MODE	LOCK			DIAG_CLR
Operation Type		RW	RW	RW	RW	RW			RW

Table 8.14 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	DRV_EN	RW	0x0	0b: Gate driver disabled, MOS turn off by passive discharge path 1b: Gate driver enabled, MOS turned off by ISTRONG if other control signal is off
6	CP_SS_DIS	RW	0x0	0b: Charge pump spread spectrum enable (default value) 1b: Charge pump spread spectrum disabled
5	IN1_MODE	RW	0x0	0b: Internal IN1/EN signal is from IN1/EN pin (default value) 1b: Internal IN1/EN signal is from SPI_IN1/EN bit
4	IN2_MODE	RW	0x0	0b: Internal IN2/PH signal is from IN2/PH pin (default value) 1b: Internal IN2/PH signal is from SPI_IN2/PH bit
3	LOCK	RW	0x0	lock or unlock the CTRL registers. 011b: unlock all control registers (default value) 110b: lock all control register value and ignore bit written except LOCK bit in 0x04 other values are reserved[1].
2		RW	0x1	
1		RW	0x1	
0	DIAG_CLR	RW	0x0	0b: no action (default value) 1b: Trigger action - clear all fault, this bit will be 0 after action completion

1) After LOCK bits are set to 110b, WD_RST bits will also be locked, thus a watchdog error will be detected if watchdog has been enabled

8.2.7. DRV_CTRL2

Table 8.15 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL2	0x05	VGS_TDEAD_SEL	DRV_MODE		DRV_FW	SPI_IN1	SPI_IN2	SPI_HIZ1	SPI_HIZ2
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.16 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	VGS_TDEAD_SEL	RW	0x0	0b: Dead time between HS and LS is based on VGS monitoring and configured digital dead time (VGS handshaking enabled) 1b: Dead time between HS and LS is based on configured digital dead time (VGS handshaking disabled)
6	DRV_MODE	RW	0x0	H bridge input control mode 00b: Independent half bridge input control 01b: PH/EN H bridge input control 10b: PWM H bridge input control 11b: Split HS/LS solenoid input control
5		RW	0x0	
4	DRV_FW	RW	0x0	H bridge control freewheeling setting 0b: Low side freewheeling (default value) 1b: High side freewheeling.
3	SPI_IN1	RW	0x0	SPI control internal IN1/EN signal, need enable by IN1/EN_MODE bit 0b: SPI set internal IN1/EN signal = 0 (default value) 1b: SPI set internal IN1/EN signal = 1
2	SPI_IN2	RW	0x0	SPI control internal IN1/EN signal, need enable by IN2/PH_MODE bit 0b: SPI set internal IN2/PH signal = 0 (default value) 1b: SPI set internal IN2/PH signal = 1
1	SPI_HIZ1	RW	0x0	Internal HIZ1 signal is logic OR between SPI_HIZ1 bit and nHIZ1 pin (internal HIZ1 signal only active during half bridge mode) 0b: output follow IN1/EN signal 1b: HB1 driver off
0	SPI_HIZ2	RW	0x0	Internal HIZ1 signal is logic OR between SPI_HIZ2 bit and nHIZ2 pin (internal HIZ2 signal only active during half bridge mode) 0b: output follow IN2/PH signal 1b: HB2 driver off

8.2.8. DRV_CTRL3

Table 8.17 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL3	0x06	ISOURCE_HS				ISINK_HS			
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.18 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	ISOURCE_HS	RW	0x1	High side drivers turn on current 0000b: 0.25mA 0001b: 1mA 0010b: 2mA 0011b: 3mA 0100b: 4mA 0101b: 6mA 0110b: 8mA 0111b: 12mA 1000b: 16mA 1001b: 20mA 1010b: 24mA 1011b: 28mA
6		RW	0x1	
5		RW	0x1	
4		RW	0x1	

				1100b: 32mA 1101b: 40mA 1110b: 48mA 1111b: 64mA
3	ISINK_HS	RW	0x1	High side drivers turn off current 0000b: 0.25mA 0001b: 1mA 0010b: 2mA 0011b: 3mA 0100b: 4mA 0101b: 6mA 0110b: 8mA 0111b: 12mA 1000b: 16mA 1001b: 20mA 1010b: 24mA 1011b: 28mA 1100b: 32mA 1101b: 40mA 1110b: 48mA 1111b: 64mA
2		RW	0x1	
1		RW	0x1	
0		RW	0x1	

8.2.9. DRV_CTRL4

Table 8.19 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL4	0x07	ISOURCE_LS				ISINK_LS			
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.20 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	ISOURCE_LS	RW	0x1	Low side drivers turn on current 0000b: 0.25mA 0001b: 1mA 0010b: 2mA 0011b: 3mA 0100b: 4mA 0101b: 6mA 0110b: 8mA 0111b: 12mA 1000b: 16mA 1001b: 20mA 1010b: 24mA 1011b: 28mA 1100b: 32mA 1101b: 40mA 1110b: 48mA 1111b: 64mA
6		RW	0x1	
5		RW	0x1	
4		RW	0x1	
3	ISINK_LS	RW	0x1	Low side drivers turn off current 0000b: 0.25mA 0001b: 1mA 0010b: 2mA 0011b: 3mA 0100b: 4mA 0101b: 6mA 0110b: 8mA 0111b: 12mA 1000b: 16mA 1001b: 20mA 1010b: 24mA 1011b: 28mA 1100b: 32mA 1101b: 40mA 1110b: 48mA 1111b: 64mA
2		RW	0x1	
1		RW	0x1	
0		RW	0x1	

8.2.10. DRV_CTRL5

Table 8.21 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL5	0x08	VGS_FLT_MODE		TDRIVE		TDEAD			VGS_FLT_IND
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.22 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	VGS_FLT_MODE	RW	0x0	00b: Set VGS fault as latch fault 01b: Set VGS fault as cycle by cycle fault, fault automatically clear by new command 10b: Set VGS fault as warning fault, only report error by register, not turn off gate driver operation 11b: Set VGS fault as no fault, no reaction
6		RW	0x0	

5	TDRIVE	RW	0x1	Driver tdrive time setting also for VGS and VDS blanking time 00b: 96us 01b: 2us 10b: 4us 11b: 8us
4		RW	0x0	
3	TDEAD	RW	0x0	set digital dead time 000b: 0ns 001b: 250ns 010b: 500ns 011b: 750ns 100b: 1000ns 101b: 2000ns 110b: 4000ns 111b: 8000ns
2		RW	0x0	
1		RW	0x0	
0	VGS_FLT_IND	RW	0x0	This bit only active when BRG_MODE = 00b or 11b to set VGS fault whether turn off both half bridge or only fault half bridge 0b: turn off both half bridge 1b: only turn off fault half bridge

8.2.11. DRV_CTRL6

Table 8.23 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL6	0x09	VDS_OV_MODE		TFILTER_DS		ISINK_FLT		VGS_TH	VDS_OV_IND
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.24 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	VDS_OV_MODE	RW	0x0	00b: Set VDS OV fault as latch fault 01b: Set VDS OV fault as cycle by cycle fault, fault automatically clear by new command 10b: Set VDS OV fault as warning fault, only report error by register, not turn off gate driver operation 11b: Set VDS OV fault as no fault, no reaction
6		RW	0x0	
5	TFILTER_DS	RW	0x1	Set VDS OV filter time 00b: 1us 01b: 2us 10b: 4us 11b: 8us
4		RW	0x0	
3	ISINK_FLT	RW	0x0	Set turn off current for fault reaction 00b: ISINK_HS/LS 01b: 8mA 10b: 32mA 11b: 64mA
2		RW	0x0	
1	VGS_TH	RW	0x0	VGS threshold for handshaking and VGS fault 0b: 1.4V 1b: 1.0V
0	VDS_OV_IND	RW	0x0	This bit only active when BRG_MODE = 00b or 11b to set VDS OV fault whether turn off both half bridge or only fault half bridge 0b: turn off both half bridge 1b: only turn off fault half bridge

8.2.12. DRV_CTRL7

Table 8.25 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL7	0x0A	VDS_TH_HS				VDS_TH_LS			
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.26 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	VDS_TH_HS	RW	0x1	HS gate driver VDS threshold 0000b: 60mV 0001b: 80mV 0010b: 100mV 0011b: 120mV 0100b: 140mV 0101b: 160mV 0110b: 180mV 0111b: 200mV 1000b: 300mV 1001b: 400mV 1010b: 500mV 1011b: 600mV 1100b: 700mV 1101b: 1000mV (default) 1110b: 1400mV 1111b: 2000mV
6		RW	0x1	
5		RW	0x0	
4		RW	0x1	
3	VDS_TH_LS	RW	0x1	LS gate driver VDS threshold 0000b: 60mV 0001b: 80mV 0010b: 100mV
2		RW	0x1	

1		RW	0x0	0011b: 120mV 0100b: 140mV 0101b: 160mV 0110b: 180mV 0111b: 200mV 1000b: 300mV 1001b: 400mV 1010b: 500mV 1011b: 600mV 1100b: 700mV 1101b: 1000mV (default) 1110b: 1400mV 1111b: 2000mV
0		RW	0x1	

8.2.13. DRV_CTRL8

Table 8.27 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL8	0x0B	SYS_CLK_MOD_RAN		CP_EMI_MODE	OFF_DIAG_EN	OFF_PU_EN_HB1	OFF_PD_EN_HB1	OFF_PU_EN_HB2	OFF_PD_EN_HB2
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.28 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	SYS_CLK_MOD_RAN	RW	0x0	00b: Oscillator modulation range is 2.2% 01b: Oscillator modulation range is 5.5% 10b: Oscillator modulation range is 4.4% 11b: Oscillator modulation range is 7.7%
6		RW	0x0	
5	CP_EMI_MODE	RW	0x0	Charge pump EMI mode setting, need to be 0b for better EMI performance 0b: CP internal EMI improvement enabled (default) 1b: CP internal EMI improvement disabled
4	OFF_DIAG_EN	RW	0x0	0b: VDS comparator feedback to VGS_VDS_STA only after MOSFET is turned on with blanking and filter time (need clear VDS bits in VGS_VDS_STA if come back from off state diagnosis) 1b: change VDS comparator to real time comparator and feedback to VGS_VDS_STA
3	OFF_PU_EN_HB1	RW	0x0	0b: HB1 off state pull up current disabled 1b: HB1 off state pull up current enabled
2	OFF_PD_EN_HB1	RW	0x0	0b: HB1 off state pull down current disabled 1b: HB1 off state pull down current enabled
1	OFF_PU_EN_HB2	RW	0x0	0b: HB2 off state pull up current disabled 1b: HB2 off state pull up current enabled
0	OFF_PD_EN_HB2	RW	0x0	0b: HB2 off state pull down current disabled 1b: HB2 off state pull down current enabled

8.2.14. DRV_CTRL9

Table 8.29 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL9	0x0C	PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_TFILTER		PVDD_OV_TH	VCP_UV_MODE	VCP_UV_TH
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.30 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	PVDD_UV_MODE	RW	0x0	PVDD UV fault mode setting 0b: latch fault 1b: auto recover fault
6	PVDD_OV_MODE	RW	0x0	PVDD OV fault mode 00b: latch fault 01b: auto recover fault 10b: warning fault 11b: disabled, no fault
5		RW	0x0	
4	PVDD_OV_TFILTER	RW	0x1	PVDD OV filter time 00b: 1µs 01b: 2µs 10b: 4µs 11b: 8µs
3		RW	0x0	
2	PVDD_OV_TH	RW	0x1	PVDD OV threshold 0b: 22.5V 1b: 28.5V
1	VCP_UV_MODE	RW	0x0	VCP UV fault mode setting 0b: latch fault 1b: auto recover fault
0	VCP_UV_TH	RW	0x0	VCP UV threshold 0b: 2.5V 1b: 5V

8.2.15. DRV_CTRL10

Table 8.31 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL10	0x0D	CSA_SH_EN	CSA_BLANK_SOURCE	CSA_BLANK_SEL			CSA_OFFSET	CSA_GAIN	
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.32 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	CSA_SH_EN	RW	0x0	Current sense amplifier sample and hold function enabled or not 0b: disabled 1b: enabled
6	CSA_BLANK_SOURCE	RW	0x0	Current sense amplifier blanking trigger source 0b: half bridge1 1b: half bridge2
5	CSA_BLANK_SEL	RW	0x0	CSA output blanking timing % of Tdrive during turn on and Tdead (starting defined by VGS_TDEAD_SEL) during turn off 000b: 0%, blanking disabled 001b: 25% 010b: 37.5% 011b: 50% 100b: 62.5% 101b: 75% 110b: 87.5% 111b: 100%
4		RW	0x0	
3		RW	0x0	
2	CSA_OFFSET	RW	0x0	CSA offset setting 0b: AREF/2 1b: AREF/8
1	CSA_GAIN	RW	0x0	CSA gain setting 00b: 10V/V 01b: 20V/V 10b: 40V/V 11b: 80V/V
0		RW	0x1	

8.2.16. DRV_CTRL11

Table 8.33 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL11	0x0E	SYS_CLK_MOD	CP_SS_CONFIG	CP_DIS_PVDD_OV	VCP_UV_TH_M	WD_EN	WD_FLT_MODE	WD_TIMER	WD_RST
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.34 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	SYS_CLK_MOD	RW	0x0	0b: disable system clock frequency modulation 1b: enable system clock frequency modulation
6	CP_SS_CONFIG	RW	0x0	0b: CP modulation frequency is 16.5KHZ 1b: CP modulation frequency is 33KHZ
5	CP_DIS_PVDD_OV	RW	0x0	0b: charge pump keeps running during PVDD OV 1b: charge pump disables during PVDD OV
4	VCP_UV_TH_M	RW	0x0	0b: VCP UV threshold as 2.5V/5V (VCP_UV_TH mapping not change) 1b: VCP UV threshold as 6.25V/7.5V (VCP_UV_TH mapping changed, VCP_UV_TH = 0 means 6.25V, VCP_UV_TH = 1 means 7.5V)
3	WD_EN	RW	0x0	0b: watchdog timer disabled 1b: watchdog timer enabled
2	WD_FLT_MODE	RW	0x0	0b: set as warning fault, watchdog fault asserts register bit, while keeps gate driver active and not report on nFault logic 1b: set as latch fault, watchdog fault not only asserts register bit, but also disable gate pre-driver and reports on nFault logic
1	WD_TIMER	RW	0x0	0b: watchdog timer window 4 to 40ms 1b: watchdog timer window 10 to 100ms
0	WD_RST	RW	0x0	0b: default value after POR. The watchdog timer counting need refresh by periodly inverting WD_RST bit sent from microcontroller

8.2.17. DRV_CTRL12

Table 8.35 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL12	0x0F	CSA_OC_TH			CSA_OC_TFLT			CSA_OC_FLT_MODE	
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.36 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	CSA_OC_TH	RW	0x1	Configure CSA OC threshold when CSA offset=VAREF/8 000b: VSO>VAREF/8+2*VAREF/24 001b: VSO>VAREF/8+4*VAREF/24 010b: VSO>VAREF/8+6*VAREF/24 011b: VSO>VAREF/8+8*VAREF/24 100b: VSO>VAREF/8+10*VAREF/24 101b: VSO>VAREF/8+12*VAREF/24 110b: VSO>VAREF/8+14*VAREF/24 111b: VSO>VAREF/8+16*VAREF/24 Configure CSA OC threshold when CSA offset=VAREF/2 000b: VSO>VAREF/2+1*VAREF/24 or VSO<VAREF/2-1*VAREF/24 001b: VSO>VAREF/2+2*VAREF/24 or VSO<VAREF/2-2*VAREF/24 010b: VSO>VAREF/2+3*VAREF/24 or VSO<VAREF/2-3*VAREF/24 011b: VSO>VAREF/2+4*VAREF/24 or VSO<VAREF/2-4*VAREF/24 100b: VSO>VAREF/2+5*VAREF/24 or VSO<VAREF/2-5*VAREF/24 101b: VSO>VAREF/2+6*VAREF/24 or VSO<VAREF/2-6*VAREF/24 110b: VSO>VAREF/2+7*VAREF/24 or VSO<VAREF/2-7*VAREF/24 111b: Reserved
6		RW	0x0	
5		RW	0x0	
4	CSA_OC_TFLT	RW	0x0	Configure CSA OC filter time 000b: filter time = 1µs 001b: filter time = 2µs 010b: filter time = 4µs 011b: filter time = 6µs 100b: filter time = 8µs 101b: filter time = 10µs 110b: filter time = 50µs 111b: filter time = 100µs
3		RW	0x1	
2		RW	0x1	
1	CSA_OC_FLT_MODE	RW	0x0	Configure CSA OC fault behavior 00b: No fault 01b: Latch fault 10b: Warning fault 11b: Cycle by cycle
0		RW	0x0	

8.2.18. DRV_CTRL13

Table 8.37 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL13	0x10	PRE_EN	TDEAD_M	TDRIVE_M		VGS_TH_EN	LS_TIME_EN	BRAKE_DIS	CSA_DIS
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.38 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	PRE_EN	RW	0x0	0b: Disable pre-charge/discharge phase in HB1_HB2 1b: Enable pre-charge/discharge phase in HB1_HB2
6	TDEAD_M	RW	0x0	TDEAD time additional setting 0b: TDEAD time set by TDEAD bits 1b; TDEAD bits setting mapping become 000=3µs, 001=6µs,010=10µs,011=12µs,100=16µs,101=20µs,110=32µs,111=96µs
5	TDRIVE_M	RW	0x0	TDRIVE time additional setting 00b: TDRIVE time set by TDRIVE bits 01b: TDRIVE bits setting mapping become 00=0.5µs, 01=1µs, 10=1.5µs,11=2.5µs 10b: TDRIVE bits setting mapping become 00=3µs, 01=6µs, 10=10µs,11=12µs 11b: TDRIVE bits setting mapping become 00=16µs, 01=20µs, 10=24µs,11=32µs
4		RW	0x0	
3	VGS_TH_EN	RW	0x0	0b: Disable VGS monitor to end pre-charge phase during turn on and start post discharge during turn off (if disable, there will be no post-discharge and pre-charge will follow timing setting) 1b: Enable VGS monitor to end pre-charge phase during turn on and start post discharge during turn off (if disable, there will be no post-discharge and pre-charge will follow timing setting)
2	LS_TIME_EN	RW	0x0	0b: HS and LS use same timing by TDRIVE, TDRIVE_M, TDEAD and TDEAD_M 1b: HS and LS use different timing, HS timing set by TDRIVE, TDRIVE_M, TDEAD and TDEAD_M, while LS set by TDRIVE_LS and TDEAD_LS
1	BRAKE_DIS	RW	0x1	0b: Brake function can be triggered 1b: Brake function disabled
0	CSA_DIS	RW	0x0	0b: CSA enabled 1b: CSA disabled

8.2.19. DRV_CTRL14

Table 8.39 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL14	0x11	IPCHG_HS				IPDCHG_HS			
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.40 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	IPCHG_HS	RW	0x1	set pre-charge current for HS 0000b: 0.25mA 0001b: 1mA 0010b: 2mA 0011b: 3mA 0100b: 4mA 0101b: 6mA 0110b: 8mA 0111b: 12mA 1000b: 16mA 1001b: 20mA 1010b: 24mA 1011b: 28mA 1100b: 32mA 1101b: 40mA 1110b: 48mA 1111b: 64mA
6		RW	0x0	
5		RW	0x0	
4		RW	0x1	
3	IPDCHG_HS	RW	0x1	set pre-discharge current for HS 0000b: 0.25mA 0001b: 1mA 0010b: 2mA 0011b: 3mA 0100b: 4mA 0101b: 6mA 0110b: 8mA 0111b: 12mA 1000b: 16mA 1001b: 20mA 1010b: 24mA 1011b: 28mA 1100b: 32mA 1101b: 40mA 1110b: 48mA 1111b: 64mA
2		RW	0x0	
1		RW	0x0	
0		RW	0x1	

8.2.20. DRV_CTRL15

Table 8.41 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL15	0x12	TPCHG_HS		TPDCHG_HS		TPCHG_LS		TPDCHG_LS	
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.42 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	TPCHG_HS	RW	0x0	Configure pre-charge time for HS in HB1/HB2 00b: 70ns 01b: 140ns 10b: 280ns 11b: 560ns
6		RW	0x0	
5	TPDCHG_HS	RW	0x0	Configure pre-discharge time for HS in HB1/HB2 00b: 140ns 01b: 280ns 10b: 560ns 11b: 980ns
4		RW	0x1	
3	TPCHG_LS	RW	0x0	Configure pre-charge time for LS in HB1/HB2 00b: 70ns 01b: 140ns 10b: 280ns 11b: 560ns
2		RW	0x0	
1	TPDCHG_LS	RW	0x0	Configure pre-discharge time for LS in HB1/HB2 00b: 140ns 01b: 280ns 10b: 560ns 11b: 980ns
0		RW	0x1	

8.2.21. DRV_CTRL16

Table 8.43 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL16	0x13	IPCHG_LS				IPDCHG_LS			
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.44 Register Description

Bit	Field Name	Operation Type	Reset Value	Description

7	IPCHG_LS	RW	0x1	set pre-charge current for LS 0000b: 0.25mA 0001b: 1mA 0010b: 2mA 0011b: 3mA 0100b: 4mA 0101b: 6mA 0110b: 8mA 0111b: 12mA 1000b: 16mA 1001b: 20mA 1010b: 24mA 1011b: 28mA 1100b: 32mA 1101b: 40mA 1110b: 48mA 1111b: 64mA
6		RW	0x0	
5		RW	0x0	
4		RW	0x1	
3	IPDCHG_LS	RW	0x1	set pre-charge current for LS 0000b: 0.25mA 0001b: 1mA 0010b: 2mA 0011b: 3mA 0100b: 4mA 0101b: 6mA 0110b: 8mA 0111b: 12mA 1000b: 16mA 1001b: 20mA 1010b: 24mA 1011b: 28mA 1100b: 32mA 1101b: 40mA 1110b: 48mA 1111b: 64mA
2		RW	0x0	
1		RW	0x0	
0		RW	0x1	

8.2.22. DRV_CTRL17

Table 8.45 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL17	0x14	ISOURCE_L_HS		ISINK_L_HS		ISOURCE_L_LS		ISINK_L_LS	
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.46 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	ISOURCE_L_HS	RW	0x0	00b: ISOURCE for HS in HB1 and HB2 follow ISOURCE_HS map 01b: ISOURCE for HS in HB1 and HB2 follow ISOURCE_HS map+250μA 10b: ISOURCE for HS in HB1 and HB2 follow ISOURCE_HS map+500μA 11b: ISOURCE for HS in HB1 and HB2 follow ISOURCE_HS map+750μA
6		RW	0x0	
5	ISINK_L_HS	RW	0x0	00b: ISINK for HS in HB1 and HB2 follow ISINK_HS map 01b: ISINK for HS in HB1 and HB2 follow ISINK_HS map+250μA 10b: ISINK for HS in HB1 and HB2 follow ISINK_HS map+500μA 11b: ISINK for HS in HB1 and HB2 follow ISINK_HS map+750μA
4		RW	0x0	
3	ISOURCE_L_LS	RW	0x0	00b: ISOURCE for LS in HB1 and HB2 follow ISOURCE_LS map 01b: ISOURCE for LS in HB1 and HB2 follow ISOURCE_LS map+250μA 10b: ISOURCE for LS in HB1 and HB2 follow ISOURCE_LS map+500μA 11b: ISOURCE for LS in HB1 and HB2 follow ISOURCE_LS map+750μA
2		RW	0x0	
1	ISINK_L_LS	RW	0x0	00b: ISINK for LS in HB1 and HB2 follow ISINK_LS map 01b: ISINK for LS in HB1 and HB2 follow ISINK_LS map+250μA 10b: ISINK for LS in HB1 and HB2 follow ISINK_LS map+500μA 11b: ISINK for LS in HB1 and HB2 follow ISINK_LS map+750μA
0		RW	0x0	

8.2.23. DRV_CTRL18

Table 8.47 Register Map

REG_NAME	REG_ADDR	Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
DRV_CTRL18	0x15	TDEAD_LS				TDRIVE_LS			
Operation Type		RW	RW	RW	RW	RW	RW	RW	RW

Table 8.48 Register Description

Bit	Field Name	Operation Type	Reset Value	Description
7	TDEAD_LS	RW	0x0	Configure Tdead time for low side 0000b: 0μs 0001b: 0.25μs 0010b: 0.5μs
6		RW	0x0	

5		RW	0x0	0011b: 0.75µs 0100b: 1µs 0101b: 2µs 0110b: 3µs 0111b: 4µs 1000b: 6µs 1001b: 8µs 1010b: 10µs 1011b: 12µs 1100b: 16µs 1101b: 20µs 1110b: 32µs 1111b: 96µs
4		RW	0x0	
3	TDRIVE_LS	RW	0x0	Configure Tdrive time for low side 0000b: 0.5µs 0001b: 1µs 0010b: 1.5µs 0011b: 2µs 0100b: 2.5µs 0101b: 3µs 0110b: 4µs 0111b: 6µs 1000b: 8µs 1001b: 10µs 1010b: 12µs 1011b: 16µs 1100b: 20µs 1101b: 24µs 1110b: 32µs 1111b: 96µs
2		RW	0x1	
1		RW	0x1	
0		RW	0x0	

9. Application Note

9.1. Typical Application Circuit

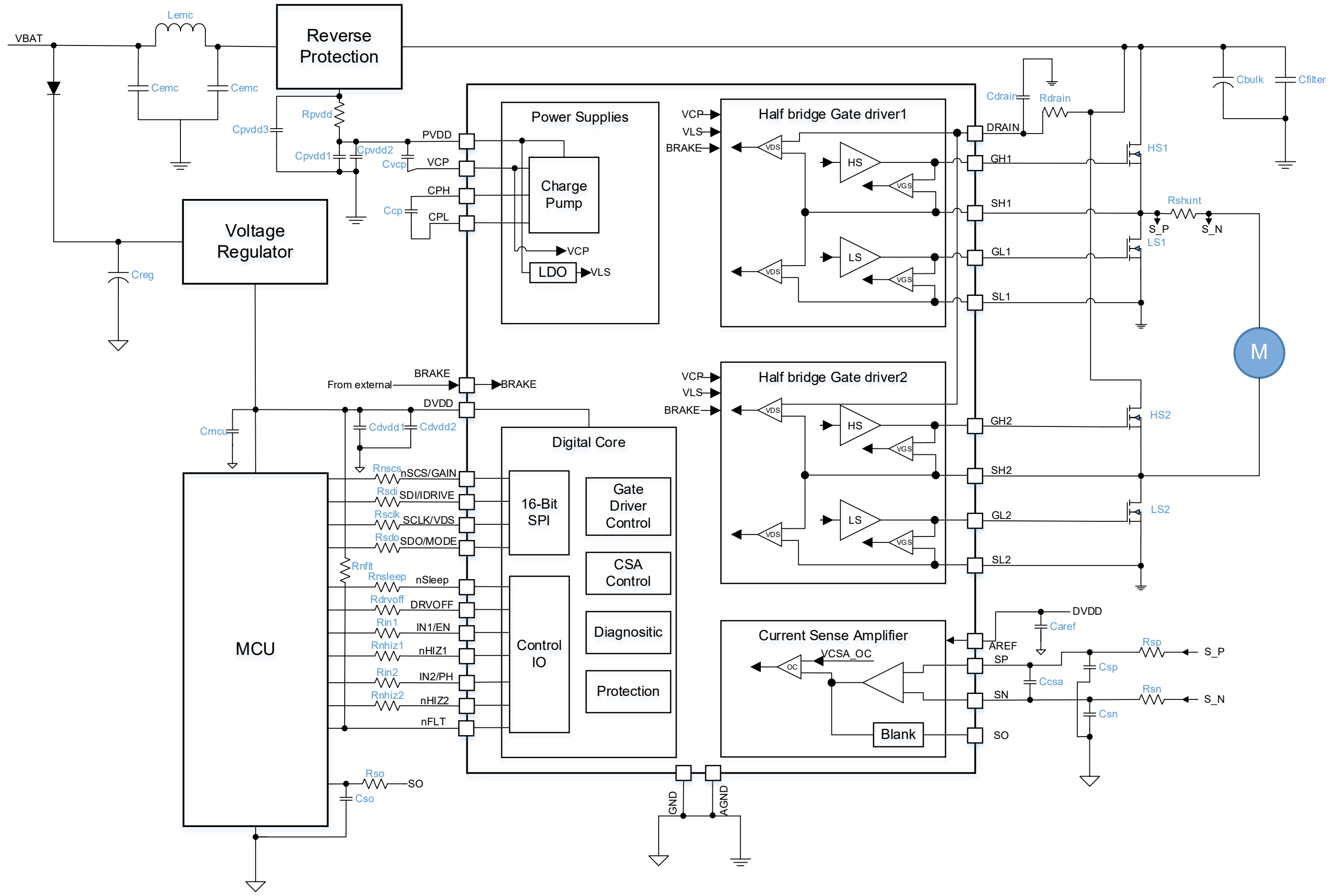


Figure 9.1 Typical Application Circuit

Table 9.1 Typical BOM List

Designer	***Value***
Recommendation	
Cpvdd1	0.1μF
Cvcp	1μF
Ccp	0.1μF
Cdvdd1	0.1μF
Cbulk	depend on application
Rshunt1/2	depend on application
Optional	
Lemc, Cemc	Depend on application
Rpvdd	1Ω~10Ω
Cpvdd2	1μF~10μF
Cpvdd3	10nF~10μF
Cdvdd2	1μF~3.3μF
Rnscs, Rsdi, Rsclk, Rsdo	10Ω~1kΩ
RnSLEEP, Rdrvoff, Rin1, Rin2, Rnhiz1, Rnhiz2	100Ω~10kΩ

Rnflt	1kΩ~100kΩ
Rso	10Ω~10kΩ
Cso	10pF~100nF
Rsp, Rsn	1Ω~10Ω
Csp, Csn	10pF~33nF
Ccsa	10pF~10nF
Cfilter	10nF~10μF
Rdrain	1Ω~100Ω
Cdrain	10pF~10nF

9.2. Application Hints

In application power supply for motors need to be lower than VCP voltage since internal there is reverse diode between VCP and GHx/SHx (better power supply for motors is same with PVDD).

10. Package Information

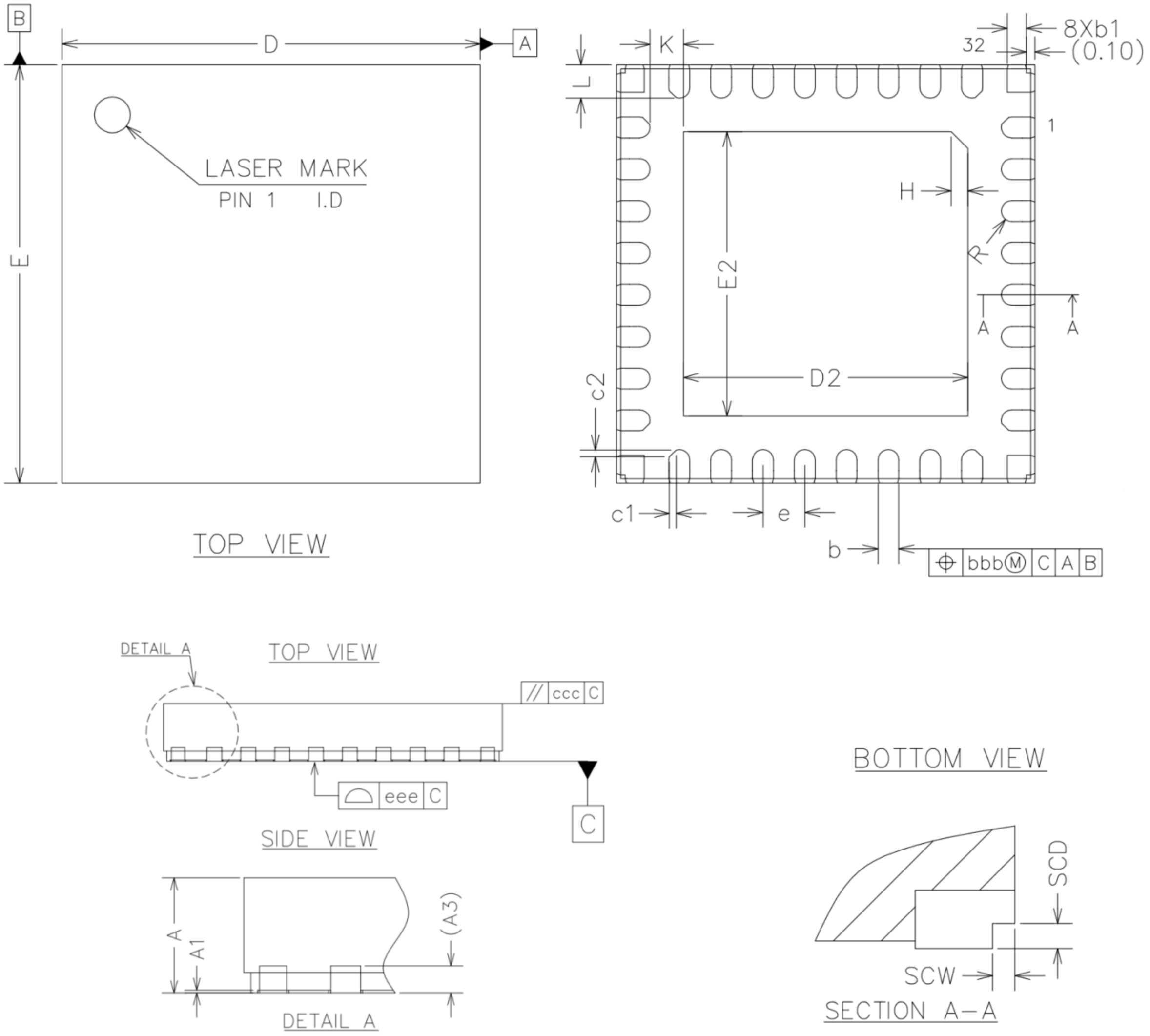


Figure 10.1 VQFN32 Package Outline

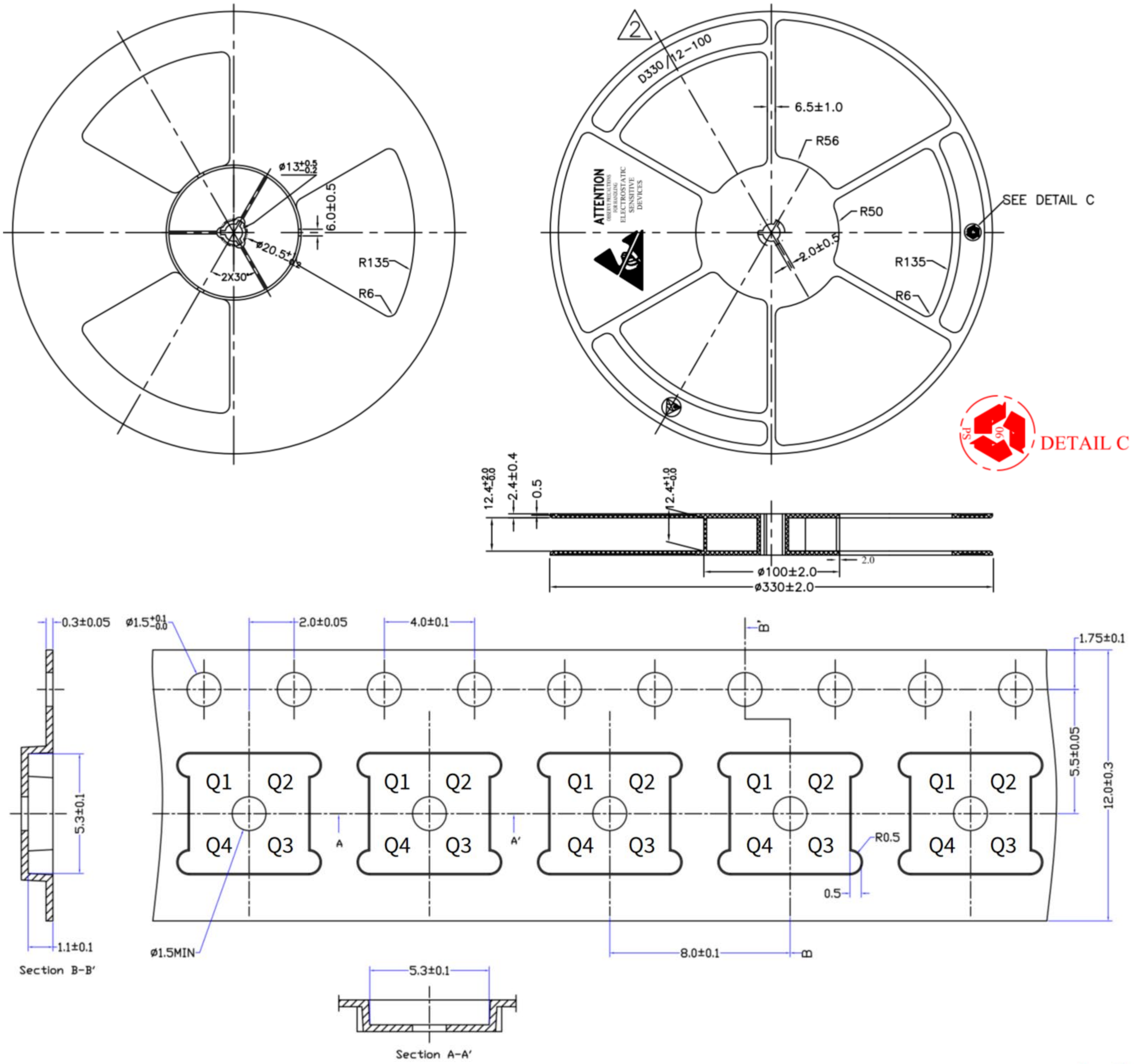
Table 10.1 VQFN32 Package Mechanical Data

Symbol	***MIN***	***TYP***	***MAX***	***Unit***
A	0.80	0.85	0.90	mm
A1	0	0.02	0.05	mm
A3		0.20		mm
b	0.20	0.25	0.30	mm
b1	0.18	0.23	0.28	mm
D	4.90	5.00	5.10	mm
E	4.90	5.00	5.10	mm
D2	3.30	3.40	3.50	mm
E2	3.30	3.40	3.50	mm
e		0.50		mm
H		0.20		mm
K	0.2			mm
L	0.30	0.40	0.50	mm
R	0.09			mm
bbb		0.10		mm
ccc		0.10		mm
eee		0.08		mm
SCW	0.01		0.09	mm
SCD	0.08		0.18	mm
c1		0.08		mm
c2		0.08		mm

11. Ordering Information

Part Number	***Package Type***	***Pins***	***Device Marking***	***Operation Temperature***	***MSL***	***SPQ***
NSD3602S-Q1QDAR	VQFN	32	NSD3602SQ	-40 to 125℃	3	5000
NSD3602H-Q1QDAR	VQFN	32	NSD3602HQ	-40 to 125℃	3	5000

12. Tape and Reel Information



Note:

1. Unit is mm
2. Device Pin 1 is in Q2 Quadrant

Figure 12.1 Tape and Reel Information

13. Revision History

Revision	Description	Date
1.0	Initial release	2025/04/15

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