NOVOSENSE

NSD10157-DSTAR

Single-Channel, High-Speed, Low-Side Gate Driver

Datasheet (EN) 1.0

Product Overview

The NSD10157 is a single-channel, high-speed gate driver. It can effectively drive MOSFET and IGBT power switches. Using a design that allows for a source of up to 3.5A and 4 A sink through symmetrical drive, coupled with the rail-to-rail drive capability, extremely small propagation delay 17ns (typical), the NSD10157 device is an ideal solution for MOSFET and IGBT power switches in demanding power electronics systems.

Key Features

- Offering optimal solution for driving FET and IGBTs
- Wide VDD range from 4.7V to 32V
- High peak drive currents: 3.5A (source) and 4A (sink)
- Fast propagation delays 17ns (typical)
- Fast rise and fall times: 9ns and 8ns (typical with 1.8nF load)
- Operation temperature: -40°C ~140°C
- REACH RoHS compliance

Applications

- PTC heaters
- Switch-mode power supplies
- Solar inverters, motor control, UPS
- HEV and EV chargers
- Home appliances
- Renewable energy power conversion
- SiC FET converters

Device Information

Part Number	*Package*	*Body Size*
NSD10157-DSTAR	SOT23-5	2.9mm × 1.6mm

Functional Block Diagrams

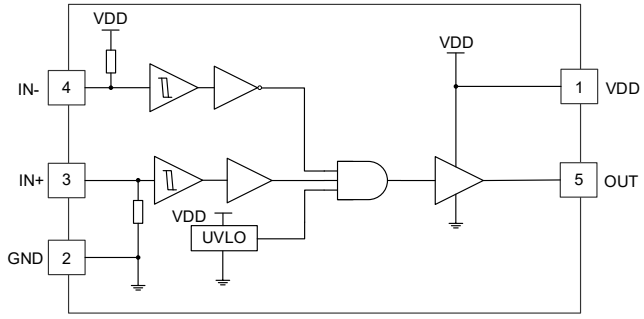

Figure 1. NSD10157 Block Diagram

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1. Pin Configuration and Functions

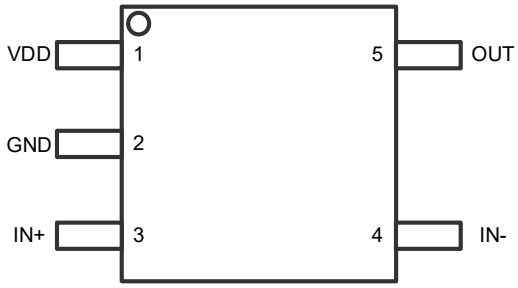


Figure 1.1 NSD10157 Pin Configuration

Table 1.1 NSD10157 Pin Configuration and Description

SYMBOL	*PIN NO.*	*FUNCTION*
1	VDD	Power supply
2	GND	Ground pin
3	IN+	Noninverting input
4	IN-	Inverting input
5	OUT	Driver output

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Comments
Power Supply Voltage	VDD	-0.3	35	V	
Input Pins Voltage	V_{IN+}, V_{IN-}	-10	35	V	
Output Voltage	V_{OUT}	-0.3	VDD+0.3	V	
		-2	VDD+0.3	V	Pulse＜200ns
Junction Temperature	T_J	-40	150	℃	
Storage Temperature	T_{stg}	-65	150	℃	

3. ESD Ratings

		Symbol	Value	Unit
Electrostatic Discharge	Human-body model (HBM), per AEC Q100-002[1)]	V_{ESD_HBM}	±2000	V
	Charged-device model (CDM), per AEC Q100-011[2)]	V_{ESD_CDM}	±2000	V

1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

2) AEC Q100-011 indicates that CDM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-002 specification.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Comments
Power Supply Voltage	VDD	4.7	32	V	
Input Pins Voltage	V_{IN+}, V_{IN-}	-5	32	V	

5. Thermal Information

Parameters	Symbol	SOT23-5	Unit
Junction-to-Ambient Thermal Resistance[1)]	$R_{\theta JA}$	168	°C/W
Junction-to-Case(top) Thermal Resistance[1)]	$R_{\theta JC\ (top)}$	102	°C/W

1) Tested using high effective thermal conductivity test board (2S2P) described in JESD51-7.

6. Specifications

6.1. Electrical Characteristics

VDD=12V, TA = -40°C to 140°C, unless otherwise noted, typical values are at TA=25°C.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Bias Current						
VDD Supply Start-up Current	I_{VDDSTR}	50	100	150	μA	VDD=3.4V, V_{IN+} = V_{IN-} =VDD
		50	100	150	μA	VDD=3.4V, V_{IN+} = V_{IN-} =GND
VDD Supply Quiescent Current	I_{VDDQ}	200	350	500	μA	V_{IN+} = V_{IN-} =VDD
		200	350	500	μA	V_{IN+} = V_{IN-} =GND
VDD Supply Operating Current	I_{VDDO}		4.3		mA	F=200kHz,1.8nF
Under Voltage Lockout (UVLO)						
VDD UVLO Rising Threshold	V_{VDD_ON}		4.2	4.6	V	
VDD UVLO Falling Threshold	V_{VDD_OFF}	3.5	3.9		V	
VDD UVLO Hysteresis	V_{VDD_HYS}		0.3		V	
Input Pin Characteristics (IN+, IN-)						
Logic High Input Threshold	V_{IN_H}		2.2	2.5	V	Output high for IN+ pin; Output low for IN- pin;
Logic Low Input Threshold	V_{IN_L}	1.0	1.3		V	Output low for IN+ pin; Output high for IN- pin;
Input Hysteresis Voltage	V_{IN_HYS}		0.9		V	
Input pull down Resistance	R_{IN+}		260		kΩ	
Input pull up Resistance	R_{IN-}		260		kΩ	
Output Pin Characteristic						
High Level Output Voltage	VDD - V_{OUT}		180	300	mV	Inject -100mA from out
Low Level Output Voltage	V_{OUT}		95	160	mV	Inject +100mA from out
Output Pull-Up Resistance	R_{OUTH}		1.80	3.0	Ω	
Output Pull-Down Resistance	R_{OUTL}		0.95	1.6	Ω	
High Level Peak Output Current[1)]	I_{OUTH}		3.5		A	Load=1μF
Low Level Peak Output Current[1)]	I_{OUTL}		4		A	Load=1μF

1) Not test covered, guaranteed by design.

6.2. Switching Characteristics

VDD=12V, TA = -40°C to 140°C, load=1.8nF, unless otherwise noted, typical values are at TA=25°C.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Minimum Pulse Width[1)]	T_{PWmin}		10		ns	
Output Rise Time[2)]	T_R		9		ns	
Output Fall Time[2)]	T_F		8		ns	
Propagation Delay[2)]	T_{PDLH}		17	30	ns	
	T_{PDHL}		17	30	ns	

1) The input pulse width increases with the increase of the load. When the load is 10nF, the minimum input pulse width required is ≥60ns.
2) See timing diagrams in Figure 6.1, Figure 6.2.

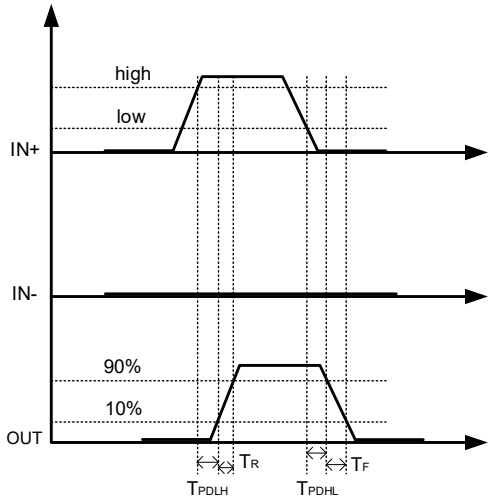


Figure 6.1 Noninverting Configuration

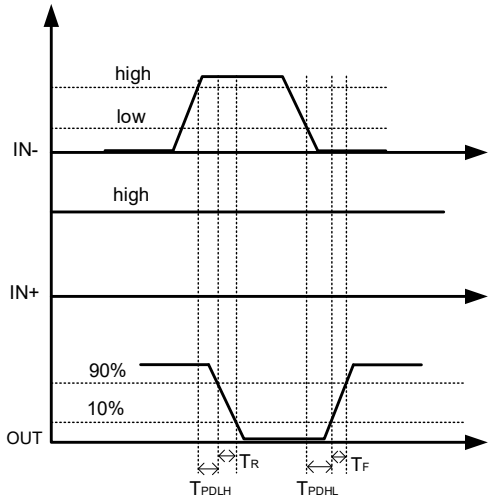


Figure 6.2 Inverting Configuration

6.3. Typical Performance Characteristics

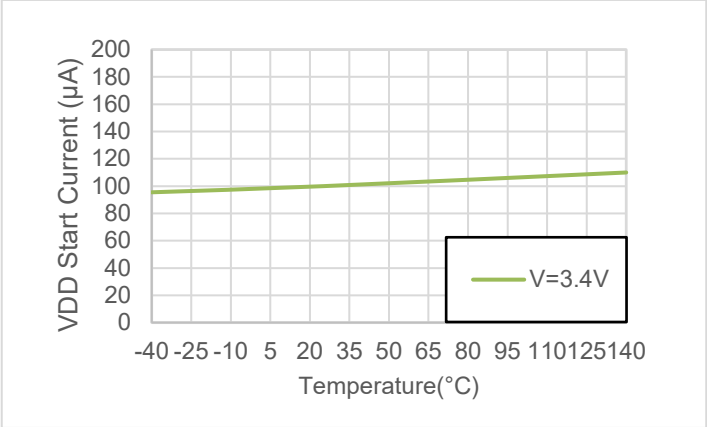


Figure 6.3 VDD(VIN=VDD) Start Current vs Temperature

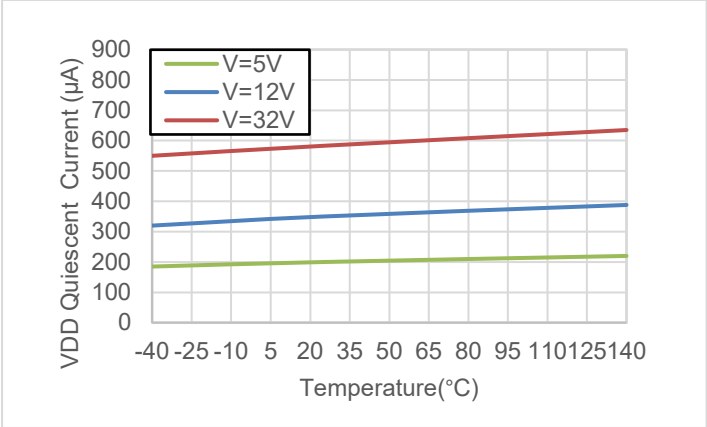


Figure 6.4 VDD(VIN=VDD) Quiescent Current vs Temperature

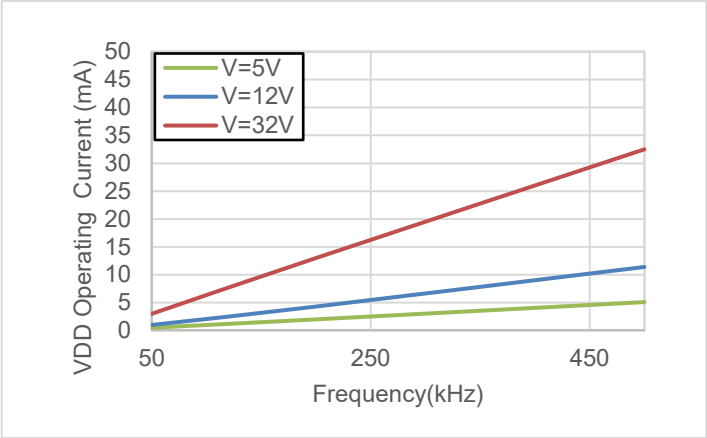


Figure 6.5 VDD Operating Current vs Frequency

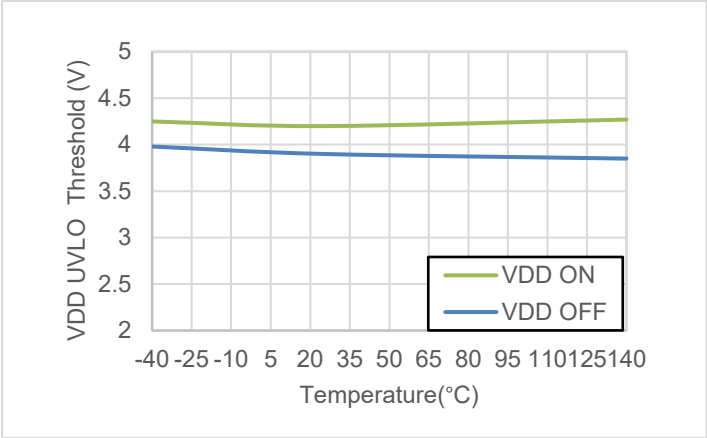


Figure 6.6 VDD UVLO Threshold vs Temperature

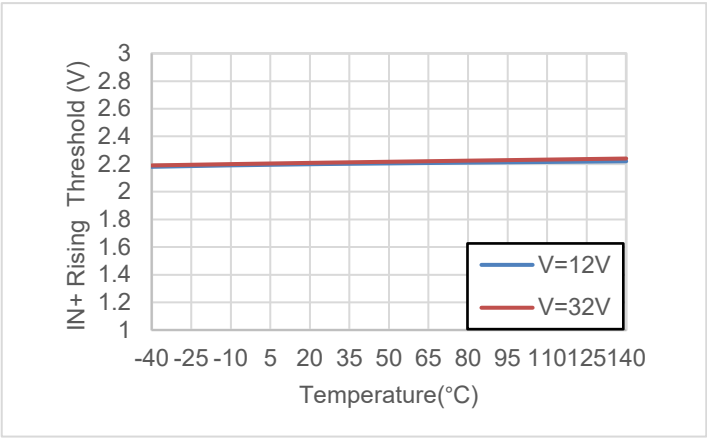


Figure 6.7 IN+ Rising vs Temperature

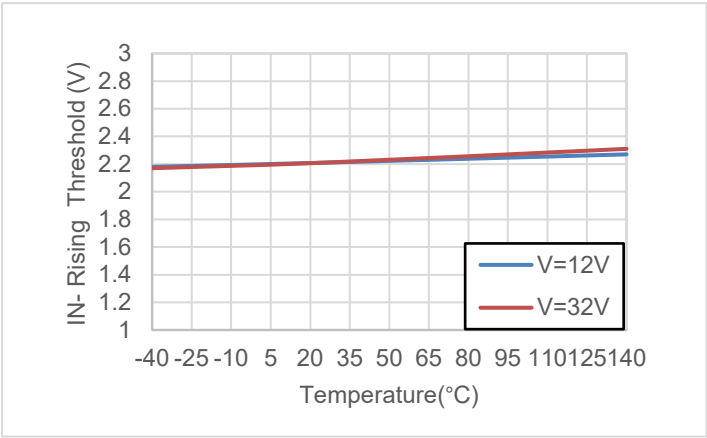


Figure 6.8 IN- Rising vs Temperature

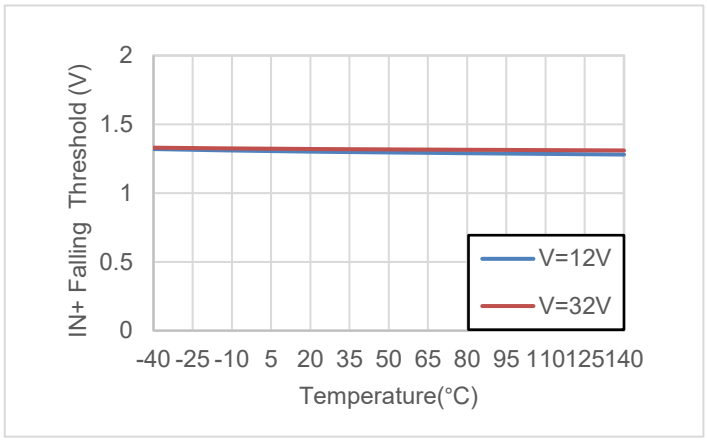


Figure 6.9 IN+ Falling vs Temperature

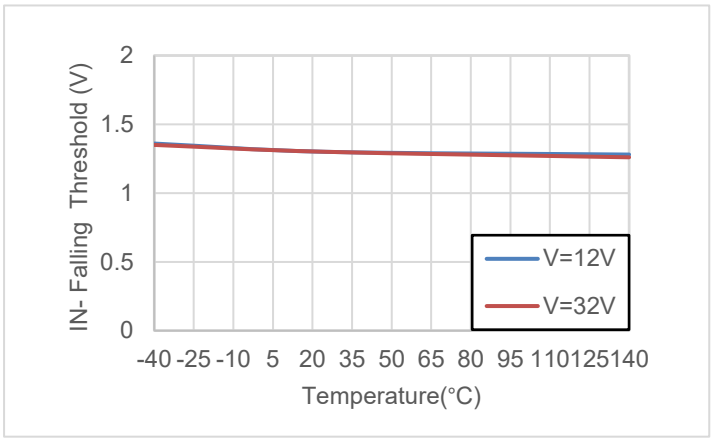


Figure 6.10 IN- Falling vs Temperature

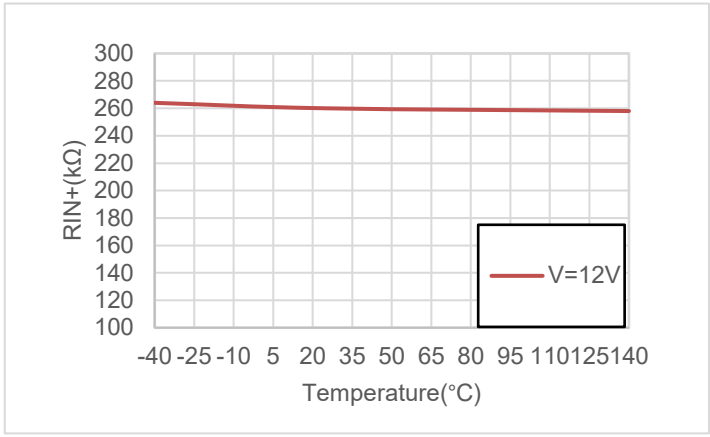


Figure 6.11 RIN+ vs Temperature

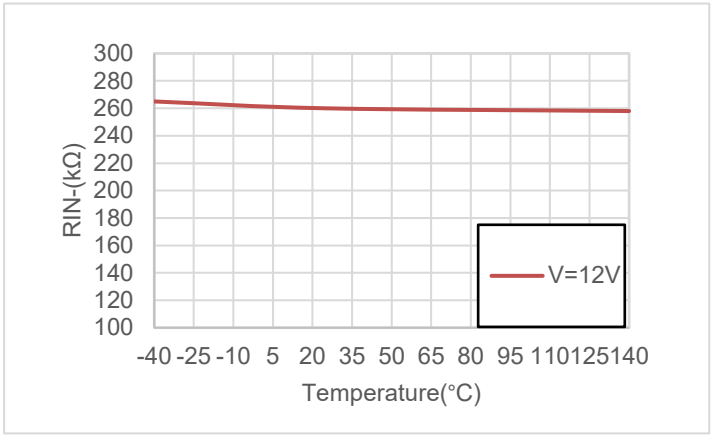


Figure 6.12 RIN- vs Temperature

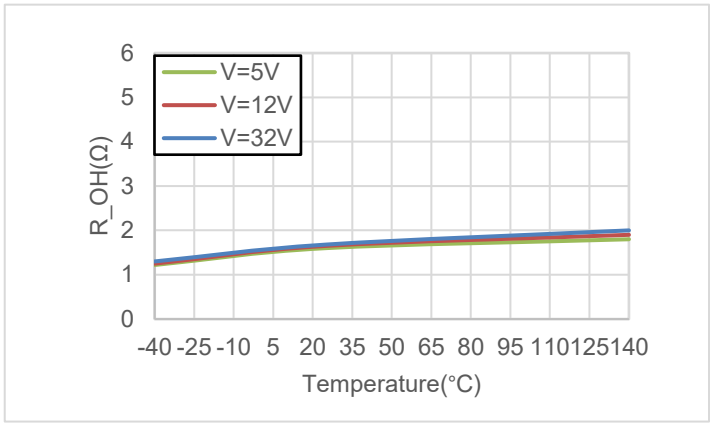


Figure 6.13 R_OH vs Temperature

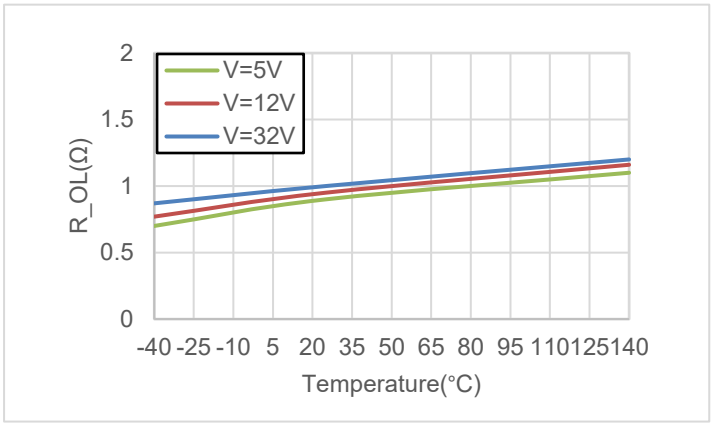


Figure 6.14 R_OL vs Temperature

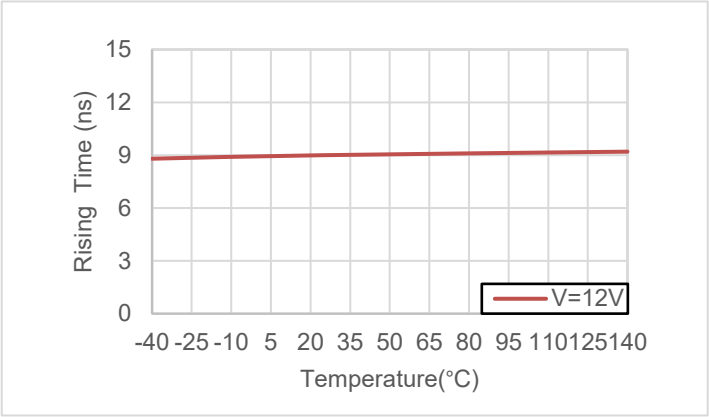


Figure 6.15 OUTPUT Rising vs Temperature

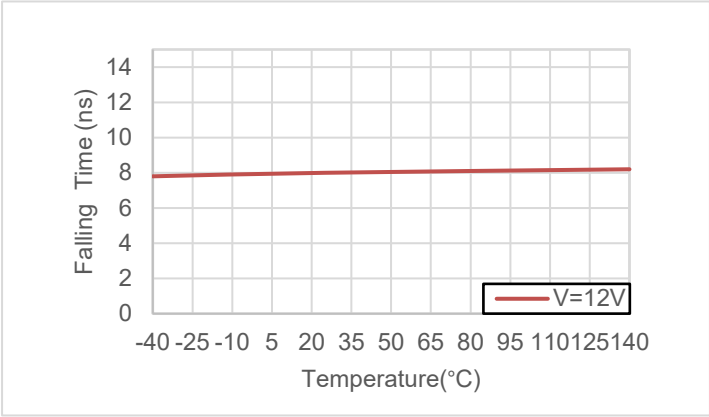


Figure 6.16 OUTPUT Falling vs Temperature

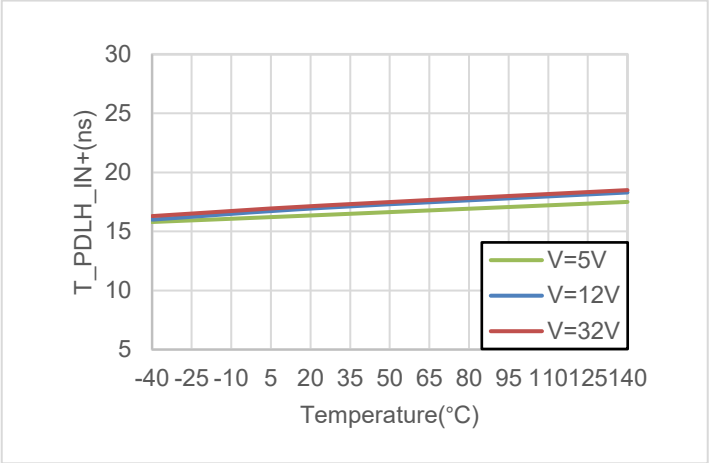


Figure 6.17 T_PDLH_IN+ vs Temperature

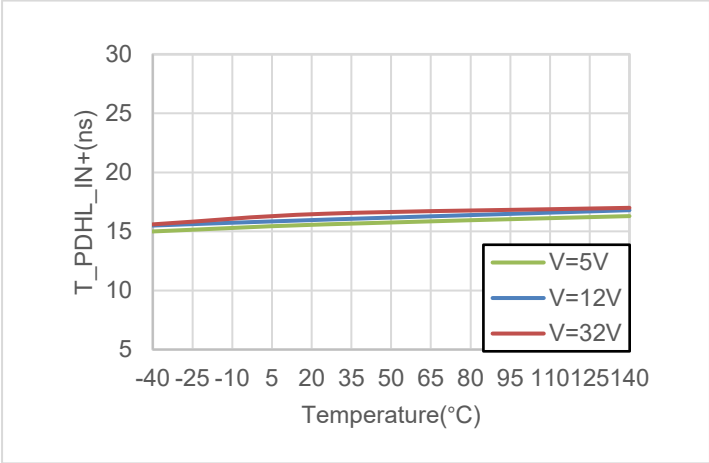


Figure 6.18 T_PDHL_IN+ vs Temperature

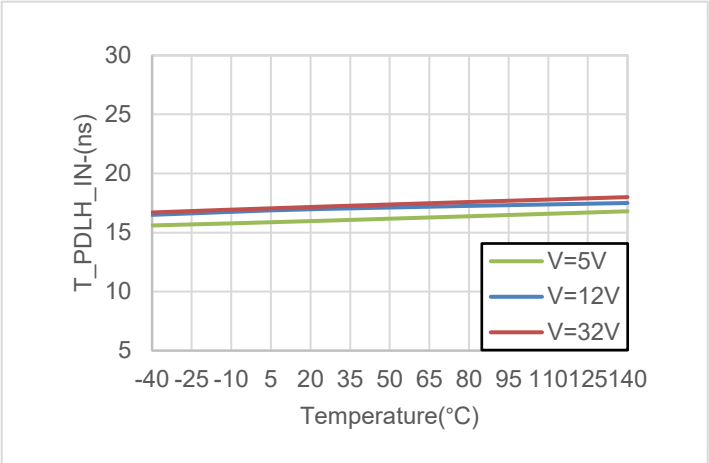


Figure 6.19 T_PDLH_IN- vs Temperature

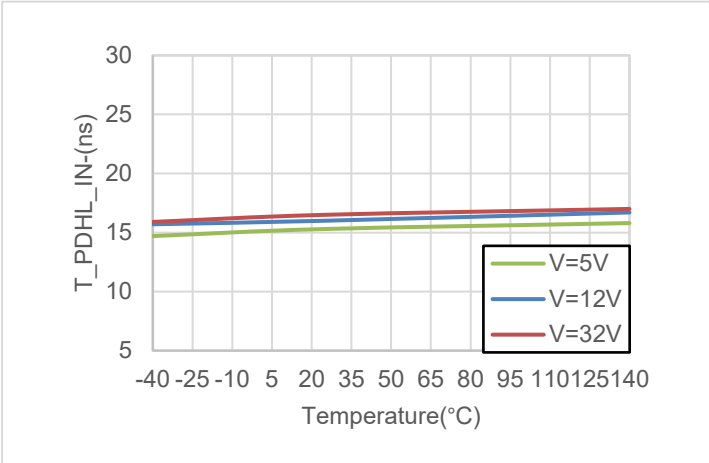


Figure 6.20 T_PDHL_IN- vs Temperature

7. Function Description

7.1. Overview

NSD10157 is a single-channel, high-speed, gate drivers capable of effectively driving MOSFET and IGBT power switches by up to 3.5A source and 4A sink (symmetrical drive) peak current. The driver has rail-to-rail drive capability and extremely small propagation delay, typically 17ns.

7.2. Input Stage

The input pins of NSD10157 device are based on TTL and CMOS compatible input threshold logic. With typical high threshold=2.2V and typical low threshold=1.3V, wider hysteresis (typically 0.9V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5V.

The device of NSD10157 features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD-pullup resistors on all the inverting inputs (IN- pin) or GND-pulldown resistors on all the noninverting input pins (IN+ pin), (refer to Functional Block Diagrams).

7.3. Enable Function

As mentioned earlier, an enable/disable function is easily implemented in the NSD10157using the unused input pin. When IN+ is pulled down to GND or IN- is pulled down to VDD, the output is disabled. Thus IN+ pin is used like an enable pin that is based on active-high logic, while IN- can be used like an enable pin that is based on active-low logic.

7.4. Output Stage

The output of NSD10157 is composed of P-Channel MOSFET and N-Channel MOSFET. The P-Channel MOSFET has a low impedance on-resistance of 1.65Ω (typ), and the N-Channel MOSFET also has a low impedance on-resistance of 0.95Ω (TYP). The NSD10157 can deliver 3.5A source, and up to 4A sink at VDD=12V. Strong sink capability results in a very low pull-down impedance in the driver output stage which boosts immunity against the parasitic Miller turn on (high slew rate dV/dt turn on) effect that is seen in both IGBT and FET power switches.

7.5. Device Functional Modes

Table 7.1 Device Logic Table

IN+ pin	IN- pin	OUT pin
H	L	H
H	H	L
L	L	L
L	H	L
Floating	Any	L
Any	Floating	L

8. Application Note

8.1. Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3V or 5V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P-N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The NSD10157 is very flexible in this role with a strong current drive capability and wide supply voltage range up to 32V. This allows the driver to be used in 12V Si MOSFET applications, 20V and -5V (relative to Source) SiC FET applications, 15V and -15V (relative to Emitter) IGBT applications and many others. As a single channel driver, the NSD10157 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. These requirements coupled with the need for low propagation delays and availability in compact, low inductance packages with good thermal capability makes gate driver devices such as the NSD10157 extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

8.2. Typical Application Circuit

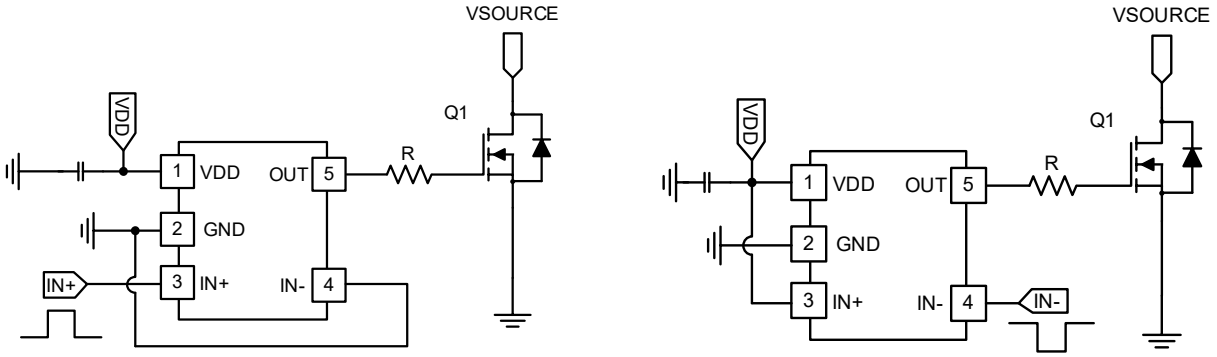
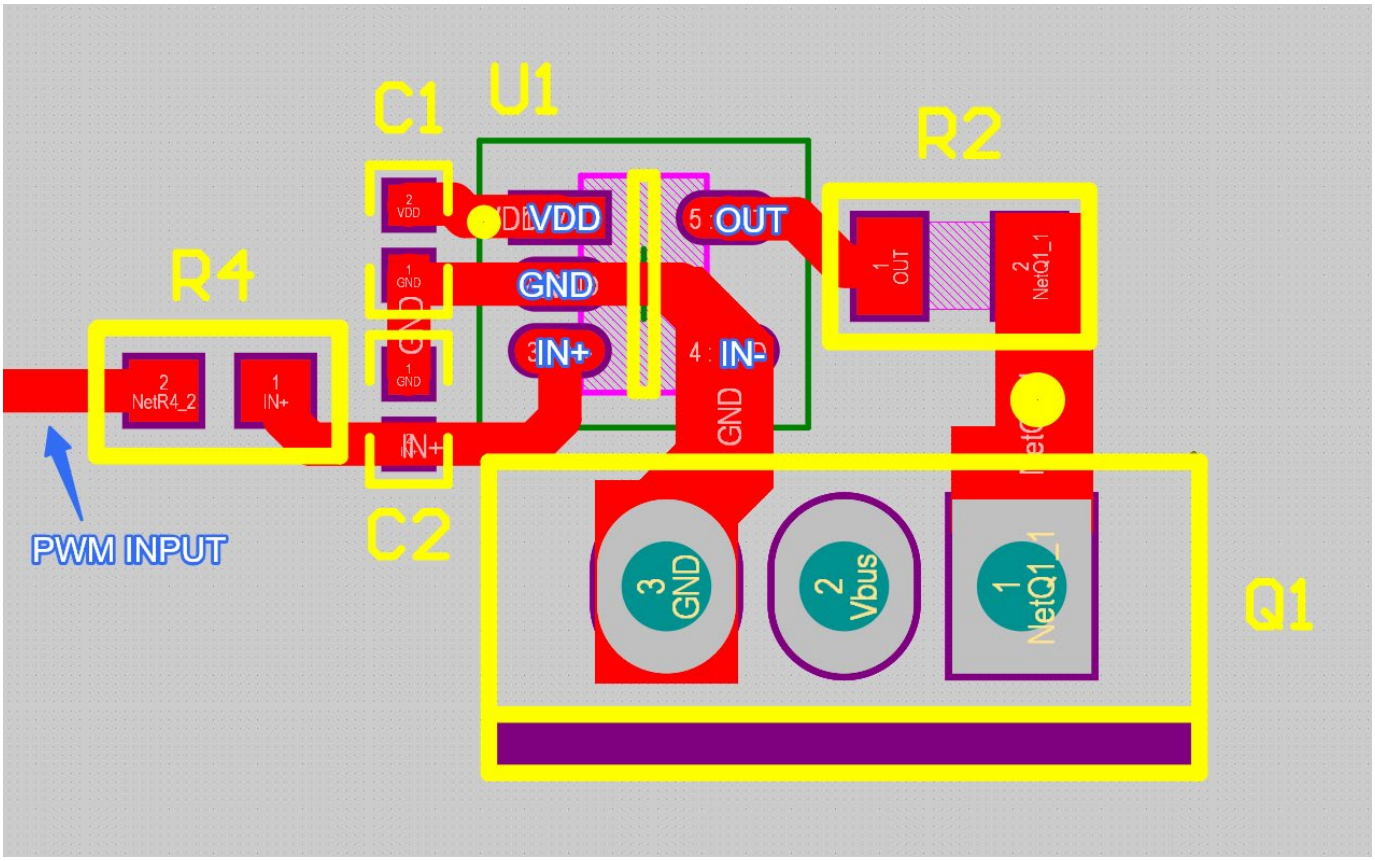


Figure 8.1 NSD10157 Typical application circuit

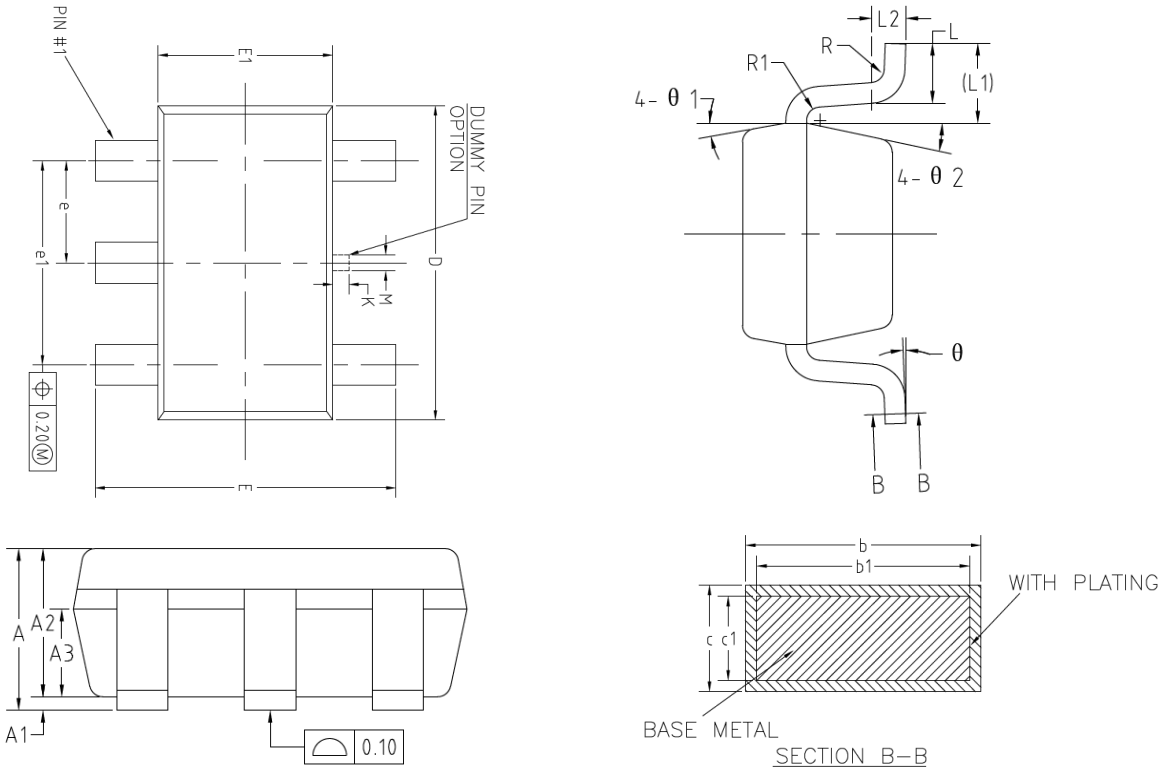
8.3. Layout Guidelines

Proper PCB layout is vitally important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The NSD10157 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of the power switch to facilitate voltage transitions very quickly. The peak current of NSD10157 is +3.5A/-4A under a power supply of VDD=12. Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Place the VDD bypass capacitor between VDD and GND, as close to the driver as possible, while minimizing the trace length to improve the noise filtering effect. These capacitors support the high peak current drawn from VDD during the conduction period of the power MOSFET. It is highly recommended to use low-inductance surface-mount devices.
- Place the driver device as close as possible to the power device in order to minimize the length of high current traces between the output pin and the gate of the power device.
- Separate power traces and signal traces, such as output and input signals.
- In noisy environments, tying the unused input pin of NSD10157 to GND (in case of IN+) or VDD (in case of IN–) using short traces to ensure that the output is enabled and to prevent noise from causing malfunction in the output is necessary.


C1
U1
R2
R4
C2
Q1
VDD
GND
IN+
IN-
OUT
PWM INPUT
NetR4_2
NetQ1_1
Vbus

9. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
4	b	0.34	–	0.45
4	b1	0.34	0.38	0.41
4	c	0.12	–	0.20
4	c1	0.12	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
3	E1	1.526	1.626	1.700
	e	0.90	0.95	1.00
	e1	1.80	1.90	2.00
2	K	0	–	0.20
	L	0.30	0.40	0.60
	L1	0.59REF		
	L2	0.25BSC		
2	M	0.10	0.15	0.20
	R	0.05	–	0.20
	R1	0.05	–	0.20
	θ	0°	–	8°
	θ 1	8°	10°	12°
	θ 2	10°	12°	14°

Figure 9.1 SOT23-5 Package Shape and Dimension

10. Tape and Reel Information

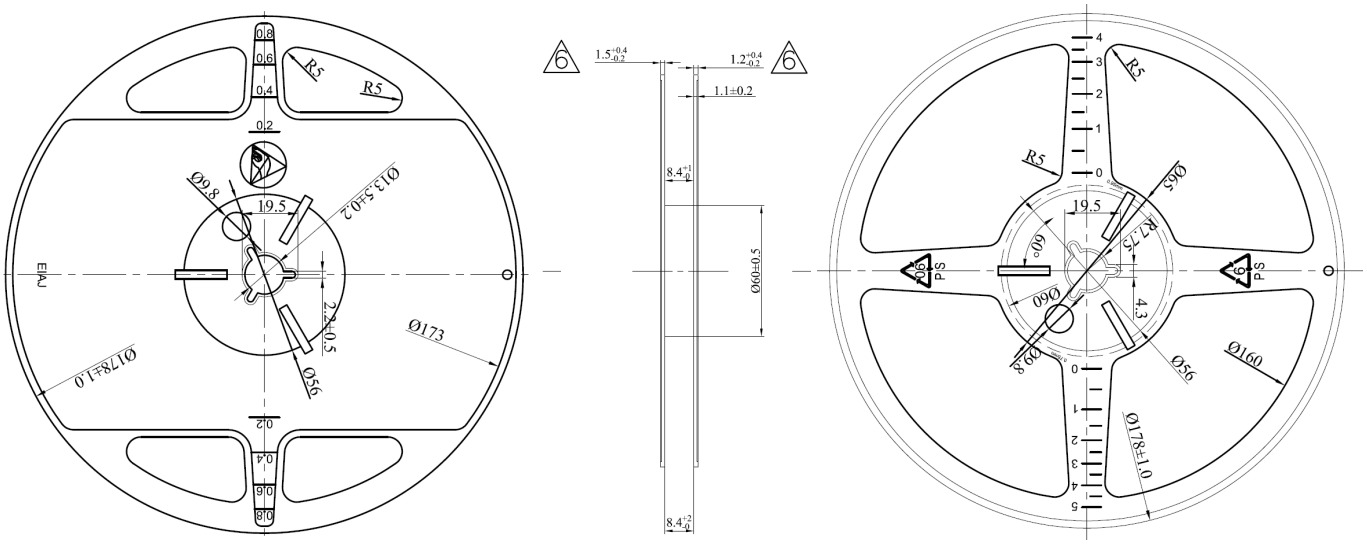
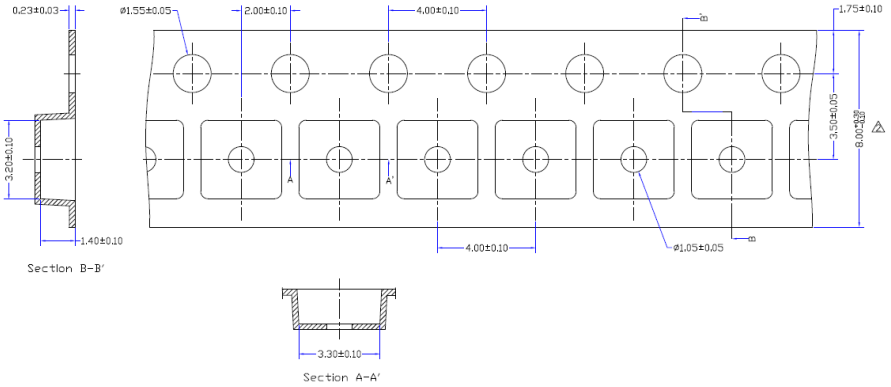


Figure 10.1 Reel Information



NOTES：

1. MATERIAL: CONDUCTIVE PS
2. ALL DIMS IN MM
3. There must not be foreign body adhesion and the state of the surface must be excellent
4. A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.2 up to 10 pitches
5. Ø560 PAPER-Reel,255000pockets(1020m)
6. Surface resistance 1×10E5~1×10E9 OHMS/SQ

Figure 10.2 Tape Information

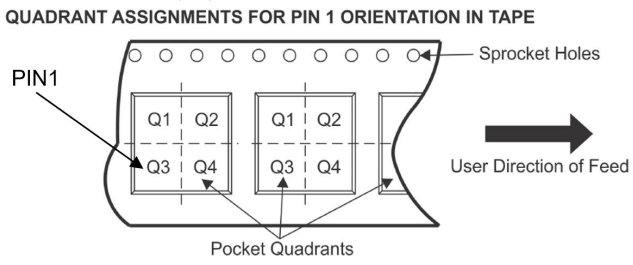


Figure 10.3 Quadrant Designation for Pin1 Orientation in Tape

11. Ordering Information

Part No.	Temperature	Qualification	Package Type	MSL	SPQ
NSD10157-DSTAR	-40 to 140°C	Industrial	SOT23-5	3	3000

12. Revision History

Revision	Description	Date
1.0	Initial Version.	2026/01/13

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