

Product Overview

The NSD10151 single-channel, high-speed gate driver can effectively drive MOSFET and IGBT power switches. Using a design that allows for a source of up to 2A and 4A sink through asymmetrical drive split outputs, coupled with the rail-to-rail drive capability, extremely small propagation delay 30ns (typical), the NSD10151 device is an ideal solution for MOSFET and IGBT power switches. The split outputs and strong asymmetrical drive boost the devices immunity against parasitic Miller turn-on effect and can help reduce ground debouncing.

Key Features

- Offering optimal solution for driving FET and IGBT
- Wide VDD range from 13V to 32V
- High peak drive currents: 2A (source) and 4A (sink)
- Fast propagation delays: 30ns (typical)
- Fast rise and fall times: 17ns and 8ns (typical with 1.8nF load)
- Split output options allow for tuning of turn on and turn off currents
- Operation temperature: -40°C~125°C
- AEC-Q100 qualified for Grade 1
- Reach RoHS compliance

Applications

- PTC heaters
- Switched-mode power supplies
- Solar inverters, motor control, UPS
- HEV and EV chargers
- Home appliances
- Renewable energy power conversion
- SiC FET converters

Device Information

Part Number	Package	Body Size
NSD10151-Q1STCR	SOT23-6	2.9mm × 1.6mm

Functional Block Diagrams

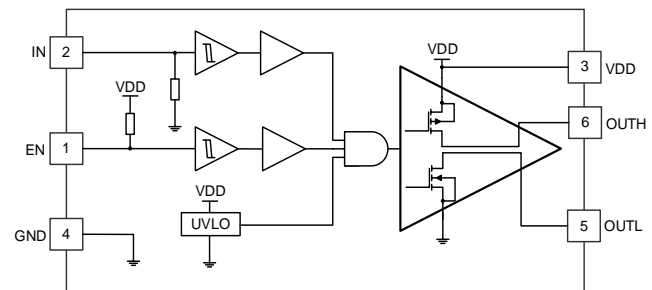


Figure 1. NSD10151 Block Diagram

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1. Pin Configuration and Functions

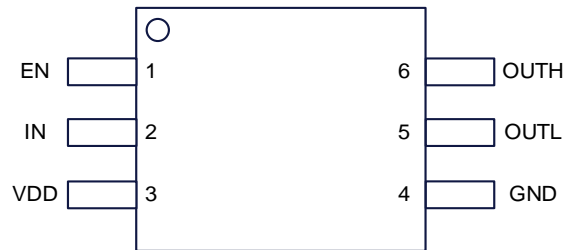


Figure 1.1 NSD10151 Pin Configuration

Table 1.1 NSD10151 Pin Configuration and Description

SYMBOL	PIN NO.	FUNCTION
EN	1	Enable (Pull EN to GND to disable output, pull it high or leave open to enable output)
IN	2	Logic Input Pin
VDD	3	Bias Supply Input
GND	4	Ground (all signals are referenced to this node)
OUTL	5	Driver Output
OUTH	6	Driver Output

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Comments
Power Supply Voltage	VDD	-0.3	35	V	
Input and Enable Pins Voltage	V_{IN}/V_{EN}	-10	VDD+0.3	V	
Output Voltage	V_{OUTL}/V_{OUTH}	-0.3	VDD+0.3	V	
		-2	VDD+0.3	V	Pulse < 200ns
Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_{stg}	-65	150	°C	

3. ESD Ratings

		Symbol	Value	Unit
Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ¹⁾	V_{ESD_HBM}	±2000	V
	Charged-device model (CDM), per AEC Q100-011	V_{ESD_CDM}	±2000	V

- 1) ACE Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Comments
Power Supply Voltage	VDD	13	32	V	
Input Pins Voltage	V _{IN} , V _{EN}	-5	32	V	
Output Pins Voltage	V _{OUTL} /V _{OUTH}	0	32	V	

5. Thermal Information

Parameters	Symbol	SOT23-6	Unit
Junction-to-Ambient Thermal Resistance ¹⁾	R _{θJA}	142	°C/W
Junction-to-Case(top) Thermal Resistance ¹⁾	R _{θJC (top)}	90	°C/W

1) Tested using high effective thermal conductivity test board (2S2P) described in JESD51-7.

6. Specifications

6.1. Electrical Characteristics

VDD=18V, TA =-40°C to 125°C, unless otherwise noted, typical values are at TA=25°C.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Bias Current						
VDD Supply Start-up Current	I _{VDDSTR}	180	290	460	μA	V _{EN} =V _{IN} =9V
		150	250	440	μA	V _{EN} =V _{IN} =GND
VDD Supply Quiescent Current	I _{VDDQ}	300	460	770	μA	V _{EN} =V _{IN} =VDD=18V
		280	420	660	μA	V _{EN} =V _{IN} =GND
VDD Supply Operating Current	I _{VDD}		7.0		mA	F=200kHz, Load:1.8nF
Under Voltage Lockout (UVLO)						
VDD UVLO Rising Threshold	V _{VDD_ON}	10.8	11.9	12.8	V	
VDD UVLO Falling Threshold	V _{VDD_OFF}	9.4	10.7	11.6	V	
VDD UVLO Hysteresis	V _{VDD_HYS}		1.2		V	
Input Pin Characteristics						
Logic High Input Threshold	V _{IN_H}	1.8	2.1	2.5	V	
Logic Low Input Threshold	V _{IN_L}	0.8	1.2	1.6	V	
Input Hysteresis Voltage	V _{IN_HYS}		0.9		V	
Input Pull Down Resistors	R _{IN}	190	260	310	kΩ	
Enable Signal High Threshold	V _{EN_H}	1.8	2.1	2.5	V	
Enable Signal Low Threshold	V _{EN_L}	0.8	1.2	1.6	V	
Enable Signal Hysteresis	V _{EN_HYS}		0.9		V	
Enable Pull Up Resistors	R _{EN}	190	260	310	kΩ	
Output Pin Characteristic						
High Level Output Voltage	V _{VDD} - V _{OUTH}		300	550	mV	Inject -100mA from OUTH
Low Level Output Voltage	V _{OUTL}		95	180	mV	Inject +100mA from OUTL
Output Pull-Up Resistance	R _{OUTH}		3.0	5.5	Ω	
Output Pull-Down Resistance	R _{OUTL}		0.95	1.8	Ω	
High Level Peak Output Current ¹⁾	I _{OUTH}		2		A	Load=1μF
Low Level Peak Output Current ¹⁾	I _{OUTL}		4		A	Load=1μF

1) Not test covered, guaranteed by design.

6.2. Switching Characteristics

VDD=18V, Load=1.8nF, TA =-40°C to 125°C, unless otherwise noted, typical values are at TA=25°C.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Minimum Pulse Width	T _{PWmin}		10	25	ns	
Output Rise Time	T _R		17		ns	
Output Fall Time	T _F		8		ns	
Propagation Delay	T _{PDLH_IN}		30	45	ns	
	T _{PDHL_IN}		30	45	ns	
Time to enable the driver once the EN pin is pulled high	T _{Delay_ON_EN}		30	47	ns	
Time to disable the driver once the EN pin is pulled low	T _{Delay_OFF_EN}		30	47	ns	

6.3. Typical Performance Characteristics

VDD =18V, TA =-40°C to 125°C, unless otherwise noted, typical values are at TA=25°C.

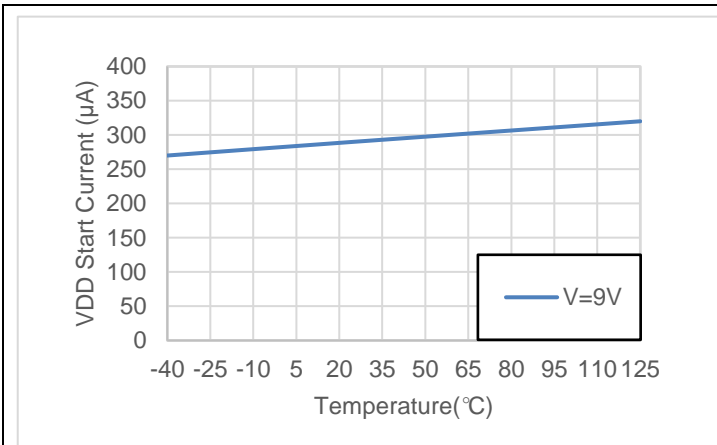


Figure 6.1 VDD Start Current (VIN=VDD) vs Temperature

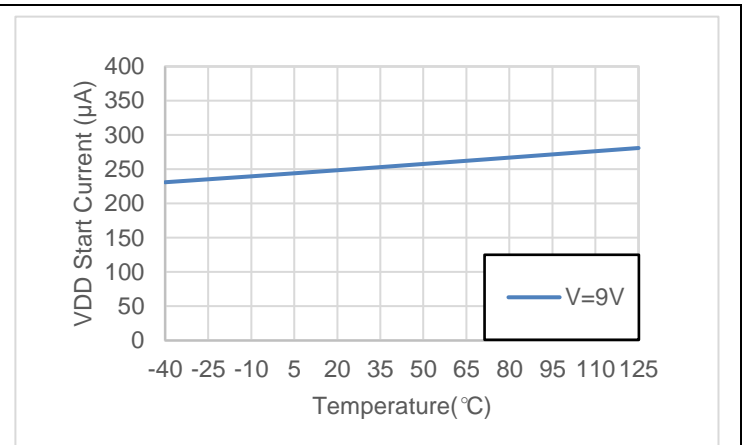


Figure 6.2 VDD Start Current (VIN=GND) vs Temperature

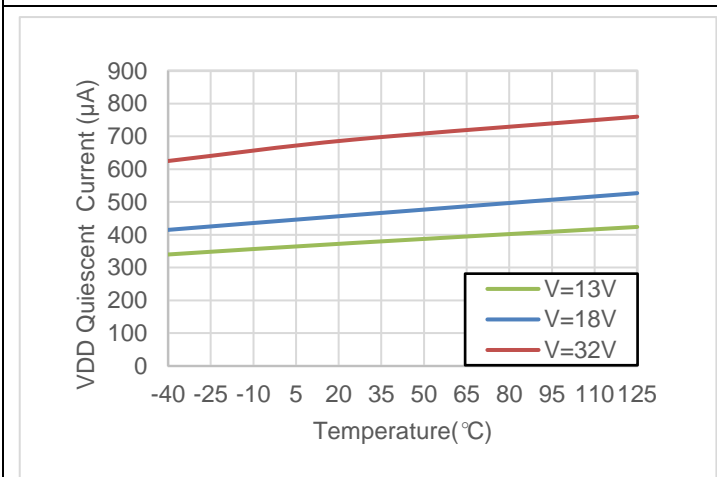


Figure 6.3 VDD Quiescent Current (VIN=VDD) vs Temperature

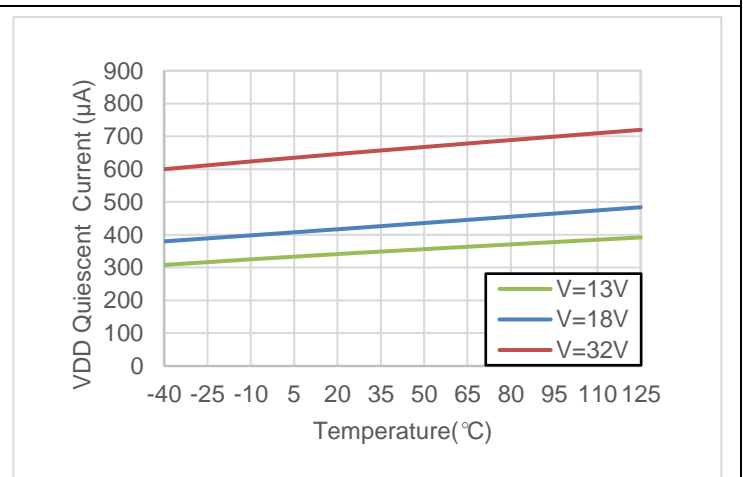


Figure 6.4 VDD Quiescent Current (VIN=GND) vs Temperature

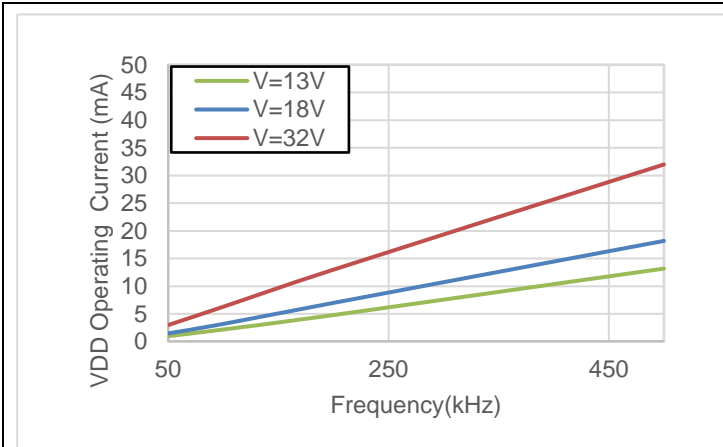


Figure 6.5 VDD Operating Current vs Frequency

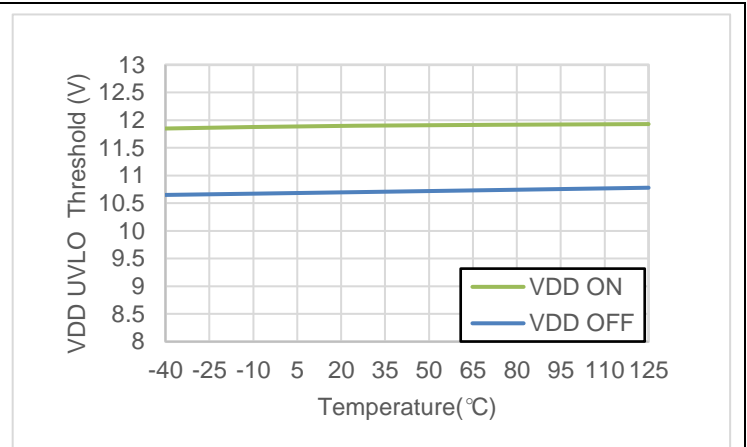


Figure 6.6 VDD UVLO Threshold vs Temperature

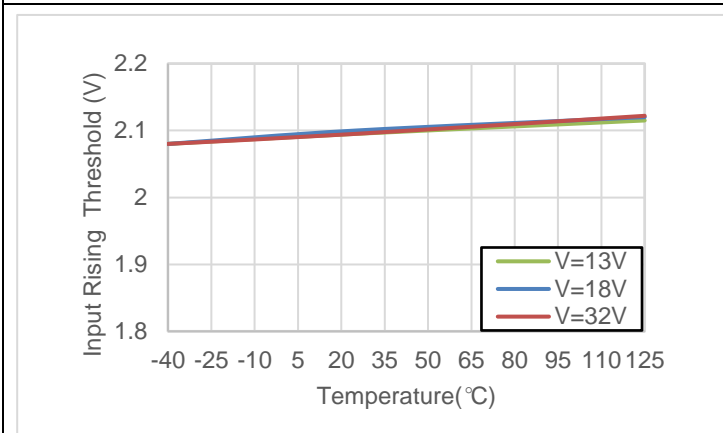


Figure 6.7 Input Rising vs Temperature

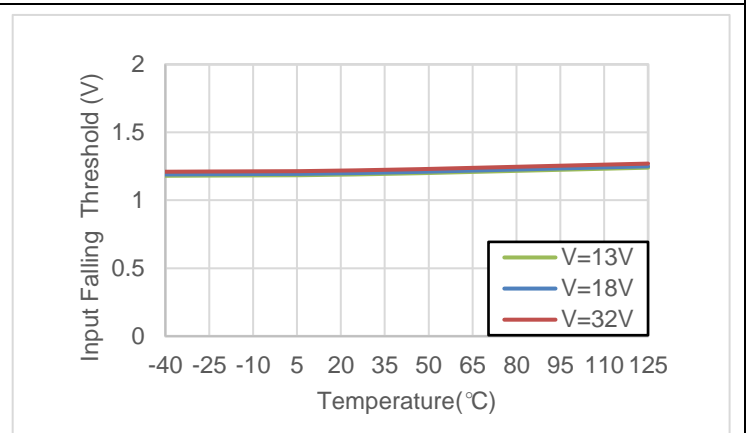


Figure 6.8 Input Falling vs Temperature

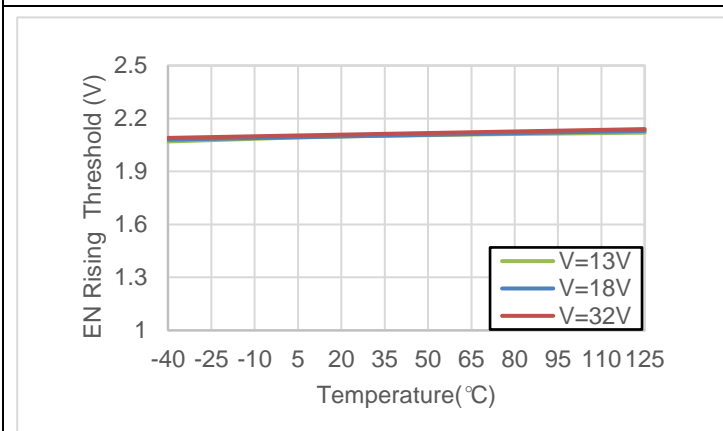


Figure 6.9 EN Rising vs Temperature

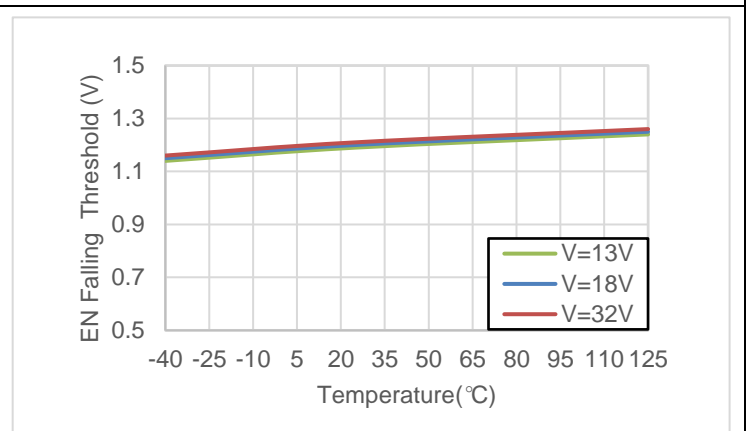


Figure 6.10 EN Falling vs Temperature

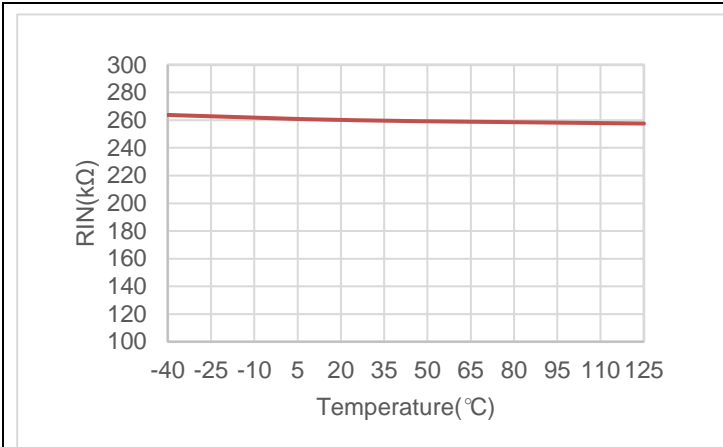


Figure 6.11 RIN vs Temperature

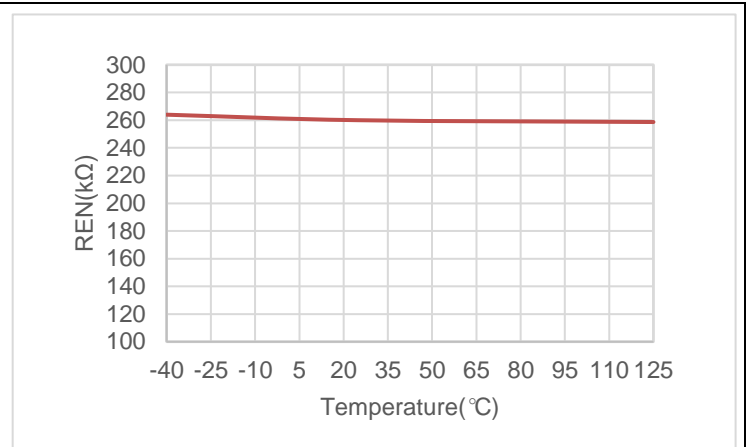


Figure 6.12 REN vs Temperature

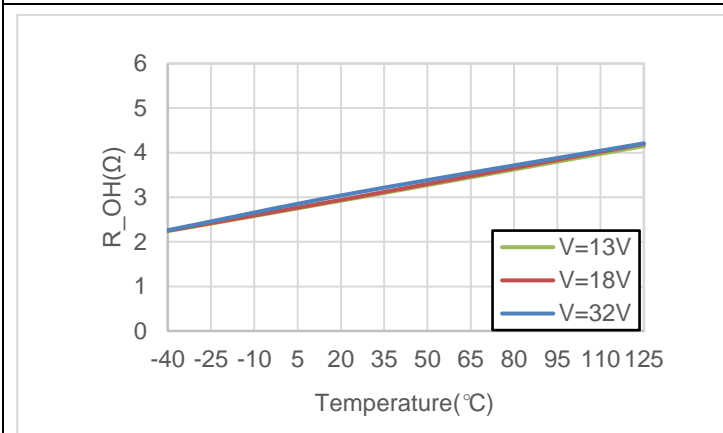


Figure 6.13 R_OH vs Temperature

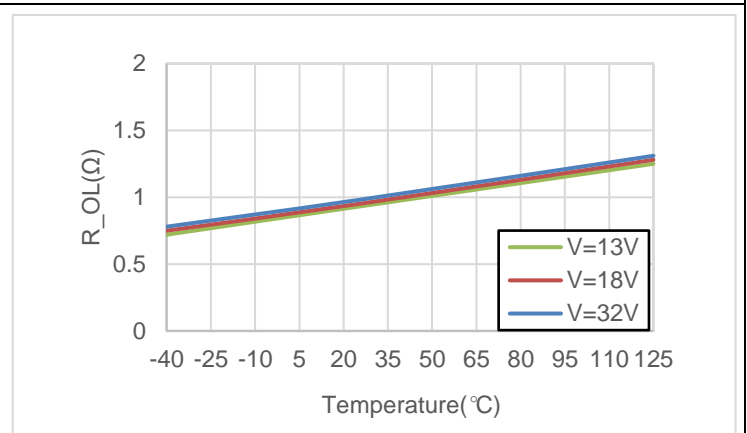


Figure 6.14 R_OL vs Temperature

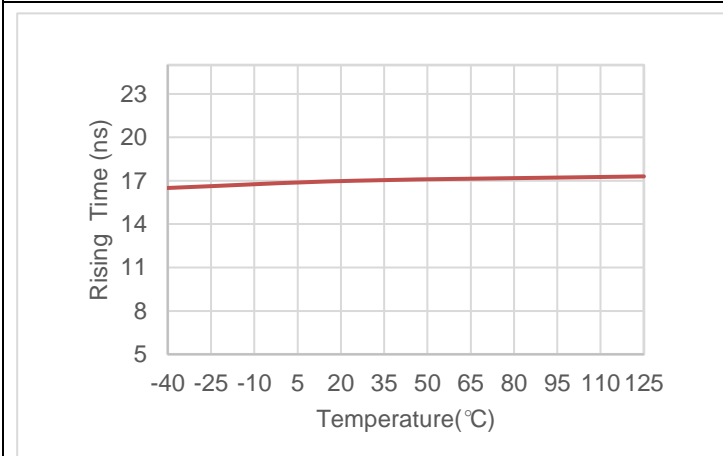


Figure 6.15 OUTPUT Rising vs Temperature

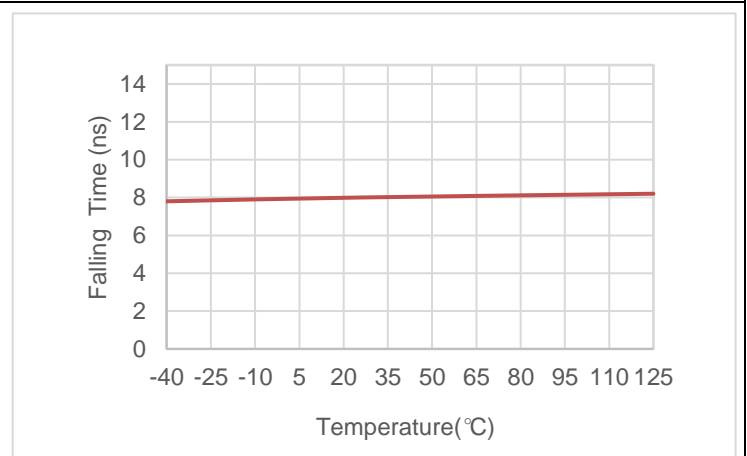


Figure 6.16 OUTPUT Falling vs Temperature

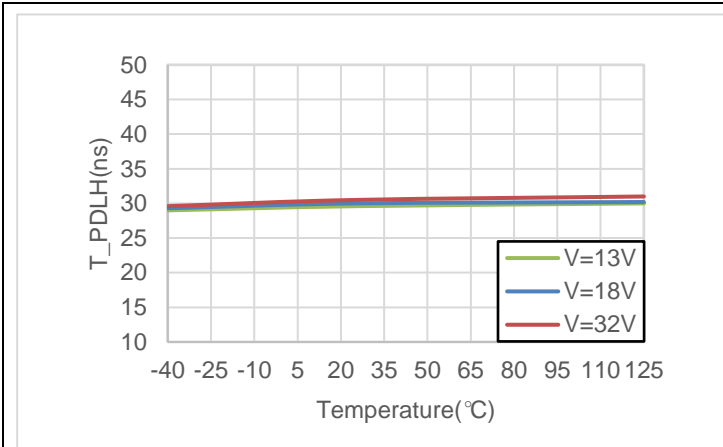


Figure 6.17 T_PDLH vs Temperature

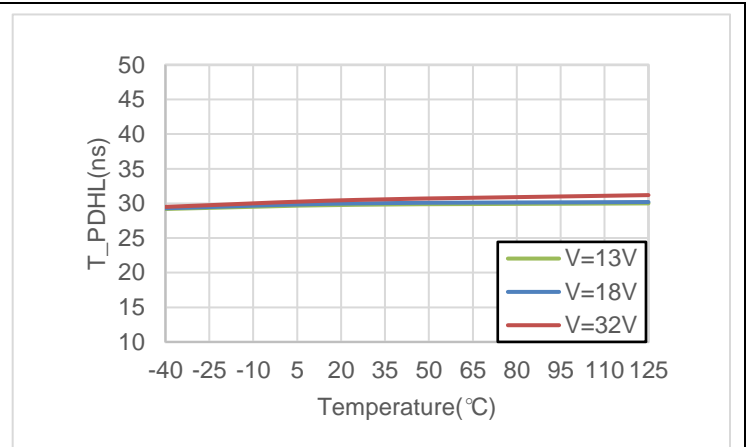


Figure 6.18 T_PDHL vs Temperature

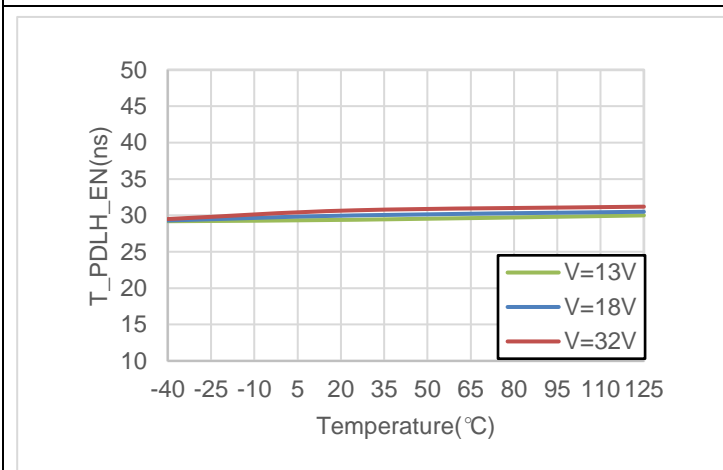


Figure 6.19 T_PDLH_EN vs Temperature

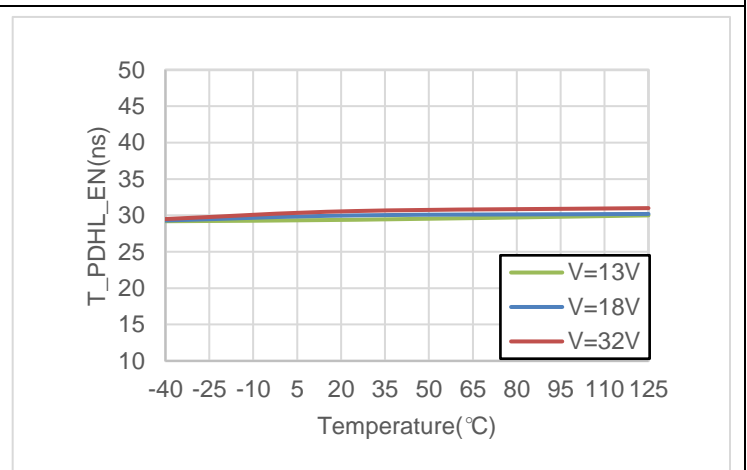


Figure 6.20 T_PDHL_EN vs Temperature

7. Function Description

7.1. Overview

NSD10151 is a single-channel, high-speed, gate driver capable of effectively driving MOSFET and IGBT power switches by up to 2A source and 4A sink (asymmetrical drive) peak current. Strong sink capability in asymmetrical drive boosts immunity against parasitic Miller turn-on effect. The NSD10151 device can also feature a split-output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement allows the user to apply independent turn on and turn-off resistors to the OUTH and OUTL pins, respectively, and easily control the switching slew rates. The driver has rail-to-rail drive capability and extremely small propagation delay, typically 30ns.

The input pins of NSD10151 device are based on a TTL and CMOS compatible input threshold logic. With typical high threshold = 2.1V and typical low threshold = 1.2V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V or 5V logic. Wider hysteresis (typically 0.9V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance, typically 20pF, on these pins reduces loading and increases switching speed. The device features an important safety function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using pull-down resistors on the input pins as shown in the block diagrams.

7.2. Enable Function

The Enable (EN) pin of the NSD10151 has an internal pull-up resistor to an internal reference voltage so leaving Enable floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver.

7.3. Input Stage

The input pin threshold voltage level of the NSD10151 is influenced by the bias voltage applied to the VDD pin. When the VDD supply voltage is greater than the threshold and less than 7V, the threshold voltage of VIN is linearly related to the VDD voltage. when the VDD supply voltage is greater than 7V and less than or equal to the recommended maximum value, the threshold voltage of VIN remains constant and is not affected by the VDD voltage. The reason for the threshold being affected is the internal use of a Schmitt trigger. In addition, the input threshold of the chip has a relatively wide hysteresis, which enables the chip to have good noise immunity.

7.4. Output Stage

The NSD10151 device can also feature a split-output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement allows the user to apply independent turn on and turn-off resistors to the OUTH and OUTL pins, respectively, and easily control the switching slew rates.

8. Application Note

8.1. Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3V or 5V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P-N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The NSD10151 is very flexible in this role with a strong current drive capability and wide supply voltage range up to 32V. This allows the driver to be used in 13V Si MOSFET applications, 20V and -5V (relative to Source) SiC FET applications, 15V and -15V (relative to Emitter) IGBT applications and many others. As a single channel driver, the NSD10151 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. Further, having the ability to control turn-on and turn-off speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for propagation delays and availability in compact, low inductance packages with good thermal capability makes gate driver devices such as the NSD10151 extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

8.2. Typical Application Circuit

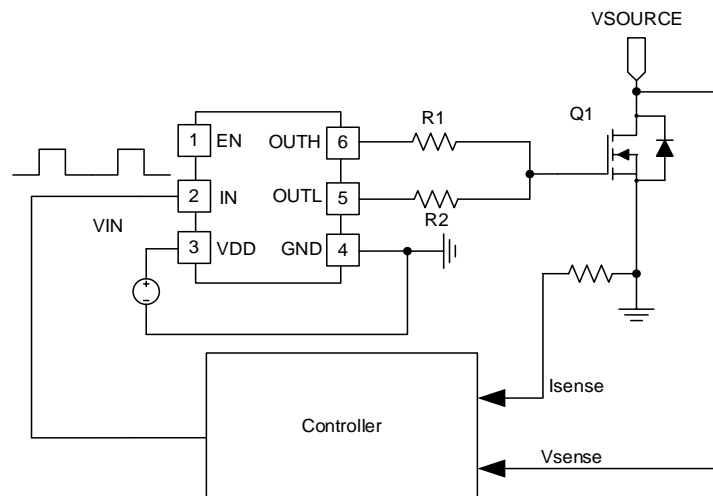
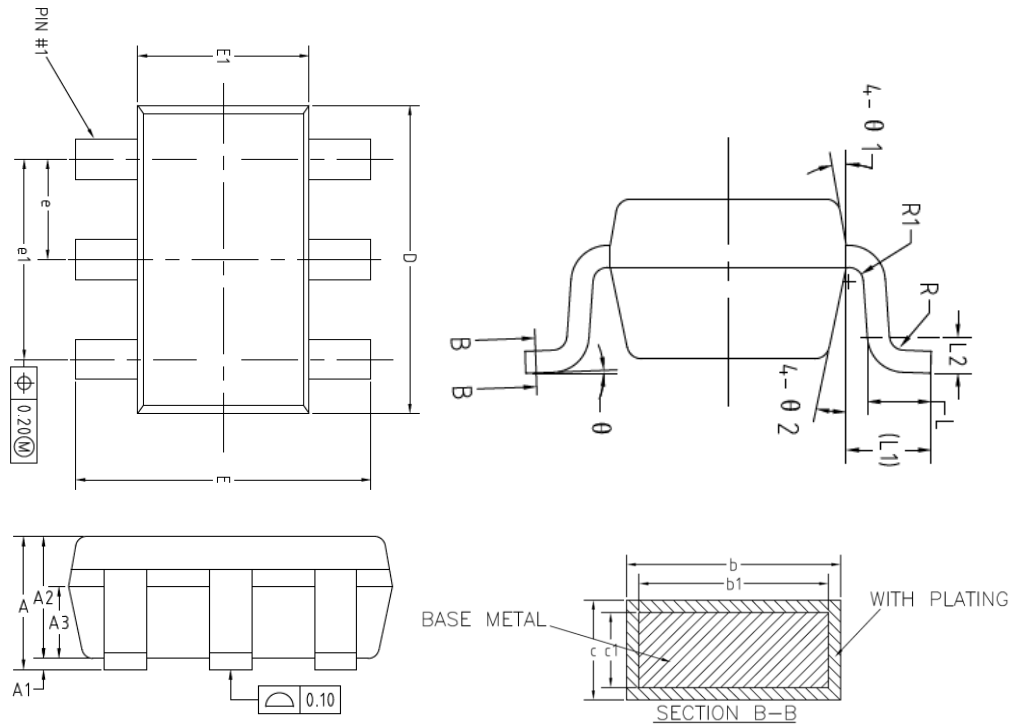


Figure 8.1 Typical application circuit

9. Package Information



SYMBOL	MIN	NOM	MAX
A	—	—	1.25
A1	0	—	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
Δ b	0.34	—	0.45
Δ b1	0.34	0.38	0.41
Δ c	0.12	—	0.20
Δ c1	0.12	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
Δ E1	1.526	1.626	1.700
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.40	0.60
L1		0.59REF	
L2		0.25BSC	
R	0.05	—	0.20
R1	0.05	—	0.20
θ	0°	—	8°
θ 1	8°	10°	12°
θ 2	10°	12°	14°

Figure 9.1 SOT23-6 Package Shape and Dimension in millimeters and (inches)

10. Tape and Reel Information

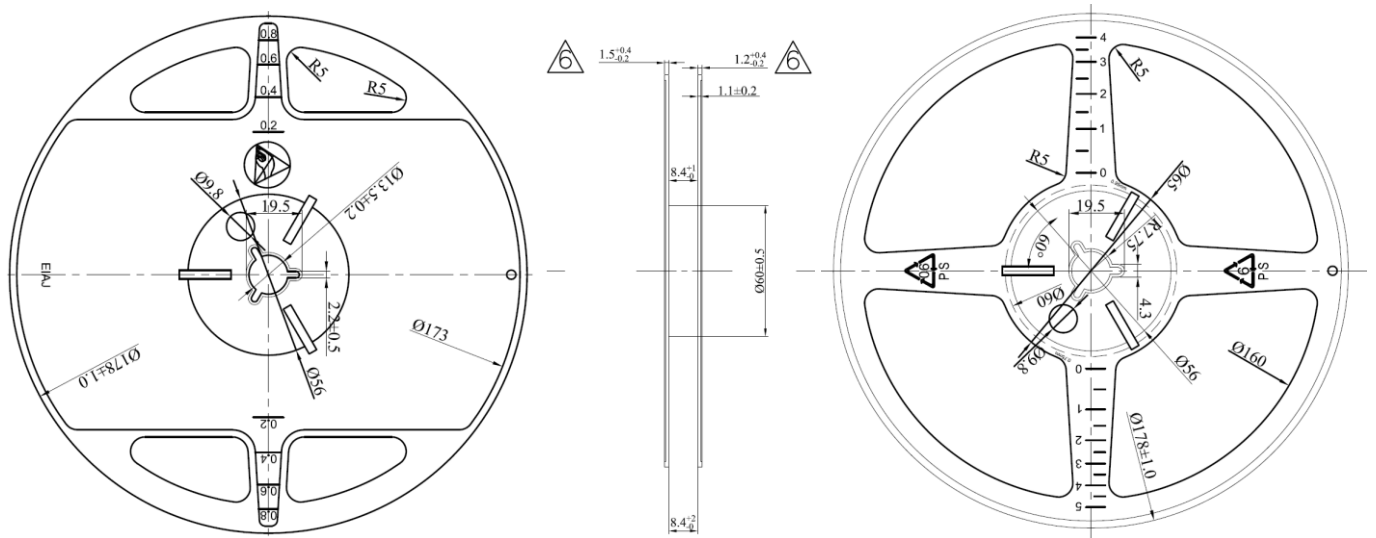


Figure 10.1 Reel Information

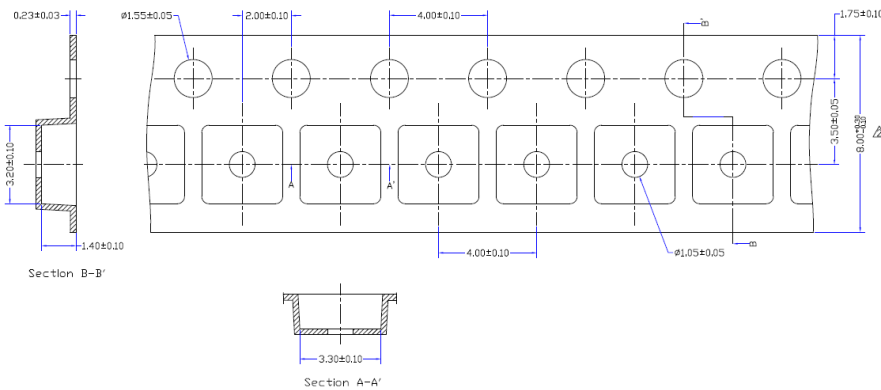


Figure 10.2 Tape Information

NOTES:

1. MATERIAL: CONDUCTIVE PS
2. ALL DIMS IN MM
3. There must not be foreign body adhesion and the state of the surface must be excellent
4. A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.2 up to 10 pitches
5. Ø560 PAPER-Reel,255000pockets(1020m)
6. Surface resistance 1×10E5~1×10E9 OHMS/SQ

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

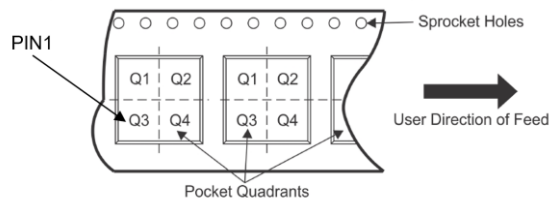


Figure 10.3 Quadrant Designation for Pin1 Orientation in Tape

11. Ordering Information

<i>Part No.</i>	<i>Temperature</i>	<i>Qualification</i>	<i>Package Type</i>	<i>MSL</i>	<i>SPQ</i>
NSD10151-Q1STCR	-40 to 125°C	Auto-motive	SOT23-6	3	3000

12. Revision History

Revision	Description	Date
1.0	Initial Version.	2025/05/06

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