NOVOSENSE

NSAD124x
Low-Power, Low-Noise, 24-Bit,4 k-SPS, Delta-Sigma ADC with PGA and Reference

Datasheet 1.0

Product Overview

The NSAD1249/NSAD1248/NSAD1247/NSAD1246 are low power, low noise, 24-bit, delta-sigma(Δ-Σ), analog-to-digital converters (ADCs). The device contains a capacitive programmable gain amplifier (capacitive PGA), with gains of 1, 2, 4, 8, 16, 32, 64 and 128, which allows to achieve rail-to-rail common-mode input range for all gains. These ADCs feature configurable digital filters with low-latency conversion and can achieve 50 Hz and 60 Hz simultaneous rejections.

The NSAD124x family have high level of integration. The device integrates a high accuracy, low-drift, 2.048-V bandgap reference, two independent programmable excitation current sources (IDACs) which allow for RTD excitation. supports up to 12 inputs that can be connected to PGA in any combination for design flexibility. In addition, these devices include features such as sensor burn-out detection, biasing voltage for thermocouple, reference monitor, PGA rail detection circuits, internal temperature sensor and up to 8 general-purpose I/Os.

The devices are offered in TSSOP28, TSSOP20 or TSSOP16 packages.

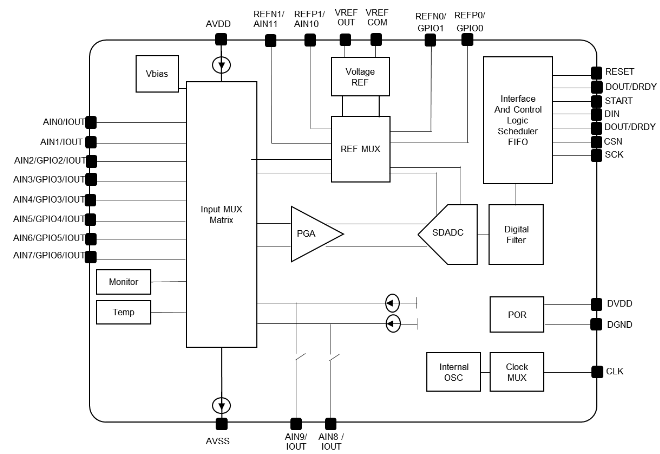
Key Features

- Integrated capacitive PGA with programmable gain (1 to 128), achieves rail-to-rail input range for all gains
- SINC3 and low-latency (single cycle settling) filter options
- Simultaneous 50Hz and 60Hz rejection at data rate 2.5Hz, 5Hz, 10Hz, 20Hz in low-latency filter option
- Two independent internal excitation current source with range 10uA to 2000uA
- Internal 2.048V bandgap reference with ±0.05% initial accuracy and 3 ppm/°C temperature drift
- Internal 4.096MHz oscillator with ±1% Accuracy
- System monitors and fault detection circuits
- Self and system calibration
- Up to 8 general-purpose I/Os
- SPI interface with optional CRC
- Analog Supply: Unipolar (3 V to 5 V) or Bipolar (±1.5 V to±2.5 V)
- Digital Supply: 3 V to 3.6 V

Device Information

Part Number	Package	Body Size
NSAD1249-DTSAR	TSSOP28	9.70 mm × 4.40 mm
NSAD1248-DTSAR	TSSOP28	9.70 mm × 4.40 mm
NSAD1247-DTSR	TSSOP20	6.50 mm × 4.40 mm
NSAD1246-DTSPR	TSSOP16	5.00 mm × 4.40 mm

Functional Block Diagrams



Typical Application

- Temperature measurement (RTD, Thermocouples)
- Pressure measurement
- Factory Automation and Industrial process control
- Instrumentation

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1. Pin Configuration and Functions

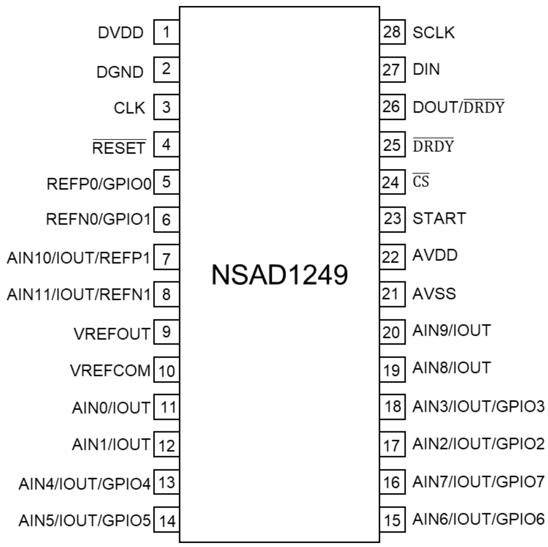

Figure 1-1 NSAD1249 28-Pin TSSOP Top View

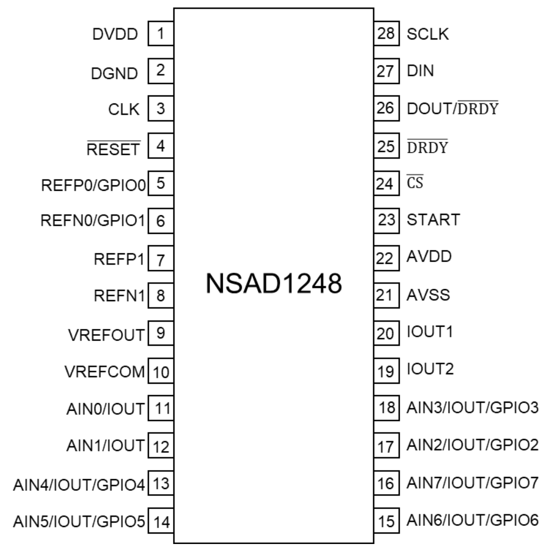

Figure 1-2 NSAD1248 28-Pin TSSOP Top View

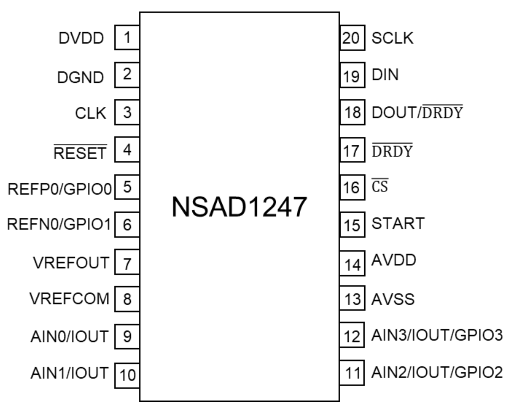

Figure 1-3 NSAD1247 20-Pin TSSOP Top View

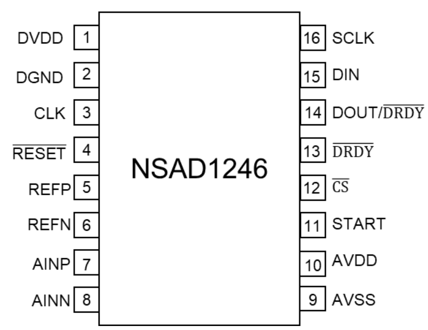

Figure 1-4 NSAD1246 16-Pin TSSOP Top View

Pin Configuration and Functions (Continued)

Symbol	NSAD1249	NSAD1248	NSAD1247	NSAD1246	Type	Description
AIN0/IOUT/VBIAS	11	11	9	—	I/O	Analog input 0 / excitation current output / Bias Voltage
AIN1/IOUT/VBIAS	12	12	10	—	I/O	Analog input 1 / excitation current output / Bias Voltage
AIN2/IOUT/VBIAS/GPIO2	17	17	11	—	I/O	Analog input 2 / excitation current output / Bias Voltage / general-purpose digital input/output pin 2
AIN3/IOUT/VBIAS/GPIO3	18	18	12	—	I/O	Analog input 3 / excitation current output / Bias Voltage / general-purpose digital input/output pin 3
AIN4/IOUT/VBIAS/GPIO4	13	13	—	—	I/O	Analog input 4 / excitation current output / Bias Voltage / general-purpose digital input/output pin 4
AIN5/IOUT/VBIAS/GPIO5	14	14	—	—	I/O	Analog input 5 / excitation current output / Bias Voltage / general-purpose digital input/output pin 5
AIN6/IOUT/VBIAS/GPIO6	15	15	—	—	I/O	Analog input 6/ excitation current output / Bias Voltage / general-purpose digital input/output pin 6
AIN7/IOUT/VBIAS/GPIO7	16	16	—	—	I/O	Analog input 7 /excitation current output / Bias Voltage / general-purpose digital input/output pin 7
AINN	—	—	—	8	I	Negative analog input (NSAD1246 only)
AINP	—	—	—	7	I	Positive analog input (NSAD1246 only)
AVDD	22	22	14	10	P	Positive analog power supply, connect a 0.1-µF capacitor to AVSS.
AVSS	21	21	13	9	P	Negative analog power supply
AVDD	22	22	14	10	P	Positive analog power supply, Relative to AVSS, connect a 0.1-µF capacitor to AVSS.
AVSS	21	21	13	9	P	Negative analog power supply
CLK	3	3	3	3	I	External clock input
$\overline{CS}$	24	24	16	12	I	Chip select, active low
DGND	2	2	2	2	G	Digital ground
DIN	27	27	19	15	I	Serial data input
DOUT/$\overline{DRDY}$	26	26	18	14	O	Serial data output combined with data ready; active low
$\overline{DRDY}$	25	25	17	13	O	Data ready; active low
DVDD	1	1	1	1	P	Digital power supply. Connect a 0.1 uF or larger capacitor to DGND.
AIN9/IOUT	20	20	—	—	I/O	Analog input 9 / excitation current source output (NSAD1249 only)
AIN8/IOUT	19	19	—	—	I/O	Analog input 8 / excitation current source output (NSAD1249 only)

Pin Configuration and Functions (Continued)

Symbol	NSAD1249	NSAD1248	NSAD1247	NSAD1246	Type	Description
REFN	—	—	—	6	I	Negative external reference input (NSAD1246 only)
REFN0/GPIO1	6	6	6	—	I/O	Negative external reference input 0 / general-purpose digital input/output pin 1
REFN1	—	8	—	—	I	Negative external reference input 1 (NSAD1248 only)
REFN1/AIN11	8	—	—	—	I	Negative external reference input 1 / Analog input 11 (NSAD1249 only)
REFP	—	—	—	5	I	Positive external reference input (NSAD1246 only)
REFP0/GPIO0	5	5	5	—	I/O	Positive external reference input 0 / general-purpose digital input/output pin 1
REFP1	—	7	—	—	I	Positive external reference input 1 (NSAD1248 only)
REFP1/AIN10	7	—	—	—	I	Positive external reference input 1 / Analog input 11 (NSAD1249 only)
RESET	4	4	4	4	I	Reset, active low
SCLK	28	28	20	16	I	Serial Clock Input
START	23	23	15	11	I	Conversion start
VREFCOM	10	10	8	—	O	Negative voltage reference output. Connect to AVSS.
VREFOUT	9	9	7	—	O	Positive voltage reference output. Connect a 0.47-μF to 47-μF capacitor to REFCOM

2. Absolute Maximum Ratings [1] [2]

Parameter	Symbol	Mim	Max	Unit
Power-supply voltage	AVDD to AVSS	-0.3	5.5	V
	AVSS to DGND	–2.8	0.3	V
	DVDD to DGND	-0.3	3.9	V
Analog Input voltage	AINx, GPIOx, REFPx, REFNx, REFCOM	AVSS - 0.3	AVDD + 0.3	V
Digital input voltage	CS, SCLK, DIN, DOUT/DRDY, DRDY, START, RESET, CLK	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, any pin except power supply pins	–10	+10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	-60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input and output pins are diode-clamped to the internal power supplies. Limit the input current to 10 mA in the event the analog input voltage exceeds AVDD + 0.3 V or AVSS – 0.3 V, or if the digital input voltage exceeds DVDD + 0.3 V or DGND – 0.3 V.

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Analog power supply	AVDD to AVSS	3	5.25	V
	AVSS to DGND	–2.65	0.1	V
	AVDD to DGND	2.25	5.25	V
Digital power supply	DVDD to DGND	2.7	3.6	V
Differential input voltage	V(AINP)– V(AINN)	–VREF / Gain	VREF / Gain	V
Common-mode input voltage	(V(AINP) + V(AINN)) / 2	AVSS	AVDD	V
Operating free-air temperature	T_A	-40	125	°C
Specified ambient temperature		–40	85	°C

5. Thermal Information

Parameters	Symbol	TSSOP28	TSSOP20	SOP14	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	54.6	87.6	95.2	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(TOP)}$	11.3	21.2	28.8	°C/W
Junction-to-board thermal resistance	θ_{JB}	13	39.9	41.1	°C/W

6. Electrical Characteristics

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096 MHz oscillator (unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Unit
ANALOG INPUTS						
Common-Mode input range		Gain = 1 to 128	AVSS		AVDD	V
Absolute input current		Common-Mode input range		3		nA
Differential input current		V_{CM} = AVDD / 2 –V_{REF} / Gain ≤ V_{IN} ≤ V_{REF} / Gain		±0.1		nA
Differential input impedance				3.5		GΩ
VOLTAGE REFERENCE INPUTS						
External REF_{IN} Voltage		REF_{IN} = $REFP_X$ - $REFN_X$	0.5		AVDD	V
Reference input Range		Reference buffers disabled		AVSS ~ AVDD		V
		Reference buffers enabled		AVSS+0.1 ~ AVDD−0.1		V
Absolute input current		Reference buffers disabled		5.5		μA/V
		Reference buffers enabled		0.1		nA
PGA						
Gain settings				1, 2, 4, 8, 16, 32, 64, 128		V/V
SYSTEM PERFORMANCE						
Resolution				24		Bits
Output data rate	ODR			2.5, 5, 10, 16.6, 20, 50, 60, 100, 200, 400, 800, 1000, 2000, 4000		SPS
Integral nonlinearity (best fit)	INL	Gain = 1 to 16, V_{CM} = AVDD / 2		±3		ppm/FSR
		Gain = 32 to 128, V_{CM} = AVDD / 2		±10		
Input offset voltage	V_{OS}	Gain = 1 to 8	-120/Gain	±20/Gain	120/Gain	μV
		Gain = 16 to 128	-15	2	15	
		Gain = 1 to 128 After internal offset calibration		On the order of peak-to-peak noise at the set ODR and gain		
		Gain = 1 to 128, Global chop enabled	-2	0.2	2	
Offset drift		T_A = –40°C to +125°C, gain = 1 to 8		0.2 / Gain		uV/°C
		T_A = –40°C to +125°C, gain = 1 to 128, Global chop enabled		0.002		
Gain error	GE	Gain = 1 to 8	-0.02%	±0.006%	0.02%	
		Gain = 16 to 128	-0.05%	±0.01%	0.05%	
Gain drift		T_A = –40°C to +85°C, gain = 1 to 128		1		ppm/°C
		T_A = –40°C to +125°C, gain = 1 to 128		1.5		
Noise (input-referred)				See the Noise Performance section for more information		
Normal-mode rejection ratio	NMRR	f_{IN} = 50 Hz (±1 Hz) ODR = 10 SPS, SINC3 filter		105		dB
		f_{IN} = 50 Hz or 60 Hz (±1 Hz) ODR = 20 SPS, low-latency filter		115		
		f_{IN} = 50 Hz (±1 Hz) ODR = 50 SPS, SINC3 filter		100		

		f_{IN} = 60 Hz (±1 Hz) ODR = 60 SPS, SINC3 filter	100	

Electrical Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096 MHz oscillator (unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Common-mode rejection ratio	CMRR	DC ODR = 2.5 to 10 SPS		130		dB
		f_{CM} = 60 Hz (±1 Hz) ODR = 2.5 to 10, 60 SPS, SINC3 filter		135		
		f_{CM} = 50 Hz or 60 Hz (±1 Hz) ODR = 2.5 to 20 SPS, low-latency filter		135		
Power-supply rejection ratio	PSRR	AVDD at DC		105		dB
		DVDD at DC		115		
INTERNAL VOLTAGE REFERENCE						
Output voltage	V_{REF}			2.048		V
Accuracy		T_A = 25°C	-0.2%	±0.02%	0.2%	
Temperature drift		T_A = –40°C to +125°C		3	10	ppm/°C
Short-circuit current limit		Sink and source		+60/-100		mA
Line regulation		AVDD = 3 V to 5.5 V at DC		20		uV/V
Load regulation		-10mA < Load current < 10mA		8	10	ppm/mA
Capacitive load stability		Between REFOUT and REFCOM Pin	1		47	μF
Reference noise		f = 0.1 Hz to 10 Hz, 1-μF capacitor		8		μVPP
Startup time		1μF capacitor, 0.1% settling		2.5		ms
		1μF capacitor, 0.01% settling		4		
EXCITATION CURRENT SOURCES (IDACS)						
Current settings			10, 50, 100, 250, 500, 750, 1000, 1500, 2000			μA
Compliance voltage		10 μA to 750 μA, 0.1% deviation		AVDD-0.3	AVDD-0.4	V
		1 mA to 2 mA, 0.1% deviation		AVDD-0.6	AVDD-0.65	
Accuracy (each IDAC)		10 μA to 100 μA	-3.5%	±1%	3.5%	
		250 μA to 2000 μA	-2%	±0.5%	2%	
Mismatch between IDACs		10 μA, 750μA		0.2%	0.8%	
		50 μA to 500 uA		0.15%	0.65%	
		1 mA to 2 mA		0.07%	0.35%	
Temperature drift each IDAC		10 μA to 100 μA		50		ppm/°C
		250 μA to 2000uA		30		
Temperature drift mismatch between IDACs		10 μA to 100 μA		5		
		250 μA to 2000uA		3		
INTERNAL OSCILLATOR						
Frequency	f_{CLK}			4.096		MHz
Accuracy			0.3%		0.3%	
		T_A = –40°C to +125°C	-1.5%		1.5%	
BIAS VOLTAGE						
Output voltage settings				(AVDD + AVSS) / 2 (AVDD + AVSS) / 12		V
Bias Voltage Accuracy				1%		
Output impedance				400		Ω
Startup time		No Load, 1% settling		100		μs
BURNOUT CURRENT SOURCES (BCS)						

Current settings			0.5, 2, 10	µA
Accuracy			10%	
Startup Time			1	ms

Electrical Characteristics (Continued)

at T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096 MHz oscillator (unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Unit
PGA RAIL DETECTION						
Positive rail threshold		Referred to the output of the PGA		AVDD–0.15		V
Negative rail threshold		Referred to the output of the PGA		AVSS+0.15		
Accuracy				10%		
REFERENCE DETECTION						
Threshold 1				0.3		V
Threshold 1 accuracy				10%		
Threshold 2				(AVDD–AVSS)/3		V
Threshold 2 accuracy				1%		
Pull-together resistance				10M		Ω
SUPPLY VOLTAGE MONITORS						
Accuracy		(AVDD – AVSS) / 4 monitor		±1%		
		(DVDD – AVSS) / 4 monitor		±1%		
TEMPERATURE SENSOR						
PGA fixed gain				8		
T_A = 25°C Output voltage				139.9		mV
Temperature coefficient		T_A = –40°C to +125°C		455		μV/°C
Accuracy		T_A = –40°C to +125°C		±1.5		°C
GENERAL-PURPOSE INPUT/OUTPUTS (GPIOs)						
Logic input level, low			AVSS		0.3AVDD	V
VIH Logic input level, high			0.7AVDD		AVDD	
DIGITAL INPUT/OUTPUTS						
VIL Logic input level, low			DGND		0.3DVDD	V
VIH Logic input level, high			0.7DVDD		DVDD	
POWER SUPPLY						
AVDD current	I_{AVDD}	Conversion Mode, AVDD=3.3 V		490	550	uA
		Conversion Mode, AVDD=5 V		560	600	
		Power-Down Mode		0.15		
ADDITIONAL ANALOG SUPPLY CURRENTS PER FUNCTION (AVDD = 5 V)						
AVDD current	I_{AVDD}	Internal reference		200		uA
		VBIAS buffer, (AVDD + AVSS) / 2		13		
		VBIAS buffer, (AVDD + AVSS) / 12		17		
		Reference buffer, each		45		
		IDAC overhead, 10 μA to 250 μA		35		
		IDAC overhead, 500 μA		40		
		IDAC overhead, 750 μA		45		
		IDAC overhead, 1 mA		50		
		IDAC overhead, 1.5 mA		65		
		IDAC overhead, 2 mA		77		
DIGITAL SUPPLY CURRENT (DVDD = 3.3 V, SPI Not Active)						
DVDD Current	I_{DVDD}	Conversion Mode Internal 4.096-MHz oscillator		230	260	uA
		Conversion Mode External f_{CLK} = 4.096 MHz		210		
		Power-Down Mode		0.15		

7. Timing Characteristics

at T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096 MHz oscillator (unless otherwise noted)

Parameters	Symbol	Min	Typ	Max	Unit
SERIAL INTERFACE					
Delay time, First SCLK rising edge after CS falling edge	t_{CSSC}	10			ns
Delay time, CS rising edge after final SCLK falling edge	t_{SCCS}	7			t_{CLK}
Pulse duration, CS high	t_{CSPW}	5			t_{CLK}
SCLK period	t_{SCLK}	100ns		2^{15} * t_{CLK}	
Pulse duration, SCLK high	t_{SPWH}	25%		75%	t_{SCLK}
Pulse duration, SCLK low	t_{SPWL}	25%		75%	t_{SCLK}
Setup time, DIN valid before SCLK falling edge	t_{DIST}	5			ns
Hold time, DIN valid after SCLK falling edge	t_{DIHD}	5			ns
Setup time, SCLK low before DRDY rising edge	t_{STD}	5			t_{CLK}
Delay time, SCLK rising edge after DRDY falling edge	t_{DTS}	1			t_{CLK}
MINIMUM START TIME PULSE					
Pulse duration, START high	t_{START}		4		t_{CLK}
RESET PULSE DURATION, SERIAL INTERFACE COMMUNICATION AFTER RESET					
Pulse duration, RESET low	t_{RESET}		4		t_{CLK}

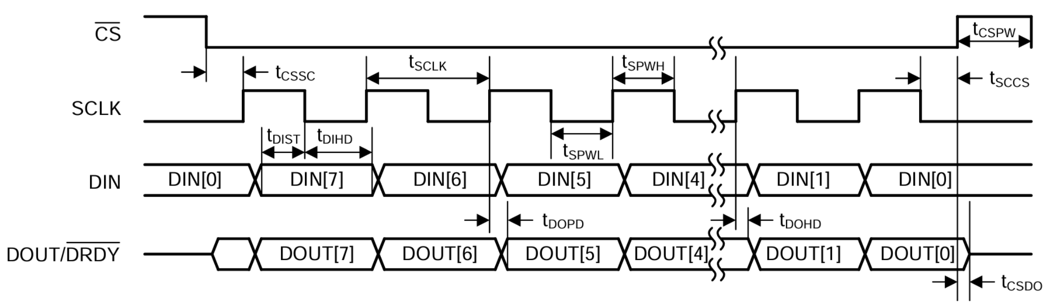

Figure 7-1 Serial Interface Switching Characteristics

8. Typical Performance Characteristics

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

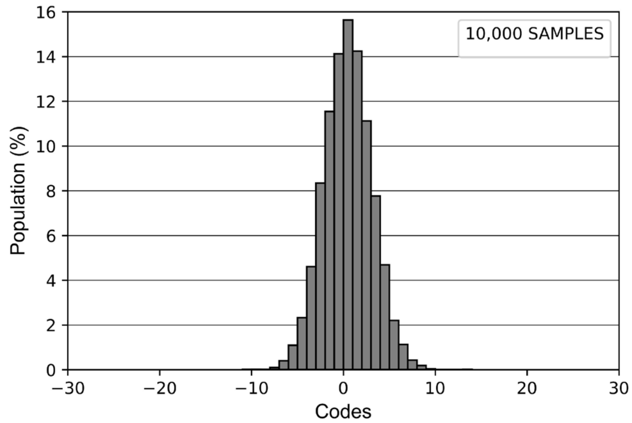

Figure 8-1 Noise Histogram, SINC3 Filter, ODR = 20 SPS,
Gain = 1, Global chop Disable

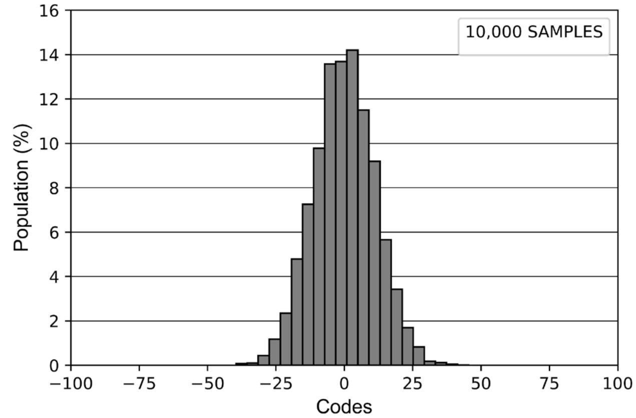

Figure 8-2 Noise Histogram, SINC3 Filter, ODR = 20 SPS,
Gain = 64, Global chop Disable

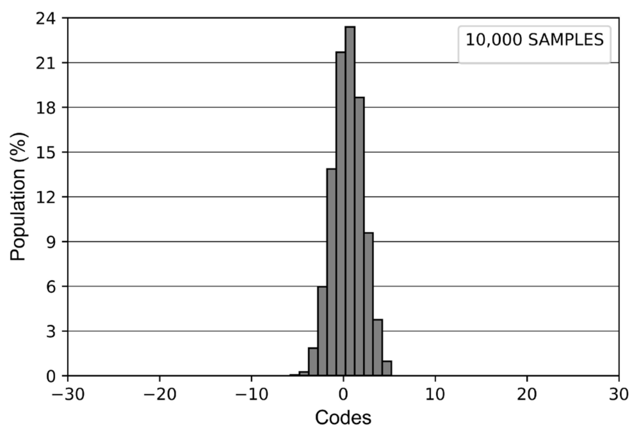

Figure 8-3 Noise Histogram, SINC3 Filter, ODR = 20 SPS,
Gain = 1, Global chop Enable

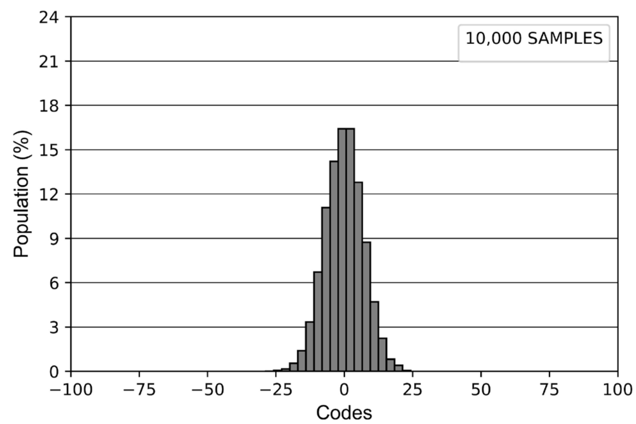

Figure 8-4 Noise Histogram, SINC3 Filter, ODR = 20 SPS,
Gain = 64, Global chop Enable

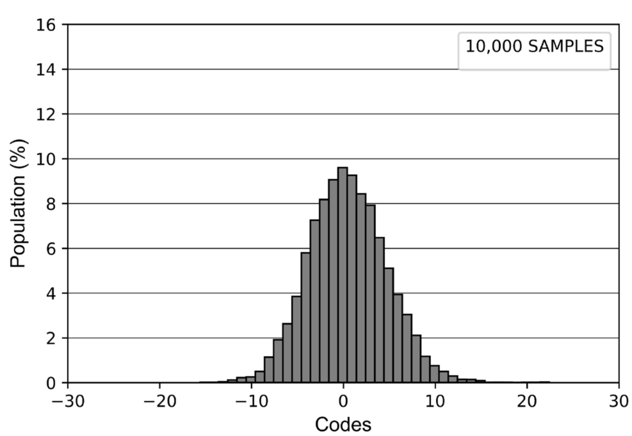

Figure 8-5 Noise Histogram Low-Latency Filter, ODR = 20 SPS, Gain = 1, Global chop Disable

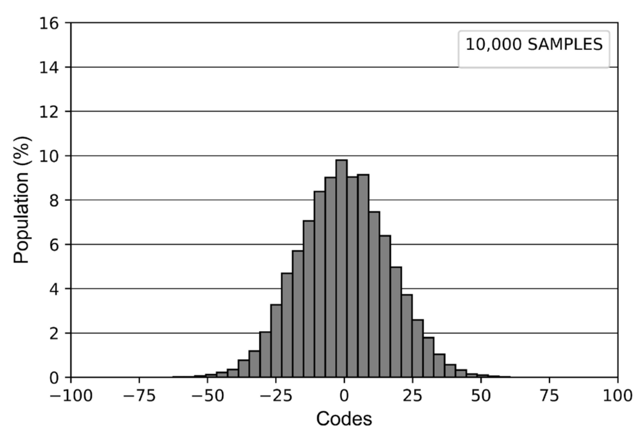

Figure 8-6 Noise Histogram Low-Latency Filter, ODR = 20 SPS, Gain = 64, Global chop Disable

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

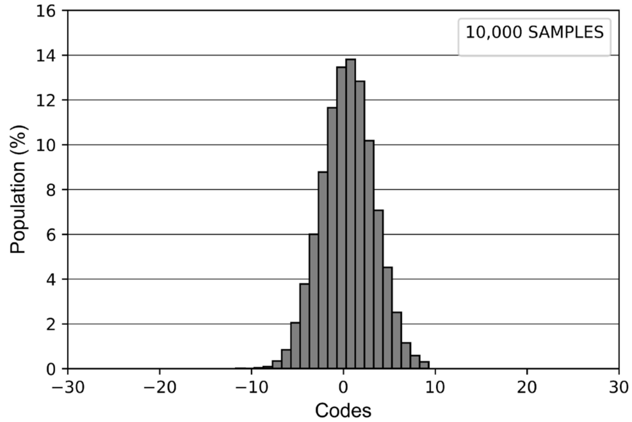

Figure 8-7 Noise Histogram, Low-Latency Filter, ODR = 20 SPS, Gain = 1, Global chop Enable

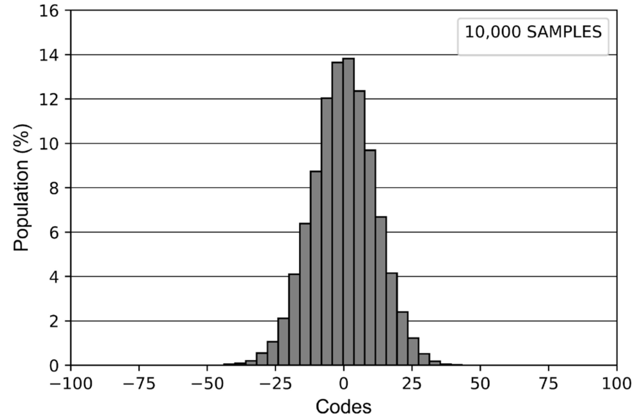

Figure 8-8 Noise Histogram, Low-Latency Filter, ODR = 20 SPS, Gain = 64, Global chop Enable

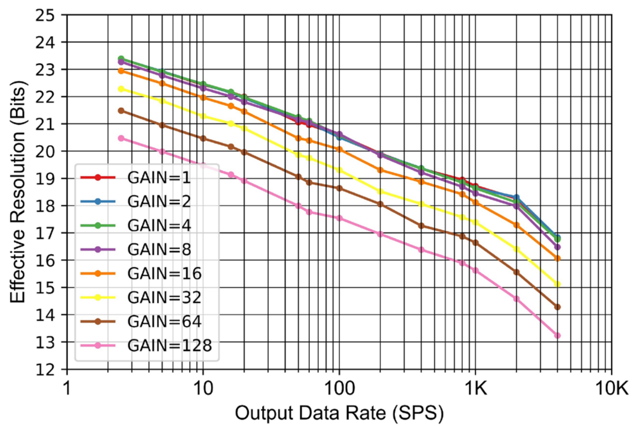

Figure 8-9 Effective Resolution vs. Output Data Rate Low-Latency Filter, Global chop Disable

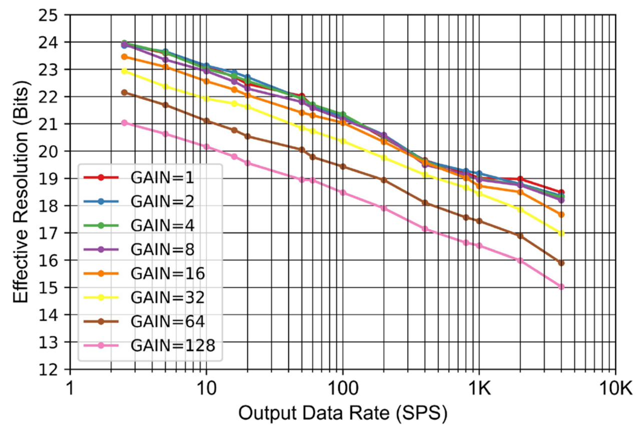

Figure 8-10 Effective Resolution vs. Output Data Rate SINC3 Filter, Global chop Disable

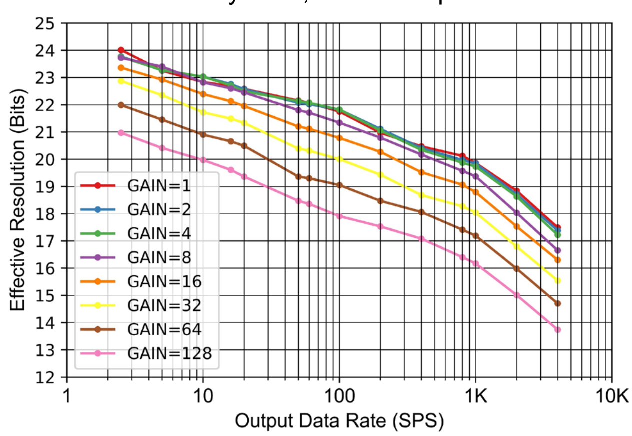

Figure 8-11 Effective Resolution vs. Output Data Rate Low-Latency Filter, Global chop Enable

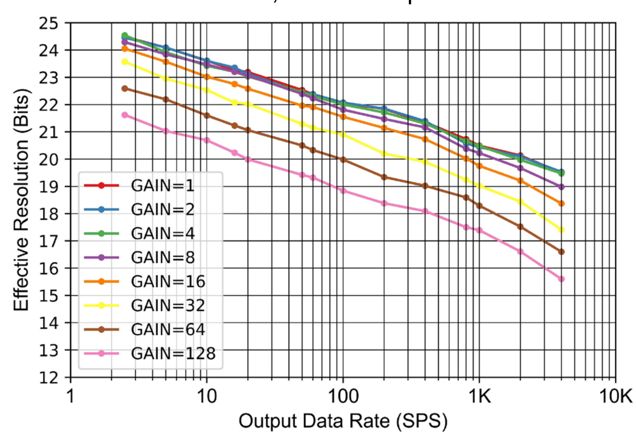

Figure 8-12 Effective Resolution vs. Output Data Rate SINC3 Filter, Global chop Enable

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

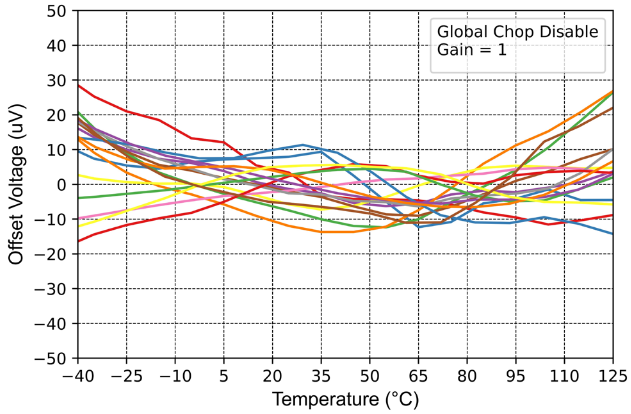

Figure 8-13 Input Referred Offset Error vs. Temperature Global Chop Disable, Gain = 1

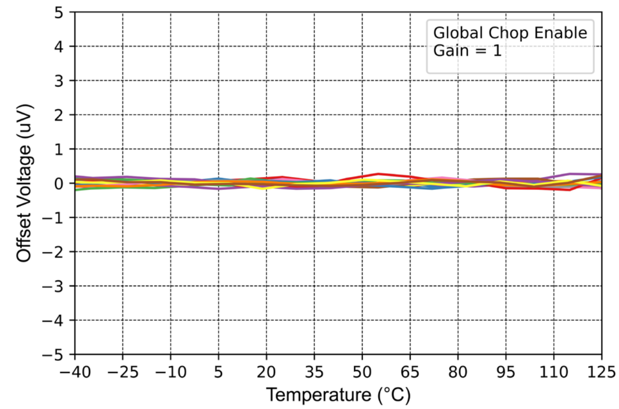

Figure 8-14 Input Referred Gain Error vs. Temperature Global Chop Enable, Gain = 1

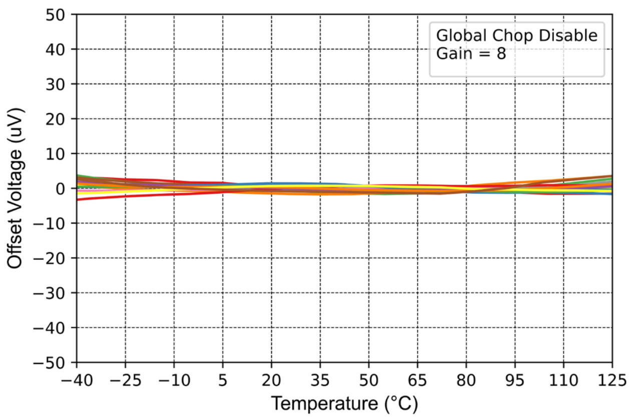

Figure 8-15 Input Referred Offset Error vs. Temperature Global Chop Disable, Gain = 8

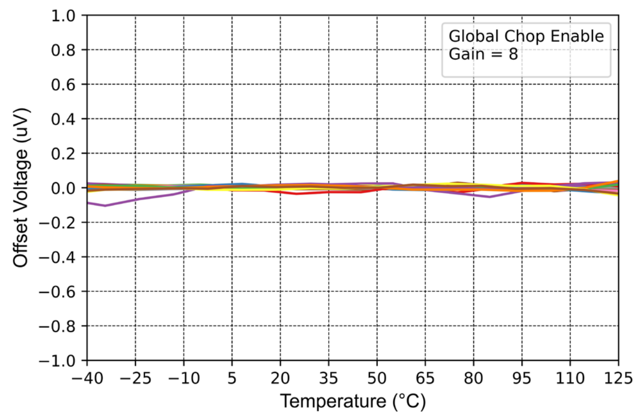

Figure 8-16 Input Referred Offset Error vs. Temperature Global Chop Enable, Gain = 8

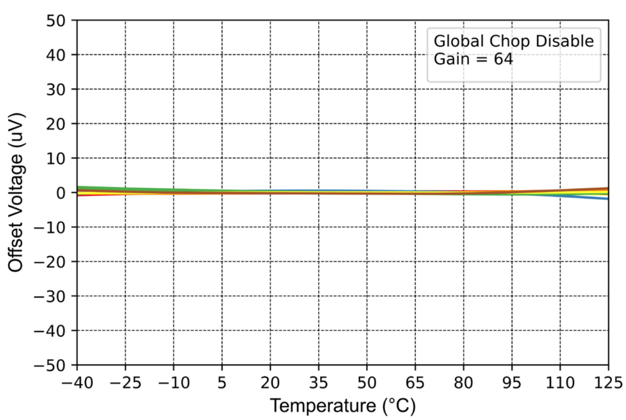

Figure 8-17 Input Referred Offset Error vs. Temperature Global Chop Disable, Gain = 64

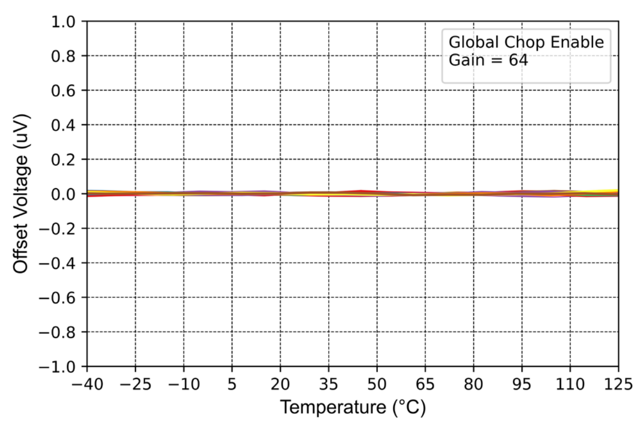

Figure 8-18 Input Referred Offset Error vs. Temperature Global Chop Enable, Gain = 64

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

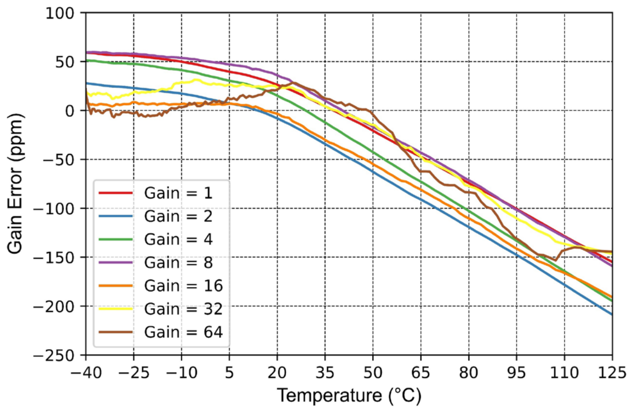

Figure 8-19 Input Referred Gain Error vs. Temperature

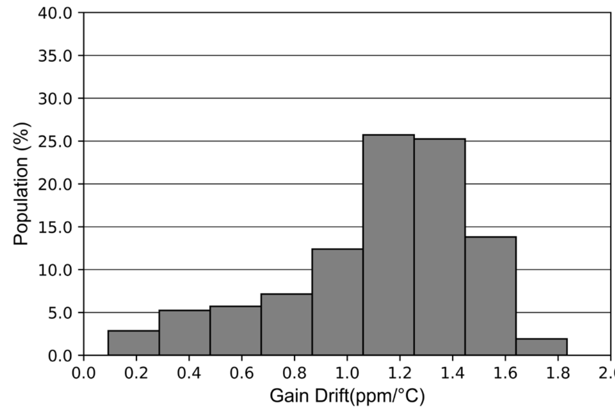

Figure 8-20 Gain Drift Distribution, T_A = –40°C to +125°C

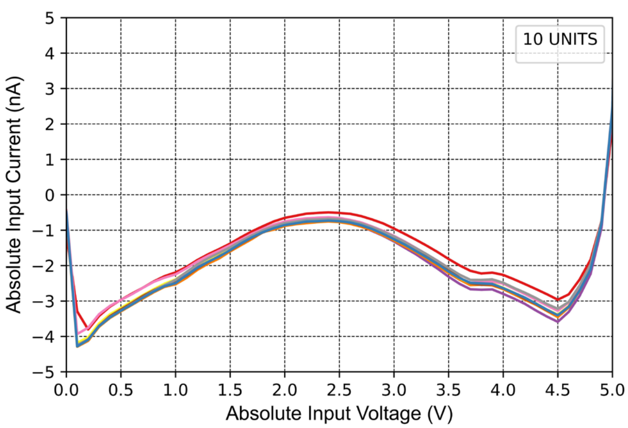

Figure 8-21 Input Bias Current vs. Absolute Input Voltage

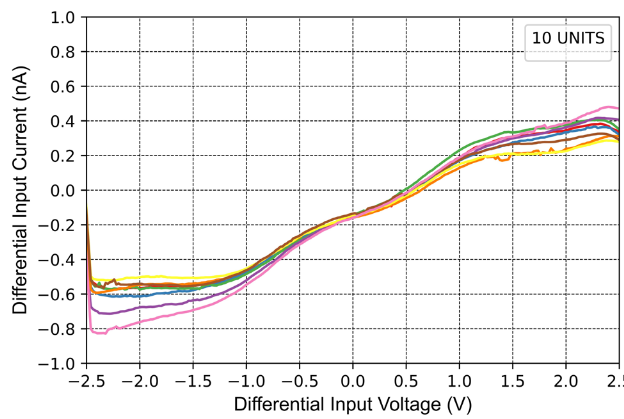

Figure 8-22 Input Offset Current vs. Differential Input Voltage

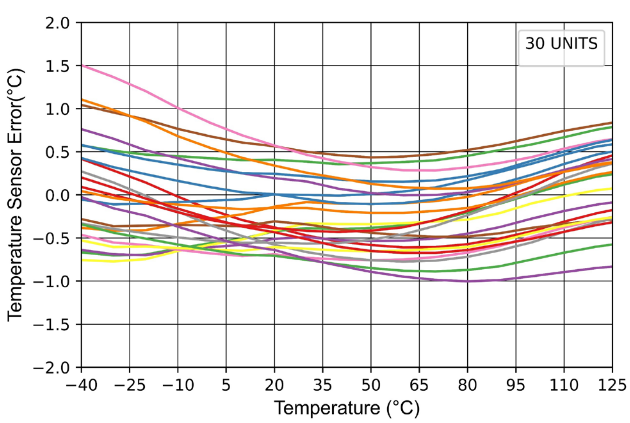

Figure 8-23 Temp Sensor Error vs. Temperature

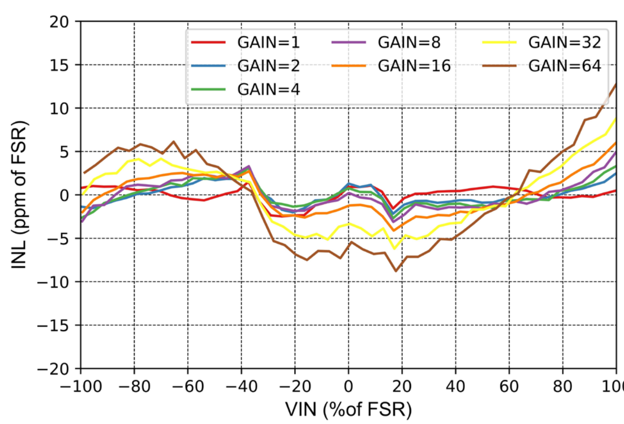

Figure 8-24 INL vs. Differential Input Signal, 2.5 V Reference

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

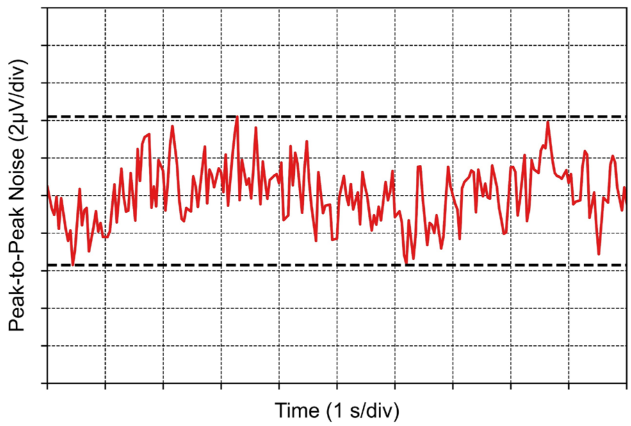

Figure 8-25 Internal Reference 0.1Hz to 10Hz Noise

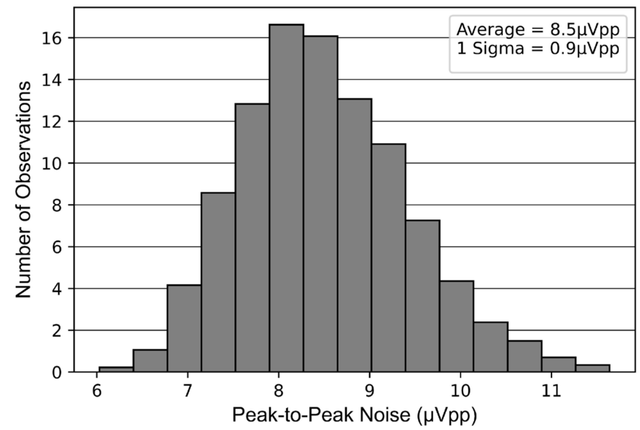

Figure 8-26 Internal Reference 0.1Hz to 10Hz Noise Histogram

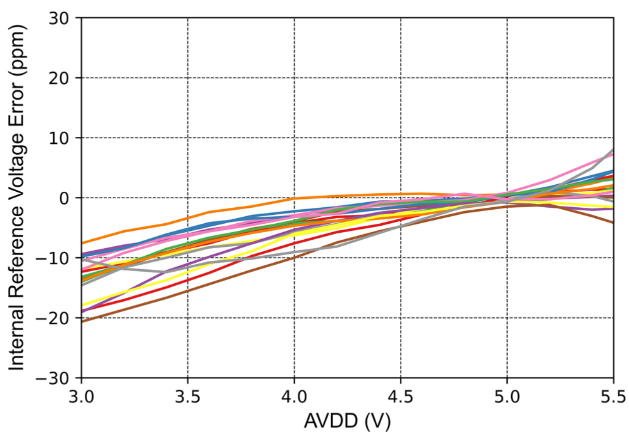

Figure 8-27 Internal Reference Voltage Error vs. AVDD

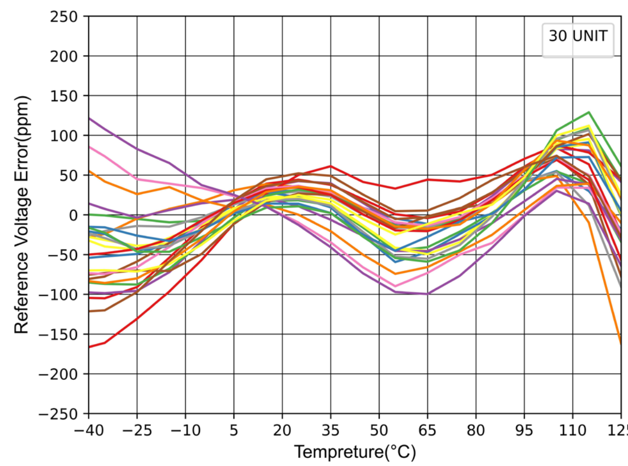

Figure 8-28 Internal Reference Voltage Error vs. Temperature

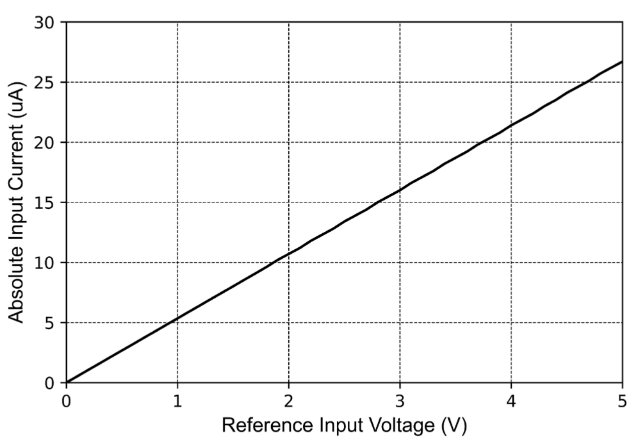

Figure 8-29 Reference Input Current vs. Input Voltage Reference buffers disabled

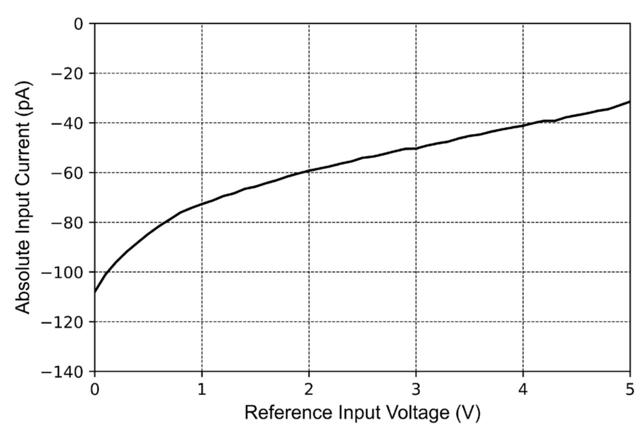

Figure 8-30 Reference Input Current vs. Input Voltage Reference buffers enabled

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

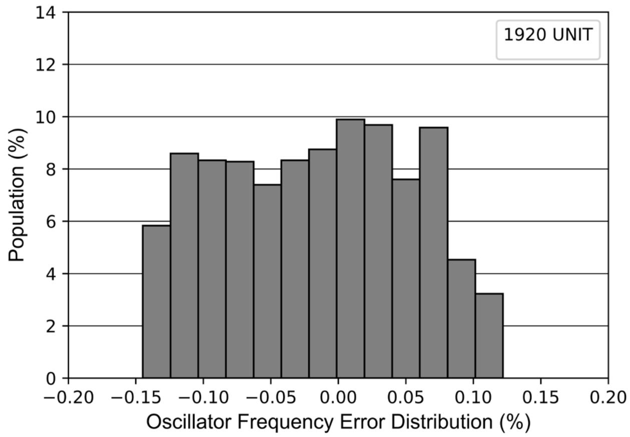

Figure 8-31 Internal Oscillator Frequency Histogram

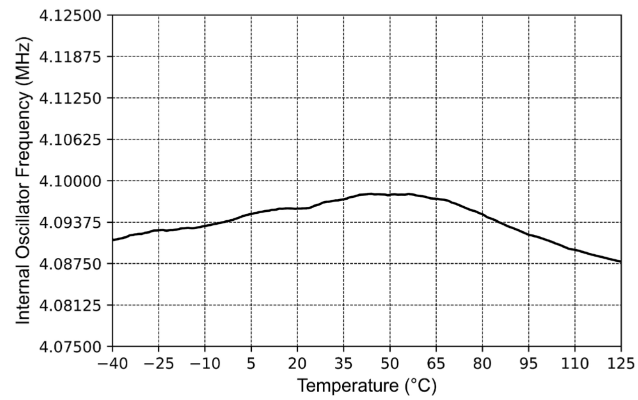

Figure 8-32 Internal Oscillator Frequency vs. Temperature

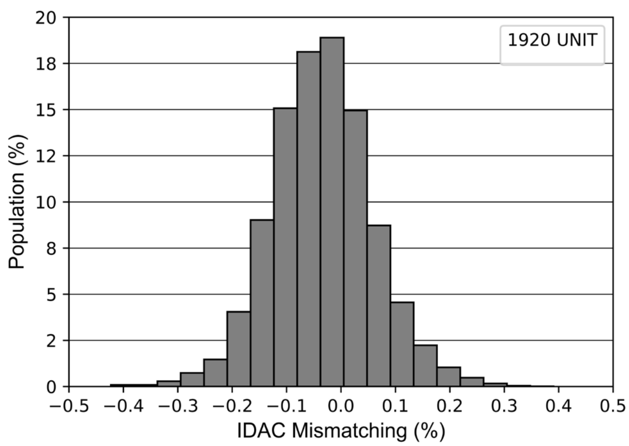

Figure 8-33 IDAC Current Mismatching Histogram

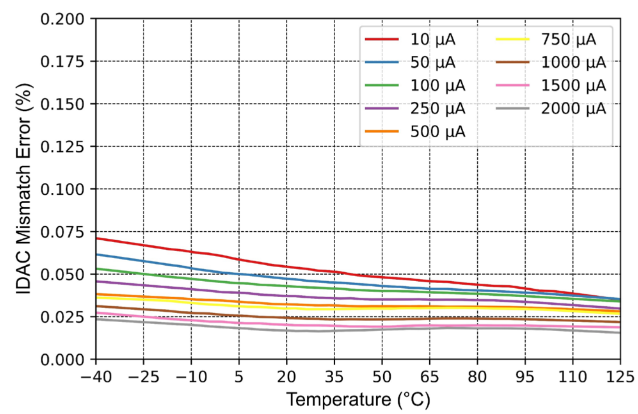

Figure 8-34 IDAC Mismatching vs. Temperature

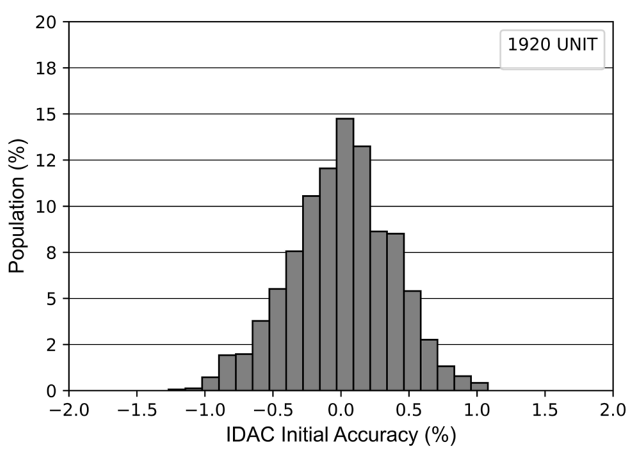

Figure 8-35 IDAC Current Initial Accuracy Histogram

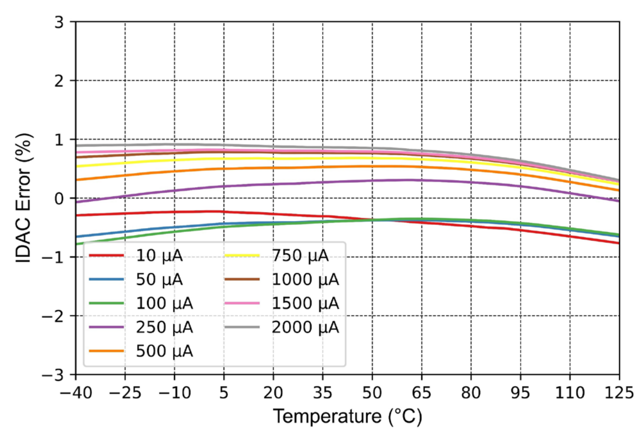

Figure 8-36 IDAC Current Accuracy vs. Temperature

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

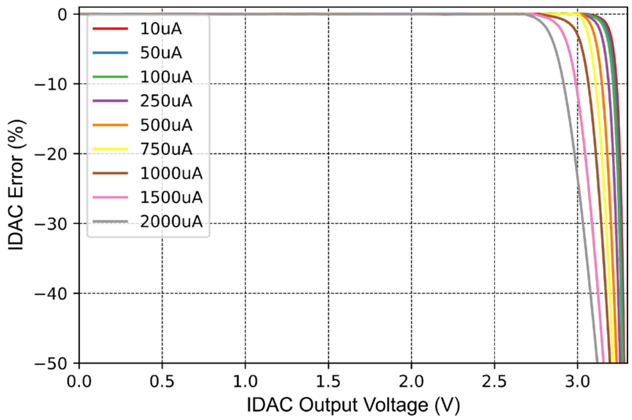

Figure 8-37 IDAC Output Compliance (AVDD = 3.3 V)

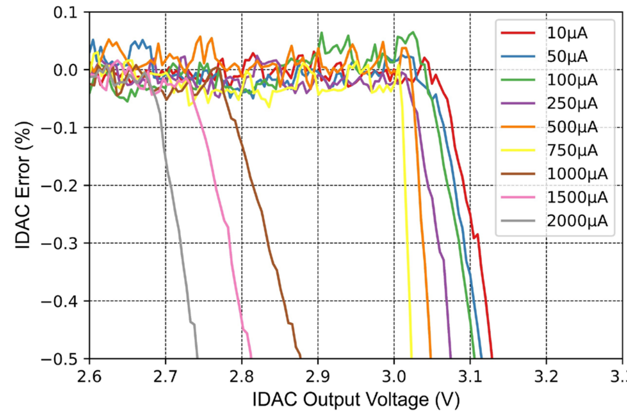

Figure 8-38 IDAC Output Compliance (AVDD = 3.3 V)

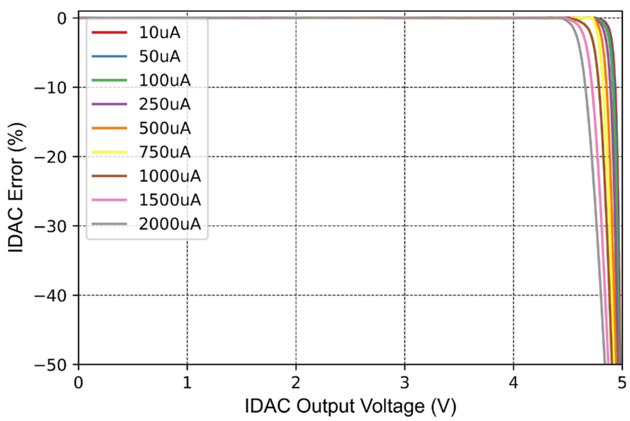

Figure 8-39 IDAC Output Compliance (AVDD = 5 V)

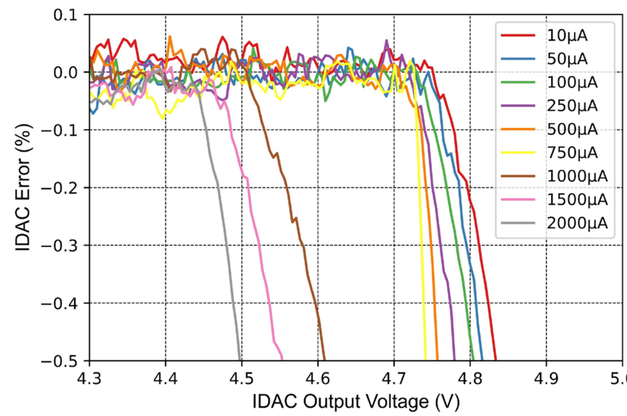

Figure 8-40 IDAC Output Compliance (AVDD = 5 V)

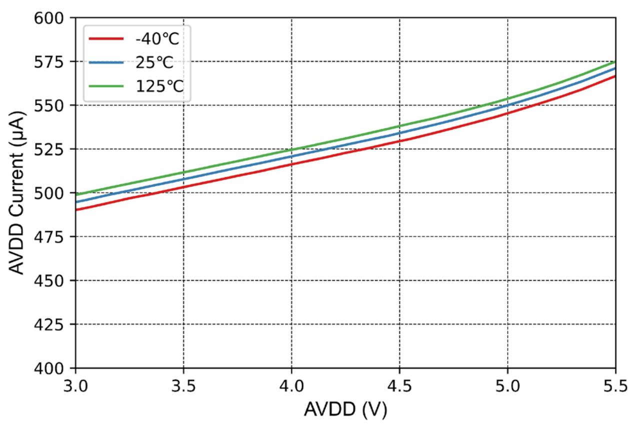

Figure 8-41 Analog Supply Current vs AVDD Conversion-mode, External V_{REF}

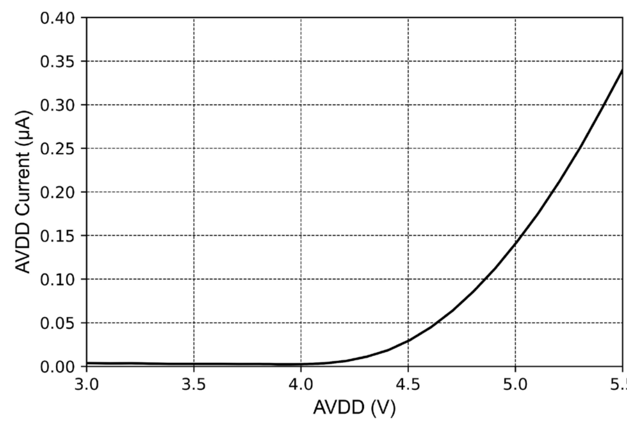

Figure 8-42 Analog Supply Current vs AVDD Power-down mode

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

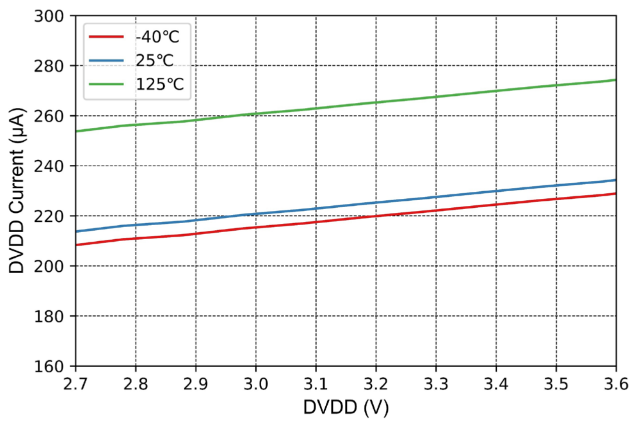

Figure 8-43 Digital Supply Current vs DVDD Conversion mode, Internal Oscillator

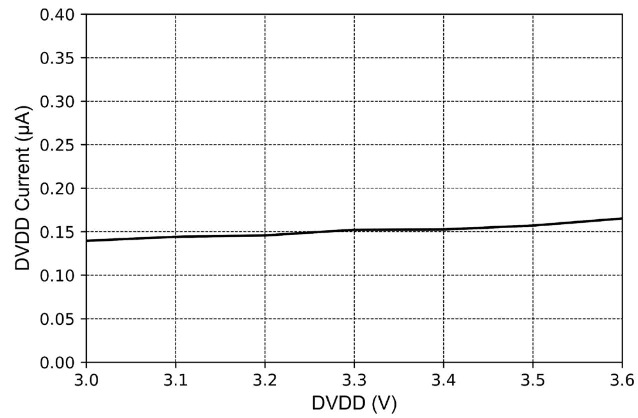

Figure 8-44 Digital Supply Current vs. DVDD Power-down mode

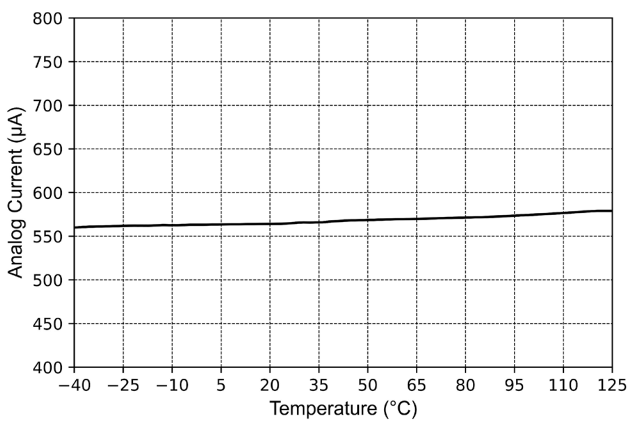

Figure 8-45 Analog Supply Current vs. Temperature

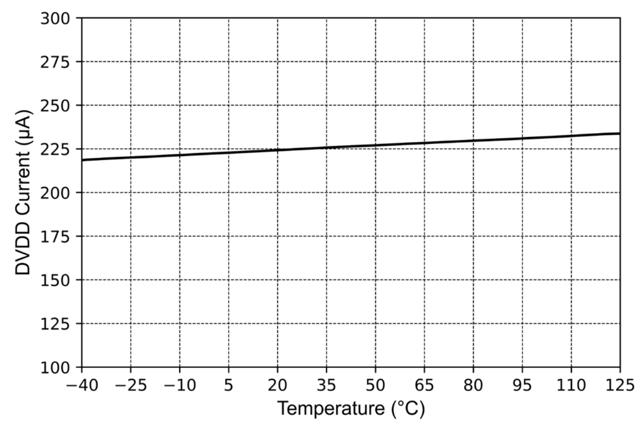

Figure 8-46 Digital Supply Current vs. Temperature

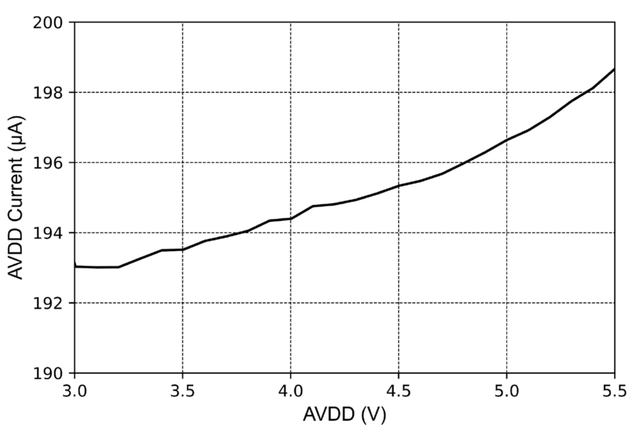

Figure 8-47 Internal Reference AVDD Current vs. AVDD

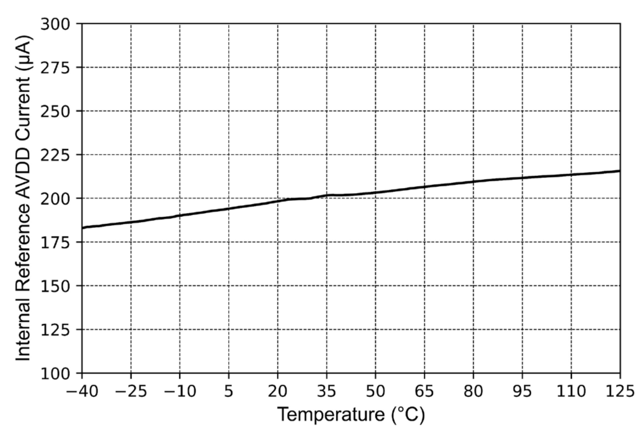

Figure 8-48 Internal Reference AVDD Current vs. Temperature

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

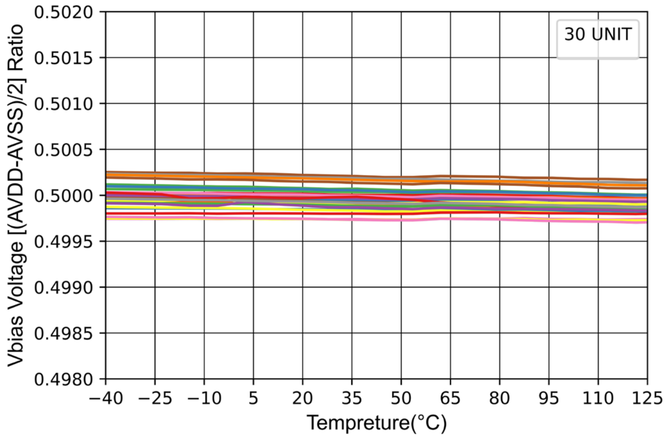

Figure 8-49 VBIAS Voltage (AVDD–AVSS)/2 vs Temperature

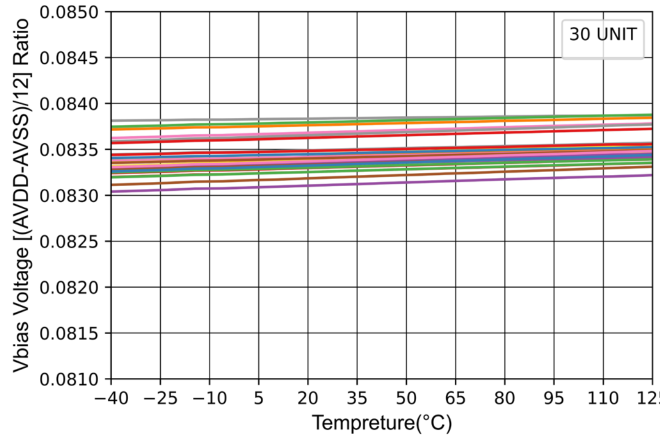

Figure 8-50 VBIAS Voltage (AVDD–AVSS)/12 vs Temperature

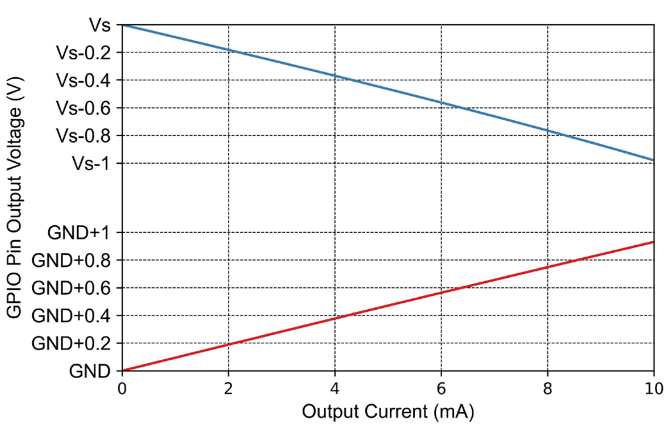

Figure 8-51 GPIO Pin Output Voltage vs Sourcing Current

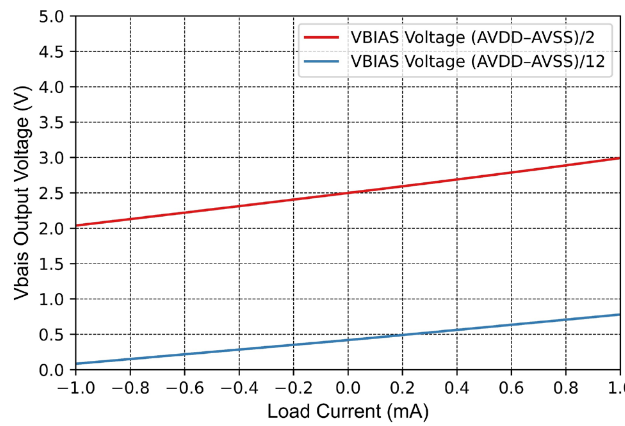

Figure 8-52 VBIAS Voltage vs Load Current

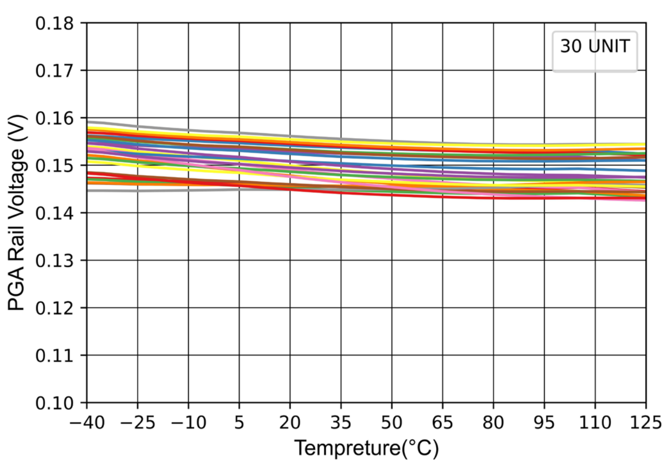

Figure 8-53 PGA Rail Detection, PGAN_RAILP, PGAP_RAILP Threshold From AVDD

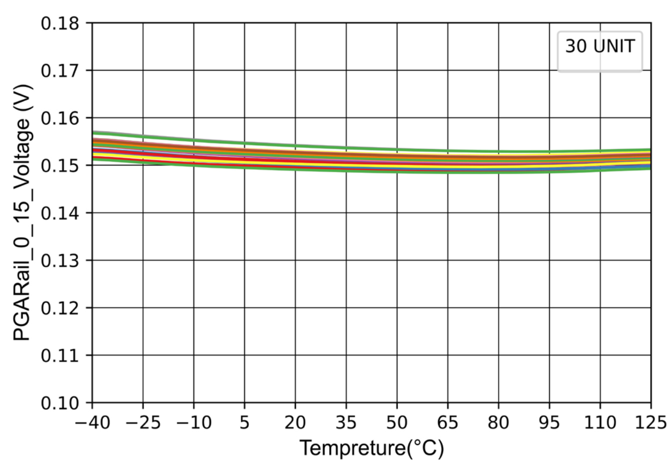

Figure 8-54 PGA Rail Detection, PGAN_RAILN, PGAP_RAILN Threshold From AVSS

Typical Performance Characteristics (Continued)

At T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, external V_{REF} = 2.5 V, and internal 4.096-MHz oscillator (unless otherwise noted)

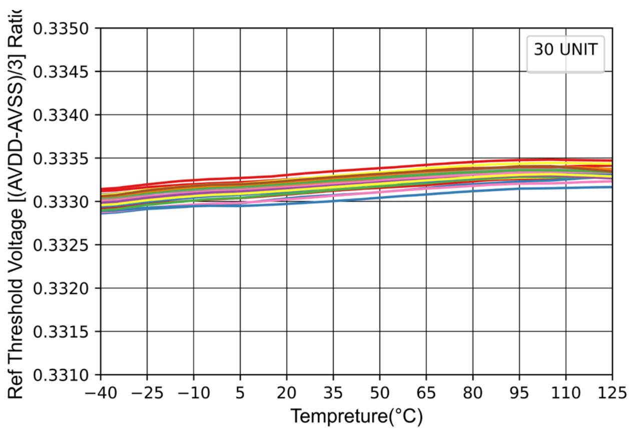

Figure 8-55 Reference Threshold (AVDD-AVSS)/3 vs. Temperature

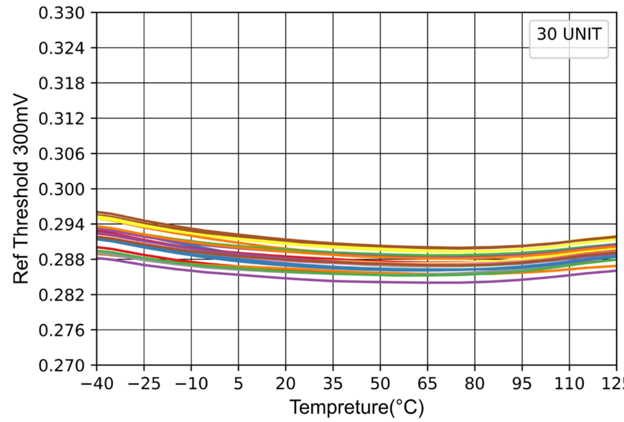

Figure 8-56 Reference Threshold (300mV) vs. Temperature

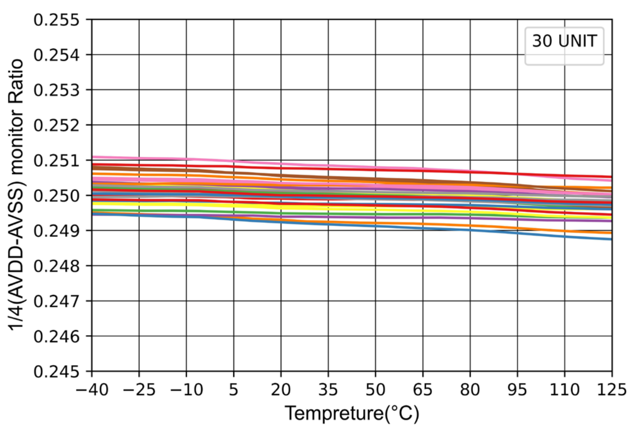

Figure 8-57 1/4(AVDD-AVSS) Monitor Ratio vs. Temperature

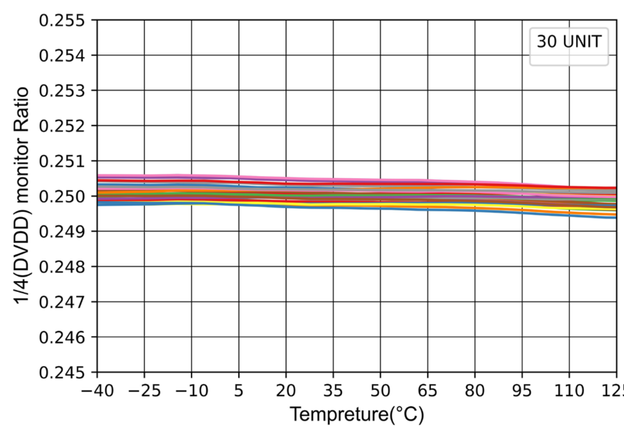

Figure 8-58 1/4(DVDD) Monitor Ratio vs. Temperature

9. Detailed Description

9.1.Overview

NSAD1249/NSAD1248/NSAD1247/NSAD1246 are low power, low noise 24bit sigma-delta analog-to-digital converter (ΣΔ-ADC), NSAD124x series incorporate a Σ-Δ modulator, an input crosspoint multiplexer (MUX), a programmable gain amplifier (PGA) stage, an internal reference and reference buffers, and on-chip digital filtering, which is intended for the measurement of high dynamic range, low frequency signals, such as those in pressure transducers, weigh scales, and temperature measurement applications.

NSAD124x series has up to 12 analog input pins. The device is configurable as either single-ended inputs, differential inputs, or any combination of the two.

The PGA is suitable for direct connection to low-level sensors. The gain is programmable from 1 to 128.

NSAD124x series contains a delta-sigma modulator, measures the input voltage relative to the reference voltage to produce the 24-bit conversion result. The differential input range of the ADC is ±VREF / Gain.

The ADC reference is either 2.048-V internal or external reference inputs. The REFOUT pin provides the buffered reference voltage output. The NSAD124x provides up to two voltage reference inputs.

The ADC includes two current sources that provide excitation to resistive sensors (RTD). Additionally, the NSAD1249 provides four GPIO control lines. The GPIOs are used for input and output of general-purpose logic signals, the GPIOs are multiplexed to the analog inputs.

The digital filter averages and decimates the modulator output data to yield the final, down-sampled conversion result. The finite impulse response (FIR) filter mode provides single-cycle settled data with simultaneous rejection of 50-Hz and 60-Hz at data rates of 20 SPS or less. The sinc3 filter has longer conversion time, and lower conversion noise, and offers simultaneous 50-Hz and 60-Hz line-cycle rejection at data rates of 2.5 SPS, 5 SPS, and 10 SPS, 50-Hz rejection at data rates of 16.6 SPS and 50 SPS, and 60-Hz rejection at data rates of 20 SPS and 60 SPS.

The NSAD124x clock is either provided by the internal low-drift oscillator, or an external clock source on the CLK input. The nominal clock frequency is 4.096 MHz.

ADC conversions are controlled by the START pin or by the START command. The ADC is programmable for continuous or one-shot conversions. The DRDY or DOUT/DRDY pin provides the conversion data ready signal. When taken low, the RESET pin resets the ADC. The ADC is powered down by the PWDN pin or is powered down in software mode.

The ADC operates in either bipolar analog supply configuration (±1.5V to ±2.5 V), or in a single supply configuration (3V to 5V). The digital power supply range is 2.7 V to 3.6 V.

9.2.Device Functional Modes

The NSAD124x series offer two power modes: conversion mode and power-down mode. This allows the user total flexibility in terms of speed, rms noise, and current consumption.

Reset

The NSAD124x is reset in three ways:

- Power-on reset
- RESET pin
- RESET command

When a reset occurs, the configuration registers reset to default values. Note that if the device had been using an external clock, the reset sets the device to use the internal oscillator as a default configuration.

Power-on Reset

The NSAD124x includes a Power-On Reset (POR) feature that ensures the analog and digital modules are initialized to a known state upon power application. The device releases reset when the analog power supply voltage (AVDD-AVSS) exceeds approximately 2.1V, and the digital power supply voltage (DVDD-DGND) exceeds approximately 2.2V. After POR is released, the device begins initialization, including enabling the internal oscillator and loading the default configuration. During power-up, NSAD1249 users can poll the RDY bit in the STATUS register via SPI. The RDY bit being 1 indicates the device is still initializing, while a 0 indicates that initialization is complete. The FL_POR bit in the STATUS register is set to 1 to indicate that a power-on reset has occurred.

The NSAD124x incorporates a power-on reset (POR) circuit that holds the device in reset until all supplies reach approximately 1.65 V. The power-on reset also ensures that the device starts operating in a known state in case a brown-out event occurs, when the supplies have dipped below the minimum operating voltages. When the device completes a POR sequence, the FL_POR flag in the status register is set high to indicate that a POR has occurred. Begin communications with the device 2.2 ms after the power supplies reach minimum operating voltages. The only exception is polling the status register for the RDY bit. If the user polls the RDY bit, then use an SCLK rate of half the maximum-specified SCLK rate to get a proper reading when the device is making internal configurations. This 2.2-ms POR time is required for the internal oscillator to start up and the device to properly set internal configurations. After the internal configurations are set, the device sets the RDY bit in the device status register (01h). When this bit is set to 0, user configurations can be programmed into the device.

At power-on, after the supply voltages cross the reset-voltage thresholds, the ADC is reset and $2^{\wedge 16} * f_{CLK}$ cycles later the ADC is ready for communication. Until this time, DRDY is held low. DRDY is driven high to indicate when the ADC is ready for communication. If the START pin is high, the conversion cycle starts 512 / f_{CLK} cycle after DRDY asserts high.

RESET Pin

Pulling the RESET pin low and holding it for at least 4 x t_{CLK} cycles, then bringing it back high, will reset the device. Where $t_{CLK} = f_{CLK}/1$, f_{CLK} is 4.096MHz nominal.

RESET Command

Sending the RESET command (06h or 07h) via SPI can reset the ADC, excluding the SPI interface itself. The RESET command takes effect on the 8th falling edge of SCLK.

Power-Down Mode

The user enters the power-down mode by sending the SLEEP command via SPI. the SLEEP command takes effect on the falling edge of the 8th SCLK, and the NSAD124x enters the power-down mode after completing the current conversion. Alternatively, the NSAD124x can enter power-down mode by pulling down the START pin, which is functionally the same in both ways. In power-down mode, all analog circuits and some digital circuits are powered down to achieve the lowest power consumption. However, the internal reference voltage can be configured to remain enabled in power-down mode through VREFCON[1:0].

In power-down mode, all register values are retained at their current settings, WAKEUP, RDATA, RDATAC, SDATAC, RREG commands can be responded to, and other commands are blocked. This means that it is possible to read the register configuration values in power-down mode and the last conversion result before entering power-down mode. The WAKEUP command must be issued to exit power-down mode and enter conversion mode.

Conversion Mode

When the START pin is high, device enters the conversion mode by default. In conversion mode, the NSAD124x completes one conversion, and the DRDY pin pulls low to indicate that a new one is ready, and immediately starts a new conversion. This configuration continues until the START pin is taken low.

Conversions can also be initiated through SPI commands as well. Similar to using the START pin, the device can be put into a power-down mode using the SLEEP command. Functionally, this is similar to taking the START pin low. To initiate a conversion, the WAKEUP command powers up the ADC and starts a conversion, similar to returning the START pin high. Note that the START pin must be held high to use commands to control conversions. Do not combine using the START pin and using commands to control conversions.

The START pin provides precise control of conversions. Pulse the START pin high to begin a conversion, The START pin can also be used to perform synchronized measurements for multi-channel applications by pulsing the START pin. With multiple devices, if each device receives the START pin pulse at the same time, all devices start a conversion on the rise of the start pin. If all devices are operating with the same data rate, all of the devices complete the conversion at the same time. The conversion completion is indicated by the DRDY pin going low and with the DOUT/DRDY pin when the DRDY MODE bit is 1 in the IDAC0 register. When the conversion completes, the device automatically powers down. During power down, the conversion result can be retrieved; however, START must be taken high before communicating with the configuration registers. The device stays powered down until the START pin is returned high to begin a new conversion.

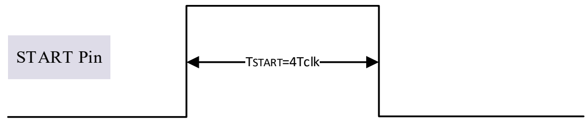

Figure 9-1 Minimum Start Pulse Duration

Programmable Conversion Delay

When a new conversion is started, the ADC provides a delay before the actual start of the conversion. This timed delay is provided to allow for the internal circuit to settle. The delay time can be configured to automatically delay the start of a conversion after the START pin is taken high, or a WREG command is sent to change any configuration register list below.

- Reset (hardware (toggle RESET pin), software (RESET command))
- Wake-up (START pin high, WAKEUP command)
- Changes the value of the bit corresponding to the following registers:
  - MUX0(00h),bits[5:0](1248/1247)
  - MUX1(02h), bits[7:0]
  - SYS0(03h), bits[6:0]
  - IDAC0(0Ah), bits[2:0]
  - IDAC1(0Bh), bits[7:0]
  - REF_MON(10h), bits[5:4] bit[0](1249)
  - FILTER_EX(11h), bits[7:0](1249)
  - SYS1(12h), bit[6]bit[4](1249)

In some cases, more delay is required to allow for external settling effects. The programmable conversion delay is intended to accommodate the analog settling time on the inputs (for example, when changing a multiplexer channel). The NSAD1249 uses the DELAY[2:0] bits in REF_MON(10h) to set the delay time from $1 \times t_{MOD}$ to $4096 \times t_{MOD}$ (where $t_{MOD}=16 \times t_{CLK}$). The default programmable conversion delay setting is $14 \times t_{MOD}$. The NSAD1248, NSAD1247, and NSAD1246 are fixed to $14 \times t_{MOD}$.

9.3.Power Supply

NSAD124x has two independent power supplies: analog power supply (AVDD, AVSS) and digital power supply (DVDD, DGND). The power supply range of the analog power supply (AVDD AVSS) is 3V~5.5V, and the analog power supply can be bipolar (AVDD=+2.5V, AVSS=-2.5V, DGND=0V) or unipolar (AVDD=5V, AVSS=DGND=0V). The power supply range of the analog power supply is 3V~3.6V. AVDD and DVDD can be powered on in any order, and it is recommended to maintain a monotonic increase in voltage during the power on process. A minimum of 0.1uF capacitor must be used for decoupling between AVDD and AVSS, as well as between DVDD and DGND. It is recommended to use a multi-layer ceramic chip capacitor (MLCC) with low equivalent series resistance (ESR) and inductance (ESL) characteristics, and place the decoupling capacitor as close to the device power pin as possible. The use of multiple via in parallel reduces the overall inductance, which is beneficial for ground connection.

9.4.ADC Feature Description

Analog Inputs

NSAD124x has a flexible input selection switch array, allowing up to 12 analog inputs. Any analog input, AINx, can be configured as a positive or negative input for PGA.

NSAD1249 has 12 analog inputs (AIN0~AIN11), MUX-P [3:0] in the MUX IN register (11h) configured with PGA positive input, and MUX-N [3:0] configured with PGA negative input.

NSAD1248 has 8 analog inputs (AIN0~AIN7), with MUX-P [2:0] in the MUX IN register (00h) configured for PGA positive input and MUX-N [2:0] configured for PGA negative input.

NSAD1247 has 4 analog inputs (AIN0~AIN3), with MUX-P [2:0] in the MUX IN register (00h) configured for PGA positive input and MUX-N [2:0] configured for PGA negative input.

NSAD1246 has two analog inputs (AIN0~AIN1), fixed as PGA positive input as AIN0 and PGA negative input as AIN1

Each analog input terminal has ESD diodes for AVDD and AVSS to protect the analog input from surge damage. Therefore, the absolute voltage value loaded on each analog input terminal should comply with the following conditions:

$$\mathrm{AVSS} - 0.3\mathrm{V} < \mathrm{V_{AINx}} < \mathrm{AVDD} + 0.3\ \mathrm{V}$$

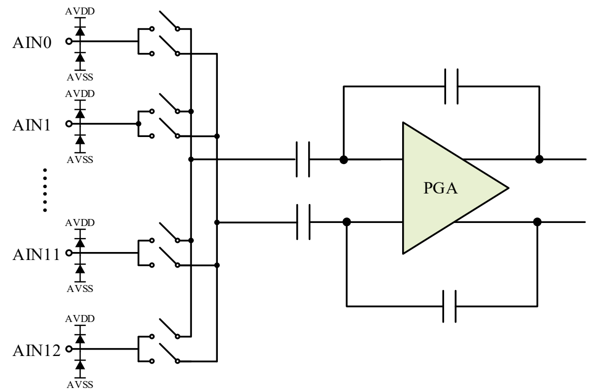

Figure 9-2 Analog Input Block Diagram

Voltage Reference

The NSAD124x (except the NSAD1246) has a built-in accurate, low noise, low temperature drift 2.048V on-chip reference source with a maximum temperature drift of 10ppm/°C. The NSAD124x also provides two fully differential external reference inputs: REF0 and REF1, which can be used to select an external voltage reference or for proportional measurements (e.g., RTD applications). In addition, the NSAD124x provides two fully differential external reference inputs: REF0 and REF1, which can be used to select an external voltage reference or for proportional measurements (e.g., RTD applications). The reference source is selectable via the REFSELT[1:0] bits.

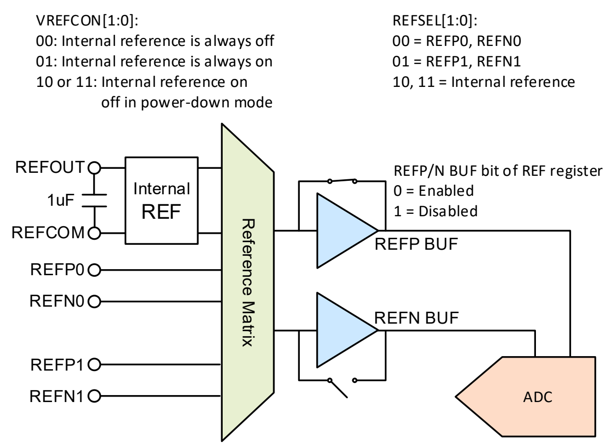

Figure 9-3 Reference Multiplexer Block Diagram

Internal Reference

The NSAD1249/NSAD1248/NSAD1247 provide a precision, low-noise, low-temperature-drift 2.048V on-chip bandgap reference. It can be enabled or disabled by the VREFCON[1:0] bits in the MUX_REF register (02h).

Setting VREFCON[1:0] to 00 disables the on-chip reference.

Setting VREFCON[1:0] to 01, the on-chip reference is enabled in continuous transition mode but disabled in power-down mode.

Setting VREFCON[1:0] to 10 or 11, the on-chip reference is enabled in both continuous conversion mode and power-down mode.

On-chip reference provides ± 10mA current drive capability, can provide reference voltage for external circuits at the same time. A 1uF ~ 10uF capacitance is needed to be placed between REFOUT and REFCOM pin to ensure the stability of the on-chip reference. Larger capacitor values help filter more noise at the expense of a longer reference start-up time. Therefore, in the ADC power-up and wake-up from power-down mode, need to leave enough delay to ensure that the first sample data is correct. When selecting the internal reference and frequently switching between power-down mode and continuous conversion mode, you can choose to set VREFCON[1:0] to 10 or 11 to save the build-up time required for re-powering up, but this will lead to a corresponding increase in power consumption.

External Reference Input

The ADC has two sets of fully differential reference inputs, REF0 and REF1, and the user can select the corresponding channels through the REFSELT[1:0] bits in the MUX_REF register (02h):

REFSELT[1:0] bits select 00: Select REFP0/REFN0 channel (default).

REFSELT[1:0] bit selection 01: Selects REFP1/REFN1 channel (NSAD1248, NSAD1249 only).

REFSELT[1:0] bits select 10 or 11: Selects the internal 2.048V reference.

The ADC has a reference voltage buffer, of which the REFP buffer is turned on by default and the REFN buffer is bypassed by default in NSAD1248/NSAD1247/NSAD1246, and can be selected to be turned on or off by the REFP_BUF bit and the REFN_BUF bit in the REF_MON register (10h) in NSAD1249.

When the reference voltage buffer is bypassed, the common-mode voltage input range of REF0 and REF1 is from AVSS to AVDD, and when the buffer is turned on, an additional margin of 100mV is required. The NSAD124x can accept voltages from 0.5v to AVDD as the reference source.

Without buffering, the reference input bias current is 5.5uA/V. A voltage source with high output impedance (reference resistor in proportional measurements) may cause DC gain errors, in which case an internal or external reference voltage buffer is recommended. In applications where the impedance of the external input voltage source is low enough (most voltage references) to not introduce gain errors into the system, an external reference voltage buffer is not necessary.

REFP0, PREFN0 are multiplexed with GPIO0, GPIO1; REFP1, REFN1 are multiplexed with AIN10, AIN11.

Programmable Gain Amplifier (PGA)

The NSAD124x utilizes a capacitive programmable gain amplifier (PGA) with gain settings of 1, 2, 4, 8, 16, 32, 64, 128. The NSAD124x's capacitive PGA has an input common-mode range to the rail at all gains (1 to 128). This allows the sensor common-mode voltage to be biased almost anywhere from the positive supply rail to the negative supply rail.

For DC or low-frequency signals, the capacitive PGA is first chopped at the input to modulate the DC input signal to the chopping frequency, which is then amplified by the capacitive amplifier. Finally, the signal is de-chopped and demodulated back to DC at the output. Due to the chopping, the amplifier's distortion and flicker noise are modulated to the chopping frequency and are low-pass filtered in the de-chopping. Thus, the capacitive PGA has very low offset voltage, offset drift and low frequency flicker noise.

Prior to the main PGA, a buffer is added to provide pre-charge to minimize the build-up time and increase the input impedance, which is also composed of a chopper amplifier with very low drift and low-frequency flicker noise.

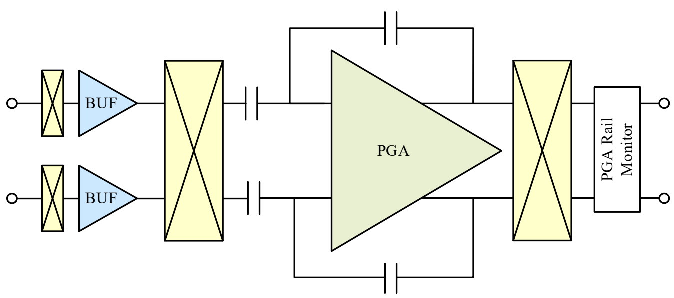

Figure 9-4 Capacitive Programmable Gain Amplifier

Oscillator

The NSAD124x integrates a high-precision, low-temperature-drift on-chip oscillator to provide the system clock at a frequency of 4.096 MHz, with ±1% accuracy over the operating temperature range. In addition, an external clock source can be selected via the CLK pin input to provide the system clock. The frequency range of the external clock source is 4.096MHz ±5%, beyond which the NSAD124x may not be able to guarantee normal operation timing.

The NSAD124x uses an internal oscillator by default. The user can select the internal 4.096 MHz oscillator or external clock source through the CLK bit in the REF CTRL register (02h).

In continuous conversion mode (after START pin is high or WAKEUP command is sent via SPI), after switching the clock source, the current conversion will be terminated immediately, the modulator and digital filter will be reset, and a new conversion will be restarted to ensure the data is correct.

Σ-Δ Modulator

The modulator is a 4-bit (-8~+8), third-order, ΔΣ modulator. The modulator samples the analog input voltage at a high sample rate ($f_{mod} = f_{CLK} / 16$), and converts the analog input to bit streams given by the ratio of the input signal to the reference voltage. The modulator shapes the noise of the converter to high frequency, where the noise is removed by the digital filter. f_{CLK} is offered by internal oscillator or external clock

Data Format

The devices provide 24 bits of data in binary twos complement format. The size of one code (LSB) is calculated as:

LSB = (2 · VREF / Gain) / 224 = +FS / 223 (11)

A positive full-scale input [VIN ≥ (+FS– 1 LSB) = (VREF / Gain– 1 LSB)] produces an output code of 7FFFFFh and a negative full-scale input (VIN ≤–FS =–VREF / Gain) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale. 表 23summarizes the ideal output codes for different input signals.

INPUT SIGNAL, VIN = VAINP– VAINN	IDEAL OUTPUT CODE
≥ FS $(2^{23}– 1) / 2^{23}$	7FFFFFh
FS / 2^{23}	000001h
0	000000h
–FS / 223	FFFFFFh
≤–FS	800000h

Digital Filter

The digital filter has two options: third-order SINC filter (SINC3) and Low-latency filter. The Low-Latency filter provides simultaneous rejection of 50-Hz and 60-Hz frequencies with data rates 2.5 SPS through 20 SPS while providing single-cycle settled conversions.

The NSAD1249 selects between a Low-Latency and a SINC3 by setting the FILTER bit in SYS CTRL (12h) to 1 selects the Low-Latency filter, and setting it to 0 selects the SINC3 filter. The NSAD1248/1247/1246 fixed Low-Latency filter is used. Figure 9-5 shows the digital filter implementation.

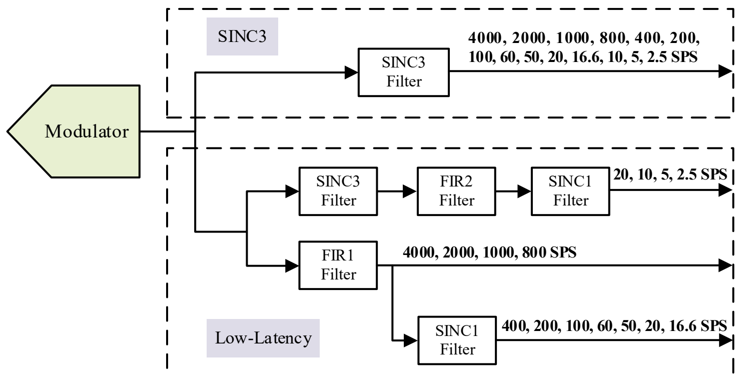

Figure 9-5 NSAD124x Digital Filter Block Diagram

Low-Latency Filter

The filter is a finite impulse response (FIR) filter that provides settled data, given that the analog input signal has settled to the final value before the conversion is started. The low-latency filter is especially useful when multiple channels must be scanned in minimal time.

Low-Latency Filter Frequency Response

Figure 9-6 to show the frequency response of the low-latency filter for different data rates.

The low-latency filter notches and output data rate scale proportionally with the clock frequency. For example, a notch that appears at 20 Hz when using a 4.096-MHz clock appears at 10 Hz if a 2.048-MHz clock is used. Note that the internal oscillator can vary over temperature as specified in the Electrical Characteristics table. The data rate, conversion time, and filter notches consequently vary by the same percentage. Consider using an external precision clock source if a digital filter notch at a specific frequency with a tighter tolerance is required.

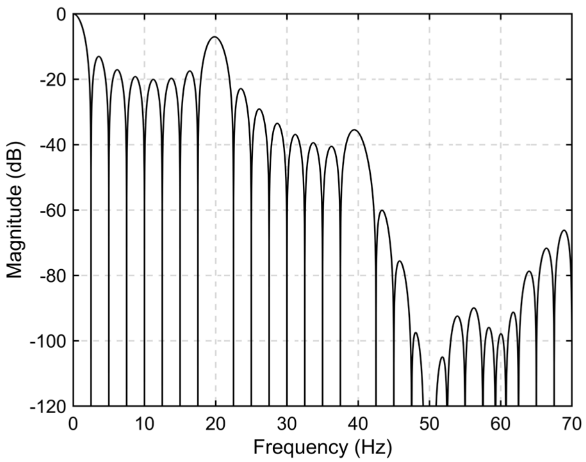

Figure 9-6 Low-Latency Filter Frequency Response (2.5 SPS)

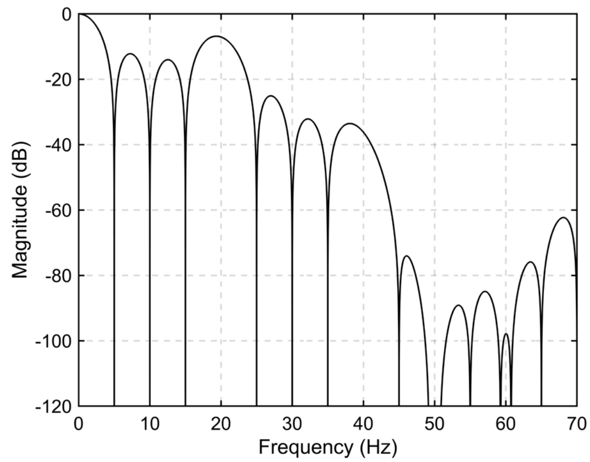

Figure 9-7 Low-Latency Filter Frequency Response (5 SPS)

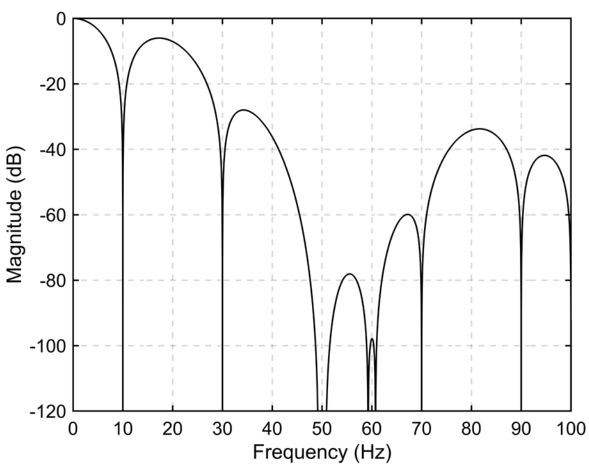

Figure 9-8 Low-Latency Filter Frequency Response (10 SPS)

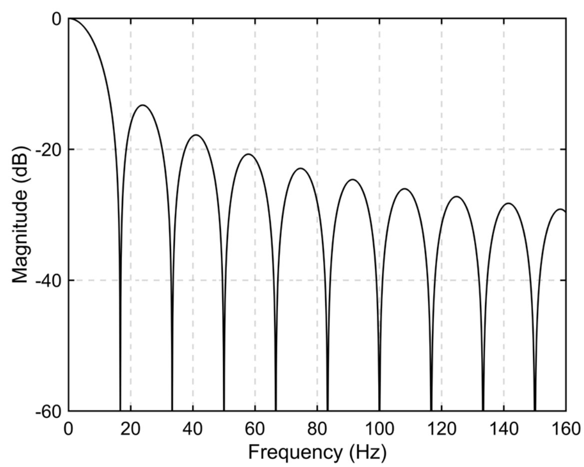

Figure 9-9 Low-Latency Filter Frequency Response (16.6 SPS)

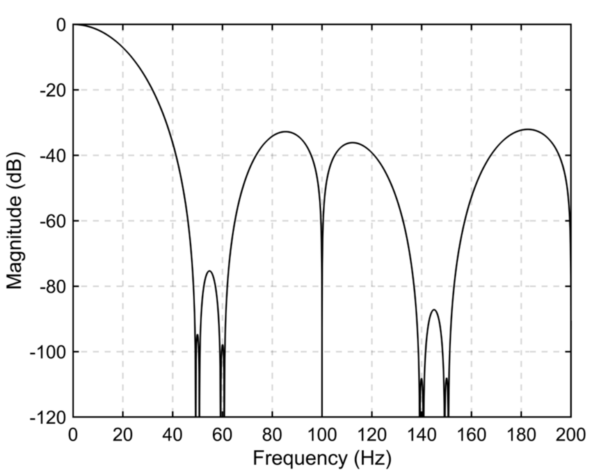

Figure 9-10 Low-Latency Filter Frequency Response (20 SPS)

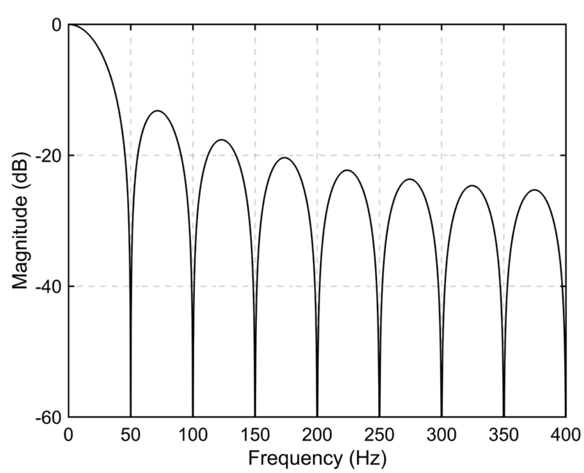

Figure 9-11 Low-Latency Filter Frequency Response (50 SPS)

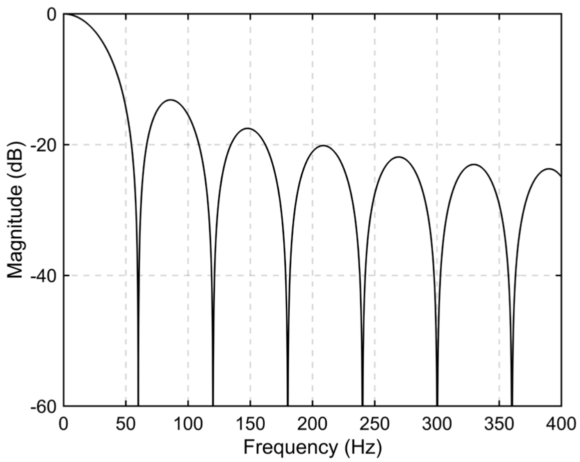

Figure 9-12 Low-Latency Filter Frequency Response (60 SPS)

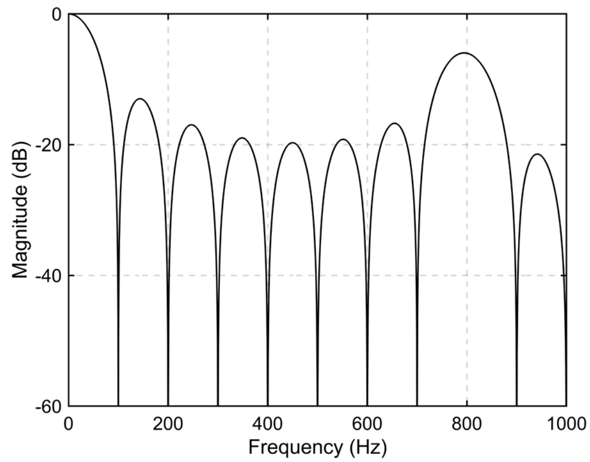

Figure 9-13 Low-Latency Filter Frequency Response (100 SPS)

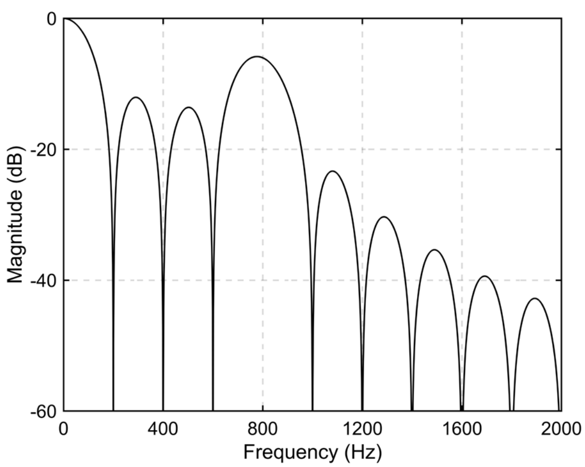

Figure 9-14 Low-Latency Filter Frequency Response (200 SPS)

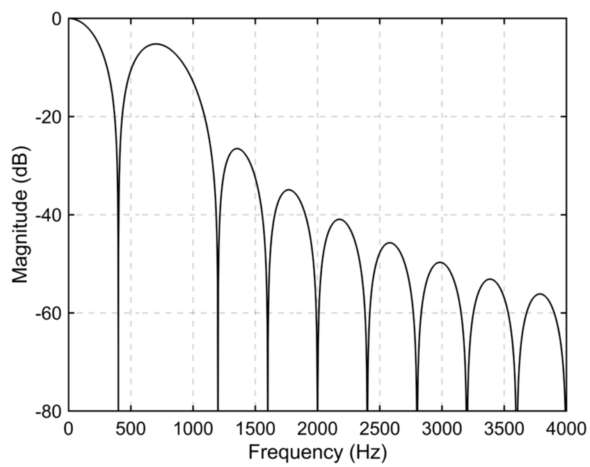

Figure 9-15 Low-Latency Filter Frequency Response (400 SPS)

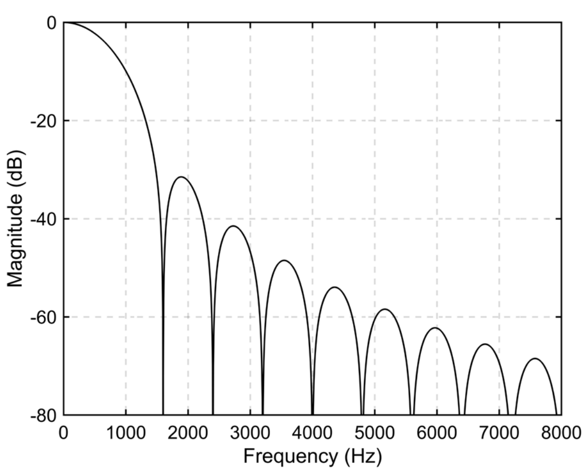

Figure 9-16 Low-Latency Filter Frequency Response (800 SPS)

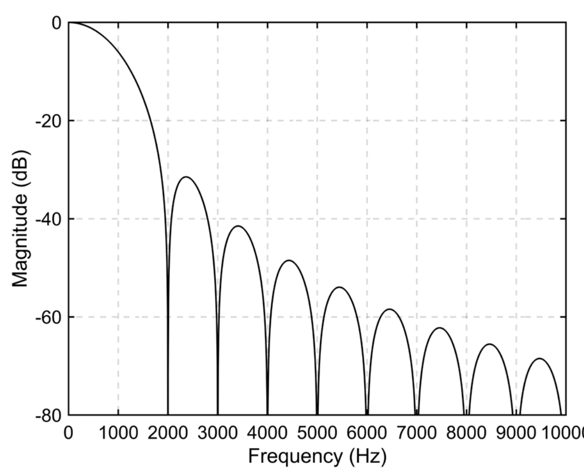

Figure 9-17 Low-Latency Filter Frequency Response (1000 SPS)

Table 9-1 shows the conversion times for the low-latency filter for each ADC data rate and various conversion modes.

Table 9-1 Data Conversion Time for the Low-Latency Filter

Output Data Rate (SPS)	First Conversion		Second Conversion& Subsequent Conversions	
	Number of t_{MOD} Periods	ms	Number of t_{MOD} Periods	ms
2.5	103697	405.07	102400	400
5	52497	205.07	51200	200
10	26897	105.07	25600	100
16	15360	60.00	15360	60
20	14097	55.07	12800	50
50	5120	20.00	5120	20
60	4264	16.66	4264	16.66
100	2560	10.00	2560	10
200	1280	5.00	1280	5
400	640	2.50	640	2.5
800	320	1.25	320	1.25
1000	256	1.00	256	1
2000	128	0.50	128	0.5
4000	64	0.25	64	0.25

50-Hz and 60-Hz Line Cycle Rejection

The digital filter provides enhanced rejection of power-line-coupled noise for data rates of 60 SPS and less. Program the filter to tradeoff data rate and conversion latency versus the desired level of line cycle rejection. Table 9-2 summarize the ADC 50-Hz and 60-Hz line-cycle rejection based on ±1Hz and ±2Hz tolerance of power-line to ADC clock frequency. The best possible power-line rejection is provided by using an accurate external ADC clock.

Table 9-2 Low-Latency Digital Filter Line Cycle Rejection

DATA RATE (SPS)	Low-Latency Digital Filter Line Cycle Rejection (dB)			
	f_{IN} = 50 Hz ±1 Hz	f_{IN} = 60 Hz ±1 Hz	f_{IN} = 50 Hz ±2 Hz	f_{IN} = 60 Hz ±2 Hz
2.5	-113.15	-97.79	-97.42	-91.20
5	-111.31	-97.78	-87.31	-81.89
10	-110.88	-97.78	-85.47	-80.05
16	-33.81	-20.94	-27.78	-20.75
20	-94.66	-97.78	-75.27	-79.61
50	-33.76	-15.53	-27.60	-15.05
60	-13.42	-35.12	-12.56	-28.98

Time does not include the programmable delay set by the DELAY[2:0] bits in the REFMON register. The default setting is an additional 14 · tMOD, where tMOD = tCLK · 16.

The low-latency filter provides many data rate options for rejecting 50-Hz and 60-Hz line cycle noise. At data rates of 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS, the filter rejects both 50-Hz and 60-Hz line frequencies. At data rates of 16.6 SPS and 50 SPS, the filter has a notch at 50 Hz. At a 60-SPS data rate, the filter has a notch at 60 Hz.

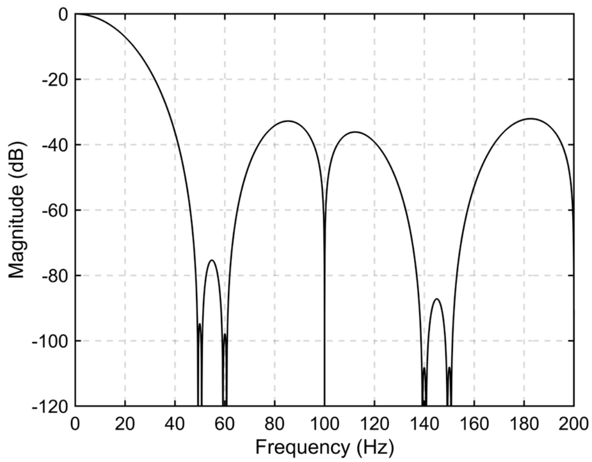

Figure 9-18 Low-Latency Filter Frequency Response (20 SPS)

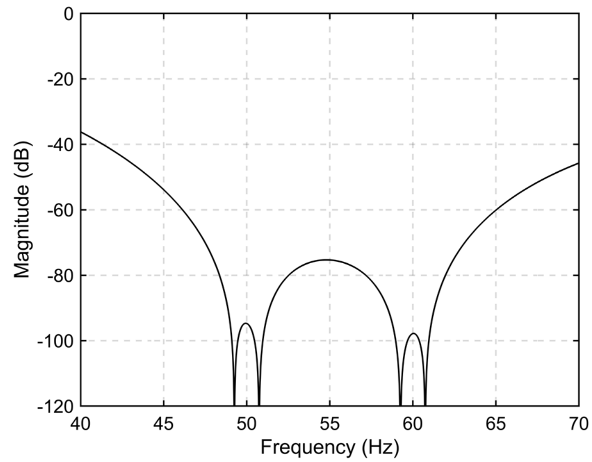

Figure 9-19 Low-Latency Filter Frequency Response(20SPS)

SINC3 Filter

SINC3 Filter Frequency Response

When the FILTER bit in SYS CTRL (12h) is set to 0, the SINC3 filter is selected. Compared with the Low-Latency filter, the SINC3 filter has improved noise performance, but the first data output is delayed by three cycles.

The sinc3 filter offers simultaneous 50-Hz and 60-Hz line cycle rejection at data rates of 2.5 SPS, 5 SPS, and 10 SPS. The sinc3 filter offers only 50-Hz rejection at data rates of 16.6 SPS and 50 SPS, and only 60-Hz rejection at data rates of 20 SPS and 60 SPS. The sinc3 digital filter response scales with the data rate and has notches at multiples of the data rate. Figure 9-20 shows the sinc3 digital filter frequency response normalized to the data rate. As an example, Figure 9-21 shows the frequency response when the data rate is set to 10 SPS, and Figure 9-22 illustrates a close-up of the filter rejection of 50-Hz and 60-Hz line frequencies.

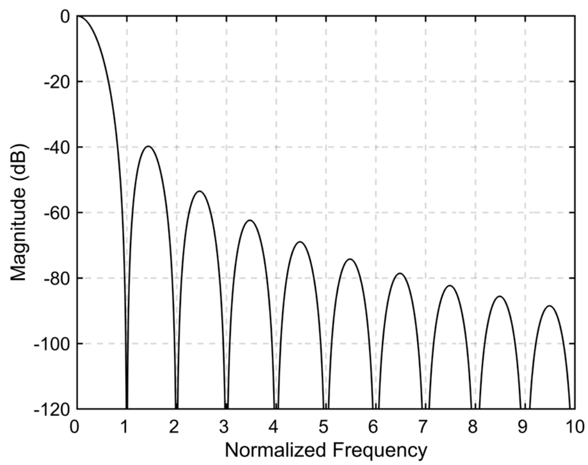

Figure 9-23 Frequency normalized to data rate, sinc3 filter

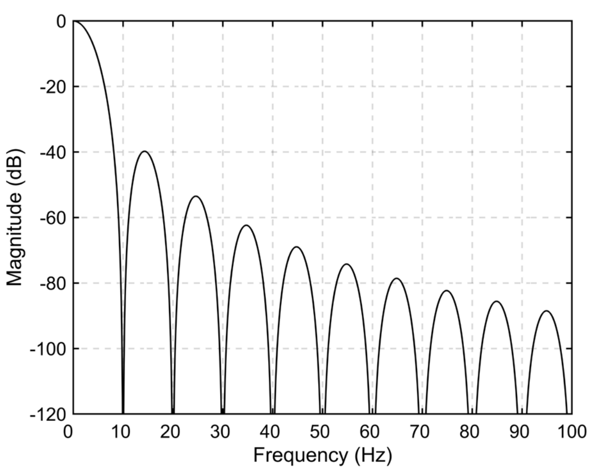

Figure 9-24 Sinc3 Filter Frequency Response, ODR = 10 SPS

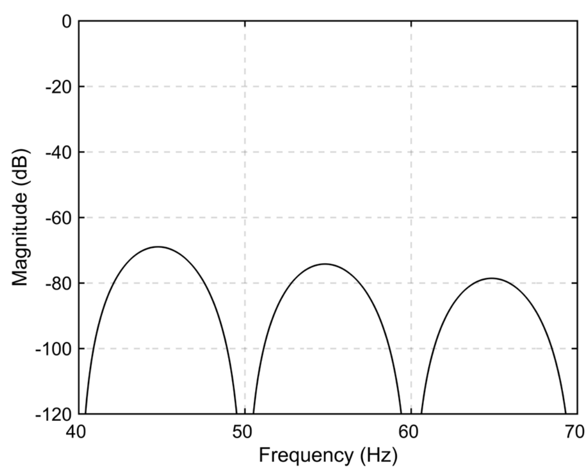

Figure 9-25 . Sinc3 Filter Frequency Response, ODR = 10 SPS, Zoomed to 50 Hz and 60 Hz

Table 9-3 Data Conversion Time for the SINC3 Filter

Output Data Rate (SPS)	First Conversion		Second Conversion& Subsequent Conversions	
	Number Of t_{MOD} Periods	ms	Number Of t_{MOD} Periods	ms
2.5	307200	1200	102400	400
5	153600	600	51200	200
10	76800	300	25600	100
16	46080	180	15360	60
20	38400	150	12800	50
50	15360	60	5120	20
60	12792	49.969	4264	16.656
100	7680	30	2560	10
200	3840	15	1280	5
400	1920	7.5	640	2.5
800	960	3.75	320	1.25
1000	768	3	256	1
2000	384	1.5	128	0.5
4000	192	0.75	64	0.25

50-Hz and 60-Hz Line Cycle Rejection

The filter notch and output data rate are proportional to the clock frequency, so the internal oscillator can vary with temperature. Therefore, the data rate, conversion time, and filter trap frequency point will vary in the same proportion. If a more accurate filter trap frequency point is desired, consider using an external precision clock source.

Table 9-4 SINC3 Digital Filter Line Cycle Rejection

Output Data Rate (SPS)	SINC3 Digital Filter Line Cycle Rejection (dB)			
	f_{IN} = 50 Hz ±1 Hz	f_{IN} = 60 Hz ±1 Hz	f_{IN} = 50 Hz ±2 Hz	f_{IN} = 60 Hz ±2 Hz
2.5	-108.7	-113.4	–107.2	–112.1
5	-103.2	–107.8	–90.1	–95.0
10	-101.8	–106.4	–84.6	–89.4
16	–101.6	–63.0	–83.4	–62.4
20	–53.5	–106.1	–53.5	–88.0
50	–101.4	–46.7	–82.9	–45.3
60	–40.3	–105.1	–37.8	–87.2

Time does not include the programmable delay set by the DELAY[2:0] bits in the REFMON register. The default setting is an additional 14 · tMOD, where tMOD = tCLK · 16.

Global Chopping Mode

The device uses a very low-drift PGA and modulator in order to provide very low input voltage offset drift. However, a small amount of offset voltage drift sometimes remains in normal measurement. To further minimize the system offset voltage and offset voltage drift, the NSAD1249 version incorporates a Global chopping option to reduce the offset voltage and offset voltage drift to very low levels. When the Global chopping is enabled, the ADC performs two internal conversions to remove the input offset voltage. The first conversion is made with normal input polarity, and then the ADC inverts the internal input polarity for the second conversion. The inverse of the two conversions is averaged to produce the final conversion, eliminating the offset voltage.

When using the low-latency filter with Global chopping, the first conversion result is available after two conversions. With the SINC3 filter, the data is available after six conversions. In continuous conversion mode with the Global chopper mode enabled, subsequent conversions are completed in half the time of the first conversion. The data used for alternate inputs is pipelined so that the average value occurs at each ADC data cycle.

Note

If the MUXCAL Function is Enabled, Global chopping Mode must be Disabled

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Bias Voltage Generator (VBIAS):

The NSAD124x provides an internal bias voltage generator (Vbias), which can be configured to load the bias voltage to the analog inputs AINx via the VBIAS register (01h).

NSAD1249, NSAD1248 can optionally load the bias voltage to AIN0~AIN7;

NSAD1247 can optionally load the bias voltage to AIN0~AIN3;

NSAD1246 can optionally load the bias voltage to AIN0~AIN1

Typical use cases for VBIAS are to provide a bias voltage for floating voltage signals such as thermocouples and to ensure that they are within the common mode input voltage range of the PGA. The bias voltage is buffered internally in the NSAD124x and an external capacitor can be placed to reduce noise. The larger the external capacitance, the slower the corresponding Vbias build-up time.

The bias voltages are ((AVDD + AVSS))⁄2 and ((AVDD + AVSS))⁄12 (NSAD1249 only, set by the VB_LEVEL bit in the SYS1 register (12h)).The block diagram of the VBIAS voltage generator and connections is shown in Figure 9-2.

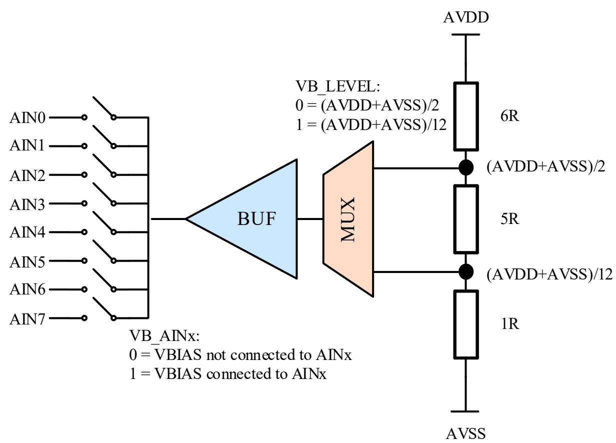

Figure 9-26 VBIAS Block Diagram

Excitation Current Sources (IDACs):

The NSAD1247, NSAD1248, and NSAD1249 provides two matched current sources (IDACs) with programmable output currents of 10 μA, 50 μA, 100 μA, 250 μA, 500 μA, 750 μA, 1000 μA, 1500 μA, and 2000 μA, 10uA and 2000 μA options is exclusive to the NSAD1249. The current sources provide excitation current to resistive temperature devices (RTDs), thermistors, diodes, and other resistive sensors that require constant current biasing. The two matched current sources can be connected to any analog input pin (NSAD1247 can be loaded to AIN0~AIN4; NSAD1248 can be loaded to AIN0~AIN7; NSAD1249 can be loaded to AIN0~AIN11). Both current sources can also be connected to the same pin. The excitation current is generated by the internal reference, so the internal reference must be enabled when using the excitation current source.

As a current source, the IDAC requires voltage headroom to the positive supply to operate. This voltage headroom is the compliance voltage. When driving resistive sensors and biasing resistors, take care not to exceed the compliance voltage of the IDACs, otherwise the specified accuracy of the IDAC current may not be met.

System Monitor

Reference Monitor

The NSAD1249 provides a voltage reference monitoring feature, allowing users to continuously monitor the ADC reference voltage status. This feature is enabled through the REF_MON register (10h) by setting the FL_REF_EN[1:0] bits. The voltage reference monitor compares the reference voltage against two threshold levels: the first threshold is 0.3V, and the second threshold is ((AVDD–AVSS))/3. If the reference voltage is below these thresholds, a latched flag in the STATUS register (0Fh) is updated after each data conversion.

A reference voltage below 0.3V indicates a possible short circuit of the reference voltage or an open circuit between the RTD and the reference resistor during RTD ratio measurements. By setting FL_REF_EN[1:0] to 01 in the REF_MON register (10h), this comparison function is enabled. If the reference voltage is below 0.3V, the FL_REF_L0 bit in the STATUS register (0Fh) is set to 1.

If the reference voltage is between 0.3V and ((AVDD–AVSS))/3, it can indicate a broken sensor excitation line in a 3-wire RTD setup. By setting FL_REF_EN[1:0] to 10 in the REF_MON register (10h), this comparison function is enabled. If the reference voltage is below ((AVDD–AVSS))/3, the FL_REF_L1 bit in the STATUS register (0Fh) is set to 1.

A 10MΩ resistor is connected between the REFPx and REFNx inputs. This resistor helps detect floating reference inputs. When the REFPx and REFNx inputs are floating, the 10MΩ resistor pulls both differential reference inputs to the same potential, allowing the reference voltage detection circuitry to detect this condition. By setting FL_REF_EN[1:0] to 11 in the REF_MON register (10h), this comparison function is enabled.

This 10MΩ resistor can reduce the input impedance of the reference inputs, posing a risk of increased gain error. Therefore, it is not recommended to enable this feature when precision measurements are required, but only for monitoring and diagnostic purposes.

A latched flag is set in the STATUS register (0Fh) after each data conversion and is updated on the falling edge of DRDY.

The NSAD1249 provides a voltage reference monitoring function, which allows the user to continuously monitor whether the ADC reference voltage is normal or not. This function is enabled by FL_REF_EN[1:0] in the REF_MON register (10h). Voltage reference monitoring compares the reference voltage to two level thresholds, the first threshold is 0.3 V and the second is ((AVDD-AVSS))⁄3. If the voltage reference falls below the thresholds, a latching flag is updated in the STATUS register (0Fh) after each data transition.

A reference voltage less than 0.3V indicates a possible short circuit in the reference voltage or, in the case of RTD scaling measurements, a broken wire between the RTD and the reference resistor. This comparison function is enabled by setting 01 to FL_REF_EN[1:0] in the REF_MON register (10h). If the reference voltage is less than 0.3V, the FL_REF_L0 bit in STATUS(0Fh) is set to one.

A reference voltage between 0.3V and ((AVDD-AVSS))⁄3 can indicate a broken sensor excitation line in a 3-wire RTD setup. This comparison function is enabled by setting FL_REF_EN[1:0] in the REF_MON register (10h) to 10. If the reference voltage is less than ((AVDD-AVSS))⁄3 , the FL_REF_L1 bit in STATUS(0Fh) is set 1.

A 10MΩ resistor is connected between REFPx and REFNx. This resistor can be used to detect the floating reference input. When the REFPx and REFNx inputs are floating, the 10MΩ resistor pulls both differential reference inputs to the same potential so that the reference voltage detection circuit can detect this condition. The comparison function is enabled by setting FL_REF_EN[1:0] to 11 in the REF_MON register (10h).

The 10MΩ resistor reduces the input impedance of the reference input and may increase the gain error. Therefore, it is not recommended to enable this function when precision measurement is required, but only when monitoring and diagnosis are required.

In the STATUS register (0Fh), a latch flag is set after each data conversion and updated on the falling edge of DRDY.

PGA Output Voltage Rail Monitors

In the NSAD1249, the Programmable Gain Amplifier (PGA) integrates an output voltage-to-rail monitoring function. If the PGA output voltage level exceeds AVDD-0.15V or falls below AVSS+0.15V, it triggers a PGA output flag in the STATUS register (0Fh) [bits 5:2]. This latched flag is updated after each data conversion.

The PGA output, VOUTN and VOUTP, can trigger overvoltage or undervoltage flags, resulting in a total of four flags. The PGA output-to-rail monitoring function is enabled through the FL_REF_EN bit in the Excitation Current Register 1. The block diagram of the PGA output-to-rail monitoring function is shown in Figure 8-22.

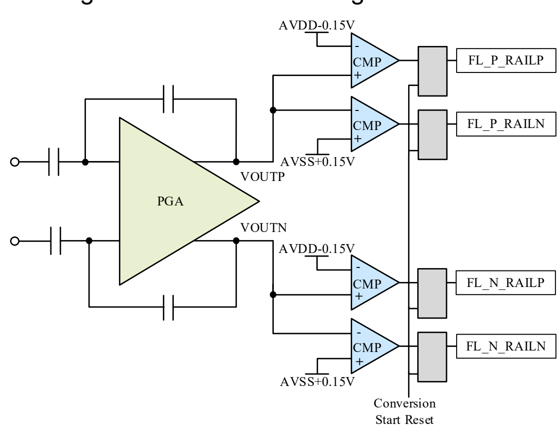

Figure 9-27 PGA Output Voltage Rail Monitors

Power Supply Monitors

The NSAD124x provides analog power supply (AVDD) and digital power supply (DVDD) monitor.

Setting MUXCAL[2:0] to 110 enables analog power supply monitoring, while setting MUXCAL[2:0] to 111 enables digital power monitoring (DVDD - DGND) / 4.

the positive and negative inputs of the PGA are disconnected from the analog input matrix and are connected to the resistor string divider and the PGA forced to Gain=1, independent of the PGA[2:0] bits in the system setup register 03h,. The positive and negative inputs of PGA are disconnected from the analog input channel and connected to a resistor string divider with a voltage of (AVDD - AVSS) / 4.

To obtain a valid reading of the power monitoring function, ensure that the reference voltage is higher than (DVDD - DGND) / 4 or (AVDD - AVSS) / 4 when the DVDD monitor or AVDD monitor function is enabled.

Notice

When Global chop is enabled, MUXCAL functions including the power monitoring function, temperature sensors, gain calibration, and internal misalignment calibration will not get a correct reading.

Temperature Sensor

The internal temperature sensor is enabled by setting MUX_CAL[2:0] = 010 in the REF_MUX register (address = 02h). The temperature sensor outputs a voltage proportional to the device temperature specified in the electrical characteristics table. When measuring the internal temperature sensor, the PGA input is disconnected from the external and connected to the output voltage of the temperature sensor. When the PGA is switched to temperature acquisition, the gain is fixed to 4 to achieve high signal-to-noise acquisition over the operating temperature range. The temperature sensor function can be used to monitor the temperature of the device itself, and the small thermal resistance to the PCB allows the temperature sensor to detect the temperature of the PCB.

$$\text{Temperature } (°\text{C}) = [(\text{Temperature Reading } (\text{mV}) - 282.073(\text{mV})) * 2.195\, mV/°\text{C}]$$

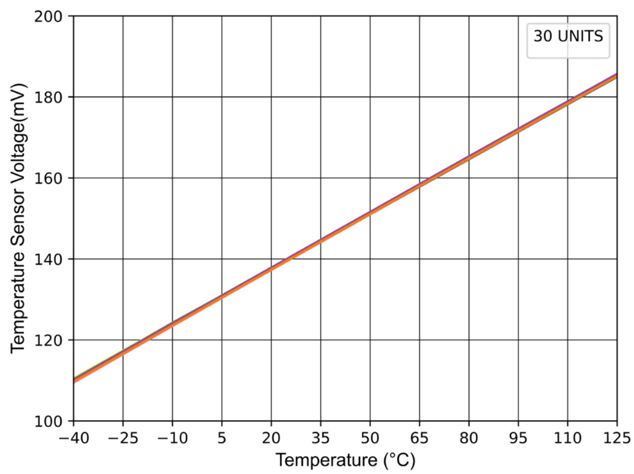

Figure 9-28 Temperature Voltage vs temperature

Open Circuit Test Current Source

The NSAD124x integrates a burn-out current source (BCS) to help detect open-circuit or short-circuit faults on the analog inputs. The user can enable this current source and set the current level through the BCS[1:0] bits in the MUX_IN register (00h).

When BCS[1:0] bits are 00, the Burn-out current source is disabled (default).

When BCS[1:0] bits are 01, the Burn-out current source is enabled, and the BCS current is 0.5μA.

When BCS[1:0] bits are 10, the Burn-out current source is enabled and the BCS current is 2μA.

When BCS[1:0] bits are 11, the Burn-out current source is enabled, and the BCS current is 10μA.

The BCS is a combination of two current sources. When the BCS is enabled, one current source pulls current from the selected positive analog input (AINP), and the other current source pours current from the selected negative analog input (AINN). If there is an open circuit between the positive and negative analog inputs, the positive analog input will be pulled up to AVDD and the negative analog input will be pulled down to AVSS, producing saturated input and ADC full-scale conversion result. Correspondingly, a short between the positive and negative analog inputs will result in an ADC conversion to near zero. The BCS current may introduce additional IR drop when the external sensor output resistance is large, so it is recommended that it be disabled for precision measurements and turned on only when needed for diagnostics.

CRC Check

The checksum is 8 bits wide and is generated using the following polynomial:

$$x^8 + x^2 + x + 1$$

System and Self Offset Calibration and Gain Calibration:

The NSAD124x has three calibration modes, which can be used to correct internal ADC errors or overall system errors. Calibration can be performed by sending calibration commands to the ADC.

Calibration should be carried out under stable power and reference voltage conditions. As shown in Figure 17, the digital filter output is adjusted by subtracting the value of the Offset Calibration (OFC) register, then multiplying by the Full-Scale Calibration (FSC) register value and dividing by 400000h. The data is then clipped to a 24-bit value to provide the final output.

When switching reference voltages, PGA gain, and input channels, recalibration should be performed as necessary. Offset calibration should be executed before system gain calibration to ensure accuracy. The ADC does not respond to calibration commands while in sleep mode.

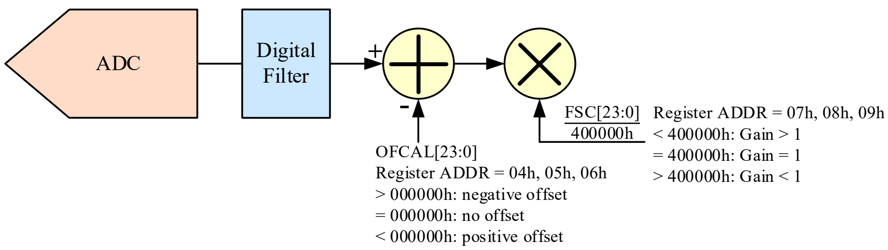

Figure 9-29 ADC Calibration Flowchart

Self-Offset Calibration

Self-Offset Calibration can be performed by sending the SELFOCAL (62h) command. The ADC initiates the self-offset calibration immediately upon receiving the SELFOCAL (62h) command on the 8th falling edge of SCLK. Any ongoing conversion is immediately terminated, DRDY is pulled high, and the PGA's positive and negative inputs are disconnected from the originally specified analog inputs and shorted to the internal bias voltage (AVDD-AVSS)/2. The PGA's gain and data output rate are determined by the PGA[2:0] and ODR[3:0] bits in the SYS0 register (03h). The ADC performs 16 continuous conversions at the current ODR, computes the average value, updates the OFC register with this offset calibration value, and DRDY falls to indicate that the self-offset calibration is complete.

The OFC register consists of three 8-bit registers, with a total length of 24 bits. The offset value is in two's complement format, with the maximum positive value being 7FFFFFh and the maximum negative value being 800000h. A register value of 000000h corresponds to no offset. This value is subtracted from each output count to produce the final output. If the Global chopping function is enabled, the offset calibration register is ignored. It should be noted that offset calibration should be performed before gain calibration.

System-Offset Calibration

System-Offset Calibration can be performed by sending the SYSOCAL (60h) command. The ADC initiates system-offset calibration immediately upon receiving the SYSOCAL (60h) command on the 8th falling edge of SCLK. Any ongoing conversion is immediately terminated, DRDY is pulled high. Unlike self-offset calibration, SYSOCAL is a system-offset calibration where the input is the user-defined system zero level to calibrate the offset. The PGA connections remain unchanged and are determined by the MUXP[2:0] and MUXN[2:0] bits in the MUX_IN register (00h). Other configurations and modes are the same as SELFOCAL. Once system-offset calibration is complete, DRDY falls and the OFC register is automatically updated.

Note

If Gain=128 is chosen, Offset Calibration should not be adopted

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System-Gain Calibration

The SYGCAL (61h) command initiates system gain calibration. The ADC starts the system gain calibration immediately upon receiving the SYGCAL (61h) command on the 8th falling edge of SCLK. Any ongoing conversion is immediately terminated, and DRDY is pulled high. The NSAD124x treats the signal at the analog input at this time as the full-scale signal. Therefore, during system gain calibration, the user must define an input signal as the full-scale input signal. However, it must not exceed ±1 times the reference voltage/gain, and the absolute voltage value on both the positive and negative input terminals must not exceed the PGA input range limits. Otherwise, the NSAD124x cannot guarantee the accuracy of the calibration result. Similar to offset calibration, the falling edge of DRDY indicates the completion of the calibration, and the FSC register will be updated.

The FSC register consists of three 8-bit registers, with a total length of 24 bits. The gain calibration value is binary, and the gain calibration coefficient is (FSC[23:0])/400000h. Therefore, when FSC[23:0] equals 400000h, it represents a gain coefficient of 1.

Note
The input signal must not exceed the reference voltage/gain

General-Purpose Inputs and Outputs (GPIOs)

NSAD1249, NSAD1248 provide 8 General-Purpose Input/Output (GPIO) pins, while NSAD1247 provides 4 GPIO pins. The functionality of the GPIO pins is controlled by two registers. The GPIO function of the corresponding pins is enabled using the CON[7:0] bits (CON[3:0] for NSAD1247) in the GPIO Configuration Register (0Ch). The GPIO Direction Register (0Dh) uses the DIR[7:0] bits (DIR[3:0] for NSAD1247) to configure the GPIO pins as inputs or outputs. The GPIO Data Register (0Eh) contains the DAT[7:0] bits (DAT[3:0] for NSAD1247) which hold the input or output GPIO data. If a GPIO pin is configured as an input, the corresponding DAT[x] bit reflects the state of the pin; if the GPIO pin is configured as an output, the output state is written to the corresponding DAT[x] bit. When pins are configured for GPIO functionality, they are powered by the analog supply, meaning the high level is AVDD and the low level is AVSS. Note that when used as outputs, care must be taken to prevent short circuits.

9.5.Programming

SPI

The NSAD124x has a full-duplex four-wire SPI interface, through which the user reads conversion data and configures and controls the ADC in SPI mode 1 (CPOL=0, CPHA=1). Similar to other SPI interfaces, the NSAD124x has four pins, namely CS, SCLK, DIN, and DOUT/DRDY, but DOUT/DRDY is a functionally multiplexed pin. However, DOUT/DRDY is a multiplexed pin, which will be discussed in detail in this chapter.

The chip select signal (CS) is a low active input, i.e., the SPI communication is enabled in the low-level device, which can be used to select a specific device when multiple devices share the SPI. When CS is high, SPI is in reset state, SCLK is ignored, and DOUT/DRDY goes into high resistance state. If the SPI is not shared with other devices, CS can be connected to DGND to keep the SPI enabled at all times and save pin overhead.

The serial clock (SCLK) is used to clock the SPI interface to the ADC. Data is sampled on the falling edge of SCLK and updated on the rising edge. It is recommended to connect a small resistor in series with SCLK to avoid SCLK burrs.

Serial data input (DIN) is used in conjunction with SCLK to send commands and register data to the device. The device samples DIN data on the falling edge of SCLK. During data readback, if there is no command, hold DIN high (equivalent to a NOP command).

DOUT/DRDY is a functionally multiplexed pin that can be used either as a regular digital data output (default mode) or as an ADC data-ready indication when the DRDYMOD bit is at position 1 in IDAC0 (0Ah).

When used as a digital output, this pin is used in conjunction with SCLK to send out conversion data and register values, which are updated on the rising edge.

When DOUT is multiplexed with the ADC data ready indication function, CS goes low, and every time an ADC conversion is completed, the DOUT/DRDY and dedicated DRDY pins go low simultaneously to indicate that new conversion data is ready. Both signals can be used to detect whether new data is ready or not. However, since DOUT/DRDY goes into a high-resistance state when CS goes high, the DOUT multiplexed ADC data-ready indication is disabled when monitoring conversions on multiple devices on the SPI bus, requiring the use of the dedicated DRDY pin.

Timeout

The NSAD1249 provides an SPI timeout reset function for resuming communication in case of an SPI interruption. The system controls TIMEOUT bit position 1 of register 1 (12h) to enable this function. When the SPI timeout reset function is enabled, the SPI interface resets if the SPI interface does not receive a valid 8-bit bit within 2^{15} tCLK. This feature is useful in situations where the chip select signal (CS) is permanently pulled low.

$\overline{\text{DRDY}}$

$\overline{\text{DRDY}}$ is a dedicated conversion data ready indication pin, when a conversion is complete, $\overline{\text{DRDY}}$ will pull low to indicate data ready, in continuous conversion mode after $\overline{\text{DRDY}}$ goes low, $\overline{\text{DRDY}}$ is driven high on the first SCLK rising edge. If data are not read, $\overline{\text{DRDY}}$ remains low, then pulses high 24 tCLK before the next DRDY falling edge. Data must be retrieved before the next $\overline{\text{DRDY}}$ update, otherwise the data will be overwritten by the new data and any previous data will be lost.

Command

The NSAD124x provides 13 commands to access the configuration registers, and retrieve data, as shown in Table 9-5. Some of the commands are stand-alone commands (WAKEUP, SLEEP, SYNC, RESET, SYSOCAL, SYSGCAL, and SELFOCAL) There are also three additional commands to control reading data from the device (RDATA, RDATAC, and SDATAC). The commands to read (RREG) and write (WREG) configuration register data from the device require additional information as part of the instruction.

Table 9-5 SPI Command Definitions

Command	Description	First command byte	Second command byte
WAKEUP	Wake-up from power-down mode	0000 000x (00h, 01h)	N/A
SLEEP	Enter power-down mode	0000 001x (02h, 03h)	N/A
SYNC	Synchronize ADC conversions	0000 010x (04h, 05h)	0000 010x (04h, 05h)
RESET	Reset the device to default values	0000 011x (06h, 07h)	N/A
NOP	No operation	1111 1111 (FFh)	N/A
RDATA	Read data once	0001 001x (12h, 13h)	N/A
RDATAC	Enter read data continuous mode	0001 010x (14h, 15h)	N/A
SDATAC	Exit read data continuous mode	0001 011x (16h, 17h)	N/A
RREG	Read from register rrrrr	001r rrrr (2xh)	000n nnnn
WREG	Write to register rrrrr	010r rrrr (4xh)	000n nnnn
SYSOCAL	System offset calibration	0110 0000 (60h)	N/A
SYSGCAL	System gain calibration	0110 0001 (61h)	N/A
SELFOCAL	Self offset calibration	0110 0010 (62h)	N/A

WAKEUP (0000 000x)

Issue the WAKEUP command to exit power-down mode and to place the device into standby mode. When running off the external clock, the external clock must be running before sending the WAKEUP command, otherwise the command is not decoded.

SLEEP (0000 001x)

The SLEEP command puts the NSAD124x into power-down mode. the NSAD124x receives the SLEEP command, completes the current conversion, and then goes to sleep. In power-down mode, the NSAD124x analog power supply will be turned off, but the configuration in the registers will be saved, and the internal reference voltage will be turned off in power-down mode by the VREFCON[1:0] bits. Issue the WAKEUP command to exit the power-down mode. A single conversion can be executed by issuing the WAKEUP command followed by the SLEEP command. The WAKEUP and SLEEP commands are functionally equivalent to pulling the START pin high or low, but the WAKEUP command is invalidated if the START pin is held low.

SYNC (0000 010x)

The NSAD124x will immediately reset the ADC digital filter and start a new conversion if receives a SYNC command. The user synchronizes each NSAD124x by sending SYNC commands to multiple devices at the same time, with synchronization occurring on the falling edge of the eighth SCLK of the SYNC command.

RESET (0000 011X)

The RESET command and the RESET pin function similarly but are not identical. Pulling the RESET pin low will reset the entire device. The RESET command will reset all parts except the SPI interface, as pulling CS high will reset the SPI.

After sending the RESET command, pulling the CS pin high will have the same effect as toggling the RESET pin.

The RESET command is similar to the RESET pin, but not identical. in that pulling the RESET pin low will reset the entire device. The RESET command will reset everything except the SPI interface, as pulling CS high will reset the SPI. The RESET command will reset all parts of the device except the SPI interface, as the CS pin is pulled high.

RDATA (0001 001x)

After issuing the RDATA command followed by 24 SCLKs, the NSAD124x will return a 24-bit conversion result. When using the RDATA command to read data, the 24-bit data will not be interrupted by new conversions, making the RDATA command particularly suitable for applications where monitoring the falling edge of the DRDY pin is not possible. Similarly, while the NSAD124x is returning the 24-bit data, SDI will ignore any commands, and SPI full-duplex communication will be disabled to ensure data integrity. This command is also valid in RDATAC mode.

RDATAC (0001 010x)

The RDATAC command enables continuous data read mode. This is the default mode upon reset. In continuous data read mode, new conversion results are automatically loaded into the output shift register. The DRDY signal transitions from high to low to indicate a new conversion is complete, and the conversion results can be read from the NSAD124x by sending SCLKs. The RDATAC command must be issued after DRDY goes low, and it will take effect on the next DRDY. Ensure that data retrieval (conversion results or register readback) is completed before DRDY returns low again; otherwise, the generated data will be corrupted. In RDATAC mode, a successful register read operation requires knowledge of when the next DRDY falling edge will occur.

In this data retrieval method, ADC conversion data is directly shifted out from the output shift register. No command is required. Direct data reading demands that no serial activity occurs from the falling edge of DRDY until the readback, otherwise the data will be invalid. The serial interface is full-duplex in direct read data mode; this means commands are decoded during data readback. If there are no commands, keep DIN low during the readback. If an input command is sent during readback, the ADC will execute the command, which may cause data corruption. Synchronize the data readback to DRDY or DOUT/DRDY to ensure that data is read before the next DRDY update, or old data is overwritten by new data. As shown in Figure 90, the ADC data field length can be 3, 4, or 5 bytes. The data field consists of an optional STATUS byte, three bytes of conversion data, and an optional CRC byte. After reading all bytes, the data byte sequence (including STATUS and CRC bytes, if selected) will repeat when subsequent SCLKs are sent. The byte sequence repeats from the first byte. To help verify error-free communication, read the same data multiple times within each conversion interval, or use the optional CRC byte.

SDATAC (0001 011x)

The SDATAC command terminates continuous data read mode. In terminated continuous data read mode, when DRDY goes low, the conversion results are not automatically loaded into the output shift register. Instead, the RDATA command is required to retrieve the conversion data, and it will not be interrupted by new conversion results being loaded into the output shift register. If DRDY data conversion is not actively monitored, terminating continuous data read mode is the preferred method for reading data. In this mode, reading ADC data is not interrupted by the completion of a new ADC conversion.

RREG (001r rrrr, 000n nnnn)

The RREG command reads data from a register. The RREG command consists of two bytes. The first command byte is: 001r rrrr, where rrrrr is the address of the first register to be read. The second command byte is: 000n nnnn, where nnnnn-1 is the number of bytes to be read. After receiving the two-byte command, the NSAD124x will return the register values on SDO, with the address incrementing by 1. If the offset address exceeds the last register address, it will remain at the highest address. During the register data readout, the NSAD124x will ignore other commands on DIN, meaning full-duplex communication is disabled. It is recommended to use NOP for data reading from the register.

WREG (010r rrrr, 000n nnnn)

The WREG command writes values to a register. The WREG command consists of two bytes. The first command byte is: 001r rrrr, where rrrrr is the address of the first register to be written. The second command byte is: 000n nnnn, where nnnnn-1 is the number of bytes to be written.

SYSOCAL (0110 0000)

The SYSOCAL command initiates system offset calibration. For system offset calibration, the input is a user-defined zero level. It is necessary to ensure that the analog positive input and analog negative input are within the common-mode input range. Upon completion of the calibration, the OFC register will be updated.

SYSGCAL (0110 0001)

The SYSGCAL command initiates system gain calibration. For system gain calibration, the input is a user-defined full-scale level. Upon completion of the calibration, the FSC register will be updated.

SELFOCAL (0110 0010)

The SELFOCAL command initiates self-offset calibration. The device internally shorts the input to the mid-supply and performs the calibration. Upon completion of the calibration, the OFC register will be updated.

NOP (1111 1111)

This is a No Operation (NOP) command. Upon receiving this command, no operations are performed. The NOP command can be used for reading data and registers.

10. Noise and Resolution

Two significant factors affecting noise performance are data rate and PGA gain. Decreasing the data rate proportionally decreases bandwidth and therefore, total noise. Since the noise of the PGA is lower than that of the modulator of the ADC, increasing the gain reduces noise when treated as an input-referred quantity. Noise performance also depends on the digital filter and chop mode. As the order of the digital filter increases, the noise bandwidth correspondingly decreases resulting in lower noise. Further, as a result of two-point data averaging in chop mode, noise performance improves by √2 compared to normal operation.

The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the effective resolution is calculated using the rms noise, whereas the noise free resolution (shown in parentheses) is calculated based on peak-to-peak noise (shown in parentheses). The peak-to-peak resolution represents the resolution for which there is no code flicker.

$$\text{Effective Resolution} = \text{Log2}((\text{Input Range})/(\text{RMS Noise}))$$

$$\text{NoiseFree Resolution} = \text{Log2}((\text{Input Range})/(\text{PeaktoPeak Noise}))$$

Table 10-1 Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) with Low-Latency Filter at AVDD = 5 V, AVSS = 0 V, Global Chop Disabled, and 2.5-V Reference

Output Data Rate (SPS)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	23.4(20.8)	23.4(20.8)	23.4(20.8)	23.3(20.7)	22.9(20.4)	22.3(19.8)	21.5(18.9)	20.5(17.9)
5	22.9(20.4)	22.9(20.4)	22.9(20.3)	22.8(20.2)	22.5(19.9)	21.8(19.2)	21.0(18.4)	20.0(17.4)
10	22.4(19.9)	22.4(19.9)	22.5(19.9)	22.3(19.7)	22.0(19.4)	21.3(18.7)	20.5(17.9)	19.5(16.9)
16	22.2(19.6)	22.1(19.6)	22.2(19.6)	22.0(19.4)	21.7(19.1)	21.0(18.4)	20.2(17.6)	19.1(16.5)
20	22.0(19.4)	21.9(19.4)	22.0(19.4)	21.8(19.2)	21.4(18.9)	20.8(18.2)	20.0(17.4)	18.9(16.3)
50	21.1(18.5)	21.2(18.6)	21.2(18.7)	21.2(18.5)	20.5(17.8)	19.9(17.3)	19.1(16.5)	18.0(15.4)
60	21.0(18.4)	21.0(18.5)	21.1(18.5)	21.0(18.5)	20.4(17.7)	19.7(17.2)	18.8(16.3)	17.8(15.2)
100	20.6(18.0)	20.5(17.9)	20.6(18.0)	20.6(18.0)	20.1(17.5)	19.3(16.7)	18.6(16.1)	17.5(14.9)
200	19.9(17.3)	19.9(17.3)	19.9(17.3)	19.8(17.3)	19.3(16.7)	18.5(15.9)	18.1(15.5)	17.0(14.4)
400	19.4(16.8)	19.4(16.8)	19.4(16.8)	19.2(16.6)	18.9(16.3)	18.1(15.4)	17.3(14.7)	16.4(13.8)
800	18.9(16.4)	18.9(16.3)	18.8(16.3)	18.7(16.1)	18.4(15.8)	17.6(15.1)	16.9(14.3)	15.9(13.3)
1000	18.7(16.1)	18.6(16.1)	18.6(16.0)	18.4(15.9)	18.1(15.5)	17.4(14.8)	16.6(14.1)	15.6(13.0)
2000	18.3(15.7)	18.3(15.7)	18.1(15.5)	18.0(15.4)	17.3(14.6)	16.4(13.9)	15.6(13.0)	14.6(12.0)
4000	16.8(14.3)	16.8(14.3)	16.8(14.2)	16.5(13.9)	16.1(13.4)	15.1(12.5)	14.3(11.7)	13.2(10.6)

Table 10-2 Noise in µVRMS (µVPP) with Low-Latency Filter, at AVDD = 5 V, AVSS = 0 V, Global Chop Disabled, and 2.5-V Reference

Output Data Rate (SPS)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	0.46(2.7)	0.23(1.4)	0.11(0.67)	0.06(0.37)	0.04(0.23)	0.03(0.18)	0.03(0.16)	0.03(0.16)
5	0.63(3.6)	0.32(1.8)	0.16(0.96)	0.09(0.52)	0.05(0.32)	0.04(0.25)	0.04(0.23)	0.04(0.23)
10	0.88(5.1)	0.44(2.6)	0.22(1.3)	0.12(0.73)	0.08(0.46)	0.06(0.37)	0.05(0.32)	0.05(0.32)
16	1.1(6.4)	0.54(3.2)	0.27(1.6)	0.15(0.89)	0.09(0.57)	0.07(0.44)	0.07(0.4)	0.07(0.41)

20	1.2(7.2)	0.62(3.7)	0.3(1.9)	0.17(1.0)	0.11(0.65)	0.08(0.5)	0.08(0.46)	0.08(0.48)
50	2.3(14)	1.1(6.3)	0.5(3.0)	0.27(1.6)	0.22(1.4)	0.16(0.99)	0.14(0.86)	0.15(0.9)
60	2.4(15)	1.2(6.9)	0.55(3.3)	0.29(1.7)	0.23(1.5)	0.18(1.1)	0.17(0.99)	0.18(1.1)
100	3.2(19)	1.7(10)	0.8(4.8)	0.39(2.3)	0.28(1.7)	0.24(1.4)	0.19(1.2)	0.21(1.3)
200	5.1(30)	2.6(15)	1.3(7.9)	0.66(4.0)	0.48(2.9)	0.42(2.5)	0.29(1.7)	0.31(1.8)
400	7.5(45)	3.7(22)	1.9(11)	1.0(6.2)	0.65(3.9)	0.57(3.5)	0.5(3.0)	0.46(2.7)
800	9.9(59)	5.3(32)	2.7(16)	1.5(8.9)	0.89(5.4)	0.8(4.5)	0.65(3.9)	0.64(3.8)
1000	12(70)	6.1(37)	3.1(18)	1.7(10)	1.1(6.6)	0.91(5.4)	0.76(4.6)	0.77(4.6)
2000	16(96)	7.7(46)	4.4(26)	2.4(15)	2.0(12)	1.8(10)	1.6(9.7)	1.6(9.6)
4000	44(253)	21(128)	11(67)	6.8(41)	4.6(29)	4.4(26)	3.9(24)	4.1(25)

Table 10-3 Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) with Low-Latency Filter at AVDD = 5 V, AVSS = 0 V, Global Chop Enabled, and 2.5-V Reference

Output Data Rate (SPS)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	24.1(21.7)	23.8(20.8)	23.8(21.2)	23.7(21.0)	23.4(21.0)	22.9(20.5)	22.0(19.2)	21.0(18.3)
5	23.2(20.5)	23.3(20.8)	23.3(20.8)	23.4(20.7)	22.9(20.3)	22.4(19.8)	21.4(18.8)	20.4(17.7)
10	22.8(20.1)	23.0(20.4)	23.0(20.4)	22.8(20.1)	22.4(19.8)	21.7(19.1)	20.9(18.3)	20.0(17.3)
16	22.2(19.5)	22.4(19.6)	22.4(19.7)	22.5(20.0)	21.7(19.4)	21.0(18.5)	20.2(17.6)	19.2(16.7)
20	22.6(20.0)	22.6(20.0)	22.5(19.4)	22.4(19.8)	22.0(19.2)	21.3(18.6)	20.5(18.1)	19.4(16.8)
50	22.0(19.1)	21.9(19.2)	21.9(19.4)	21.4(18.9)	21.0(18.5)	20.4(17.8)	19.4(16.9)	18.5(15.9)
60	22.0(19.3)	22.0(19.2)	21.9(19.4)	21.6(18.8)	20.9(18.4)	20.0(17.5)	19.3(16.8)	18.4(15.8)
100	21.8(19.2)	21.8(19.1)	21.8(19.2)	21.3(18.9)	20.8(18.4)	20.0(17.1)	19.0(16.2)	17.9(15.4)
200	21.0(18.4)	21.1(18.3)	21.0(18.4)	20.8(18.1)	20.3(17.5)	19.4(16.9)	18.5(15.7)	17.5(15.0)
400	20.5(18.0)	20.4(17.8)	20.3(17.8)	20.2(17.6)	19.5(16.8)	18.7(16.0)	18.1(15.5)	17.1(14.6)
800	20.1(17.6)	20.0(17.5)	19.9(17.2)	19.6(17.1)	19.1(16.6)	18.3(15.7)	17.4(14.8)	16.4(13.6)
1000	19.9(17.4)	19.8(17.3)	19.7(17.2)	19.4(16.8)	18.8(16.2)	18.0(15.3)	17.2(14.7)	16.2(13.4)
2000	18.8(16.4)	18.7(16.2)	18.6(15.9)	18.0(15.4)	17.5(15.0)	16.8(14.4)	16.0(13.5)	15.0(12.5)
4000	17.5(14.8)	17.4(14.9)	17.2(14.8)	16.6(14.2)	16.3(13.8)	15.5(12.8)	14.7(12.3)	13.7(11.2)

Table 10-4 Noise in µVRMS (µVPP) with Low-Latency Filter, at AVDD = 5 V, AVSS = 0 V, Global Chop Enabled, and 2.5-V Reference

Output Data Rate (SPS)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	0.3(1.8)	0.17(1.0)	0.09(0.53)	0.05(0.27)	0.03(0.17)	0.02(0.12)	0.02(0.11)	0.02(0.11)
5	0.5(3.0)	0.25(1.5)	0.12(0.74)	0.06(0.34)	0.04(0.24)	0.03(0.18)	0.03(0.16)	0.03(0.17)
10	0.67(4.0)	0.29(1.8)	0.15(0.88)	0.08(0.51)	0.06(0.34)	0.05(0.27)	0.04(0.24)	0.04(0.23)
16	0.74(4.5)	0.35(2.1)	0.18(1.1)	0.1(0.59)	0.07(0.41)	0.05(0.32)	0.05(0.28)	0.05(0.29)
20	0.8(4.8)	0.4(2.4)	0.21(1.3)	0.11(0.65)	0.08(0.46)	0.06(0.36)	0.05(0.32)	0.06(0.35)
50	1.1(6.4)	0.57(3.4)	0.27(1.6)	0.17(1.0)	0.13(0.78)	0.11(0.68)	0.12(0.7)	0.11(0.65)
60	1.1(6.8)	0.59(3.5)	0.28(1.7)	0.18(1.1)	0.14(0.83)	0.12(0.72)	0.12(0.73)	0.12(0.7)
100	1.4(8.5)	0.68(4.1)	0.34(2.0)	0.24(1.4)	0.17(1.0)	0.15(0.89)	0.14(0.86)	0.16(0.95)
200	2.4(15)	1.1(6.6)	0.58(3.5)	0.34(2.1)	0.25(1.5)	0.22(1.3)	0.22(1.3)	0.21(1.2)
400	3.4(21)	1.8(11)	0.94(5.7)	0.53(3.2)	0.42(2.5)	0.37(2.2)	0.29(1.7)	0.28(1.7)
800	4.4(26)	2.4(15)	1.3(7.8)	0.8(4.8)	0.57(3.4)	0.49(3.0)	0.45(2.7)	0.45(2.7)
1000	5.3(32)	2.7(16)	1.4(8.6)	0.92(5.5)	0.69(4.1)	0.58(3.5)	0.52(3.1)	0.53(3.2)
2000	11(64)	5.8(35)	3.1(18)	2.3(14)	1.7(9.9)	1.4(8.3)	1.2(7.3)	1.2(7.1)
4000	27(163)	15(88)	8.2(49)	6.1(36)	3.9(23)	3.3(20)	2.9(18)	2.9(17)

Table 10-5 Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) with SINC3 Filter at AVDD = 5 V, AVSS = 0 V, Global Chop Disabled, and 2.5-V Reference

Output Data Rate (SPS)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	23.9(21.3)	23.9(21.3)	24.0(21.4)	23.9(21.3)	23.5(20.9)	22.9(20.3)	22.2(19.6)	21.0(18.5)
5	23.6(21.0)	23.6(21.1)	23.6(21.0)	23.4(20.8)	23.1(20.5)	22.4(19.8)	21.7(19.1)	20.6(18.0)
10	23.1(20.5)	23.1(20.5)	23.0(20.4)	22.9(20.3)	22.6(20.0)	21.9(19.3)	21.1(18.5)	20.2(17.6)
16	22.7(20.1)	22.9(20.3)	22.7(20.2)	22.5(20.0)	22.3(19.7)	21.7(19.2)	20.8(18.2)	19.8(17.2)
20	22.5(19.9)	22.7(20.1)	22.6(20.0)	22.3(19.7)	22.0(19.5)	21.6(19.0)	20.5(18.0)	19.6(17.0)
50	22.0(19.4)	21.9(19.3)	21.9(19.3)	21.8(19.2)	21.4(18.8)	20.8(18.3)	20.0(17.5)	19.0(16.4)
60	21.7(19.1)	21.7(19.1)	21.7(19.1)	21.6(19.0)	21.3(18.7)	20.7(18.1)	19.8(17.2)	18.9(16.3)
100	21.3(18.8)	21.3(18.7)	21.3(18.8)	21.2(18.6)	21.0(18.5)	20.4(17.8)	19.4(16.8)	18.5(15.9)
200	20.5(17.9)	20.6(18.0)	20.5(17.9)	20.6(18.0)	20.3(17.8)	19.8(17.2)	18.9(16.4)	17.9(15.3)
400	19.7(17.1)	19.6(17.0)	19.6(17.0)	19.5(16.9)	19.6(17.0)	19.1(16.5)	18.1(15.5)	17.1(14.6)
800	19.2(16.6)	19.3(16.7)	19.0(16.5)	19.1(16.6)	19.0(16.4)	18.7(16.1)	17.6(15.0)	16.6(14.1)
1000	19.0(16.4)	19.2(16.6)	19.0(16.4)	19.0(16.4)	18.7(16.1)	18.4(15.9)	17.4(14.8)	16.5(13.9)
2000	19.0(16.4)	18.8(16.2)	18.8(16.2)	18.7(16.2)	18.5(15.9)	17.9(15.3)	16.9(14.3)	16.0(13.4)
4000	18.5(15.9)	18.4(15.8)	18.3(15.7)	18.2(15.6)	17.7(15.1)	17.0(14.4)	15.9(13.3)	15.0(12.4)

Table 10-6 Noise in µVRMS (µVPP) with SINC3 Filter, at AVDD = 5 V, AVSS = 0 V, Global Chop Disabled, and 2.5-V Reference

Output Data Rate (SPS)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	0.32(1.9)	0.16(0.98)	0.08(0.46)	0.04(0.24)	0.03(0.16)	0.02(0.12)	0.02(0.1)	0.02(0.11)
5	0.4(2.4)	0.19(1.1)	0.1(0.59)	0.06(0.35)	0.03(0.21)	0.03(0.17)	0.02(0.14)	0.02(0.14)
10	0.56(3.3)	0.27(1.6)	0.15(0.89)	0.08(0.47)	0.05(0.3)	0.04(0.24)	0.03(0.21)	0.03(0.2)
16	0.73(4.4)	0.32(1.9)	0.18(1.1)	0.1(0.61)	0.06(0.37)	0.04(0.27)	0.04(0.26)	0.04(0.26)
20	0.87(5.2)	0.36(2.2)	0.2(1.2)	0.12(0.73)	0.07(0.43)	0.05(0.29)	0.05(0.31)	0.05(0.3)
50	1.2(7.1)	0.63(3.8)	0.31(1.9)	0.17(1.0)	0.11(0.67)	0.08(0.5)	0.07(0.43)	0.08(0.46)
60	1.5(9.1)	0.75(4.5)	0.37(2.2)	0.2(1.2)	0.12(0.72)	0.09(0.54)	0.09(0.52)	0.08(0.47)
100	1.9(11)	0.99(6.0)	0.47(2.8)	0.27(1.6)	0.15(0.87)	0.12(0.7)	0.11(0.66)	0.11(0.64)
200	3.4(20)	1.6(9.5)	0.83(5.0)	0.4(2.4)	0.24(1.4)	0.18(1.1)	0.16(0.93)	0.16(0.96)
400	6.0(36)	3.1(19)	1.6(9.4)	0.85(5.1)	0.4(2.4)	0.27(1.6)	0.28(1.7)	0.27(1.6)
800	8.3(50)	4.0(24)	2.3(14)	1.1(6.5)	0.59(3.6)	0.38(2.3)	0.4(2.4)	0.38(2.3)
1000	9.5(57)	4.2(25)	2.4(14)	1.2(7.4)	0.72(4.3)	0.44(2.6)	0.44(2.6)	0.41(2.5)
2000	9.7(58)	5.5(33)	2.8(17)	1.4(8.5)	0.85(5.1)	0.66(3.9)	0.64(3.9)	0.6(3.6)
4000	14(82)	7.4(45)	3.9(23)	2.1(12)	1.5(9.0)	1.2(7.2)	1.3(7.7)	1.2(7.0)

Table 10-7 Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) with SINC3 Filter at AVDD = 5 V, AVSS = 0 V, Global Chop Enabled, and 2.5-V Reference

Output Data Rate (SPS)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	24.5(21.9)	24.4(21.9)	24.5(22.0)	24.3(21.7)	24.0(21.5)	23.6(21.0)	22.6(20.0)	21.6(19.0)
5	24.1(21.5)	24.1(21.5)	23.9(21.3)	23.8(21.3)	23.6(21.0)	23.0(20.4)	22.2(19.6)	21.0(18.4)
10	23.6(21.0)	23.6(21.0)	23.4(20.8)	23.5(20.9)	23.0(20.4)	22.5(19.9)	21.6(19.0)	20.7(18.1)
16	23.3(20.7)	23.4(20.8)	23.2(20.6)	23.2(20.6)	22.8(20.2)	22.1(19.5)	21.2(18.6)	20.2(17.6)
20	23.2(20.6)	23.1(20.5)	23.0(20.4)	23.1(20.5)	22.6(20.0)	22.0(19.4)	21.1(18.5)	20.0(17.4)
50	22.5(19.9)	22.4(19.9)	22.5(19.9)	22.4(19.8)	22.0(19.4)	21.3(18.7)	20.5(17.9)	19.4(16.8)
60	22.4(19.8)	22.4(19.8)	22.3(19.7)	22.2(19.6)	21.9(19.3)	21.2(18.6)	20.3(17.7)	19.3(16.7)
100	22.0(19.5)	22.1(19.5)	22.0(19.4)	21.8(19.2)	21.5(19.0)	20.9(18.3)	20.0(17.4)	18.8(16.3)
200	21.8(19.3)	21.8(19.3)	21.7(19.1)	21.5(18.9)	21.1(18.6)	20.2(17.6)	19.3(16.8)	18.4(15.8)
400	21.4(18.8)	21.4(18.8)	21.3(18.7)	21.2(18.6)	20.7(18.1)	19.9(17.3)	19.0(16.4)	18.1(15.5)
800	20.7(18.1)	20.6(18.0)	20.7(18.1)	20.4(17.8)	20.0(17.4)	19.2(16.7)	18.6(16.0)	17.5(14.9)
1000	20.5(17.9)	20.4(17.9)	20.5(17.9)	20.2(17.6)	19.8(17.2)	19.0(16.4)	18.3(15.7)	17.4(14.8)
2000	20.1(17.5)	20.1(17.5)	20.0(17.4)	19.7(17.1)	19.2(16.6)	18.4(15.9)	17.5(14.9)	16.6(14.0)
4000	19.5(16.9)	19.5(16.9)	19.5(16.9)	19.0(16.4)	18.4(15.8)	17.4(14.8)	16.6(14.0)	15.6(13.0)

Table 10-8 Noise in μVRMS (μVPP) with SINC3 Filter, at AVDD = 5 V, AVSS = 0 V, Global Chop Enabled, and 2.5-V Reference

Output Data Rate (SPS)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	0.21(1.3)	0.11(0.65)	0.05(0.31)	0.03(0.18)	0.02(0.11)	0.01(0.08)	0.01(0.07)	0.01(0.07)
5	0.28(1.7)	0.14(0.84)	0.08(0.47)	0.04(0.25)	0.03(0.15)	0.02(0.12)	0.02(0.1)	0.02(0.11)
10	0.39(2.3)	0.2(1.2)	0.11(0.67)	0.05(0.32)	0.04(0.22)	0.03(0.15)	0.02(0.15)	0.02(0.14)
16	0.5(3.0)	0.23(1.4)	0.13(0.78)	0.06(0.39)	0.04(0.27)	0.04(0.21)	0.03(0.19)	0.03(0.19)
20	0.52(3.1)	0.27(1.6)	0.15(0.88)	0.07(0.43)	0.05(0.3)	0.04(0.22)	0.04(0.21)	0.04(0.23)
50	0.83(5.0)	0.44(2.6)	0.22(1.3)	0.11(0.68)	0.08(0.46)	0.06(0.37)	0.05(0.32)	0.06(0.33)
60	0.92(5.5)	0.46(2.7)	0.24(1.4)	0.13(0.76)	0.08(0.48)	0.07(0.4)	0.06(0.36)	0.06(0.36)
100	1.2(6.9)	0.57(3.4)	0.3(1.8)	0.17(1.0)	0.1(0.61)	0.08(0.48)	0.08(0.45)	0.08(0.5)
200	1.3(8.0)	0.66(4.0)	0.36(2.2)	0.22(1.3)	0.14(0.81)	0.13(0.78)	0.12(0.71)	0.11(0.69)
400	1.9(11)	0.91(5.5)	0.48(2.9)	0.27(1.6)	0.18(1.1)	0.16(0.96)	0.15(0.88)	0.14(0.84)
800	2.9(17)	1.6(9.6)	0.75(4.5)	0.46(2.7)	0.29(1.8)	0.25(1.5)	0.2(1.2)	0.21(1.3)
1000	3.4(20)	1.8(11)	0.85(5.1)	0.51(3.1)	0.35(2.1)	0.29(1.8)	0.24(1.5)	0.23(1.4)
2000	4.4(26)	2.2(13)	1.2(7.3)	0.75(4.5)	0.52(3.1)	0.44(2.6)	0.42(2.5)	0.39(2.3)
4000	6.7(40)	3.3(20)	1.7(10)	1.2(7.3)	0.92(5.5)	0.9(5.4)	0.79(4.7)	0.79(4.7)

11. Register Map

11.1.NSAD1246 Register Summery

<table>
<tr><th>ADDRESS</th><th>NAME</th><th>BIT 7</th><th>BIT 6</th><th>BIT 5</th><th>BIT 4</th><th>BIT 3</th><th>BIT 2</th><th>BIT 1</th><th>BIT 0</th><th>Reset Value</th></tr>
<tr><td rowspan="2">00h</td><td rowspan="2">MUX IN</td><td colspan="2">R/W</td><td colspan="6">R</td><td rowspan="2">01h</td></tr>
<tr><td colspan="2">BCS[1:0]</td><td colspan="6">RESERVED</td></tr>
<tr><td rowspan="2">01h</td><td rowspan="2">VBIAS</td><td colspan="4">R</td><td colspan="4">R/W</td><td rowspan="2">00h</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">VBIAS[3:0]</td></tr>
<tr><td rowspan="2">02h</td><td rowspan="2">REF CTRL</td><td>R/W</td><td colspan="4">R</td><td colspan="3">R/W</td><td rowspan="2">00h</td></tr>
<tr><td>CLK</td><td colspan="4">RESERVED</td><td colspan="3">MUXCAL[2:0]</td></tr>
<tr><td rowspan="2">03h</td><td rowspan="2">SYS0</td><td>R</td><td colspan="3">R/W</td><td colspan="4">R/W</td><td rowspan="2">04h</td></tr>
<tr><td>RESERVED</td><td colspan="3">PGA[2:0]</td><td colspan="4">DR[3:0]</td></tr>
<tr><td rowspan="2">04h
05h
06h</td><td rowspan="2">OFC0
OFC1
OFC2</td><td colspan="8">R/W</td><td rowspan="2">000000h</td></tr>
<tr><td colspan="8">OFC[7:0]
OFC[15:8]
OFC[23:16]</td></tr>
<tr><td rowspan="2">07h
08h
09h</td><td rowspan="2">FSC0
FSC1
FSC2</td><td colspan="8">R/W</td><td rowspan="2">400000h</td></tr>
<tr><td colspan="8">FSC[7:0]
FSC[15:8]
FSC[23:16]</td></tr>
<tr><td rowspan="2">0Ah</td><td rowspan="2">ID</td><td colspan="4">R</td><td>R/W</td><td colspan="3">R</td><td rowspan="2">10h</td></tr>
<tr><td colspan="4">ID[3:0]</td><td>DRDYMOD</td><td colspan="3">RESERVED</td></tr>
</table>

BCS—Burn-out Current Source Register
address = 00h

Power-On/Reset = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W		R					
BCS[1:0]		RESERVED, always=01h					

Bits	Name	Description
[7:6]	BCS[1:0]	Open Rate Test Current Source Control These bits set the open rate test current source 00: Open-circuit test current source disable (default) 01: Open-circuit test current source enable, 0.5μA 10: Open-circuit test current source enable, 2 μA 11: Open-circuit test current source enable, 10μA
[5:0]	RESERVED	Reserved Bits, always 0h

Bias Voltage Configuration Register (VBIAS)

address = 01h

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R						R/W	
RESERVED, Always=0h						VBIAS[1:0]	

Bits	Name	Description
7:2	RESERVED	Reserved Bits, always 0h
1:0	VBIAS[1:0]	**Internal Bias Voltage Generator Control** The internal bias voltage can be enabled on multiple channels to apply a bias voltage to the AINx channels. When set to 1, the internal bias voltage is applied to AINx. 0: Bias voltage Vbias disabled (default) 1: Bias voltage Vbias applied to AINx (x = 0, 1)

Reference Control Register (REFCTRL)

address = 02h

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W	R				R/W		
CLK	0000				MUXCAL[2:0]		

Bits	Name	Description
7	CLK	**Clock Source Selection** Configure the clock source by selecting either the internal 4.096MHz clock or an external clock source input via the CLK pin. 0: Internal clock source (default) 1: External clock source
[6:3]	RESERVED	Reserved Bits, always 0h
[2:0]	MUXCAL[2:0]	**System Monitoring Function Control** These bits select the system monitoring function. When the system monitoring function is enabled, it overrides the MUX IN, VREFCON, and REFSELT configurations. 000: Normal operation, system monitoring function off (default) 001: Offset calibration, analog inputs disconnected, internally shorted to (AVDD-AVSS)/2 level 010: Gain calibration, analog inputs connected to the reference voltage 011: Temperature measurement, analog inputs connected to the internal temperature sensor 101: (V(REFP) – V(REFN)) / 4 110: Analog power supply monitoring, analog inputs connected to (AVDD – AVSS)/4 111: Digital power supply monitoring, analog inputs connected to (DVDD – DGND)/4

Table 11-1 MUXCAL Settings

MUXCAL[2:0]	PGA Gain Settings	PGA Input Settings	Voltage Reference Settings
000	Set by PGA[2:0] in SYS0 register	Normal Operation	Fixed as V(REFP) – V(REFN)
001	Set by PGA[2:0] in the SYS0 register	Internally shorted to (AVDD-AVSS) /2	
010	Automatically set to 1	Set by REFSELT[1:0] in the REFCTRLR register	
011	Automatically set to 4	Internal Temperature Sensor	
100	Invalid write, ADC output data will not be guaranteed		
101	Automatically set to 1	(V(REFP) – V(REFN)) / 4	
110	Automatically set to 1	(AVDD – AVSS) / 4	
111	Automatically set to 1	(DVDD – DGND) / 4	

System Control Register 0(SYS0)

address = 03h

Power-On/Reset = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R	R/W			R/W			
RESERVED	PGA[2:0]			DR[3:0]			

Bits	Name	Description
7	RESERVED	Reserved bits, always 0h
[6:5]	PGA[2:0]	**PGA Gain Setting** These bits set the gain of the PGA. 000: PGA = 1 (default) 001: PGA = 2 010: PGA = 4 011: PGA = 8 100: PGA = 16 101: PGA = 32 110: PGA = 64 111: PGA = 128
[3:0]	DR[3:0]	**Data Output Rate Setting** These bits set the data output rate of the ADC. 0000: 2.5 SPS 0001: 5 SPS 0010: 10 SPS 0011: 16.6 SPS 0100: 20 SPS**(default)** 0101: 50SPS 0110: 60 SPS 0111: 100 SPS 1000: 200 SPS 1001: 400 SPS 1010: 800 SPS 1011: 1000 SPS 1100: 2000 SPS 1101: 4000 SPS 1110 or 1111: 4000 SPS

Offset Calibration Coefficient Register(OFC)

address = 04h, 05h, 06h

Power-On/Reset = 00h, 00h, 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
OFC[7:0]							
OFC[15:8]							
OFC[23:16]							

Gain Calibration Coefficient Register(FSC)

address = 07h, 08h, 09h

Power-On/Reset = 00h, 00h, 40h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
OFC[7:0]							
OFC[15:8]							
OFC[23:16]							

ID Register(ID)

address = 0Ah

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W	R		
ID[3:0]				DRDYMOD	RESERVED		

Bits	Name	Description
7:4	ID[3:0]	NSAD124x Identification Number 0000: NSAD1249 0001: NSAD1248 0010: NSAD1247 0011: NSAD1246
3	DRDYMOD	DOUT/DRDY Pin Mode Selection This bit sets the functions of the DOUT/DRDY pin. The dedicated DRDY pin always maintains the data-ready function. 0: DOUT/DRDY The pin is for data output function only (default). 1: DOUT/DRDY The pin multiplexes both data output and data ready functions.
2:0	RESERVED	Reserved Always 0

11.2.NSAD1247 Register Summery

ADDRESS	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Reset Value
00h	MUX IN	R/W		R/W			R/W			01h
		BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]			
01h	VBIAS	R				R/W				00h
		RESERVED				VBIAS[3:0]				
02h	MUX REF	R/W	R/W		R/W		R/W			00h
		CLK	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]			
03h	SYS0	R	R/W			R/W				04h
		RESERVED	PGA[2:0]			DR[3:0]				
04h	OFC0	R/W								000000h
		OFC[7:0]								
05h	OFC1	OFC[15:8]								
06h	OFC2	OFC[23:16]								
07h	FSC0	R/W								400000h
		FSC[7:0]								
08h	FSC1	FSC[15:8]								
09h	FSC2	FSC[23:16]								
0Ah	IDAC0	R				R/W	R/W			10h
		ID[3:0]				DRDYMOD	IMAG[2:0]			
0Bh	IDAC1	R/W				R/W				FFh
		I1DIR[3:0]				I2DIR[3:0]				
0Ch	GPIOCFG	R				R/W				00h
		RESERVED				IOCFG[3:0]				
0Dh	GPIODIR	R				R/W				00h
		RESERVED				IODIR[3:0]				
0Eh	GPIODAT	R				R/W				00h
		RESERVED				IODAT[3:0]				

Analog Input Channel Configuration Register(MUXIN)

address = 00h

Power-On/Reset = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W		R/W			R/W		
BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		

Bits	Name	Description
[7:6]	BCS[1:0]	Open-Circuit Test Current Source Control These bits configure the open-circuit test current source: 00: Open-circuit test current source disabled **(default)** 01: Open-circuit test current source enabled,0.5μA 02: Open-circuit test current source enabled,2μA 03: Open-circuit test current source enabled, 10μA
[5:3]	MUX_SP[2:0]	Multiplexer Selection These bits select which analog input is connected to the positive input of the PGA: 000:AIN0 **(default)** 001:AIN1 010:AIN2 011:AIN3
[2:0]	MUX_SN[2:0]	Multiplexer Selection These bits select which analog input is connected to the negative input of the PGA: 000:AIN0 001:AIN1 **(default)** 010:AIN2 011:AIN3

Bias Voltage Configuration Register(VBIAS)

address = 01h

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W			
RESERVED, Always=0h				VBIAS[7:0]			

Bits	Name	Description
7:2	RESERVED	Reserved, always 0
3:0	VBIAS[3:0]	Internal Bias Voltage Generator Control The internal bias voltage can be enabled on multiple channels to load the bias voltage on the AINx channel. When set to 1, the internal bias voltage is loaded onto AINx. 0: Disable bias voltage Vbias (default) 1: Load bias voltage Vbias onto AINx (x = 0, 1, 2, 3)

Reference Control Register(REFCTRL)

address = 02h

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W	R/W		R/W		R/W		
CLK	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		

Bits	Name	Description
7	CLK	Clock Source Selection Configure the clock source to select either the internal 4.096MHz clock or an external clock source input via the CLK pin. 0: Internal clock source **(default)** 1: External clock source
[6:5]	VREFCON[1:0]	Internal Reference Control Control the internal voltage reference by enabling or disabling it permanently or based on the device's state. 00: Internal voltage reference permanently disabled (default) 01: Internal voltage reference permanently enabled 10 or 11: Internal voltage reference enabled in continuous conversion mode and disabled in sleep mode.
[4:3]	REFSELT[1:0]	Reference Voltage Selection Control Select the ADC reference voltage input channel. 00: Select REFP0/REFN0 reference input 01: Select REFP1/REFN1 reference input 10 or 11: Select internal reference
[2:0]	MUXCAL[2:0]	System Monitoring Function Control These bits select the system monitor function. When the system monitor function is enabled, it may override the MUX IN, VREFCON, and REFSELT configurations. 000: Normal operation, system monitoring function disabled (default) 001: Offset calibration, analog input disconnected and internally shorted to (AVDD-AVSS)/2 level 010: Gain calibration, analog input connected to voltage reference 011: Temperature measurement, analog input connected to internal temperature sensor 101: REF0 monitoring, analog input connected to (REFP0 –REFN0)/4 110: Analog power supply monitoring, analog input connected to (AVDD –AVSS)/4 111: Digital power supply monitoring, analog input connected to (DVDD –DGND)/4

Table 11-2 MUXCAL SETTINGS

MUXCAL[2:0]	PGA Gain Settings	PGA Input Settings	Voltage Reference
000	Set by PGA[2:0] in SYS0 Register	Normal Settings	Set by the EFSELT[1:0] bits in the REFCTRLR register.
001	Set by PGA[2:0] in SYS0 Register	Internal short connection to (AVDD-AVSS)/2 level	
010	Automatically set to 1	Set by the EFSELT[1:0] bits in the REFCTRLR register	
011	Automatically set to 4	Internal Temperature Sensor	
101	Automatically set to 1	(V(REFP0) – V(REFN0)) / 4	
110	Automatically set to 1	(AVDD – AVSS) / 4	
111	Automatically set to 1	(DVDD – DGND) / 4	

System Control Register 0(SYS0)

address = 03h

Power-On/Reset = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R	R/W			R/W			
RESERVED	PGA[2:0]			DR[3:0]			

Bits	Name	Description
7	RESERVED	RESERVED
[6:5]	PGA[2:0]	PGA Gain Settings These bits set the gain of the PGA as follows: 000: PGA = 1 (default) 001: PGA = 2 010: PGA = 4 011: PGA = 8 100: PGA = 16 101: PGA = 32 110: PGA = 64 111: PGA = 128
[3:0]	DR[3:0]	Data Output Rate Settings These bits set the data output rate of the ADC as follows: 0000: 2.5 SPS 0001: 5 SPS 0010: 10 SPS 0011: 16.6 SPS 0100: 20 SPS **(default)** 0101: 50 SPS 0110: 60 SPS 0111: 100 SPS 1000: 200 SPS 1001: 400 SPS 1010: 800 SPS 1011: 1000 SPS 1100: 2000 SPS 1101: 4000 SPS 1110 or 1111: 4000 SPS

Offset Calibration Coefficient Register(OFC)

address = 04h, 05h, 06h

Power-On/Reset = 00h, 00h, 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
OFC[7:0]							
OFC[15:8]							
OFC[23:16]							

Gain Calibration Coefficient Register(FSC)

address = 07h, 08h, 09h

Power-On/Reset = 00h, 00h, 40h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
OFC[7:0]							
OFC[15:8]							
OFC[23:16]s							

Excitation Current Control Register 0(IDAC0)

address = 0Ah

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W	R/W		
ID[3:0]				DRDYMOD	IMAG[2:0]		

Bits	Name	Description
[7:4]	ID[3:0]	NSAD124x Identification Number 0000: NSAD1249 0001: NSAD1248 0010: NSAD1247 0011: NSAD1246
3	DRDYMOD	DOUT/DRDY Function Setting This bit configures the DOUT/DRDY function. The dedicated DRDY pin is always used for data ready functionality. 0: DOUT/DRDY pin is used only for data output **(default)** 1: DOUT/DRDY pin is used for both data output and data ready functionality
[2:0]	IMAG[2:0]	Excitation Current Amplitude Setting These bit configurations determine the excitation current value of the IOUT 000: off (default) 001: 50 μA 010: 100 μA 011: 250 μA 100: 500 μA 101: 750 μA 110: 1000 μA 111: 1500 μA

Excitation Current Control Register 1(IDAC1)

address = 0Bh

Power-On/Reset = FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W			
I1DIR[3:0]				I2DIR[3:0]			

Bits	Name	Description
[7:4]	I1DIR[3:0]	IOUT1 Channel Selection Bits for Excitation Current These bit configurations determine the loading pin for IDAC1: 0000: AIN0 0001: AIN1 0010: AIN2 0011: ANI3 111x: Open circuit **(default)**
[3:0]	I2DIR[3:0]	IOUT2 Channel Selection Bits for Excitation Current These bit configurations determine the loading pin for IDAC2: 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 111x: Open circuit **(default)**

GPIO Configuration Register(GPIOCFG)

address = 0Ch

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W			
RESERVED, Always=0h				IOCFG[3:0]			

Bits	Name	Description
7:4	RESERVED	Reserved bits. Always = 00h
3:0	IOCFG[3:0]	IOCFG[3:0]: GPIO[x] Pins configuration 0: GPIO[x] Disabled **(default)** 1: GPIO[x] Enabled

GPIO Direction Register(GPIODIR)

address = 0Dh

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W			
RESERVED, always=0h				IOCFG[3:0]			

Bits	Name	Description
7:4	RESERVED	Reserved bits, always = 00h
3:0	IODIR[3:0]	IODIR[3:0]: GPIO[x] Direction Configure GPIO[x] as input or output 0: GPIO[x] as output **(default)** 1: GPIO[x] as input

GPIO Data Register(GPIODAT)

address = 0Eh

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W			
RESERVED, Always=0h				IOCFG[3:0]			

Bits	Name	Description
7:4	RESERVED	Reserved bits, always = 00h
3:0	GPIODAT[3:0]	IODAT[3:0]: GPIO[x] data Represents the level status of GPIO[x] 0: GPIO[x] is low **(default)** 1: GPIO[x] is high

11.3.NSAD1248 Register Summery

ADDRESS	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Reset Value
00h	MUX IN	R/W		R/W			R/W			01h
		BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]			
01h	VBIAS	R/W								00h
		VBIAS[7:0]								
02h	MUX REF	R/W	R/W		R/W		R/W			00h
		CLK	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]			
03h	SYS0	R	R/W			R/W				04h
		RESERVED	PGA[2:0]			DR[3:0]				
04h 05h 06h	OFC0 OFC1 OFC2	R/W								000000h
		OFC[7:0] OFC[15:8] OFC[23:16]								
07h 08h 09h	FSC0 FSC1 FSC2	R/W								400000h
		FSC[7:0] FSC[15:8] FSC[23:16]								
0Ah	IDAC0	R				R/W	R/W			10h
		ID[3:0]				DRDYMOD	IMAG[2:0]			
0Bh	IDAC1	R/W				R/W				FFh
		I1DIR[3:0]				I2DIR[3:0]				
0Ch	GPIOCFG	R/W								00h
		IOCFG[7:0]								
0Dh	GPIODIR	R/W								00h
		IODIR[7:0]								
0Eh	GPIODAT	R/W								00h
		IODAT[7:0]								

Analog Input Channel Configuration Register (MUXIN)

address = 00h

Power-On/Reset = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W		R/W			R/W		
BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		

Bits	Name	Description
[7:6]	BCS[1:0]	Open Circuit Test Current Source Control These bits are used to set the open circuit test current source. 00: Open circuit test current source disabled **(default)** 01: Open circuit test current source enabled, 0.5μA 10: Open circuit test current source enabled, 2μA 11: Open circuit test current source enabled, 10μA
[5:3]	MUX_SP[2:0]	Multiplexer Selection These bits select which analog input terminal is connected to the positive input terminal of the PGA. 000: AIN0 **(default)** 001: AIN1 010: AIN2 011: AIN3 100: AIN4 101: AIN5 110: AIN6 111: AIN7
[2:0]	MUX_SN[2:0]	Multiplexer Selection These bits select which analog input terminal is connected to the negative input terminal of the PGA. 000: AIN0 001: AIN1 **(default)** 010: AIN2 011: AIN3 100: AIN4 101: AIN5 110: AIN6 111: AIN7

Bias Voltage Configuration Register(VBIAS)

address = 01h

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
VBIAS[7:0]							

Bits	Name	Description
7:0	VBIAS[7:0]	Internal Bias Voltage Generator Control The internal bias voltage can be enabled on multiple channels to load the bias voltage on AINx channels. 0: Bias voltage Vbias disabled (default) 1: Bias voltage Vbias loaded to AINx (x = 0,1,2,3,4,5,6,7)

Reference Control Register(REFCTRL)
address = 02h
Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W	R/W		R/W		R/W		
CLK	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		

Bits	Name	Description
7	CLK	Clock Source Selection Configure the clock source, select either the on-chip 4.096MHz clock or an external clock source input via the CLK pin. 0: Internal clock source **(default)** 1: External clock source
[6:5]	VREFCON[1:0]	Internal Reference Control Control the internal voltage reference, either turning it on or off, or enabling it based on the device state. 00: Internal voltage reference always off **(default)** 01: Internal voltage reference always on 10 or 11: Internal voltage reference enabled in continuous conversion mode, disabled in sleep mode
[4:3]	REFSELT[1:0]	Reference Voltage Selection Control Select the ADC reference voltage input channel. 00: Select REFP0/REFN0 reference input 01: Select REFP1/REFN1 reference input 10 or 11: Select internal reference
[2:0]	MUXCAL[2:0]	System Monitoring Function Control These bits select the system monitor function. When the system monitor function is enabled, it may preempt **MUX IN, VREFCON,** and **REFSELT** configurations. 000: Normal operation, system monitoring function disabled **(default)** 001: Offset calibration, analog input disconnected from input, internally shorted to (AVDD-AVSS)/2 level 010: Gain calibration, analog input connected to voltage reference 011: Temperature measurement, analog input connected to internal temperature sensor 100: REF1 monitoring. Analog input connected to (REFP1 –REFN1)/4 101: REF0 monitoring. Analog input connected to (REFP0 –REFN0)/4 110: Analog power supply monitoring. Analog input connected to (AVDD –AVSS)/4 111: Digital power supply monitoring. Analog input connected to (DVDD –DGND)/4

Table 11-3 MUXCAL SETTINGS

MUXCAL[2:0]	PGA Gain Settings	PGA Input Settings	Voltage Reference Settings
000	Set by the PGA[2:0] configuration in the SYS0 register	Normal operation	The configuration is set by the REFSELT[1:0] in the REFCTRLR register.
001	Set by the PGA[2:0] configuration in the SYS0 register.	Internally shorted to (AVDD-AVSS)/2	
010	Automatically set to 1	V(REFP) – V(REFN)	
011	Automatically set to 4	Internal temperature sensor	
100	Automatically set to 1	(V(REFP1) – V(REFN1)) / 4	
101	Automatically set to 1	(V(REFP0) – V(REFN0)) / 4	
110	Automatically set to 1	(AVDD – AVSS) / 4	
111	Automatically set to 1	(DVDD – DGND) / 4	

System Control Register 0(SYS0)

address = 03h

Power-On/Reset = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R	R/W			R/W			
RESERVED	PGA[2:0]			DR[3:0]			

Bits	Name	Description
7	RESERVED	Reserved bits, always 0h
[6:5]	PGA[2:0]	PGA Gain Settings These bits set the gain of the PGA. 000: PGA = 1 **(default)** 001: PGA = 2 010: PGA = 4 011: PGA = 8 100: PGA = 16 101: PGA = 32 110: PGA = 64 111: PGA = 128
[3:0]	DR[3:0]	Data Output Rate Settings These bits set the data output rate of the ADC. 0000: 2.5 SPS 0001: 5 SPS 0010: 10 SPS 0011: 16.6 SPS 0100: 20 SPS **(default)** 0101: 50 SPS 0110: 60 SPS 0111: 100 SPS 1000: 200 SPS 1001: 400 SPS 1010: 800 SPS 1011: 1000 SPS 1100: 2000 SPS 1101: 4000 SPS 1110 or 1111: 4000 SPS

Offset Calibration Coefficient Register(OFC)

address = 04h, 05h, 06h

Power-On/Reset = 00h, 00h, 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
OFC[7:0]							
OFC[15:8]							
OFC[23:16]							

Gain Calibration Coefficient Register(FSC)

address = 07h, 08h, 09h

Power-On/Reset = 00h, 00h, 40h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
OFC[7:0]							
OFC[15:8]							
OFC[23:16]							

Excitation Current Control Register 0(IDAC0)

address = 0Ah

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W	R/W		
ID[3:0]				DRDYMOD	IMAG[2:0]		

Bits	Name	Description
[7:4]	ID[3:0]	NSAD124x Identification Number 0000: NSAD1249 0001: NSAD1248 0010: NSAD1247 0011: NSAD1246
3	DRDYMOD	This bit sets the DOUT/DRDY function. The dedicated DRDY pin always maintains the data ready function. 0: DOUT/DRDY pin is only for data output function **(default)** 1: DOUT/DRDY pin is multiplexed for both data output and data ready functions.
[2:0]	IMAG[2:0]	Excitation Current Amplitude Settings These bits set the value of the IOUT excitation current. 000: Off **(default)** 001: 50 μA 010: 100 μA 011: 250 μA 100: 500 μA 101: 750 μA 110: 1000 μA 111: 1500 μA

Excitation Current Control Register 1(IDAC1)

address = 0Bh

Power-On/Reset = FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W			
I1DIR[3:0]				I2DIR[3:0]			

Bits	Name	Description
[7:4]	I1DIR[3:0]	IOUT1 Excitation current channel select bits. These bits set load pins for IDAC1. 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 10x0: IEXC1 10x1: IEXC2 1100: AIN10 1101: AIN11 111x: Open circuit **(default)**
[3:0]	I2DIR[3:0]	IOUT1 Excitation current channel select bits. These bits set load pins of IDAC1. 0000: AIN0 0001: AIN1 0010: AIN2 0011: ANI3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 10x0: IEXC1 10x1: IEXC2 1100: AIN10 1101: AIN11 111x: Open circuit **(default)**

GPIO Configuration Register(GPIOCFG)

address = 0Ch

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
IOCFG[7:0]							

Bits	Name	Description
7:0	IOCFG[7:0]	IOCFG[7:0]: GPIO[x] Pin Configuration 0: GPIO[x] Disabled **(default)** 1: GPIO[x] Enabled

GPIO Direction Register(GPIODIR)

address = 0Dh

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
IOCFG[7:0]							

Bits	Name	Description
7:0	IODIR[7:0]	IODIR[7:0]: GPIO[x] Direction Configure GPIO[x] as input or output. 0: GPIO[x] is an output **(default)** 1: GPIO[x] is an input

GPIO Data Register(GPIODAT)

address = 0Eh

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
IOCFG[3:0]							

Bits	Name	Description
7:0	GPIODAT[7:0]	IODAT[7:0]: GPIO[x] Data Represents the level state of GPIO[x]. 0: GPIO[x] is low **(default)** 1: GPIO[x] is high

11.4.NSAD1249 Register Summery

ADDRESS	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Reset Value
00h	BCS	R/W		R						01h
		BCS[1:0]		RESERVED						
01h	VBIAS	R/W								00h
		VBIAS[7:0]								
02h	REFCTRL	R/W	R/W		R/W		R/W			
		CLK	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]			00h
03h	SYS0	R	R/W			R/W				04h
		RESERVED	PGA[2:0]			DR[3:0]				
04h 05h 06h	OFC0 OFC1 OFC2	R/W								000000h
		OFC[7:0] OFC[15:8] OFC[23:16]								
07h 08h 09h	FSC0 FSC1 FSC2	R/W								400000h
		FSC[7:0] FSC[15:8] FSC[23:16]								
0Ah	IDAC0	R				R/W	R/W			x0h
		ID[3:0]				DRDYMOD	IMAG[2:0]			
0Bh	IDAC1	R/W				R/W				FFh
		I1DIR[3:0]				I2DIR[3:0]				
0Ch	GPIOCFG	R/W								00h
		IOCFG[7:0]								
0Dh	GPIODIR	R/W								00h
		IODIR[7:0]								
0Eh	GPIODAT	R/W								00h
		IODAT[7:0]								
0Fh	STATUS	R/W	R	R	R	R	R	R	R	80h
		FL_POR	RDY	FLP_RAILP	FLP_RAILN	FLN_RAILP	FLN_RAILN	FL_REF_L1	FL_REF_L0	
10h	REFMON	R/W		R/W	R/W	R/W			R/W	10h
		FL_REF_EN[1:0]		REFP_BUF	REFN_BUF	DELAY[2:0]			IMAG_EXP	
11h	MUXIN	R/W				R/W				01h
		MUXP[3:0]				MUXN[3:0]				
12h	SYS1	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	00h
		RESERVED	FILTER	VB_LEVEL	G_CHOP	FL_RAIL_EN	TIMEOUT	CRC	SENDSTAT	

Open Circuit Current Configuration Register (BCS)
address = 00h
Power-On/Reset = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W		R					
BCS[1:0]		RESERVED, always=01h					

Bits	Name	Description
7:6	BCS[1:0]	Open Circuit Test Current Source Control, these bits set the open circuit test current source. 00: Open circuit test current source disabled **(default)** 01: Open circuit test current source enabled, 0.5μA 10: Open circuit test current source enabled, 2μA 11: Open circuit test current source enabled, 10μA
5:0	RESERVED	Reserved bits, always = 01h

Bias Voltage Configuration Register(VBIAS)

address = 01h

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
VBIAS[7:0]							

Bits	Name	Description
7:0	VBIAS [7:0]	Internal Bias Voltage Generator Control, the internal bias voltage can be enabled on multiple channels to apply bias voltage to the analog input AINx channels. When set to 1, the internal bias voltage is loaded to AINx. 0: Bias voltage Vbias disabled **(default)** 1: Bias voltage Vbias loaded to AINx (x = 0,1,2,3,4,5,6,7)

Reference Control Register(REFCTRL)

address = 02h

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W	R/W		R/W		R/W		
CLK	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		

Bits	Name	Description
7	CLK	Clock Source Selection Configure the clock source, select either the internal 4.096MHz clock or an external clock source via the CLK pin. 0: Internal clock source **(default)** 1: External clock source
6:5	VREFCON[1:0]	Internal Reference Control Control the internal voltage reference, control the on or off state of the internal voltage reference within the chip, or enable or disable it based on the device state. 00: Internal voltage reference is normally off **(default)** 01: Internal voltage reference is normally on 10 or 11: Internal voltage reference is enabled in continuous conversion mode and disabled in sleep mode
4:3	REFSELT[1:0]	Reference Select Control Select the ADC reference voltage input channel 00: Select REFP0/REFN0 reference input 01: Select REFP1/REFN1 reference input 10 or 11: Select internal reference
2:0	MUXCAL[2:0]	System Monitoring Function Control These bits select the system monitor function. When the system monitor function is enabled, it may preempt MUX IN, VREFCON, and REFSELT configurations. 000: Normal operation, system monitoring function is disabled **(default)** 001: Offset calibration, analog input disconnected from input, internally shorted to (AVDD-AVSS)/2 level 010: Gain calibration, analog input connected to voltage reference 011: Temperature measurement, analog input connected to internal temperature sensor 100: REF1 monitoring. Analog input connected to (REFP1 –REFN1)/4 101: REF0 monitoring. Analog input connected to (REFP0 –REFN0)/4 110: Analog power supply monitoring. Analog input connected to (AVDD –AVSS)/4 111: Digital power supply monitoring. Analog input connected to (DVDD –DGND)/4

Table 11-4 MUXCAL SETTINGS

MUXCAL[2:0]	PGA Gain Settings	PGA Input Settings	Voltage Reference Settings
000	Set by PGA[2:0] in SYS0 Register	Normal operation	Set by EFSELT[1:0] in the REFCTRLR Register

001	Set by PGA[2:0] in the SYS0 Register	Internally shorted to (AVDD-AVSS)/2	
010	Automatically set to 1	V(REFP) – V(REFN)	
011	Automatically set to 4	Internal Temperature Sensor	
100	Automatically set to 1	(V(REFP1) – V(REFN1)) / 4	
101	Automatically set to 1	(V(REFP0) – V(REFN0)) / 4	
110	Automatically set to 1	(AVDD – AVSS) / 4	
111	Automatically set to 1	(DVDD – DGND) / 4	

System Control Register 0(SYS0)
address = 03h
Power-On/Reset = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R	R/W			R/W			
RESERVED	PGA[2:0]			DR[3:0]			

Bits	Name	Description
7	RESERVED	Reserved bits, always = 0
6:5	PGA[2:0]	**The PGA Gain Setting** These bits set the gain of the PGA (Programmable Gain Amplifier). 000: PGA = 1 **(default)** 001: PGA = 2 010: PGA = 4 011: PGA = 8 100: PGA = 16 101: PGA = 32 110: PGA = 64 111: PGA = 128
3:0	DR[3:0]	**The Data Output Rate Setting** These bits set the data output rate of the ADC (Analog-to-Digital Converter). 0000: 2.5 SPS 0001: 5 SPS 0010: 10 SPS 0011: 16.6 SPS 0100: 20 SPS **(default)** 0101: 50SPS 0110: 60 SPS 0111: 100 SPS 1000: 200 SPS 1001: 400 SPS 1010: 800 SPS 1011: 1000 SPS 1100: 2000 SPS 1101: 4000 SPS 1110 or 1111: 4000 SPS

Offset Calibration Coefficient Register (OFC)

address = 04h, 05h, 06h

Power-On/Reset = 00h, 00h, 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
OFC[7:0]							
OFC[15:8]							
OFC[23:16]							

Gain Calibration Coefficient Register (FSC)

address = 07h, 08h, 09h

Power-On/Reset = 00h, 00h, 40h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
OFC[7:0]							
OFC[15:8]							
OFC[23:16]							

Excitation Current Control Register 0(IDAC0)

address = 0Ah

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W	R/W		
ID[3:0]				DRDYMOD	IMAG[2:0]		

Bits	Name	Description
7:4	ID[3:0]	NSAD124x Identification Number 0000: NSAD1249 0001: NSAD1248 0010: NSAD1247 0011: NSAD1246
3	DRDYMOD	This bit sets the DOUT/DRDY function. The dedicated DRDY pin always maintains the data ready function. 0: The DOUT/DRDY pin only has the data output function **(default)** 1: The DOUT/DRDY pin multiplexes the two functions of data output and data ready.
2:0	IMAG[2:0]	Excitation current amplitude setting. These bits set the value of the IOUT excitation current. 000: off **(default)** 001: 50 μA 010: 100μA 011: 250 μA 100: 500 μA 101: 750 μA 110: 1000 μA 111: 1500 μA

Excitation Current Control Register 1(IDAC1)

address = 0Bh

Power-On/Reset = FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R				R/W			
I1DIR[3:0]				I2DIR[3:0]			

Bits	Name	Description
7:4	I1DIR[3:0]	IOUT1 excitation current channel selects bits. These bits set the load pin of IDAC1. 0000: AIN0 0001: AIN1 0010: AIN2 0011: ANI3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000/1010: AIN9 1001/1011: AIN8 1100: AIN10 1101: AIN11 1110/1111: Open circuit**(default)**
3:0	I2DIR[3:0]	IOUT2 excitation current channel selects bits. These bits set the load pin of IDAC2. 0000: AIN0 0001: AIN1 0010: AIN2 0011: ANI3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000/1010: AIN9 1001/1011: AIN8 1100: AIN10 1101: AIN11 1110/1111: Open circuit**(default)**

GPIO Configuration Register (GPIOCFG)

address = 0Ch

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
IOCFG[7:0]							

Bits	Name	Description
7:0	IOCFG[7:0]	IOCFG[7:0]: GPIO[x] Pins Configuration 0: GPIO[x] Disabled**(default)** 1: GPIO[x] Enabled

GPIO Direction Register (GPIODIR)

address = 0Dh

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
IOCFG[7:0]							

Bits	Name	Description
7:0	IODIR[7:0]	IODIR[7:0]: GPIO[x] direction, configure GPIO[x] as input or output 0: GPIO[x] as output **(default)** 1: GPIO[x] as input

GPIO Data Register(GPIODAT)

address = 0Eh

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W							
IOCFG[3:0]							

Bits	Name	Description
7:0	GPIODAT[7:0]	IODAT[7:0]: GPIO[x] data, indicating the corresponding GPIO[x] level status 0: GPIO[x] is low **(default)** 1: GPIO[x] is high

Device Status Register (STATUS)

address = 0Fh

Power-On/Reset = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W	R	R	R	R	R	R	R
FL_POR	RDY	FLP_RAILP	FLP_RAILN	FLN_RAILP	FLN_RAILN	FL_REF_L1	FL_REF_L0

Bits	Name	Description
7	FL_POR	Power-on reset flag, indicating that a power-on reset event has occurred and has not been cleared 0: The POR flag has been cleared by writing 0, and no power-on reset has occurred. 1: The power-on reset event has occurred and has not been cleared. It must be cleared by writing 0 **(default)**
6	$\overline{\text{RDY}}$	RDY: ADC ready flag, indicating that the ADC is ready 0: ADC power-on initialization is complete and ready **(default)** 1: ADC not ready
5	FLP_RAILP	The positive output of PGA is to the AVDD flag. Setting it to 1 indicates that the voltage difference between the negative output terminal of PGA and AVDD is less than 150mV. 0: no error **(default)** 1: The voltage difference between the PGA positive output terminal and AVDD is less than 150mV
4	FLP_RAILN	The positive output of PGA is to the AVSS flag. Setting it to 1 indicates that the voltage difference between the negative output terminal of PGA and AVSS is less than 150mV. 0: no error **(default)** 1: The voltage difference between the PGA negative output terminal and AVSS is less than 150mV
3	FLN_RAILP	PGA negative output terminal to positive power rail flag, set to 1 to indicate that the voltage difference between the PGA negative output terminal and AVDD is less than 150mV 0: no error **(default)** 1: The voltage difference between the PGA negative output terminal and AVDD is less than 150mV
2	FLN_RAILN	PGA negative output to negative power rail flag, set to 1 to indicate that the voltage difference between the PGA negative output and AVSS is less than 150mV 0: no error **(default)** 1: The voltage difference between the PGA negative output terminal and AVSS is less than 150mV
1	FL_REF_L1	Reference voltage monitoring flag, setting it to 1 indicates that the external reference input voltage is less than 1/3*(AVDD – AVSS), which can be used to locate faults such as reference disconnection or floating. 0: Differential reference voltage ≥ 1/3*(AVDD – AVSS) **(default)** 1: Differential reference voltage < 1/3*(AVDD – AVSS)

0	FL_REF_L0	Reference voltage monitoring flag, setting it to 1 indicates that the external reference input voltage is less than 0.3V, which can be used to locate faults such as reference disconnection or floating. 0: Differential reference voltage ≥ 0.3 V **(default)** 1: Differential reference voltage < 0.3 V

Reference Monitoring Configuration Register (REFMON)

address = 10h

Power-On/Reset = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W		R/W	R/W	R/W			R/W
REF_EN[1:0]		$\overline{\text{REFP\_BUF}}$	REFN_BUF	DELAY[2:0]			IMAG_EXP

Bits	Name	Description
[7:6]	REF_EN[1:0]	Reference output monitoring function configuration, enable and configure the reference input monitoring function 00: Disabled **(default)** 01: FL_REF_L0 monitoring enable, threshold is 0.3 V 10: FL_REF_L0 and FL_REF_L1 monitoring enable, Threshold is 0.3 V and 1/3 * (AVDD – AVSS)
5	$\overline{\text{REFP\_BUF}}$	The reference positive input buffer is disabled. Set 1 to disable the reference positive input buffer. It is recommended to disable it when the reference positive input section is close to AVDD-0.1V. 0: enabled **(default)** 1: Disabled
4	$\overline{\text{REFN\_BUF}}$	The reference negative input terminal buffer is disabled. Set 1 to disable the reference negative input terminal buffer. It is recommended to disable the reference negative input terminal when it is close to AVSS+0.1V. 0: enabled 1: Disabled **(default)**
[3:1]	DELAY[2:0]	Programmable delay conversion selection, before the first new conversion, inserts a programmable delay that occurs after changing the ADC configuration, resetting the digital filter and starting a new conversion 000: 14 * tMOD**(default)** 001: 25 * tMOD 010: 64 * tMOD 011: 256 * tMOD 100: 1024 * tMOD 101: 2048 * tMOD 110: 4096 * tMOD 111: 1 * tMOD
0	IMAG_EXP	The excitation current amplitude sets the extension bits. These bits are linked with the IMAG[2:0] bits in the Excitation Current Control Register 0 (IDAC0, 0Ah) to set the value of the IOUT excitation current. When IMAG[2:0] is 001 and IMAG_EXP is set to 1, the IDAC current is 10uA When IMAG[2:0] is 111 and IMAG_EXP is set to 1, the IDAC current is 2000uA IMAG[2:0] = 001 && IMAG_EXP = 1: 10uA IMAG[2:0] = 111 && IMAG_EXP = 1: 2000uA

Analog Input Channel Configuration Register (MUXIN)

address = 11h

Power-On/Reset = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/W				R/W			
MUXP0				MUXN0			

Bits	Name	Description
[7:4]	MUX_SP[3:0]	PGA positive input selection These bits select which analog input of the multiplexer is connected to the PGA positive input. 0000: AIN0**(default)** 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AIN10 1011/11xx: AIN11
[3:0]	MUX_SN[3:0]	PGA negative input selection These bits select which analog input of the multiplexer is connected to the PGA negative input. 0000: AIN0 0001: AIN1**(default)** 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AIN10 1011/11xx: AIN11

System Control Register1(SYS1)

address = 12h

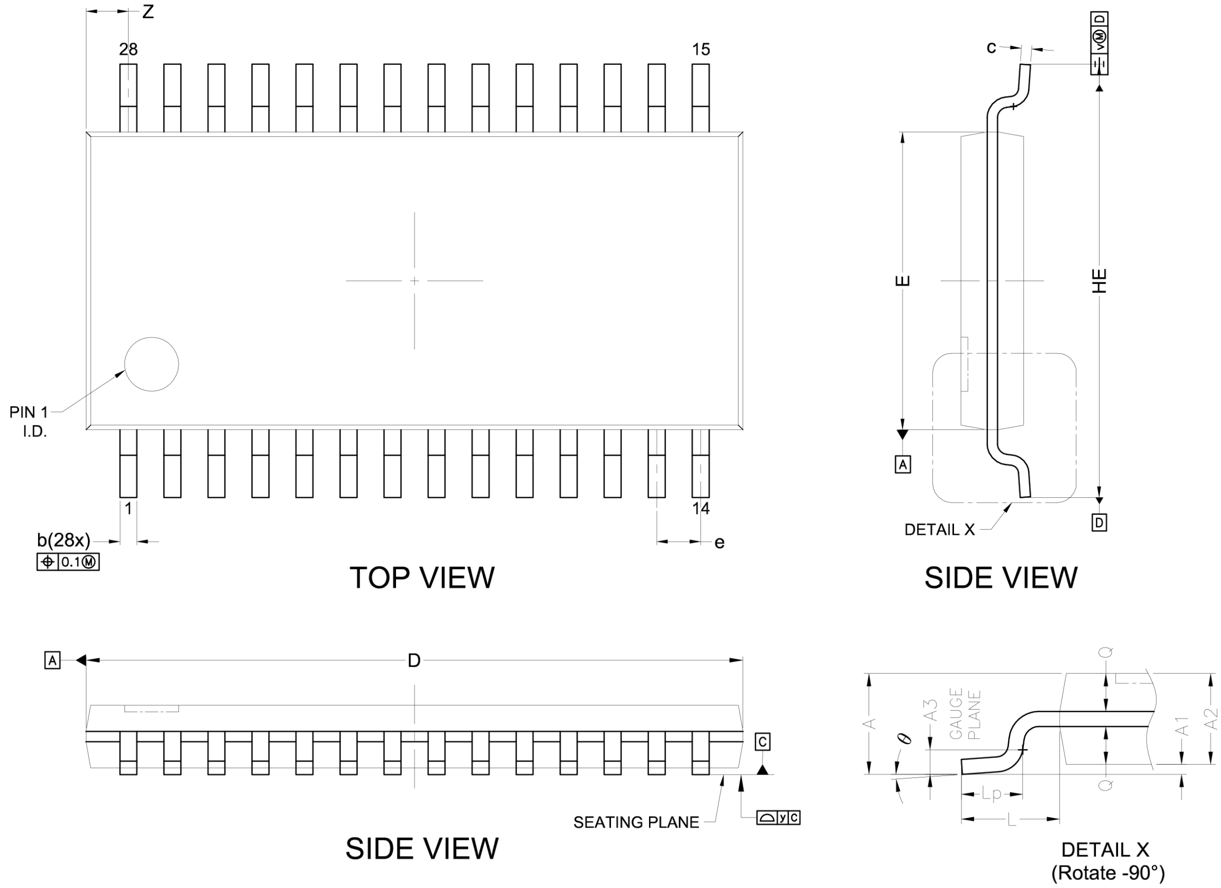
Power-On/Reset = 40h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESERVED	FILTER	VB_LEVEL	G_CHOP	FL_RAIL_EN	TIMEOUT	CRC	SENDSTAT

Bits	Name	Description
7	RESERVED	Reserved bit, always 0
6	FILTER	Digital filter selection Choose ADC to use SINC3 filter or low latency filter 0: SINC3 filter 1: low latency filter **(default)**
5	VB_LEVEL	Select the level of the bias voltage, (AVDD+AVSS)/2 and (AVDD+AVSS)/12 are optional 0: (AVDD + AVSS) / 2 **(default)** 1: (AVDD + AVSS) / 12
4	SYS_CHOP	Select the level of the bias voltage, (AVDD+AVSS)/2 and (AVDD+AVSS)/12 are optional 0 : (AVDD + AVSS) / 2 **(default)** 1: (AVDD + AVSS) / 12
3	FL_RAIL_EN	PGA output to rail monitoring function control, set to 1 to enable 0: Disabled **(default)** 1: enable
2	TIMEOUT	TIMEOUT: SPI timeout function, set to 1 to enable 0: Disabled **(default)** 1: Enable
1	CRC	Enable CRC check. When CRC check is enabled, when reading back 24-bit ADC data, a CRC byte will be added at the end to calculate the CRC of the 24-bit ADC data and STATUS byte (when the SENDSTAT bit is set to 1). 0: Disabled **(default)** 1: Enable
0	SENDSTAT	Enable STATUS. If STATUS is enabled, a STATUS byte will be added before the 24bit ADC data. 0: Disabled **(default)** 1: Enable

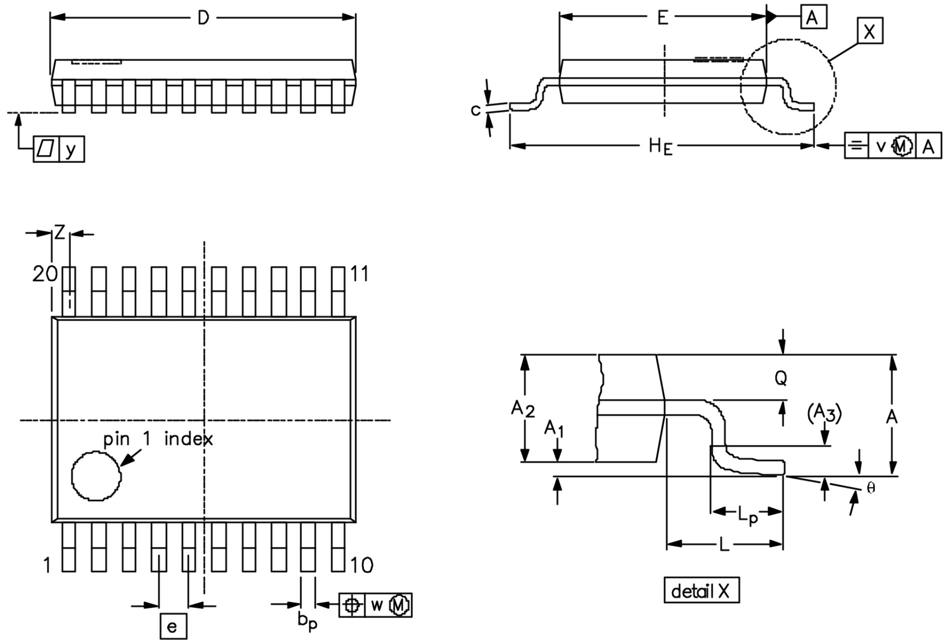
12. Package Information

12.1.TSSOP28



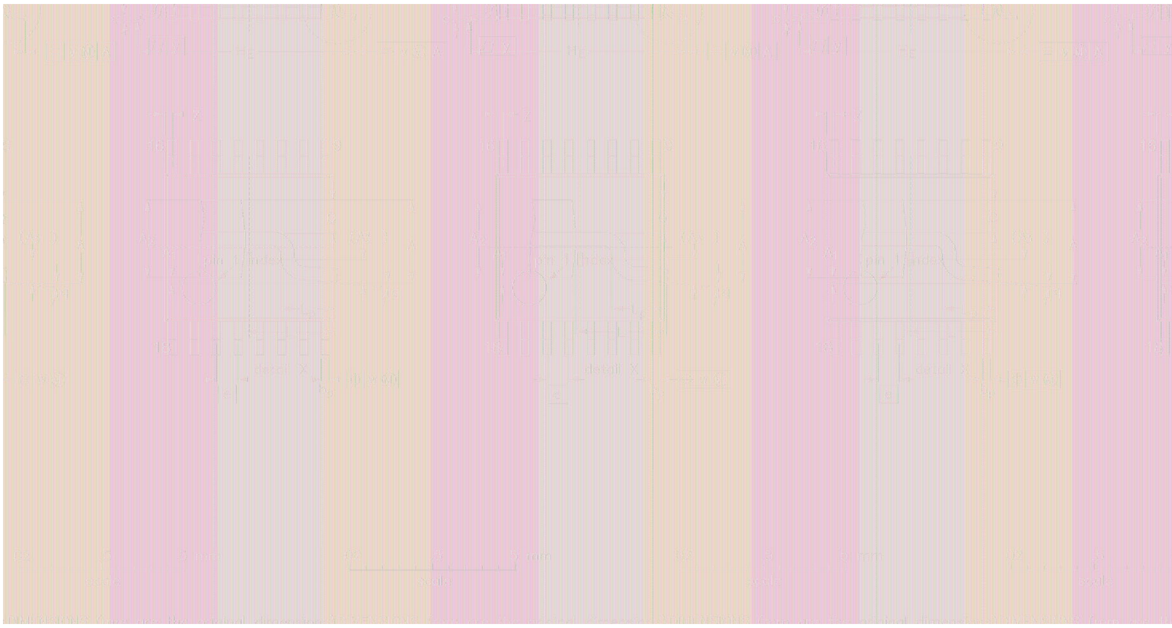
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A		1.2		0.4724
A1	0.05	0.15	0.0197	0.0591
A2	0.85	0.95	0.3346	0.3740
A3	0.25 BSC		0.0984	
b_p	0.19	0.30	0.0748	0.1181
c	0.152 BSC		0.0598	
D	6.4	2.5197	2.5984	2.5984
E	4.3	1.6929	1.7717	1.7717
e	0.65 BSC			
H_E	6.2	2.4409	2.5984	2.5984
L	1.0			
L_P	0.5	0.1969	0.2953	0.2953
Q	0.3	0.1181	0.1614	0.1614
v	0.2		0.0787	
w	0.13		0.0512	
y	0.1		0.0394	
Z	0.625 BSC		0.2461	
θ	0°	8°		

12.2.TSSOP20



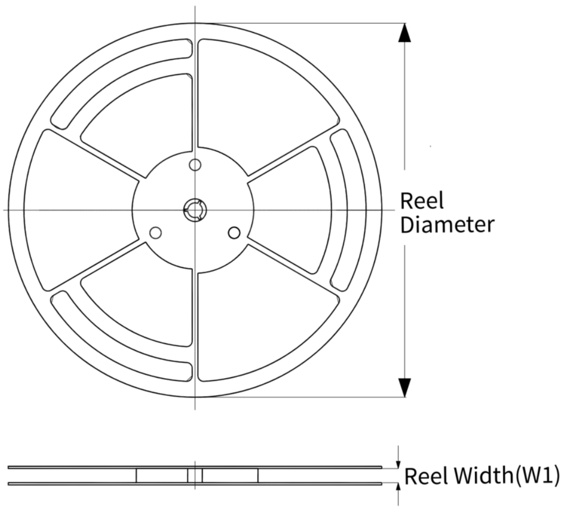
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A		1.1		0.4331
A1	0.05	0.15	0.0197	0.0591
A2	0.80	0.95	0.3150	0.3740
A3	0.25		0.0984	
b_p	0.19	0.30	0.0748	0.1181
c	0.1	0.2	0.0394	0.0787
D	6.4	6.6	2.5197	2.5984
E	4.3	4.5	1.6929	1.7717
e	0.65		2.4409	
H_E	6.2	6.6	0.3937	0.0000
L	1.0		0.1969	
L_P	0.5	0.75	0.1181	0.1575
Q	0.3	0.4	0.0787	0.0000
v	0.2		0.0512	
w	0.13		0.0394	
y	0.1		0.0787	
Z	0.2	0.5	0.0787	0.1969
θ	0°	8°		

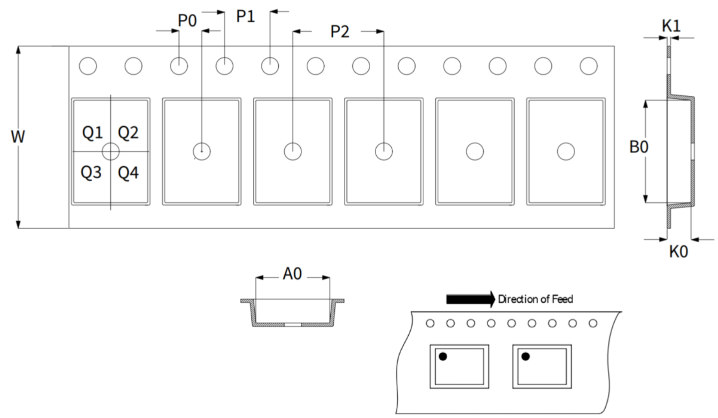
12.1.TSSOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A		1.1		0.4331
A1	0.05	0.15	0.0197	0.0591
A2	0.80	0.95	0.3150	0.3740
A3	0.25		0.0984	
b_p	0.19	0.30	0.0748	0.1181
c	0.1	0.2	0.0394	0.0787
D	4.9	5.1	2.5197	2.5984
E	4.3	4.5	1.6929	1.7717
e	0.65		2.4409	
H_E	6.2	6.6	0.3937	0.0000
L	1.0		0.1969	
L_P	0.5	0.75	0.1181	0.1575
Q	0.3	0.4	0.0787	0.0000
v	0.2		0.0512	
w	0.13		0.0394	
y	0.1		0.0787	
Z	0.2	0.5	0.0787	0.1969
θ	0°	8°		

13. Tape and Reel Information





Device	Reel Diameter	Reel Width(W1)	W	A0	B0	P0	P1	P2	K0	K1	PIN1 Quadrant
NSAD1249-DTSAR	330	24.4	24	6.75	10.3	2.0	4.0	8.0	1.4	0.3	Q1
NSAD1248-DTSAR	330	24.4	24	6.75	10.3	2.0	4.0	8.0	1.4	0.3	Q1
NSAD1247-DTSR	330	16.4	16	6.95	7.1	2.0	4.0	8.0	1.6	0.3	Q1
NSAD1246-DTSPR	330	12.4	12	6.9	5.6	2.0	4.0	8.0	11.6	0.3	Q1

14. Ordering Information

Product Number	Package	MSL Level	Op Temp (°C)	SPQ
NSAD1249-DTSAR	TSSOP28	1	-40 ~ +125	2500
NSAD1248-DTSAR	TSSOP28	1	-40 ~ +125	2500
NSAD1247-DTSR	TSSOP20	1	-40 ~ +125	2500
NSAD1246-DTSPR	TSSOP16	1	-40 ~ +125	2500
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.				

15. Revision History

Revision	Description	Date
V0.1	First draft completed	2023/12
V1.0	Initial version	2024/09

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