

Product Overview

The NLC530x devices are single-channel multipoint low voltage differential signaling (MLVDS) transceivers. The NLC5301/NLC5302 can support 100Mbps data rate and the NLC5303/NLC5304 can operate at signaling rates up to 200Mbps.

The device is compatible with the M-LVDS standard TIA/EIA-899 and combines a differential driver and a differential receiver. Additionally, the NLC530x devices support type1 and type2 receiver input, NLC5301 and NLC5303 are type1 receiver input while NLC5302 and NLC5304 are type2 receiver input.

Controlled edge rates, tight input receiver thresholds and increased drive capability are some of the key enhancements that make MLVDS device an ideal choice for distributing signals via multipoint networks. The NLC530x devices accept LVTTTL signals at the driver inputs and convert them to differential MLVDS signals. The receiver inputs accept low voltage differential signals and convert them to LVCOMS signals.

Key Features

- Fully compatible with the TIA/EIA-899 standard
- Support 100Mbps and 200Mbps signaling rates
- Power supply voltage: 3V to 3.6V
- Type-1 receiver with a Hysteresis of 25mV
- Type-2 receiver with an offset Threshold of 100mV
- Wide common mode voltage input: -1V to 3.4V
- Bus I/O Protection:
 - meet $\pm 8\text{kV}$ HBM
 - meet $\pm 8\text{kV}$ IEC 61000-4-2 contact discharge

- Operation temperature: $-40^{\circ}\text{C} \sim 105^{\circ}\text{C}$
- RoHS & REACH compliant package: SOP 8

Applications

- Cellular base stations
- Backplane or cabled multipoint data and clock transmission
- Network switches and routers

Device Information

Part Number	Function Description	Package	Body Size
NLC5301-DSPR	100Mbps & Type1	SOP8	4.90× 3.90mm
NLC5302-DSPR	100Mbps & Type2	SOP8	4.90 × 3.90mm
NLC5303-DSPR	200Mbps & Type1	SOP8	4.90 × 3.90mm
NLC5304-DSPR	200Mbps & Type2	SOP8	4.90 × 3.90mm

Functional Block Diagrams

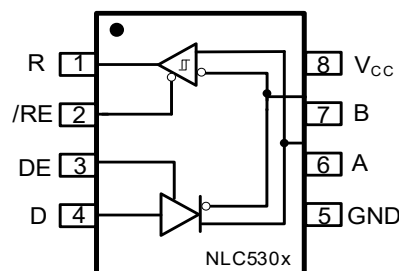


Figure 1. NLC530x Block Diagram

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1. Pin Configuration and Functions

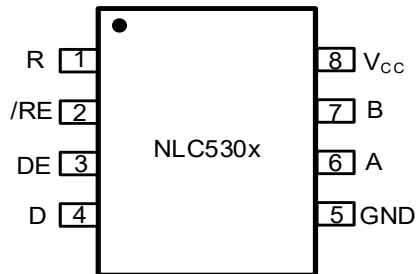


Figure 1.1 NLC530x Package

Table 1.1 NLC530x Pin Configuration and Description

<i>NLC530x Pin No.</i>	<i>Symbol</i>	<i>Function</i>
1	R	Receiver output
2	/RE	Receiver enable input, active low
3	DE	Driver enable input, active high
4	D	Driver input
5	GND	Ground
6	A	Differential output for driver and differential input for receiver
7	B	Differential output for driver and differential input for receiver
8	V _{CC}	Power supply

2. Absolute Maximum Ratings

<i>Parameters</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Comments</i>
Power Supply Voltage	V _{CC}	-0.3		4	V	
Control Input Voltage	/RE, DE	-0.3		V _{CC} +0.3	V	
Driver Input Voltage	D	-0.3		V _{CC} +0.3	V	
Output Voltage	A, B	-1.8		4	V	
Receiver Output Voltage	R	-0.3		V _{CC} +0.3	kV/us	
Storage Temperature	T _{stg}	-65		150	°C	

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD		
	● A, B	±8.0	kV
	● All pins except A, B	±4.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB		
	● All pins	±1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	V_{CC}	3	3.3	3.6	V	
Operating Temperature	T_{opr}	-40		105	°C	
High Level Input Voltage	V_{IH}	2		V_{CC}	V	
Low Level Input Voltage	V_{IL}	0		0.8	V	
Voltage at any bus pin	V_{bus}	-40		125	V	
Common mode voltage at bus	V_{CM}	-1		3.4	V	
Magnitude of differential input voltage	$ V_{ID} $			V_{CC}	V	
Data rate	DR			100	Mbps	NLC5301, NLC5302
				200		NLC5303, NLC5304

5. Thermal Information

Parameters	Symbol	SOP8	Unit
Junction-to-ambient thermal resistance	θ_{JA}	98.9	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC (top)}$	49.8	°C/W
Junction-to-board thermal resistance	θ_{JB}	44.5	°C/W

6. Specifications

6.1. Electrical Characteristics

($V_{CC}=3V\sim 3.6V$, $T_a=-40^{\circ}C$ to $105^{\circ}C$. Unless otherwise noted, Typical values are at $V_{CC}= 3.3V$, $T_a = 25^{\circ}C$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage	V _{CC}	3	3.3	3.6	V	
Supply current	I _{CC}		15	22	mA	/RE and DE at V _{CC} , R _L = 50 Ω, All others open
			2.4	5	mA	/RE at V _{CC} , DE at 0 V, R _L = No Load, All others open
			16	24	mA	/RE at 0 V, DE at V _{CC} , R _L = 50 Ω, All others open
			4	13	mA	/RE at 0 V, DE at 0 V, All others open
Driver						
Differential output voltage magnitude	V _{AB}	480		650	mV	R _L = 50Ω, C _L = 5pF See Figure 6.2
Change in differential output voltage magnitude between logic states	ΔV _{AB}	-50		50	mV	
Steady-state common-mode output voltage	V _{OS(SS)}	0.8		1.2	V	R _L = 50Ω, C _L = 5pF; See Figure 6.3
Change in steady-state common-mode output voltage between logic states	ΔV _{OS(SS)}	-50		50	mV	
Peak-to-peak common-mode output voltage	V _{OS(PP)}			150	mV	
Maximum steady-state open-circuit output voltage	V _{A(OC)}	0		2.4	V	See Figure 6.7
Maximum steady-state open-circuit output voltage	V _{B(OC)}	0		2.4	V	
Voltage overshoot, low-to-high level output	V _{PH}			1.2V _{SS}	V	
Voltage overshoot, high-to-low level output	V _{PL}	-0.2V _{SS}			V	
High-level input current (D、DE)	I _{IH}	-15		15	μA	V _{IH} = 2.0V to V _{CC}
Low-level input current (D、DE)	I _{IL}	-15		15	μA	V _{IL} =GND to 0.8V
Differential short-circuit output current	I _{os}	-30		30	mA	See Figure 6.4
Receiver						

Positive-going differential input voltage threshold	V_{IT+}			50	mV	Type 1
				150	mV	Type 2
Negative-going differential input voltage threshold	V_{IT-}	-50				Type 1
		50				Type 2
Differential input voltage hysteresis	V_{HYS}		25		mV	Type 1
			0		mV	Type 2
High-level output voltage (R)	V_{OH}	2.4			V	$I_{OH}=-8mA$
Low-level output voltage (R)	V_{OL}			0.4	V	$I_{OL}=8mA$
High-level input current (/RE)	I_{IH}	-10			μA	$V_{IH} = 2.0V$ to V_{CC}
Low-level input current (/RE)	I_{IL}	-10			μA	$V_{IL} = GND$ to $0.8V$
TRI-STATE output current (R)	I_{OZ}	-10		15	μA	$V_O = 0V$ or $3.6V$
Bus (Input and Output) Pins-Pin A and Pin B						
High-impedance state current	I_{OZ}	-32		32	μA	$V_A/V_B = -1.4\sim 3.8V$, other pin = $1.2V$
Power-off current	$I_{O(OFF)}$	-34		34	μA	$-1.4 V \leq (V_A \text{ or } V_B) \leq 3.8 V$, Other pin = $1.2 V$, $0 V \leq V_{CC} \leq 1.5 V$
Output capacitance	C_A or C_B		9		pF	$V_I = 0.4 \sin(30E6\pi t) + 0.5V$, Other input at $1.2 V$, driver disabled
Differential output capacitance	C_{AB}		5.7		pF	$V_{AB} = 0.4 \sin(30E6\pi t) V$ driver disabled
Output capacitance balance, (C_A/C_B)	$C_{A/B}$	0.98		1.02	pF	Guarantee by design

6.2. Switching Characteristics

($V_{CC}=3V\sim 3.6V$, $T_a=-40^{\circ}C$ to $105^{\circ}C$. Unless otherwise noted, Typical values are at $V_{CC} = 3.3V$, $T_a = 25^{\circ}C$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Driver						
Differential Propagation Delay Low to High	t_{PLH}	1.3		7	ns	See Figure 6.5
Differential Propagation Delay High to Low	t_{PHL}	1.3		7	ns	
Pulse Skew ($ t_{PHL}-t_{PLH} $)	$t_{sk(P)}$		0.4	0.8	ns	

Part-to-Part Skew	$t_{sk(PP)}^{(1)}$			1.3	ns	See Figure 6.6
Rise Time	t_r	1		3	ns	
Fall Time	t_f	1		3	ns	
Enable Time (Z to Active High)	t_{PZH}		8	12	ns	
Enable Time (Z to Active Low)	t_{PZL}		8	12	ns	See Figure 6.6
Disable Time (Active Low to Z)	t_{PLZ}		8	12	ns	
Disable Time (Active High to Z)	t_{PHZ}		8	12	ns	
Period jitter, rms	$t_{jit(per)}^{(1)}$		3	4	ps	50-MHz clock input
Receiver						
Differential Propagation Delay Low to High	t_{PLH}	2		6	ns	See Figure 6.8
Differential Propagation Delay High to Low	t_{PHL}	2		6	ns	
Pulse Skew ($ t_{PHL} - t_{PLH} $)	$t_{sk(P)}$		0.4	0.8	ns	
Part-to-Part Skew	$t_{sk(PP)}^{(1)}$			1.3	ns	
Rise Time	t_r	0.5		2.5	ns	See Figure 6.9
Fall Time	t_f	0.5		2.5	ns	
Enable Time (Z to Active High)	t_{PZH}		4.5	6	ns	
Enable Time (Z to Active Low)	t_{PZL}		4.5	6	ns	
Disable Time (Active Low to Z)	t_{PLZ}		4.5	6	ns	
Disable Time (Active High to Z)	t_{PHZ}		4.5	6	ns	
Period jitter, rms	$t_{jit(per)}^{(1)}$		5	8	ps	50-MHz clock input

⁽¹⁾ Not test covered, guaranteed by design.

6.3. Parameter Measurement Information

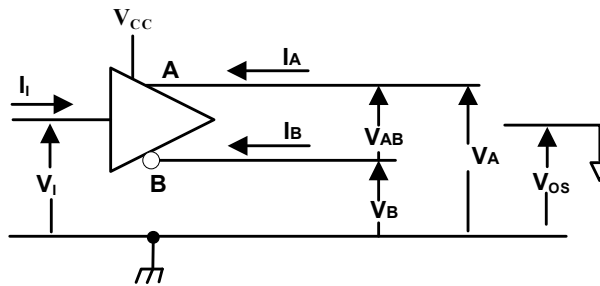
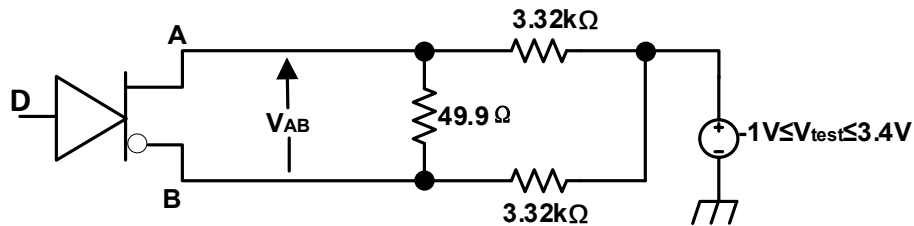
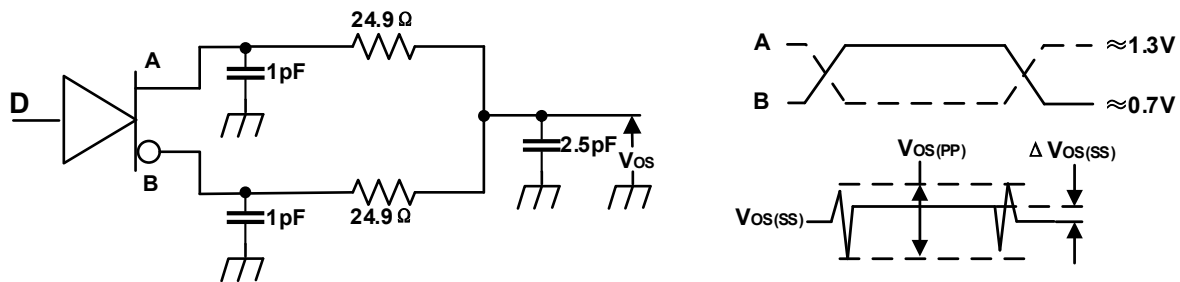


Figure 6.1 Driver Voltage and Current Definitions



- 1) All resistors are 1% tolerance.

Figure 6.2 Differential Output Voltage Test Circuit



- 1) C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- 2) R1 and R2 are metal film, surface mount, $\pm 1\%$, and located within 2 cm of the D.U.T.
- 3) The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

[Figure 6.3 Test Circuit and Definitions for the Driver Common-Mode Output Voltage](#)

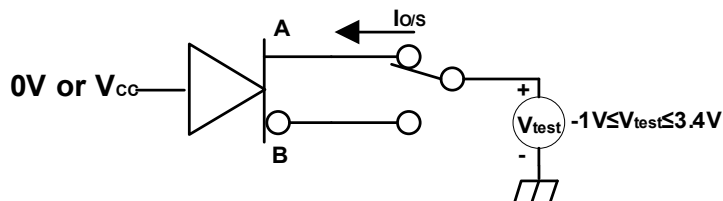
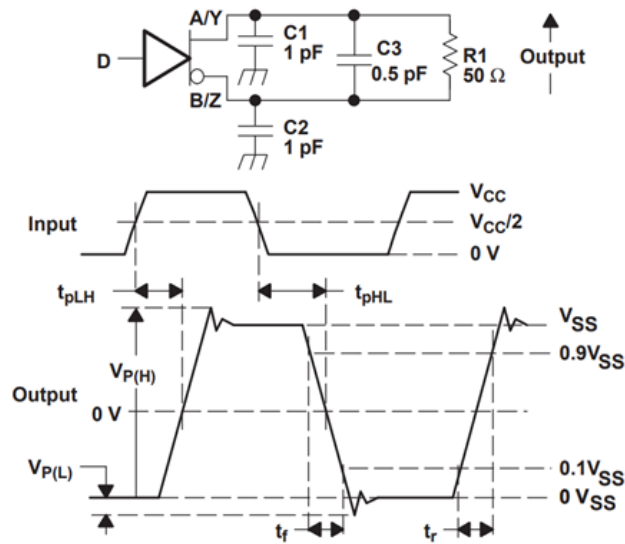
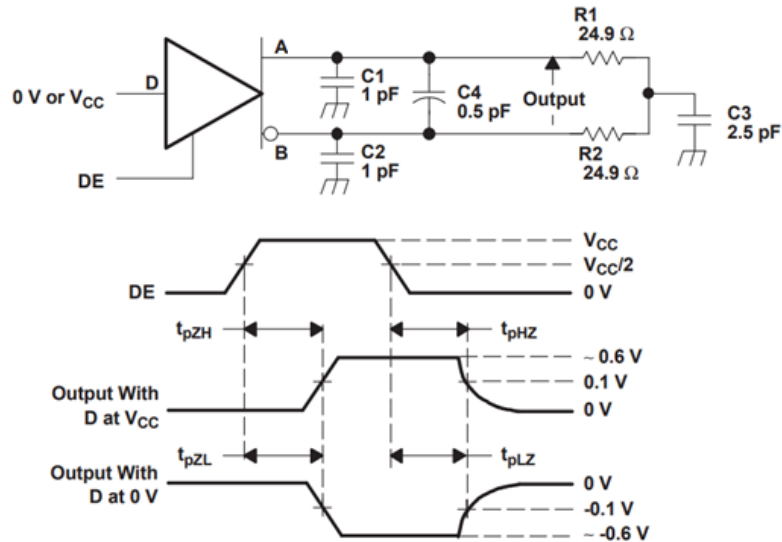


Figure 6.4 Driver Short-Circuit Test Circuit



- 1) C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- 2) R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- 3) The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 6.5 Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal.



- 1) C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- 2) R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- 3) The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 6.6 Driver Enable and Disable Time Circuit and Definitions

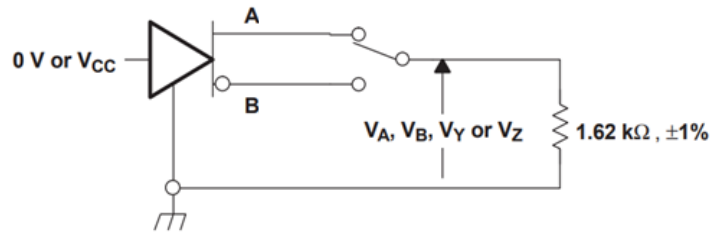
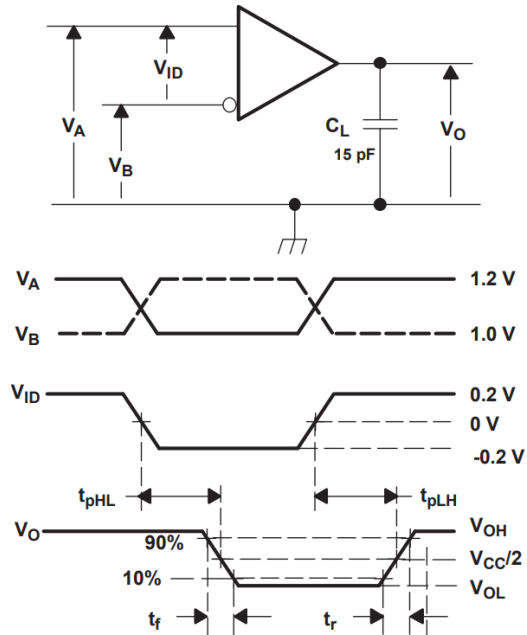


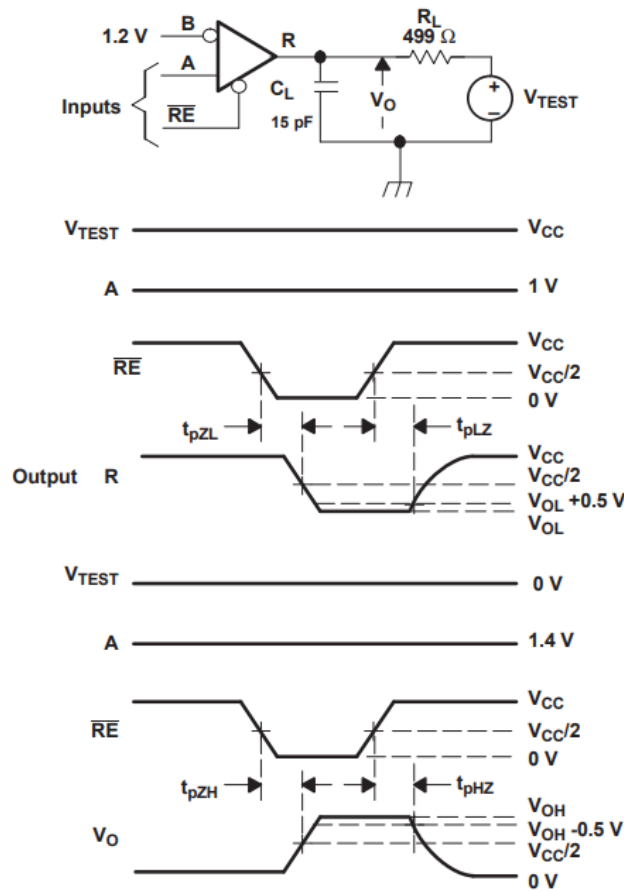
Figure 6.7 Maximum Steady State Output Voltage



1) All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.

2) The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 6.8 Receiver Timing Test Circuit and Waveforms



- 1) All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- 2) R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- 3) C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and $\pm 20\%$.

Figure 6.9 Receiver Enable and Disable Time Test Circuit and Waveforms

7. Function Description

7.1. Overview

The NLC530x devices are single-channel multipoint low voltage differential signaling (MLVDS) transceivers. The 5301/5302 can support 100Mbps data rate and the 5303/5304 can operate at signaling rates up to 200Mbps. The device is compatible with the M-LVDS standard TIA/EIA-899 and combines a differential driver and a differential receiver.

The NLC530x devices accept LVTTTL signals at the driver inputs and convert them to differential MLVDS signals. The receiver inputs accept low voltage differential signals and convert them to LVCOMS signals. The NLC530x devices support Type-1 and Type-2 receiver input with 50 mV (for Type-1) or 150 mV (for Type-2) of differential input voltage detection. Additionally, the NLC530x devices support a wide common-mode voltage range of -1 V to 3.4 V.

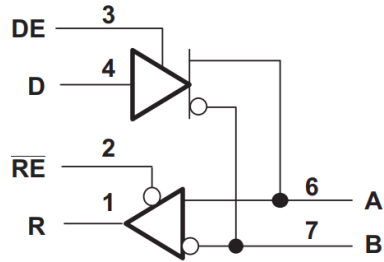


Figure7.1 Logic Diagrams

7.2. FUNCTION TABLES

Table 7.1 NLC530x Function Table-Driver

V_{CC}	DE	D	A	B	<i>Comment</i>
Ready	H ⁽¹⁾	H	H	L	Driver Normal operation
Ready	H	L	L	H	
Ready	L	X	Z	Z	Driver Disabled, the output is high impedance
Unready	X	X	Z	Z	Unpowered, the output is high impedance

(1) L=Logic low; H=Logic high; X=Logic low or logic high.

Table 6.2 NLC530x Function Table-Receiver (Type1)

V_{CC}	$/RE$	$V_{ID}=V_A-V_B$	R	<i>Comment</i>
Ready	L	$\geq 50\text{mV}$	H	Receiver Normal operation
Ready	L	$\leq -50\text{mV}$	L	
Ready	L	$-50\text{mV} \leq V_{ID} \leq 50\text{mV}$	? ⁽¹⁾	
Ready	H	X	Z	Receiver Disabled, the output is high impedance
Unready	X	X	Z	Unpowered, the output is high impedance

(1) '?' — Indeterminate state.

Table 6.3 NLC530x Function Table-Receiver (Type2)

V_{CC}	$/RE$	$V_{ID}=V_A-V_B$	R	<i>Comment</i>
Ready	L	$\geq 150\text{mV}$	H	Receiver Normal operation
Ready	L	$\leq 50\text{mV}$	L	
Ready	L	$50\text{mV} \leq V_{ID} \leq 150\text{mV}$	? ⁽¹⁾	
Ready	H	X	Z	Receiver Disabled, the output is high impedance
Unready	X	X	Z	Unpowered, the output is high impedance

(1) '?' — Indeterminate state.

8. Package Information

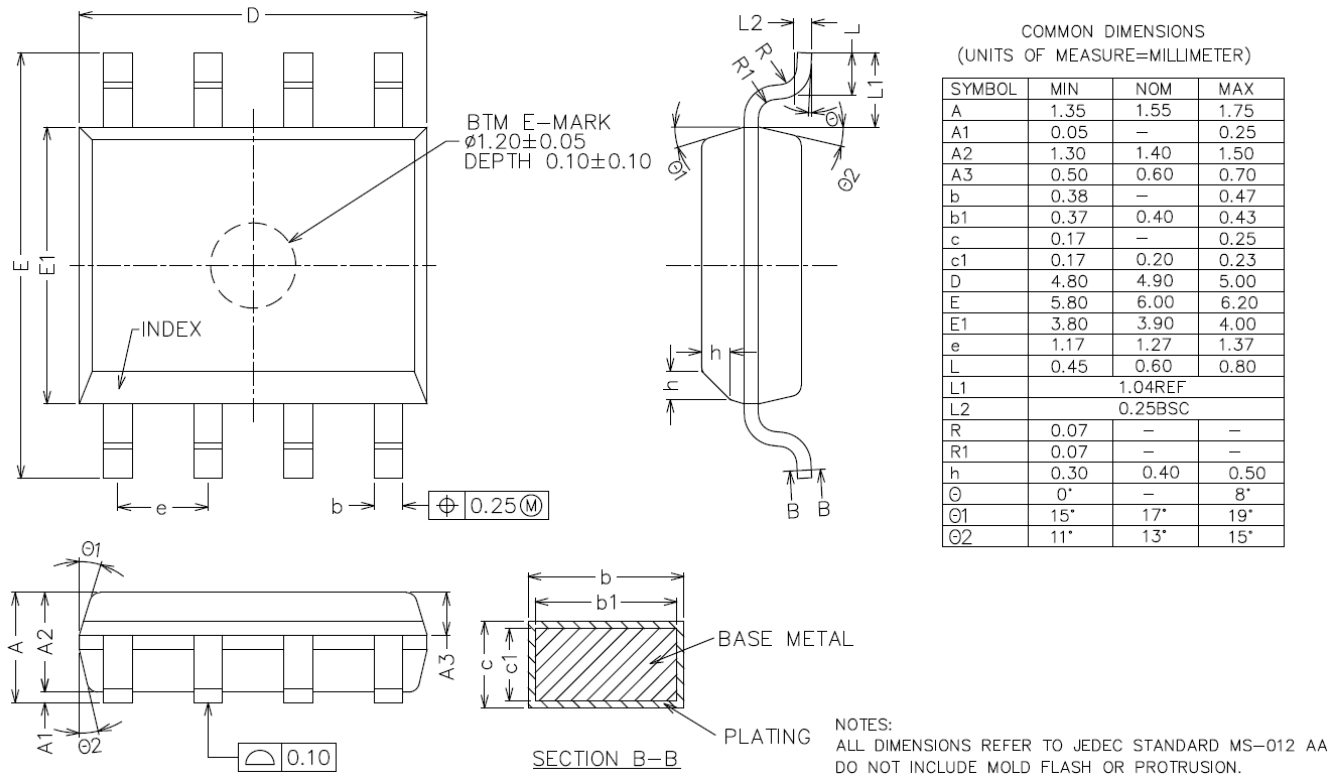
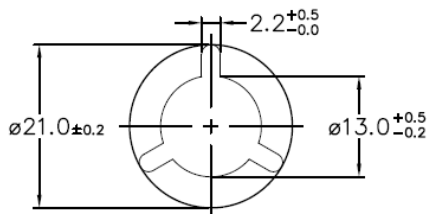
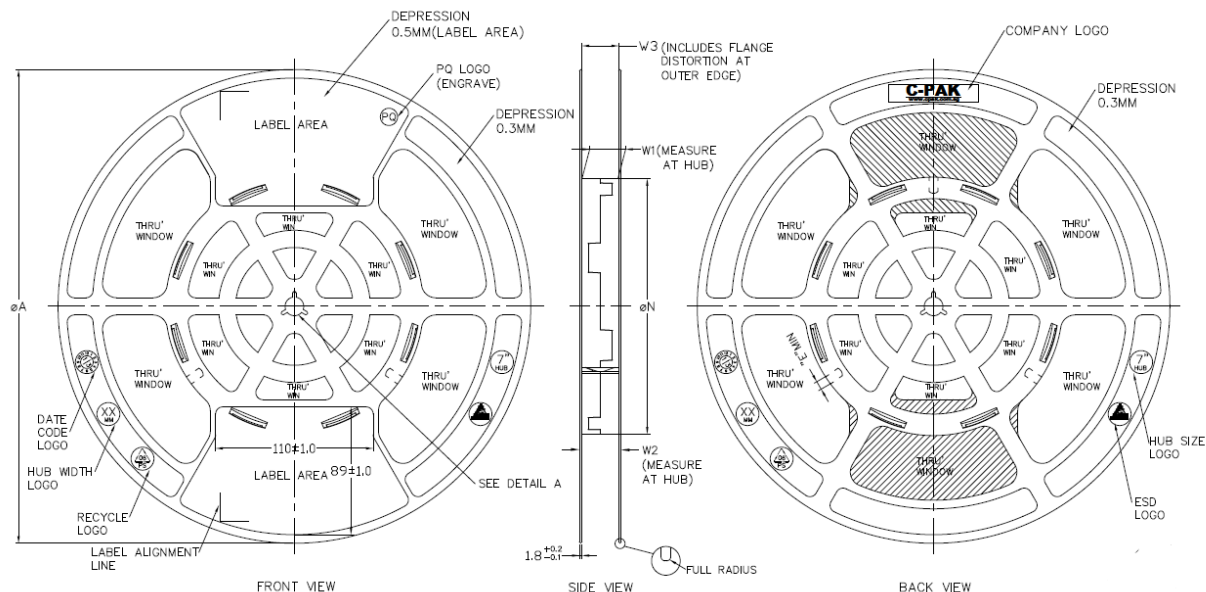


Figure 8.1 SOP8 Package Shape and Dimension in millimeters

9. Ordering Information

Orderable Part	SPQ	Package Type Pins	Operating Temp	MSL
NLC5301-DSPR	2500	SOP-8	-40 to 105°C	1
NLC5302-DSPR	2500	SOP-8	-40 to 105°C	1
NLC5303-DSPR	2500	SOP-8	-40 to 105°C	1
NLC5304-DSPR	2500	SOP-8	-40 to 105°C	1

10. Tape and Reel Information



ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION

TAPE WIDTH	$\phi A \pm 2.0$	$\phi N \pm 2.0$	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 $\pm^{+0.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 $\pm^{+0.5}_{-0.0}$	18.4		5.5
16MM	330	178	16.4 $\pm^{+0.5}_{-0.0}$	22.4		5.5
24MM	330	178	24.4 $\pm^{+0.5}_{-0.0}$	30.4		5.5
32MM	330	178	32.4 $\pm^{+0.5}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY

LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^6 TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^5 & BELOW 10^5	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^8 TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

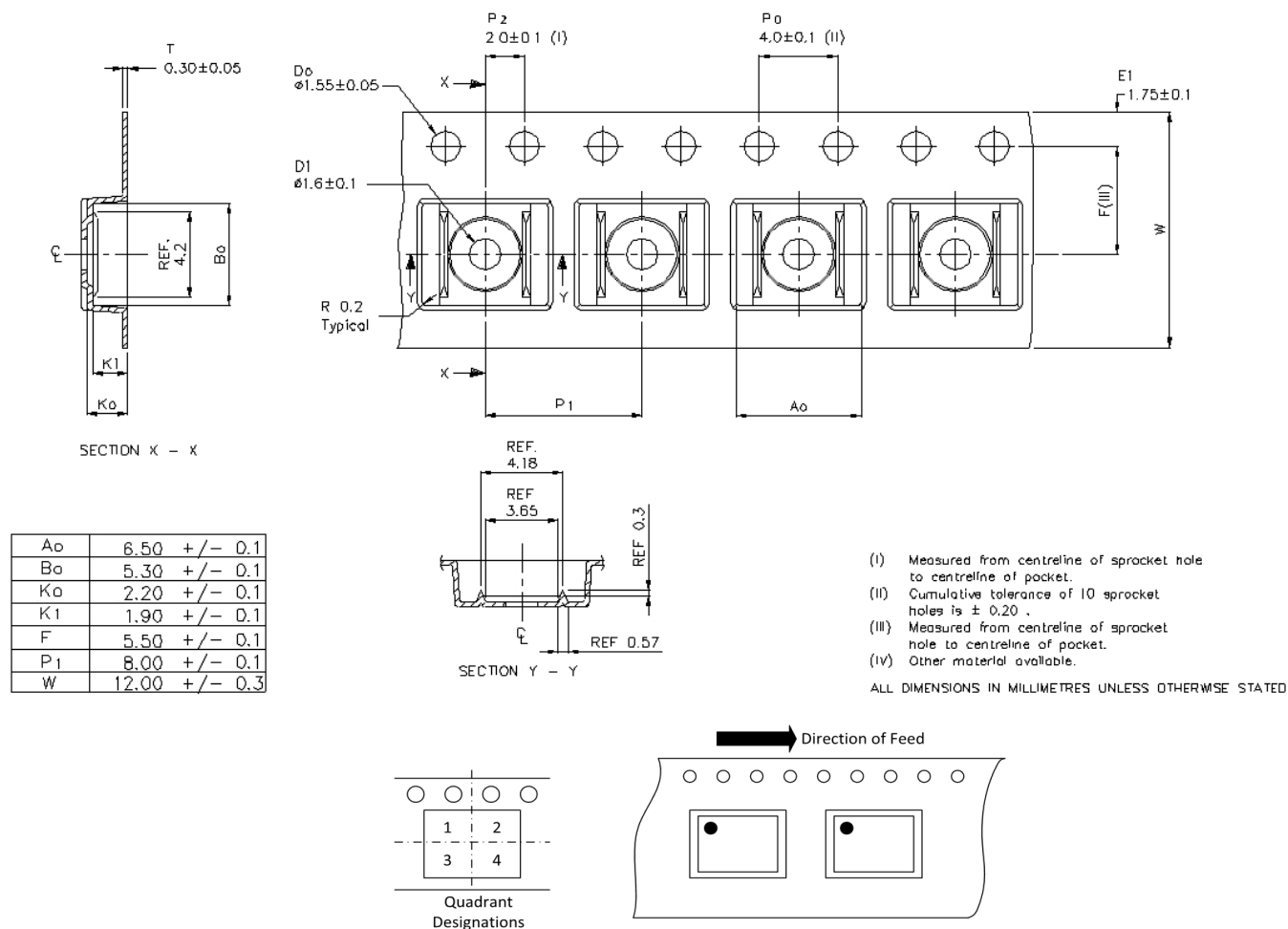


Figure 10.1 Tape and Reel Information of SOP8

11. Revision History

Revision	Description	Date
1.0	Initial version	2024/12/20

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