NOVOSENSE

NIRSP31E

Triple-Channel Digital Isolators With Integrated DC to DC Converter

Datasheet (EN) 1.0

Product Overview

The NIRSP31E device is a triple-channel digital isolator with integrated isolated DC-DC converter. The isolated DC-DC converter provides stable output voltage and up to 400mW output power by closed-loop control and transformer on chip. The feedback PWM signal is sent to the primary side by a digital isolator based on Novosense capacity isolation technology. The high integrated solution can help simplify system design, save PCB area and improve reliability. The NIRSP31E device supports 3kVrms insulation for 1min withstand voltage. The data rate of the NIRSP31E device is up to 20Mbps.

The NIRSP31E device provides 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion mode. The output voltage can be set by SEL pin.

Key Features

- Power supply voltage:
  - VDD: 3V to 3.6V, 4.5V to 5.25V
  - VDDL: 1.8V to 3.6V, 4.5V to 5.25V
- Max Output Support Current:
  - 85mA for 5V to 5V
  - 90mA for 5V to 3.3V
  - 45mA for 3.3V to 3.3V
- Excellent electromagnetic compatibility (EMI):
  - Low radiation
- Over current and over temperature protection
- Date rate: DC to 20Mbps
- Propagation delay: <75ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages: LGA-18

Applications

- Industrial Battery Management System
- Industrial automation system
- Isolated RS232, RS485, CAN
- General-purpose multichannel isolation

Device Information

Part Number	*Package*	*Body Size*
NIRSP31E-DLARR	LGA 18	5.00 × 5.00mm

Functional Block Diagrams

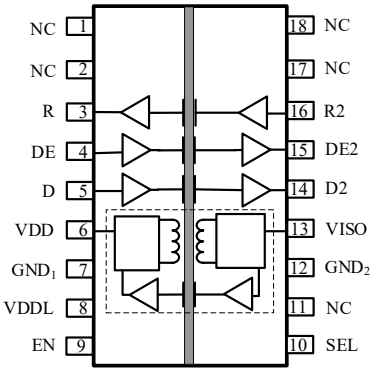

Figure 1. NIRSP31E Block Diagram

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1. Pin Configuration and Functions

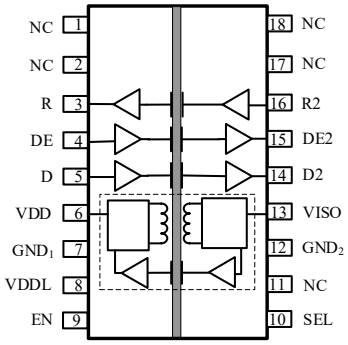


Figure 1.1 18-Pin LGA, Top View

Table1.1 Pin Functions

PIN NO.	SYMBOL	FUNCTION
1	NC	Not connected
2	NC	Not connected
3	R	Logic Output of R2
4	DE	Logic Input of DE2
5	D	Logic Input of D2
6	VDD	Power Supply for Isolator Side 1
7	GND_1	Isolator Side 1 Ground, The ground reference for VDD.
8	VDDL	Side1 I/O logic Power Supply input
9	EN	Power enable, When tied to VDDL or floating, the VISO output voltage is active. When a logic low voltage is applied, the VISO output voltage is shut down.
10	SEL	VISO output voltage select, VISO=5V when SEL pulled up to VISO or floating; VISO=3.3V when SEL pulled low.
11	NC	Not connected
12	GND_2	Isolator Side 2 Ground, The ground reference for VISO.
13	VISO	Secondary Supply Voltage Output Load
14	D2	Logic Output of D
15	DE2	Logic Output of DE
16	R2	Logic Input of R
17	NC	Not connected
18	NC	Not connected

2. Device Comparison Table

The NIRSP31E devices provide 5V to 5V, 5V to 3.3V,3.3V to 3.3V conversion modes. The output voltage can be set by SEL pin, Supply configuration table is showed below.

VDD	SEL PIN	NIRSP31E
VDD = (4.5V to 5.25V)	SEL = VISO	VISO = 5V
	SEL = GND_2	VISO = 3.3V
VDD = (3.0V to 3.6V)	SEL = GND_2	VISO = 3.3V

3. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD	-0.5		6	V
	VDDL	-0.5		6	V
Maximum Input Voltage	DE, D	-0.4		VDDL+0.4	V
	R2	-0.4		VISO+0.4	
Maximum Output Voltage	R	-0.4		VDDL +0.4	V
	DE2, D2	-0.4		VISO+0.4	
Output current of digital channels	I_O	-15		15	mA
Operating Temperature	T_{opr}	-40		125	℃
Junction temperature	T_J	-40		150	℃
Storage Temperature	T_{stg}	-65		150	℃

4. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-PrevD ● All pins	±2.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±2.0	kV

5. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage of NIRSP31E	VDD	3.0	3.3/5	5.25	V
Power of VDDL	VDDL	1.8		5.25	V
Operating Temperature	T_{opr}	-40		125	℃
High Level Input Voltage	V_{IH}	0.7*VCC[1]		VCC	V
Low Level Input Voltage	V_{IL}	0		0.3*VCC[1]	V
Data rate	DR			20	Mbps

(1) VCC of DE、D is VDDL；VCC of R2 is VISO.

6. Thermal Information

Parameters	Symbol	LGA18	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	75.8	°C/W
Junction-to-board thermal resistance	θ_{JB}	34.2	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	6.7	°C/W

Notes

(1) Four layers 2s2p PCB JEDEC JESD 51-7.

(2) TX, RX and transformer loss distribution in line with the normal use of customers, and through simulation to obtain the thermal resistance parameters.

7. Specifications

7.1. Isolated DC/DC Converter Static Specifications

(VDD= 4.5V～5.25V, SEL= VISO, Ta= -40℃ to 125℃. Unless otherwise noted, Typical values are at VDD =5V, Ta=25℃.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	VISO	4.5	5	5.5	V	
Line Regulation	VISO(LINE)			2	mV/V	I_{ISO} = 40mA, VDD= 4.5V to 5.25V
Load Regulation	VISO(LOAD)		0.4	5	%	I_{ISO} = 8mA to 72 mA
Output Ripple	VISO(RIP)		64		mVpp	20-MHz bandwidth, I_{ISO} = 40 mA, C_{LOAD} = 0.1 μF || 10 μF
Efficiency at maximum load current	EFF		50.6		%	I_{ISO} = 80 mA, C_{LOAD} = 0.1 μF || 10μF
Max Output supply current	Max_I_{ISO}		85		mA	Ta= -40℃ to 125℃
VDD supply current without digital isolator	I_{VDD_POWER}		13		mA	No VISO Load
			157		mA	Full VISO Load(I_{ISO} = 80mA)
Thermal Shutdown Temperature	T_{TSD}		165		℃	
VDD supply current when EN is low	I_{VDD_POWER}			30	μA	EN = 0, DE=GND_1 or VDD, D= GND_1 or VDD

(VDD= 4.5V～5.25V, SEL=GND_2, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD= 5V, Ta=25℃.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	VISO	3	3.3	3.6	V	
Line Regulation	VISO(LINE)			6	mV/V	I_{ISO} = 40mA, VDD= 4.5V to 5.25V
Load Regulation	VISO(LOAD)		0.6	5	%	I_{ISO} = 8mA to 72 mA
Output Ripple	VISO(RIP)		57.7		mVpp	20-MHz bandwidth, I_{ISO} = 40 mA, C_{LOAD} = 0.1 μF || 10 μF
Efficiency at maximum load current	EFF		40.8		%	I_{ISO} = 80 mA, C_{LOAD} = 0.1 μF || 10μF
Max Output supply current	Max_I_{ISO}		90		mA	Ta= -40℃ to 125℃
VDD supply current without digital isolator	I_{VDD_POWER}		11		mA	No VISO Load
			129		mA	Full VISO Load(I_{ISO}=80mA)

(VDD= 4.5V～5.25V, SEL=GND_2, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD= 5V, Ta=25℃.)

Thermal Shutdown Temperature			165		℃	
VDD supply current when EN is low	I_{VDD_POWER}			27	μA	EN = 0, DE=GND_1 or VDD, D= GND_1 or VDD

(VDD= 3.0V～3.6V, SEL=GND2, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD= 3.3V, Ta=25℃.)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Isolated Supply Voltage	VISO	3	3.3	3.6	V	
Line Regulation	VISO(LINE)			2	mV/V	I_{ISO} = 40mA, VDD= 3.0V to 3.3V
Load Regulation	VISO(LOAD)		0.6	5	%	I_{ISO} = 4.5mA to 40.5 mA
Output Ripple	VISO(RIP)		48.9		mVpp	20-MHz bandwidth, I_{ISO} = 40 mA, C_{LOAD} = 0.1 μF || 10 μF
Efficiency at maximum load current	EFF		40.9		%	I_{ISO} = 45 mA, C_{LOAD} = 0.1 μF || 10μF
Max Output supply current	Max_I_{ISO}		45		mA	(Ta= -40℃ to 125℃)
VDD supply current without digital isolator	I_{VDD_POWER}		11		mA	No VISO Load
			110		mA	Full VISO Load(I_{ISO}=45mA)
Thermal Shutdown Temperature			165		℃	
VDD supply current when EN is low	I_{VDD_POWER}			24	μA	EN = 0, DE=GND_1 or VDD, D= GND_1 or VDD

7.2. Digital Isolator Electrical Characteristics

(VDD= 4.5V～5.25V, SEL=VISO; VDD= 4.5V～5.25V, SEL= GND_2; VDD= 3.0V～3.6V, SEL= GND_2 ; Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD= 5V, Ta=25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
High Level Input Voltage	V_{IH}	0.7*VDDL			V	DE、D
		0.7*VISO				R2
Low Level Input Voltage	V_{IL}			0.3*VDDL	V	DE、D
				0.3*VISO		R2
High Level Output Voltage	V_{OH}	0.8*VDDL			V	R, I_{OH} ≥-4mA
		0.8*VISO				DE2、D2, I_{OH} ≥-4mA
Low Level Output Voltage	V_{OL}			0.2*VDDL	V	R, I_{OL} ≤ 4mA
				0.2*VISO		DE2、D2, I_{OL} ≤ 4mA
Output Impedance	R_{out}		50		ohm	
High level input current	I_{IH}		8	25	μA	DE =V_{DDL}
low level input current	I_{IL}	-25	-8		μA	EN、D、R2、SEL=0
EN logic high	V_{EN_H}	0.7 * VDDL		VDDL	V	
EN logic low	V_{EN_L}			0.3* VDDL	V	

(VDD= 4.5V～5.25V, SEL=VISO, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD= 5V, Ta=25℃.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current	IDD(Q0)		19		mA	All Input at 0V
	IDD(Q1)		14		mA	All Input at VCC[1]
	IDD(1M)		22		mA	All Input with square wave of 1Mbps, C_L=15pF
Data Rate	DR	0		20	Mbps	
Minimum Pulse Width	PW			50	ns	Guaranteed by Design
Propagation Delay	t_{PLH}		36	75	ns	See Figure 8.5, C_L = 15pF
	t_{PHL}		36	75	ns	See Figure 8.5, C_L = 15pF
Pulse Width Distortion	PWD		5.0		ns	See Figure 8.5, C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 8.5, C_L = 15pF

(VDD= 4.5V～5.5V, SEL=VISO, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD= 5V, Ta=25℃.)

Falling Time	t_f			5.0	ns	See Figure 8.5 , C_L = 15pF
Channel-to-Channel Delay Skew	t_{SK}(c2c)		8.0		ns	
Part-to-Part Delay Skew	t_{SK}(p2p)		8.0		ns	

(1) VCC of DE、D is VDDL, VCC of R2 is VISO.

(VDD= 4.5V～5.5V, SEL=GND_2, Ta=-40℃ to 125℃, Unless otherwise noted, Typical values are at VDD= 5V, Ta=25℃.)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Current	IDD(Q0)		15		mA	All Input at 0V
	IDD(Q1)		13		mA	All Input at VCC[1]
	IDD(1M)		18		mA	All Input with square wave of 1Mbps, C_L=15pF
Data Rate	DR	0		20	Mbps	
Minimum Pulse Width	PW			50	ns	Guarantee by Design
Propagation Delay	t_{PLH}		36	75	ns	See Figure 8.5 , C_L = 15pF
	t_{PHL}		36	75	ns	See Figure 8.5 , C_L = 15pF
Pulse Width Distortion	PWD		5.0		ns	See Figure 8.5 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 8.5 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 8.5 , C_L = 15pF
Channel-to-Channel Delay Skew	t_{SK}(c2c)		8.0		ns	
Part-to-Part Delay Skew	t_{SK}(p2p)		8.0		ns	

(1) VCC of DE、D is VDDL；VCC of R2 is VISO.

(VDD= 3.0V～3.6V, SEL=GND_2, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD= 3.3V, Ta=25℃.)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Current	IDD(Q0)		15		mA	All Input at 0V
	IDD(Q1)		12		mA	All Input at VCC[1]
	IDD(1M)		17		mA	All Input with square wave of 1Mbps, C_L=15pF
Data Rate	DR	0		20	Mbps	
Minimum Pulse Width	PW			50	ns	Guaranteed by Design
Propagation Delay	t_{PLH}		36	75	ns	See Figure 8.5 , C_L = 15pF
	t_{PHL}		36	75	ns	See Figure 8.5 , C_L = 15pF
Pulse Width Distortion	PWD		5.0		ns	See Figure 8.5 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 8.5 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 8.5 , C_L = 15pF
Channel-to-Channel Delay Skew	t_{SK}(c2c)		8.0		ns	
Part-to-Part Delay Skew	t_{SK}(p2p)		8.0		ns	

(1) VCC of DE、D is VDDL；VCC of R2 is VISO.

7.3. Typical Performance Characteristics

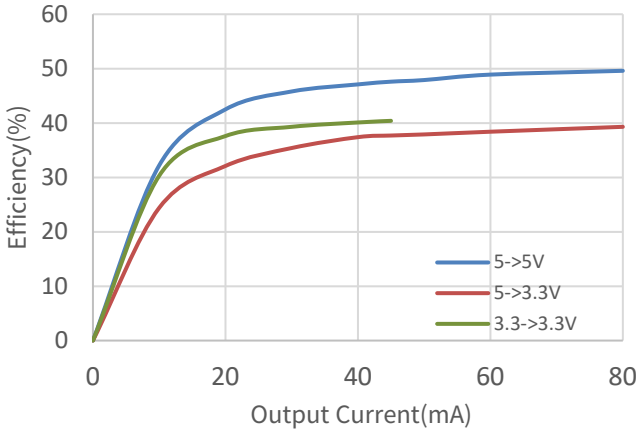


Figure 8.1 Output current vs efficiency

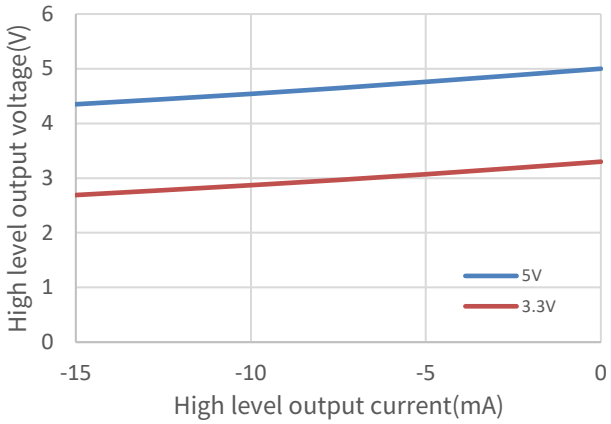
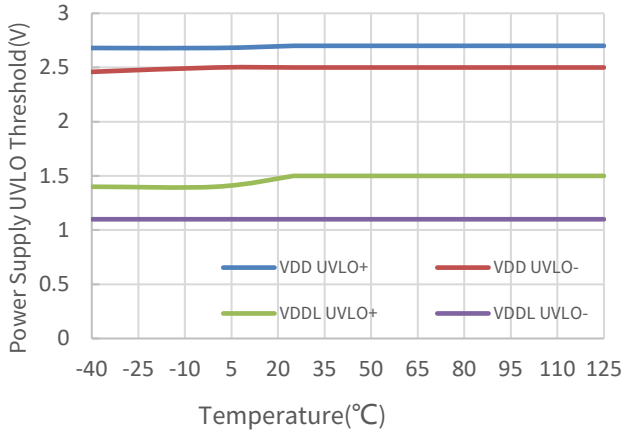


Figure 8.2 High-Level Output Voltage vs



Output Current

Figure 8.3 Power-Supply Undervoltage Threshold vs Temp

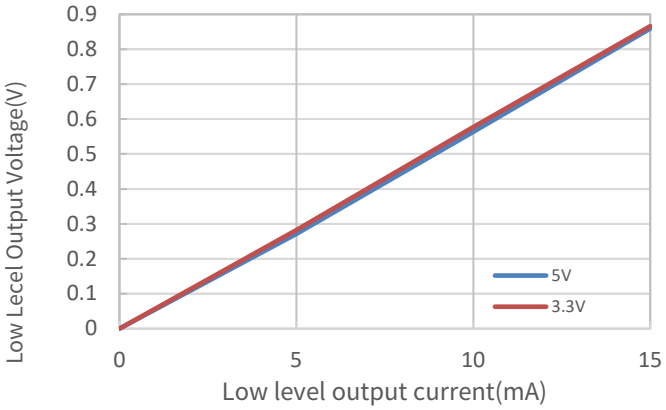
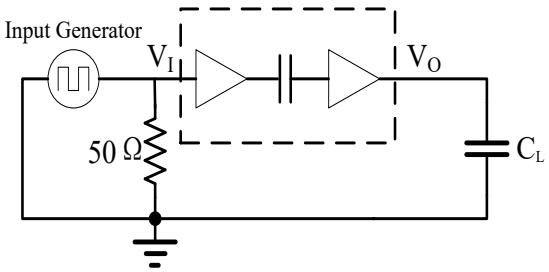


Figure 8.4 Low-Level Output Voltage vs Output Current

7.4. Parameter Measurement Information



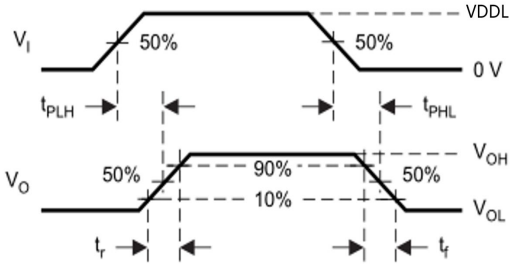


Figure 8.5 Switching Characteristics Test Circuit and Waveform

8. High Voltage Feature Description

Parameters	Symbol	value	unit	comments
Minimum External Air Gap (Clearance)	L(I01)	4.2	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.2	mm	Shortest terminal-to-terminal distance across the package surface
Minimum Internal Gap	DTI	42.5	um	Distance through insulation
Maximum Isolation Voltage	V_{ISO}	3000	V_{RMS}	t = 60 sec
Total Power Dissipation at 25℃	Ps	1726	mW	
Safety Input, Output, or Supply Current	Is	313.91	mA	θ_{JA} = 72.4°C/W, VDD = V_{DDL} =VISO = 5.25 V, T_J = 150 °C, Ta = 25 °C.
Max Safety Temperature	Ts	150	℃	

9. Function Description

The NIRSP31E device is triple-channel digital isolator with integrated isolated DC-DC converter. The isolated DC-DC converter provides up to 400mW power output using on-chip transformers. The feedback PWM signal is sent to the primary side by a digital isolator. The NIRSP31E device supports 3kVrms insulation for 1min withstand voltage. The data rate of the NIRSP31E is up to 20Mbps. The logical level of digital isolators on left side can be set by VDDL pin, which can support the application when the supply voltage and I/O voltage level are different.

The high integrated solution can help to simplify system design and improve reliability. Because of its smaller package of LGA, the NIRSP31E device are suitable for the limited PCB space applications. Meanwhile, the devices are also suitable for wide temperature application, which most power modules cannot support.

9.1. Device Functional Modes

The NIRSP31E device provide triple-channel digital isolators. The digital isolators have default output status when VCCIN is unready and VCCOUT is ready as shown in below table.

VCCIN[1] status	VCCOUT status	Input			Output			Comment
		D	DE	R2	D2	DE2	R	
Ready[2]	Ready	H	H	H	H	H	H	Normal operation
Ready	Ready	L	L	L	L	L	L	
Ready	Ready	floating	floating	floating	H	L	H	
Unready	Ready	X	X	X	H	L	X	
Ready	Unready	X	X	X	X	X	H	

(1) VCCIN is VDD, VDDL and VCCOUT is VISO.

(2) Ready = Powered up; Unready = Powered down; X = Irrelevant; H = High level; L = Low level.

9.2. Output Short and Over Temperature Protection

The NIRSP31E devices are protected against output short. When the device detects the output is short, the device will be in Hiccup mode and the transferred power will be limited. So the temperature of the device will be low, and the device is

protected. The NIRSP31E devices are also protected against over temperature. When device detect the chip is over 165℃, the chip will be shut down until the temperature of the device is below 145℃.

10. Application Note

10.1. Typical Application

The NIRSP31E requires 0.1 μF and 10uF bypass capacitors between VDD and GND_1、VISO and GND_2, a 0.1uF bypass capacitor between VDDL and GND_1. The capacitor should be placed as close as possible to the package. This is very important for the performance of the device. Figure 11.1 is the typical isolated RS485 schematic using NIRSP31E.

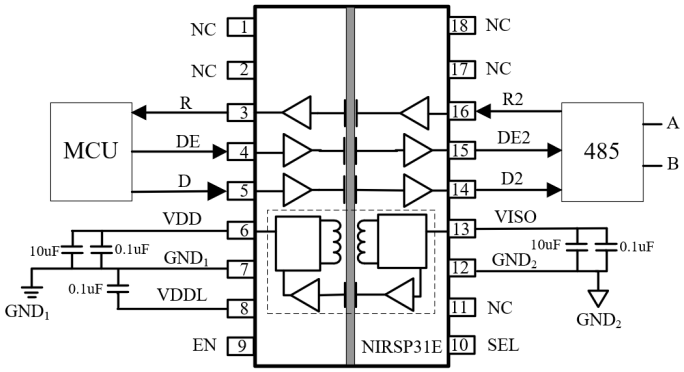


Figure 11.1 Isolated RS485 schematic using NIRSP31E

10.2. PCB Layout

The low ESR capacitors should be connected between Pin 7 (GND_1) and Pin 6 (VDD), Pin 7 (GND_1) and Pin 8 (VDDL). The VISO capacitors are connected between Pin 12 (GND_2) and Pin 13 (VISO). To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required with the smaller of the two capacitors located closest to the device, The recommended capacitor values are 0.1 μF and 10 μF for VDD between Pin 6 and Pin 7 and VISO between pin13 and pin12, values of 0.1 μF are recommended for VDDL Pin 8 and GND_1 Pin 7. The recommended best practice is to use a very low inductance ceramic capacitor, or its equivalent, for the smaller value capacitors. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 10 mm.

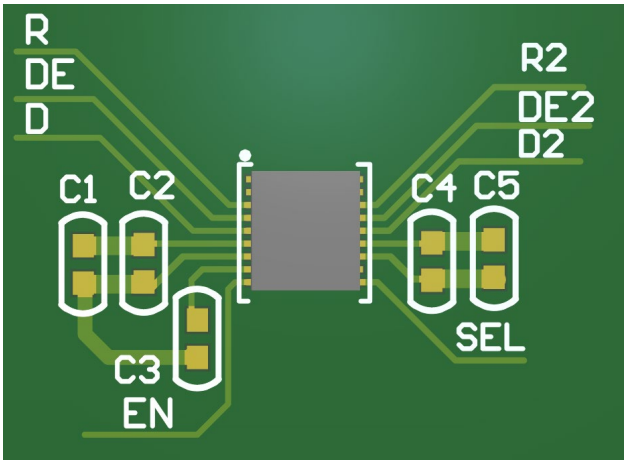
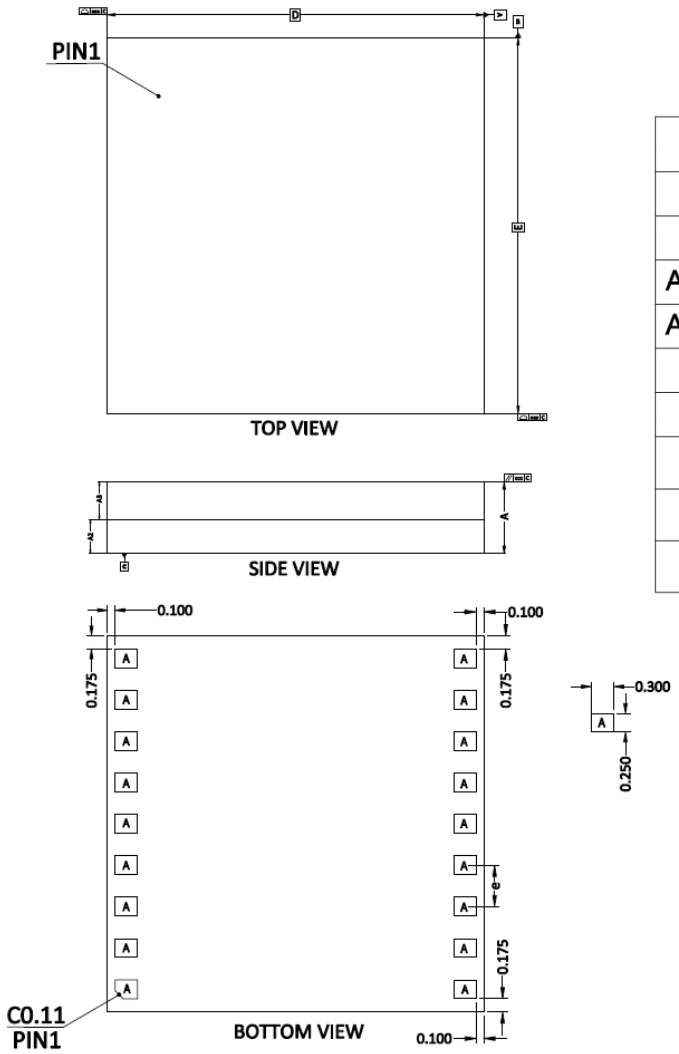


Figure 11.2 Recommended PCB Layout

11. Package Information



MILLIMETER			
SYMBOL	MIN	NOR	MAX
A	0.855	0.955	1.055
A2 (substrste thickness)	0.405	0.455	0.505
A3(moldcap thickness)	0.450	0.500	0.550
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.550 BSC		
aaa	0.1		
ccc	0.05		

Figure 12.1 LGA18 Package Shape and Dimension in millimeters

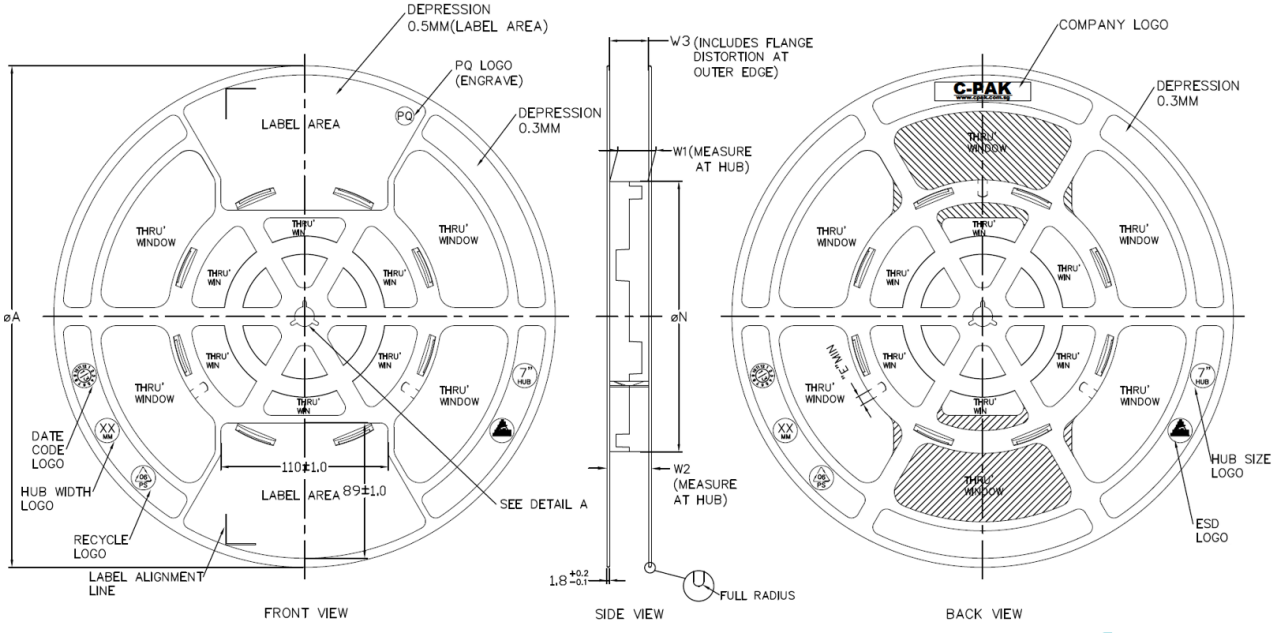
12. Order Information

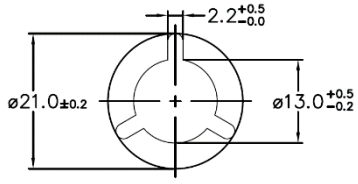
Part Number	Isolation Rating (kV)	Max Data Rate (Mbps)	Temperature	MSL	Package	SPQ
NIRSP31E-DLARR	3	20	-40 to 125℃	3	LGA18	3000

13. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NIRSP31E	Click here	Click here	Click here	Click here

14. Tape and Reel Information

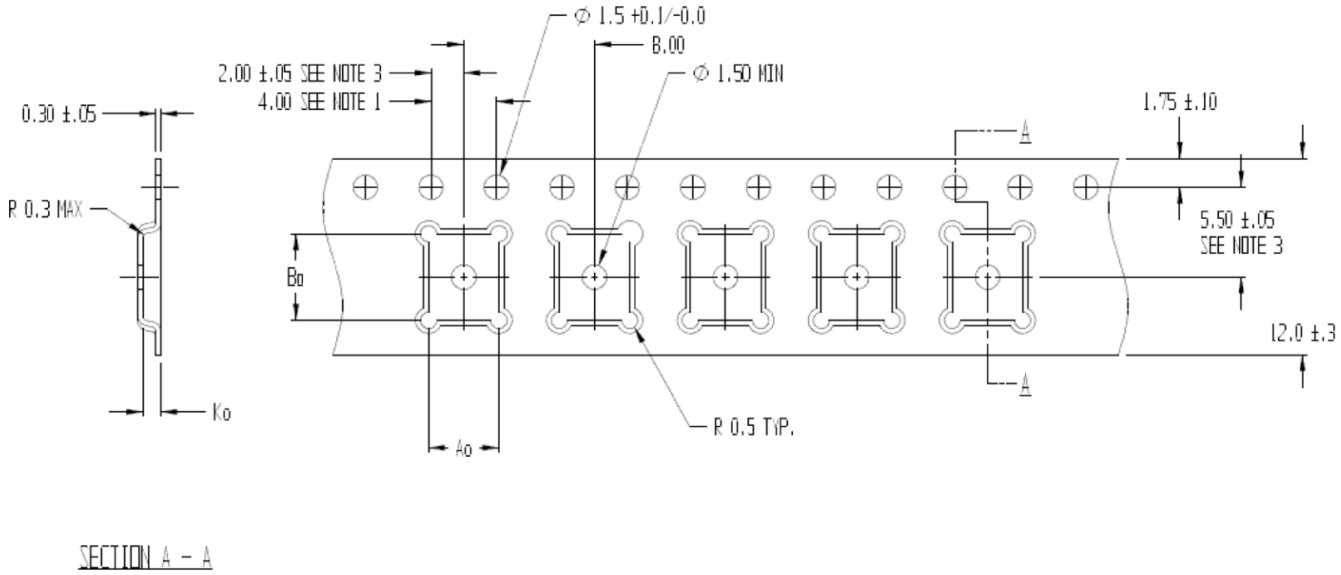




ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SMALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{8} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



A0 =5.25, B0 = 5.25, K0 =1.1

Figure 15.1 Tape and Reel Information of LGA18

15. Revision History

Revision	Description	Date
1.0	Initial Version	2025/4/15

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