NCAB0104-Q1

4-bit Bidirectional Voltage Level Translator

Datasheet (EN) 1.0

Product Overview

The NCAB0104-Q1 is a 4-bit directionless voltage level translator for push-pull applications. It includes two supply pins (V_{CCA} and V_{CCB}), one output-enable (OE) and two 4-bit I/O ports (An and Bn).

V_{CCA} pin accepts any supply voltage from 1.1 V to 3.6 V and V_{CCB} pin accepts any supply voltage from 1.65 V to 5.5 V such that V_{CCA} is no higher than V_{CCB}. It makes the device suitable for translating between any of the voltage nodes (1.2V, 1.8 V,2.5 V, 3.3 V and 5.0 V).

The A and B ports (An and Bn) are designed to track V_{CCA} and V_{CCB} respectively. The pin OE is referenced to V_{CCA}. Setting pin OE low causes all outputs to enter the high-impedance state. Setting pin OE high will enable the device. To ensure the high-impedance state during power up or power down, the OE pin must be tied to the GND pin through a pull-down resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver.

Key Features

- AEC-Q100 qualified for automotive applications (Grade 1)
- 1.1 V to 3.6 V on V_{CCA}
- 1.65 V to 5.5 V on V_{CCB} ($V_{CCA} \leq V_{CCB}$)
- Maximum data rates: 100 Mbps (push-pull)
- ESD protection exceeds JESD 22:
  - ± 8 kV HBM (A114) for A port
  - ± 15 kV HBM (A114) for B port
  - ± 2 kV CDM (C101) for A port
  - ± 2 kV CDM (C101) for B port
- IEC 61000-4-2 ESD (B port): ±15 kV Contact Discharge
- Latch-up performance exceeds 100 mA per JESD78E, class II
- RoHS compliance
- Multiple package options

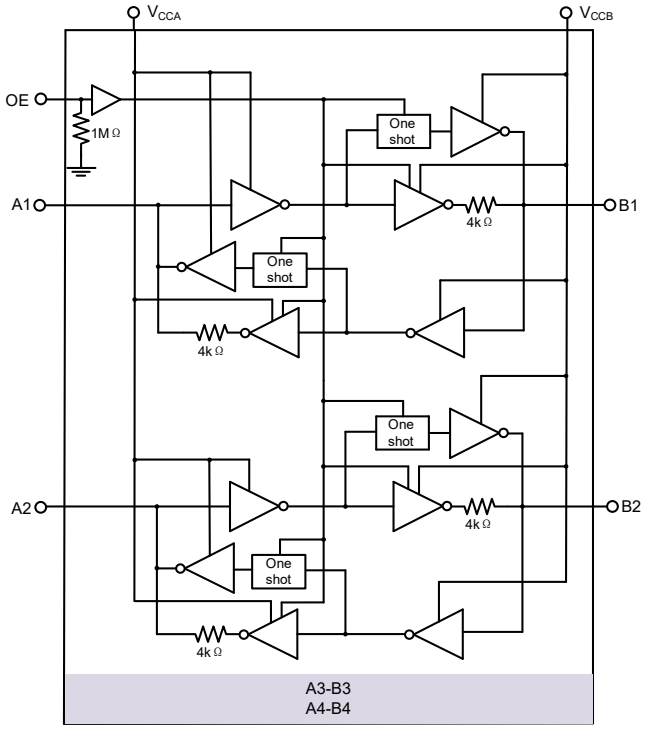
Applications

- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers, Industrial, Automation
- Isolates and level translators between main processor and peripheral modules

Device Information

Part Number	Package	Body Size
NCAB0104-Q1TSKR	TSSOP14	5.00mm ×4.40mm
NCAB0104-Q1QBCR	VQFN14	3.50mm ×3.50mm
NCAB0104-Q1QDDR	WQFN14	3.00mm ×2.50mm
NCAB0104-Q1QBDR	UQFN12	2.00mm ×1.70mm

Functional Block Diagram



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1. Pin Configuration and Functions

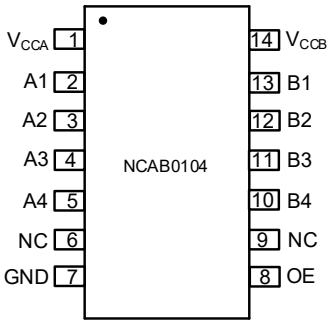


Figure 1.1 NCAB0104 TSSOP14 Package

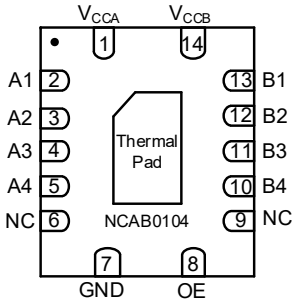


Figure 1.2 NCAB0104 VQFN14 and WQFN14 Package

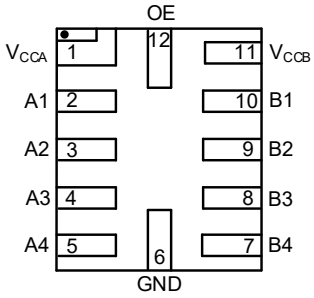


Figure 1.3 NCAB0104 UQFN12 Package

Table 1.1 Pin Configuration and Description of TSSOP14, VQFN14 and WQFN14

NCAB0104 PIN NO.	*SYMBOL*	*FUNCTION*
1	V_{CCA}	A port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
2/3/4/5	A1/A2/A3/A4	Input-output 1/2/3/4 for the A port (referenced to V_{CCA}).
6	NC	No connection
7	GND	Ground
8	OE	Output-enable pin (referenced to V_{CCA}). Active high. Set OE pin low to place all I/Os in high-impedance state.
9	NC	No connection
10/11/12/13	B4/B3/B2/B1	Input-output 4/3/2/1 for the B port (referenced to V_{CCB}).
14	V_{CCB}	B port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V and V_{CCA} ≤ V_{CCB}.
Thermal Pad		Connected to the PCB ground plane to improve thermal dissipation. Only for VQFN14 and WQFN14.

Table 1. 2 Pin Configuration and Description of UQFN12

NCAB0104 PIN NO.	SYMBOL	FUNCTION
1	V_{CCA}	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
2/3/4/5	A1/A2/A3/A4	Input-output 1/2/3/4 for the A port (referenced to V_{CCA}).
6	GND	Ground
7/8/9/10	B4/B3/B2/B1	Input-output 4/3/2/1 for the B port (referenced to V_{CCB}).
11	V_{CCB}	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V and V_{CCA} ≤ V_{CCB}.
12	OE	Output-enable pin (referenced to V_{CCA}). Active high. Set OE pin low to place all I/Os in high-impedance state.

2. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1].

Parameters	Symbol	Min	Max	Unit	Comments
Supply voltage	V_{CCA}	-0.5	4.6	V	Reference to GND
	V_{CCB}	-0.5	6.5	V	
Input voltage	V_I	-0.5	4.6	V	A ports or OE
		-0.5	6.5	V	B ports
Output voltage	V_O	-0.5	V_{CCA} + 0.5	V	Active mode: A port
		-0.5	V_{CCB} + 0.5	V	Active mode: B port
		-0.5	4.6	V	3-state and power-down mode: A port
		-0.5	6.5	V	3-state and power-down mode: B port
Input clamp current	I_{IK}	-50	-	mA	V_I < 0V
Output clamp current	I_{OK}	-50	-	mA	V_O < 0V
Continuous output current	I_O	-50	50	mA	V_O = 0V to V_{CCA} or V_{CCB}
Continuous current through supply	I_{CC}	-	100	mA	Current of V_{CCA} or V_{CCB}
Ground current	I_{GND}	-100	-	mA	Current of Ground
Operation temperature	T_a	-40	125	°C	NCAB0104-Q1TSKR NCAB0104-Q1QBCR NCAB0104-Q1QDDR NCAB0104-Q1QBDR
Junction temperature	T_J	-	150	°C	
Storage temperature	T_{stg}	-65	150	°C	

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating condition for extended periods may affect device reliability.

3. ESD Ratings

Parameters	*Ratings*	*Value*	*Unit*
Electrostatic discharge $V_{ESD-HBM1}$ $V_{ESD-HBM2}$	Human body model (JESD22/A114) - 100pF, 1.5kΩ ● B ports (Bn), to GND ● Others	 ±15.0 ±8.0	 kV kV
Electrostatic discharge $V_{ESD-CDM1}$	Charged device model (JESD22/C101)	±2.0	kV
Electrostatic discharge $V_{ESD-system}$	System level ESD (Contact discharge) - 330Ω/150pF unpowered according to IEC 61000-4-2 ● B ports (Bn)	 ±15.0	 kV

4. Recommended Operating Conditions

Symbol	Parameters	Conditions	Min	Max	Unit
V_{CCA}	Supply voltage		1.1	3.6	V
V_{CCB}			1.65	5.5	V
$V_{IH(An)}$	High-level input voltage	V_{CCA} = 1.1 V ~ 3.6 V V_{CCB} = 1.65 V ~ 5.5 V	0.7 * V_{CCA}	V_{CCA}	V
$V_{IH(Bn)}$		V_{CCA} = 1.1 V ~ 3.6 V V_{CCB} = 1.65 V ~ 5.5 V	0.7 * V_{CCB}	V_{CCB}	V
$V_{IH(OE)}$		V_{CCA} = 1.1 V ~ 3.6 V V_{CCB} = 1.65 V ~ 5.5 V	0.7 * V_{CCA}	5.5	V
$V_{IL(An)}$	Low-level input voltage	V_{CCA} = 1.1 V ~ 3.6 V V_{CCB} = 1.65 V ~ 5.5 V		0.3 * V_{CCA}	V
$V_{IL(Bn)}$		V_{CCA} = 1.1 V ~ 3.6 V V_{CCB} = 1.65 V ~ 5.5 V		0.3 * V_{CCB}	V
$V_{IL(OE)}$		V_{CCA} = 1.1 V ~ 3.6 V V_{CCB} = 1.65 V ~ 5.5 V		0.3 * V_{CCA}	V
Δt/Δv(An)	Input transition rise or fall rate	A port V_{CCA} = 1.1 V ~ 3.6 V V_{CCB} = 1.65 V ~ 5.5 V		40	ns/V
Δt/Δv(Bn)		B port V_{CCA} = 1.1 V ~ 3.6 V V_{CCB} = 1.65 V ~ 5.5 V		40	ns/V
T_a	Operating free-air temperature		-40	125	°C

5. Thermal Characteristics

Parameters	Symbol	TSSOP14	VQFN14	WQFN14	UQFN12	Unit
Junction-to-air thermal resistance	θ_{JA}	121.0	52.8	77.1	119.8	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	50.0	67.7	80.7	42.6	°C/W
Junction-to-board thermal resistance	θ_{JB}	62.8	28.9	46.9	52.5	°C/W

6. Specifications

6.1. Electrical Characteristics

V_{CCA} must be no higher than V_{CCB}. Unless otherwise noted, typical values are at T_a = 25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply current: pin V_{CCA} and V_{CCB}						
I_{CCA}	V_{CCA} supply current	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, A and B ports all open			20	μA
		V_{CCA} = 3.6 V, V_{CCB} = 0 V, A and B ports all open			15	μA
		V_{CCA} = 0 V, V_{CCB} = 5.5 V, A and B ports all open	-15			μA
I_{CCB}	V_{CCB} supply current	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, A and B ports all open			20	μA
		V_{CCA} = 3.6 V, V_{CCB} = 0 V, A and B ports all open	-15			μA
		V_{CCA} = 0 V, V_{CCB} = 5.5 V, A and B ports all open			15	μA
I_{CCA} + I_{CCB}	Combined supply current	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, A and B ports all open			40	μA
I_{CCZA}	High-impedance-state, V_{CCA} supply current	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V OE = GND			15	μA
I_{CCZB}	High-impedance-state, V_{CCB} supply current	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V OE = GND			15	μA
A or B ports: pin A1, A2, A3, A4, B1, B2, B3, B4						
V_{OHA}	Port A output high voltage	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, I_{OH} = –20 μA	V_{CCA} – 0.4			V
V_{OHB}	Port B output high voltage	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, I_{OH} = –20 μA	V_{CCB} – 0.4			V
V_{OLA}	Port A output low voltage	V_{CCA} = 1.1 V~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, I_{OL} = 20 μA			0.4	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{OLB}	Port B output low voltage	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, I_{OL} = 20 μA			0.4	V
I_{OZ}	High-impedance-state output current	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, OE = GND	-2		2	μA
$I_{off(An)}$	Port A off-state current	V_{CCA} = 0 V, V_{CCB} = 0 V ~ 5.5 V, OE = GND	-2		2	μA
$I_{off(Bn)}$	Port B off-state current	V_{CCA} = 0 V ~ 3.6 V, V_{CCB} = 0 V, OE = GND	-2		2	μA
$C_{IO(An)}$	Input-output capacitance of port A(1)				6	pF
$C_{IO(Bn)}$	Input-output capacitance of port B(1)				14	pF
Output enable: pin OE						
$I_{I(OE)}$	Input leakage current of OE(2)	V_{CCA} = 1.1 V ~ 3.6 V, V_{CCB} = 1.65 V ~ 5.5 V, OE = V_{CCA} / 0 V	-10		10	μA
$C_{I(OE)}$	Input capacitance of OE(1)				4	pF

(1) *Not test covered, guaranteed by design.*

(2) *The OE internally integrates a pull-down resistor, ensuring that the chip is in a disabled state by default after power-up.*

6.2. Timing Requirements

V_{CCA} must be no higher than V_{CCB}. Push-pull input. Unless otherwise noted, typical values are at T_a = 25°C.

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Max	Unit
V_{CCA} = 1.2 V(1)						
DR	Data rate	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		20	Mbps
			V_{CCB} = 2.5 V ± 0.2 V		20	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		20	Mbps
			V_{CCB} = 5 V ± 0.5 V		20	Mbps
t_w	Pulse duration (data input)	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V	50		ns
			V_{CCB} = 2.5 V ± 0.2 V	50		ns
			V_{CCB} = 3.3 V ± 0.3 V	50		ns
			V_{CCB} = 5 V ± 0.5 V	50		ns
V_{CCA} = 1.5 V ± 0.1 V(1)						
DR	Data rate	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V		40	Mbps
			V_{CCB} = 2.5 V ± 0.2 V		40	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		40	Mbps
			V_{CCB} = 5 V ± 0.5 V		40	Mbps
t_w	Pulse duration (data input)	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	25		ns
			V_{CCB} = 2.5 V ± 0.2 V	25		ns
			V_{CCB} = 3.3 V ± 0.3 V	25		ns
			V_{CCB} = 5 V ± 0.5 V	25		ns
V_{CCA} = 1.8 V ± 0.15 V(1)						
DR	Data rate	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
			V_{CCB} = 2.5 V ± 0.2 V		60	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		60	Mbps
			V_{CCB} = 5 V ± 0.5 V		60	Mbps
t_w	Pulse duration (data input)	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V	17		ns
			V_{CCB} = 2.5 V ± 0.2 V	17		ns
			V_{CCB} = 3.3 V ± 0.3 V	17		ns
			V_{CCB} = 5 V ± 0.5 V	17		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Max	Unit
V_{CCA} = 2.5 V ± 0.2 V(1)						
DR	Data rate	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V		100	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		100	Mbps
			V_{CCB} = 5 V ± 0.5 V		100	Mbps
t_w	Pulse duration (data input)	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V	10		ns
			V_{CCB} = 3.3 V ± 0.3 V	10		ns
			V_{CCB} = 5 V ± 0.5 V	10		ns
V_{CCA} = 3.3 V ± 0.3 V(1)						
DR	Data rate	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V		100	Mbps
			V_{CCB} = 5 V ± 0.5 V		100	Mbps
t_w	Pulse duration (data input)	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V	10		ns
			V_{CCB} = 5 V ± 0.5 V	10		ns

(1) *Not test covered, guaranteed by design.*

6.3. Switching Characteristics

V_{CCA} must be no higher than V_{CCB}. Push-pull input. Unless otherwise noted, typical values are at T_a = 25°C.

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
V_{CCA} = 1.2 V(1)							
$t_{PHL(A-B)}$	Propagation delay time (high to low), from A (input) to B (output)	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		11.6	15	ns
			V_{CCB} = 2.5 V ± 0.2 V		9.4	14	ns
			V_{CCB} = 3.3 V ± 0.3 V		8	12	ns
			V_{CCB} = 5 V ± 0.5 V		8	12	ns
$t_{PLH(A-B)}$	Propagation delay time (low to high), from A (input) to B (output)		V_{CCB} = 1.8 V ± 0.15 V		11.3	15	ns
			V_{CCB} = 2.5 V ± 0.2 V		8.6	14	ns
			V_{CCB} = 3.3 V ± 0.3 V		8.4	12	ns
			V_{CCB} = 5 V ± 0.5 V		8.4	12	ns
$t_{PHL(B-A)}$	Propagation delay time (high to low), from B (input) to A (output)	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		12.8	16	ns
			V_{CCB} = 2.5 V ± 0.2 V		11.8	16	ns
			V_{CCB} = 3.3 V ± 0.3 V		11.4	15	ns
			V_{CCB} = 5 V ± 0.5 V		10.7	14	ns
$t_{PLH(B-A)}$	Propagation delay time (low to high), from B (input) to A (output)	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		9.7	14	ns
			V_{CCB} = 2.5 V ± 0.2 V		8.4	14	ns
			V_{CCB} = 3.3 V ± 0.3 V		7.8	12	ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
			V_{CCB} = 5 V ± 0.5 V		8	12	ns
$t_{r(An)}$	Rise time of port A (output)	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		8.8	12	ns
			V_{CCB} = 2.5 V ± 0.2 V		8.4	12	ns
			V_{CCB} = 3.3 V ± 0.3 V		8.7	12	ns
			V_{CCB} = 5 V ± 0.5 V		7.5	12	ns
$t_{f(An)}$	Fall time of port A (output)		V_{CCB} = 1.8 V ± 0.15 V		12.5	16	ns
			V_{CCB} = 2.5 V ± 0.2 V		13.4	16	ns
			V_{CCB} = 3.3 V ± 0.3 V		14.1	16	ns
			V_{CCB} = 5 V ± 0.5 V		11.2	16	ns
$t_{r(Bn)}$	Rise time of port B (output)	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		6.1	10	ns
			V_{CCB} = 2.5 V ± 0.2 V		5.4	10	ns
			V_{CCB} = 3.3 V ± 0.3 V		5.0	10	ns
			V_{CCB} = 5 V ± 0.5 V		4.9	10	ns
$t_{f(Bn)}$	Fall time of port B (output)		V_{CCB} = 1.8 V ± 0.15 V		6.5	12	ns
			V_{CCB} = 2.5 V ± 0.2 V		6.0	12	ns
			V_{CCB} = 3.3 V ± 0.3 V		5.9	12	ns
			V_{CCB} = 5 V ± 0.5 V		5.4	12	ns
t_{sk}	Channel-to channel skew	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		0.4		ns
			V_{CCB} = 2.5 V ± 0.2 V		0.5		ns
			V_{CCB} = 3.3 V ± 0.3 V		0.5		ns
			V_{CCB} = 5 V ± 0.5 V		1.4		ns
$t_{en(OE-A)}$	Enable time, from OE (input) to A (output), t_{PZL}	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		160		ns
			V_{CCB} = 2.5 V ± 0.2 V		160		ns
			V_{CCB} = 3.3 V ± 0.3 V		40		ns
			V_{CCB} = 5 V ± 0.5 V		20		ns
	Enable time, from OE (input) to A (output), t_{PZH}		V_{CCB} = 1.8 V ± 0.15 V		200		ns
			V_{CCB} = 2.5 V ± 0.2 V		200		ns
			V_{CCB} = 3.3 V ± 0.3 V		200		ns
			V_{CCB} = 5 V ± 0.5 V		200		ns
$t_{dis(OE-A)}$	Disable time, from OE (input) to A (output), t_{PLZ}	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		200		ns
			V_{CCB} = 2.5 V ± 0.2 V		200		ns
			V_{CCB} = 3.3 V ± 0.3 V		200		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
			V_{CCB} = 5 V ± 0.5 V		200		ns
	Disable time, from OE (input) to A (output), t_{PHZ}		V_{CCB} = 1.8 V ± 0.15 V		300		ns
			V_{CCB} = 2.5 V ± 0.2 V		300		ns
			V_{CCB} = 3.3 V ± 0.3 V		300		ns
			V_{CCB} = 5 V ± 0.5 V		300		ns
$t_{en(OE-B)}$	Enable time, from OE (input) to B (output), t_{PZL}	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		200		ns
			V_{CCB} = 2.5 V ± 0.2 V		200		ns
			V_{CCB} = 3.3 V ± 0.3 V		200		ns
			V_{CCB} = 5 V ± 0.5 V		200		ns
	Enable time, from OE (input) to B (output), t_{PZH}		V_{CCB} = 1.8 V ± 0.15 V		200		ns
			V_{CCB} = 2.5 V ± 0.2 V		200		ns
			V_{CCB} = 3.3 V ± 0.3 V		20		ns
			V_{CCB} = 5 V ± 0.5 V		20		ns
$t_{dis(OE-B)}$	Disable time, from OE (input) to B (output), t_{PLZ}	V_{CCA} = 1.2 V	V_{CCB} = 1.8 V ± 0.15 V		200		ns
			V_{CCB} = 2.5 V ± 0.2 V		200		ns
			V_{CCB} = 3.3 V ± 0.3 V		200		ns
			V_{CCB} = 5 V ± 0.5 V		200		ns
	Disable time, from OE (input) to B (output), t_{PHZ}		V_{CCB} = 1.8 V ± 0.15 V		350		ns
			V_{CCB} = 2.5 V ± 0.2 V		350		ns
			V_{CCB} = 3.3 V ± 0.3 V		350		ns
			V_{CCB} = 5 V ± 0.5 V		350		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
V_{CCA} = 1.5 V ± 0.1 V(1)							
$t_{PHL(A-B)}$	Propagation delay time (high to low), from A (input) to B (output)	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	1.4	9.6	12.9	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.2	6.9	10.1	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.1	5.4	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.8	5.3	9.9	ns
$t_{PLH(A-B)}$	Propagation delay time (low to high), from A (input) to B (output)	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	1.4	9.1	12.9	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.2	6.1	10.1	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.1	5.9	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.8	5.6	9.9	ns
$t_{PHL(B-A)}$	Propagation delay time (high to low), from B (input) to A (output)	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	0.9	8.7	14.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.7	7.4	12	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.4	7.0	11.7	ns
			V_{CCB} = 5 V ± 0.5 V	0.3	6.5	13.7	ns
$t_{PLH(B-A)}$	Propagation delay time (low to high), from B (input) to A (output)		V_{CCB} = 1.8 V ± 0.15 V	0.9	8.4	14.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.7	6.7	12	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.4	6.1	11.7	ns
			V_{CCB} = 5 V ± 0.5 V	0.3	5.9	13.7	ns
$t_{r(An)}$	Rise time of port A (output)	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	1.4	6.0	10	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	6.1	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.4	6.2	10	ns
			V_{CCB} = 5 V ± 0.5 V	1.4	6.2	10	ns
$t_{f(An)}$	Fall time of port A (output)		V_{CCB} = 1.8 V ± 0.15 V	1.4	7.6	10	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	7.9	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.4	7.9	10	ns
			V_{CCB} = 5 V ± 0.5 V	1.4	7.7	10	ns
$t_{r(Bn)}$	Rise time of port B (output)	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	0.9	6.1	10	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.6	5.4	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.5	5.1	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	4.8	10	ns
$t_{f(Bn)}$	Fall time of port B (output)		V_{CCB} = 1.8 V ± 0.15 V	0.9	7.3	10	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.6	6.1	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.5	5.9	10	ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
			V_{CCB} = 5 V ± 0.5 V	0.4	5.6	10	ns
t_{sk}	Channel-to channel skew	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V			0.5	ns
			V_{CCB} = 2.5 V ± 0.2 V			0.5	ns
			V_{CCB} = 3.3 V ± 0.3 V			0.5	ns
			V_{CCB} = 5 V ± 0.5 V			0.5	ns
$t_{en(OE-A)}$	Enable time, from OE (input) to A (output), t_{PZL}	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V		150		ns
			V_{CCB} = 2.5 V ± 0.2 V		150		ns
			V_{CCB} = 3.3 V ± 0.3 V		150		ns
			V_{CCB} = 5 V ± 0.5 V		150		ns
$t_{en(OE-A}$	Enable time, from OE (input) to A (output), t_{PZH}		V_{CCB} = 1.8 V ± 0.15 V		180		ns
			V_{CCB} = 2.5 V ± 0.2 V		180		ns
			V_{CCB} = 3.3 V ± 0.3 V		180		ns
			V_{CCB} = 5 V ± 0.5 V		180		ns
$t_{dis(OE-A)}$	Disable time, from OE (input) to A (output), t_{PLZ}	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V		200		ns
			V_{CCB} = 2.5 V ± 0.2 V		200		ns
			V_{CCB} = 3.3 V ± 0.3 V		200		ns
			V_{CCB} = 5 V ± 0.5 V		200		ns
$t_{dis(OE-A)}$	Disable time, from OE (input) to A (output), t_{PHZ}		V_{CCB} = 1.8 V ± 0.15 V		260		ns
			V_{CCB} = 2.5 V ± 0.2 V		260		ns
			V_{CCB} = 3.3 V ± 0.3 V		260		ns
			V_{CCB} = 5 V ± 0.5 V		260		ns
$t_{en(OE-B)}$	Enable time, from OE (input) to B (output), t_{PZL}	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V		170		ns
			V_{CCB} = 2.5 V ± 0.2 V		170		ns
			V_{CCB} = 3.3 V ± 0.3 V		170		ns
			V_{CCB} = 5 V ± 0.5 V		170		ns
$t_{en(OE-B)}$	Enable time, from OE (input) to B (output), t_{PZH}		V_{CCB} = 1.8 V ± 0.15 V		300		ns
			V_{CCB} = 2.5 V ± 0.2 V		190		ns
			V_{CCB} = 3.3 V ± 0.3 V		190		ns
			V_{CCB} = 5 V ± 0.5 V		190		ns
$t_{dis(OE-B)}$	Disable time, from OE (input) to B (output), t_{PLZ}	V_{CCA} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V		210		ns
			V_{CCB} = 2.5 V ± 0.2 V		210		ns
			V_{CCB} = 3.3 V ± 0.3 V		210		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
			V_{CCB} = 5 V ± 0.5 V		210		ns
$t_{dis(OE-B)}$	Disable time, from OE (input) to B (output), t_{PHZ}		V_{CCB} = 1.8 V ± 0.15 V		430		ns
			V_{CCB} = 2.5 V ± 0.2 V		330		ns
			V_{CCB} = 3.3 V ± 0.3 V		330		ns
			V_{CCB} = 5 V ± 0.5 V		330		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
V_{CCA} = 1.8 V ± 0.15 V(1)							
$t_{PHL(A-B)}$	Propagation delay time (high to low), from A (input) to B (output)	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V	1.6	8.8	11	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	6.2	7.7	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.3	4.5	6.8	ns
			V_{CCB} = 5 V ± 0.5 V	1.2	4.3	6.5	ns
$t_{PLH(A-B)}$	Propagation delay time (low to high), from A (input) to B (output)		V_{CCB} = 1.8 V ± 0.15 V	1.6	7.6	11	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	5.1	7.7	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.3	4.6	6.8	ns
			V_{CCB} = 5 V ± 0.5 V	1.2	4.5	6.5	ns
$t_{PHL(B-A)}$	Propagation delay time (high to low), from B (input) to A (output)	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V	1.5	7.8	12	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.3	6.4	8.4	ns
			V_{CCB} = 3.3 V ± 0.3 V	1	5.8	7.6	ns
			V_{CCB} = 5 V ± 0.5 V	0.9	5.5	7.1	ns
$t_{PLH(B-A)}$	Propagation delay time (low to high), from B (input) to A (output)		V_{CCB} = 1.8 V ± 0.15 V	1.5	7.7	12	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.3	5.9	8.4	ns
			V_{CCB} = 3.3 V ± 0.3 V	1	5.4	7.6	ns
			V_{CCB} = 5 V ± 0.5 V	0.9	5.2	7.1	ns
$t_{r(An)}$	Rise time of port A (output)	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V	1	3.8	10	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.1	3.9	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.1	4.1	10	ns
			V_{CCB} = 5 V ± 0.5 V	1.1	4.4	10	ns
$t_{f(An)}$	Fall time of port A (output)		V_{CCB} = 1.8 V ± 0.15 V	1	7.2	10	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.1	7.2	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.1	7.2	10	ns
			V_{CCB} = 5 V ± 0.5 V	1.1	7.2	10	ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
$t_{r(Bn)}$	Rise time of port B (output)	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V	0.9	6.2	10	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.6	5.4	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.5	5.0	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	4.9	10	ns
$t_{f(Bn)}$	Fall time of port B (output)		V_{CCB} = 1.8 V ± 0.15 V	0.9	7.1	10	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.6	6.0	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.5	5.9	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	5.6	10	ns
t_{sk}	Channel-to channel skew	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V			0.5	ns
			V_{CCB} = 2.5 V ± 0.2 V			0.5	ns
			V_{CCB} = 3.3 V ± 0.3 V			0.5	ns
			V_{CCB} = 5 V ± 0.5 V			0.5	ns
$t_{en(OE-A)}$	Enable time, from OE (input) to A (output), t_{PZL}	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V		150		ns
			V_{CCB} = 2.5 V ± 0.2 V		150		ns
			V_{CCB} = 3.3 V ± 0.3 V		150		ns
			V_{CCB} = 5 V ± 0.5 V		150		ns
$t_{en(OE-A}$	Enable time, from OE (input) to A (output), t_{PZH}		V_{CCB} = 1.8 V ± 0.15 V		170		ns
			V_{CCB} = 2.5 V ± 0.2 V		170		ns
			V_{CCB} = 3.3 V ± 0.3 V		170		ns
			V_{CCB} = 5 V ± 0.5 V		170		ns
$t_{dis(OE-A)}$	Disable time, from OE (input) to A (output), t_{PLZ}	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V		180		ns
			V_{CCB} = 2.5 V ± 0.2 V		180		ns
			V_{CCB} = 3.3 V ± 0.3 V		180		ns
			V_{CCB} = 5 V ± 0.5 V		180		ns
$t_{dis(OE-A)}$	Disable time, from OE (input) to A (output), t_{PHZ}		V_{CCB} = 1.8 V ± 0.15 V		260		ns
			V_{CCB} = 2.5 V ± 0.2 V		260		ns
			V_{CCB} = 3.3 V ± 0.3 V		260		ns
			V_{CCB} = 5 V ± 0.5 V		260		ns
$t_{en(OE-B)}$	Enable time, from OE (input) to B (output), t_{PZL}	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V		170		ns
			V_{CCB} = 2.5 V ± 0.2 V		170		ns
			V_{CCB} = 3.3 V ± 0.3 V		170		ns
			V_{CCB} = 5 V ± 0.5 V		170		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
$t_{en(OE-B)}$	Enable time, from OE (input) to B (output), t_{PZH}		V_{CCB} = 1.8 V ± 0.15 V		200		ns
			V_{CCB} = 2.5 V ± 0.2 V		200		ns
			V_{CCB} = 3.3 V ± 0.3 V		200		ns
			V_{CCB} = 5 V ± 0.5 V		200		ns
$t_{dis(OE-B)}$	Disable time, from OE (input) to B (output), t_{PLZ}	V_{CCA} = 1.8 V ± 0.15 V	V_{CCB} = 1.8 V ± 0.15 V		200		ns
			V_{CCB} = 2.5 V ± 0.2 V		200		ns
			V_{CCB} = 3.3 V ± 0.3 V		200		ns
			V_{CCB} = 5 V ± 0.5 V		200		ns
$t_{dis(OE-B)}$	Disable time, from OE (input) to B (output), t_{PHZ}		V_{CCB} = 1.8 V ± 0.15 V		350		ns
			V_{CCB} = 2.5 V ± 0.2 V		330		ns
			V_{CCB} = 3.3 V ± 0.3 V		330		ns
			V_{CCB} = 5 V ± 0.5 V		320		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
V_{CCA} = 2.5 V±0.2 V(1)							
$t_{PHL(A-B)}$	Propagation delay time (high to low), from A (input) to B (output)	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V	1.1	5.4	6.3	ns
			V_{CCB} = 3.3 V ± 0.3 V	1	5.0	6.2	ns
			V_{CCB} = 5 V ± 0.5 V	0.9	3.4	4.7	ns
$t_{PLH(A-B)}$	Propagation delay time (low to high), from A (input) to B (output)		V_{CCB} = 2.5 V ± 0.2 V	1.1	4.3	6.3	ns
			V_{CCB} = 3.3 V ± 0.3 V	1	3.7	5.2	ns
			V_{CCB} = 5 V ± 0.5 V	0.9	3.5	4.7	ns
$t_{PHL(B-A)}$	Propagation delay time (high to low), from B (input) to A (output)	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V	1.2	5.5	6.6	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.1	4.9	6.1	ns
			V_{CCB} = 5 V ± 0.5 V	0.9	4.6	6.4	ns
$t_{PLH(B-A)}$	Propagation delay time (low to high), from B (input) to A (output)		V_{CCB} = 2.5 V ± 0.2 V	1.2	4.2	6.6	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.1	3.6	5.1	ns
			V_{CCB} = 5 V ± 0.5 V	0.9	3.2	4.4	ns
$t_{r(An)}$	Rise time of port A (output)	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V	0.8	3.0	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.8	3.1	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.8	3.2	10	ns
$t_{f(An)}$	Fall time of port A (output)		V_{CCB} = 2.5 V ± 0.2 V	0.8	5.3	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.8	5.5	10	ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
			V_{CCB} = 5 V ± 0.5 V	0.8	5.5	10	ns
$t_{r(Bn)}$	Rise time of port B (output)	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V	0.7	5.4	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.5	5.1	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	5.0	10	ns
$t_{f(Bn)}$	Fall time of port B (output)		V_{CCB} = 2.5 V ± 0.2 V	0.7	6.0	10	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.5	5.8	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	5.6	10	ns
t_{sk}	Channel-to channel skew	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V			0.5	ns
			V_{CCB} = 3.3 V ± 0.3 V			0.5	ns
			V_{CCB} = 5 V ± 0.5 V			0.5	ns
$t_{en(OE-A)}$	Enable time, from OE (input) to A (output), t_{PZL}	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V		140		ns
			V_{CCB} = 3.3 V ± 0.3 V		140		ns
			V_{CCB} = 5 V ± 0.5 V		140		ns
	Enable time, from OE (input) to A (output), t_{PZH}		V_{CCB} = 2.5 V ± 0.2 V		160		ns
			V_{CCB} = 3.3 V ± 0.3 V		160		ns
			V_{CCB} = 5 V ± 0.5 V		160		ns
$t_{dis(OE-A)}$	Disable time, from OE (input) to A (output), t_{PLZ}	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V		180		ns
			V_{CCB} = 3.3 V ± 0.3 V		180		ns
			V_{CCB} = 5 V ± 0.5 V		180		ns
	Disable time, from OE (input) to A (output), t_{PHZ}		V_{CCB} = 2.5 V ± 0.2 V		250		ns
			V_{CCB} = 3.3 V ± 0.3 V		250		ns
			V_{CCB} = 5 V ± 0.5 V		250		ns
$t_{en(OE-B)}$	Enable time, from OE (input) to B (output), t_{PZL}	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V		170		ns
			V_{CCB} = 3.3 V ± 0.3 V		170		ns
			V_{CCB} = 5 V ± 0.5 V		170		ns
	Enable time, from OE (input) to B (output), t_{PZH}		V_{CCB} = 2.5 V ± 0.2 V		190		ns
			V_{CCB} = 3.3 V ± 0.3 V		190		ns
			V_{CCB} = 5 V ± 0.5 V		190		ns
$t_{dis(OE-B)}$	Disable time, from OE (input) to B (output), t_{PLZ}	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 2.5 V ± 0.2 V		210		ns
			V_{CCB} = 3.3 V ± 0.3 V		210		ns
			V_{CCB} = 5 V ± 0.5 V		210		ns
			V_{CCB} = 2.5 V ± 0.2 V		330		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
	Disable time, from OE (input) to B (output), t_{PHZ}	V_{CCA} = 2.5 V ± 0.2 V	V_{CCB} = 3.3 V ± 0.3 V		330		ns
			V_{CCB} = 5 V ± 0.5 V		330		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
V_{CCA} = 3.3 V±0.3 V(1)							
$t_{PHL(A-B)}$	Propagation delay time (high to low), from A (input) to B (output)	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V	0.9	4.4	5.7	ns
			V_{CCB} = 5 V ± 0.5 V	0.8	3.0	4	ns
$t_{PLH(A-B)}$	Propagation delay time (low to high), from A (input) to B (output)		V_{CCB} = 3.3 V ± 0.3 V	0.9	3.4	4.7	ns
			V_{CCB} = 5 V ± 0.5 V	0.8	3.3	4	ns
$t_{PHL(B-A)}$	Propagation delay time (high to low), from B (input) to A (output)	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V	1	4.3	5.9	ns
			V_{CCB} = 5 V ± 0.5 V	0.9	4.3	5.8	ns
$t_{PLH(B-A)}$	Propagation delay time (low to high), from B (input) to A (output)		V_{CCB} = 3.3 V ± 0.3 V	1	3.4	4.9	ns
			V_{CCB} = 5 V ± 0.5 V	0.9	2.9	3.8	ns
$t_{r(An)}$	Rise time of port A (output)	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V	0.7	2.8	5	ns
			V_{CCB} = 5 V ± 0.5 V	0.7	2.9	5	ns
$t_{f(An)}$	Fall time of port A (output)		V_{CCB} = 3.3 V ± 0.3 V	0.7	3.9	5	ns
			V_{CCB} = 5 V ± 0.5 V	0.7	4.0	5	ns
$t_{r(Bn)}$	Rise time of port B (output)	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V	0.5	5.3	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	5.1	10	ns
$t_{f(Bn)}$	Fall time of port B (output)		V_{CCB} = 3.3 V ± 0.3 V	0.5	5.8	10	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	5.6	10	ns
t_{sk}	Channel-to channel skew	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V			0.5	ns
			V_{CCB} = 5 V ± 0.5 V			0.5	ns
$t_{en(OE-A)}$	Enable time, from OE (input) to A (output), t_{PZL}	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V		140		ns
			V_{CCB} = 5 V ± 0.5 V		140		ns
$t_{en(OE-A)}$	Enable time, from OE (input) to A (output), t_{PZH}		V_{CCB} = 3.3 V ± 0.3 V		150		ns
			V_{CCB} = 5 V ± 0.5 V		150		ns
$t_{dis(OE-A)}$	Disable time, from OE (input) to A (output), t_{PLZ}	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V		180		ns
			V_{CCB} = 5 V ± 0.5 V		180		ns
$t_{dis(OE-A)}$	Disable time, from OE (input) to A (output), t_{PHZ}		V_{CCB} = 3.3 V ± 0.3 V		240		ns
			V_{CCB} = 5 V ± 0.5 V		240		ns
$t_{en(OE-B)}$			V_{CCB} = 3.3 V ± 0.3 V		170		ns

Symbol	Parameters	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
	Enable time, from OE (input) to B (output), t_{PZL}	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 5 V ± 0.5 V		170		ns
$t_{en(OE-B)}$	Enable time, from OE (input) to B (output), t_{PZH}		V_{CCB} = 3.3 V ± 0.3 V		180		ns
			V_{CCB} = 5 V ± 0.5 V		180		ns
$t_{dis(OE-B)}$	Disable time, from OE (input) to B (output), t_{PLZ}	V_{CCA} = 3.3 V ± 0.3 V	V_{CCB} = 3.3 V ± 0.3 V		210		ns
			V_{CCB} = 5 V ± 0.5 V		210		ns
$t_{dis(OE-B)}$	Disable time, from OE (input) to B (output), t_{PHZ}		V_{CCB} = 3.3 V ± 0.3 V		320		ns
			V_{CCB} = 5 V ± 0.5 V		320		ns

(1) *Not test covered, guaranteed by design.*

6.4. Parameter Measurement Information

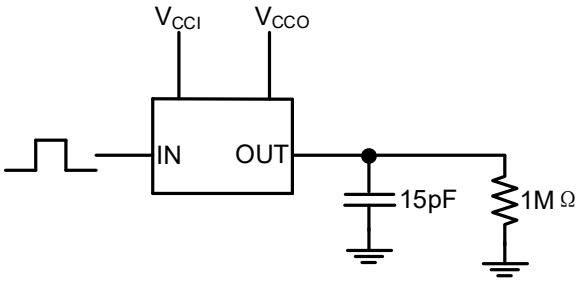


Figure 6.1 Test circuit for data rate, pulse duration, propagation delay, output rise time, and fall time using push-pull driver

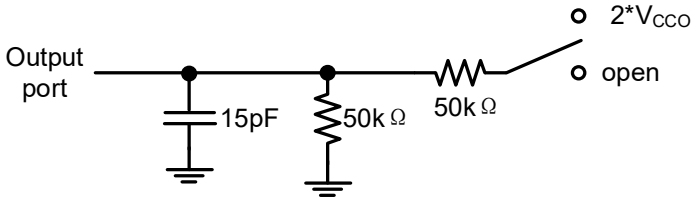


Figure 6.2 Load circuit for enable time and disable time measurement

Notes:

1. S1 switches to 2×V_{CCO} when t_{PZL} and t_{PLZ} are measured.
2. S1 switches to Open when t_{PZH} and t_{PHZ} are measured.
3. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
4. t_{PZL} and t_{PZH} are the same as t_{en}.
5. V_{CCI} is the V_{CCX} associated with the input port.
6. V_{CCO} is the V_{CCX} associated with the output port.

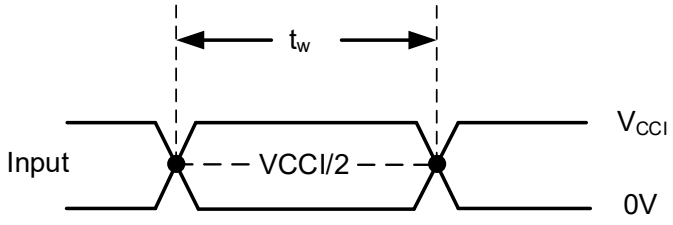


Figure 6. 3 Pulse duration

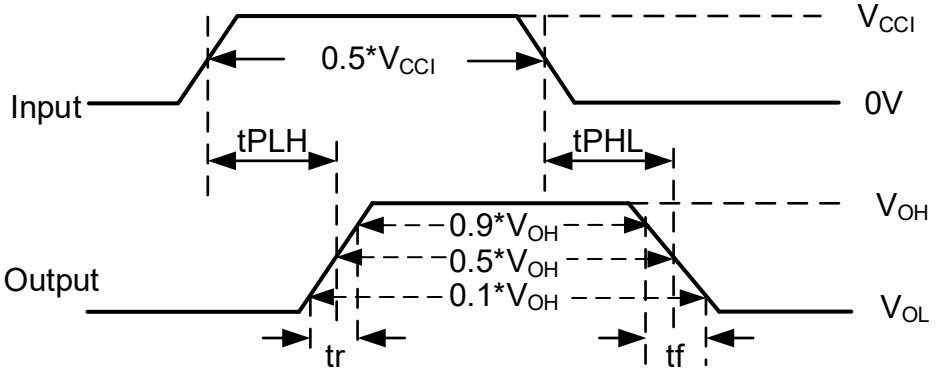


Figure 6.4 Propagation delay, rise and fall time

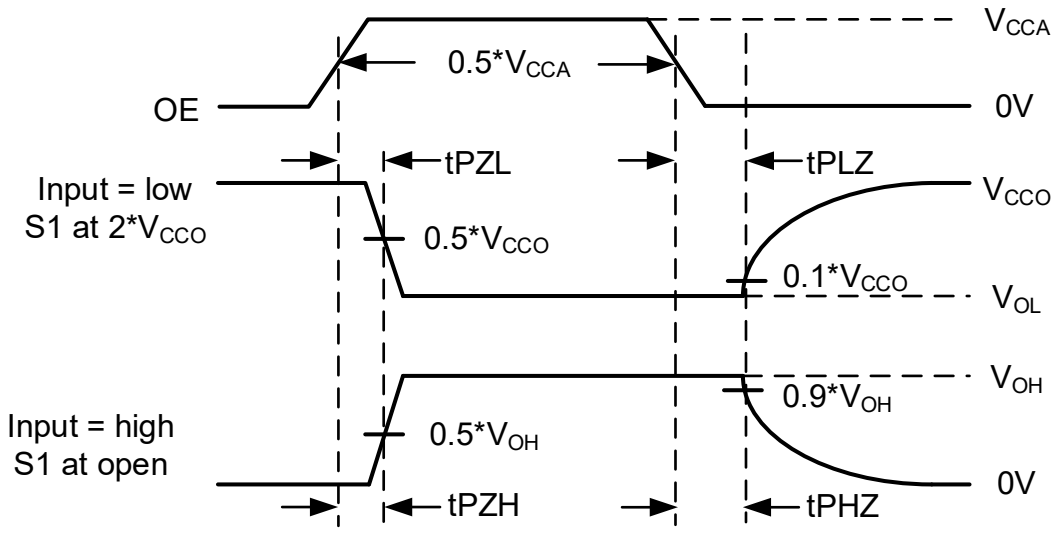


Figure 6.5 Enable and disable time

7. Function Description

7.1. Overview

NCAB0104-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port can accept I/O voltages ranging from 1.1 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device uses a buffered architecture with edge rate accelerator (one shot) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. For open-drain signal translation, please refer to NCAS0104 of NOVOSENSE.

7.2. Functional Block Diagram

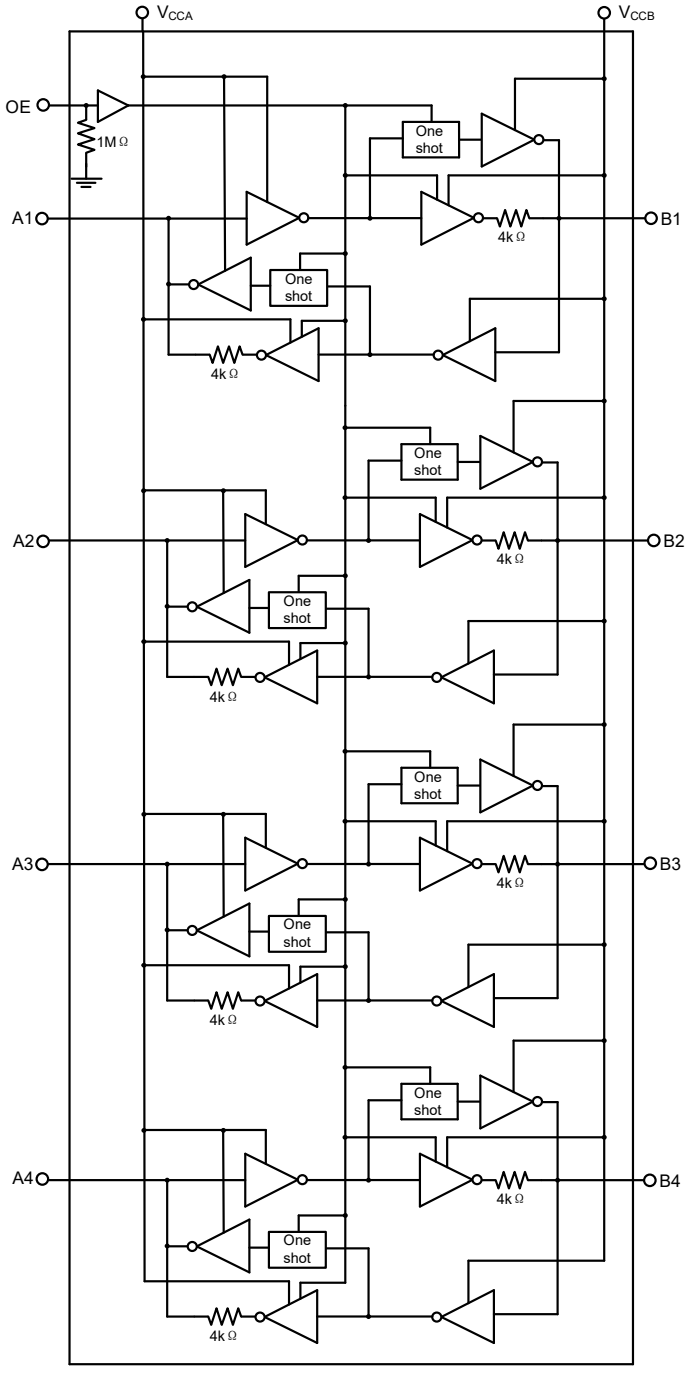


Figure 7.1 Functional block diagram of NCAB0104-Q1

7.3. Architecture

The NCAB0104-Q1 architecture does not need a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the device maintain high or low, but are designed to be weak, so the output drivers can be overdriven by an external driver when data on the bus flows in the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 80 Ω at VCCO = 1.2 V to 1.8 V, 75 Ω at VCCO = 1.8 V to 3.3 V, and 70 Ω at VCCO = 3.3 V to 5 V.

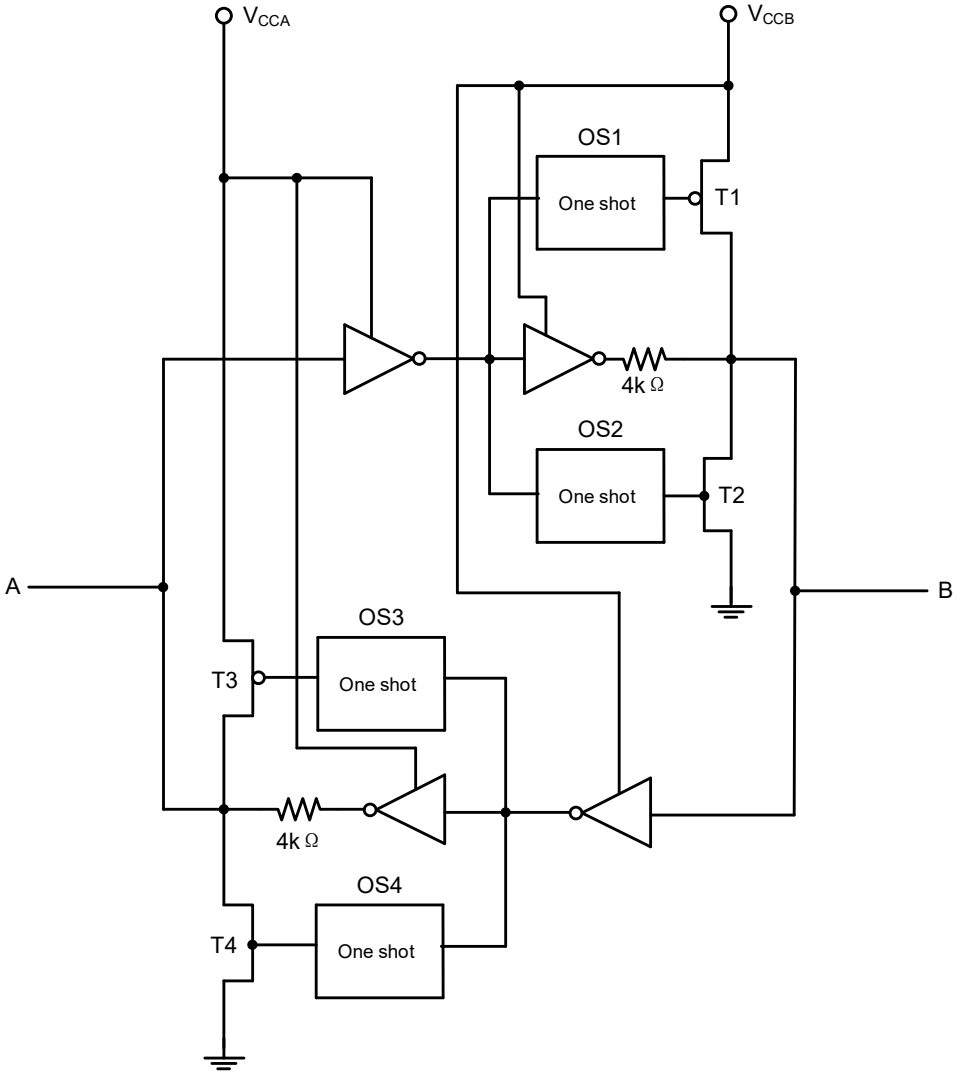


Figure 7.2 Architecture of NCAB0104-Q1 I/O cell

7.4. Input Driver Requirements

For proper operation, the device driving the data I/Os of the NCAB0104-Q1 device must have driving strength of at least ± 2 mA.

7.5. Power Up

During operation V_{CCA} must never be higher than V_{CCB}, however, during power-up $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. There is no special power-up sequencing required. The NCAB0104 includes circuitry that disables all output ports when either V_{CCA} or V_{CCB} is switched off.

7.6. Enable and Disable

The NCAB0104-Q1 device has two functional modes, enabled and disabled. To disable the device, set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver. The OE internally integrates a 1MΩ pull-down resistor, ensuring that the chip is in a disabled state by default after power-up.

The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

7.7. Pull-Up or Pull-Down Resistors on I/O Lines

The device is designed to drive capacitive loads of up to 70 pF. The output drivers of the NCAB0104-Q1 device have low DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the NCAB0104-Q1 device.

Any external pulldown or pullup resistors are recommended to be larger than 50 kΩ.

For the same reason, the NCAB0104 device must not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, please use device NCAS0104 of NOVOSENSE.

8. Typical Application

The NCAB0104-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. For open-drain signal translation, please refer to NCAS0104 of NOVOSENSE.

Unused I/O pins must not be left floating to prevent oscillation caused by high-impedance inputs, which would affect the chip's power consumption and stability. It is recommended to tie idle I/Os to the corresponding V_{CCA}/V_{CCB}.

When performing the PCB layout for NCAB0104-Q1, the following key points need to be considered:

(1) Power decoupling capacitor placement: Choose ceramic chip capacitors with low equivalent series resistance (ESR) and place them as close as possible to the chip's V_{CCA} and V_{CCB} pins. It is recommended to use capacitors with a voltage rating of 10V and a capacitance of 100nF.

(2) Ground connection and return path design: Ensure a reliable electrical connection between the system's ground and the chip's ground on both sides of the chip. Minimize the length of the ground return path and prevent any discontinuity in the ground plane to guarantee the integrity of the grounding system.

(3) Signal trace layout: Keep signal traces as short and wide as possible. Strictly avoid using connectors to prevent excessive capacitive loading, which could negatively impact signal quality and system performance.

(4) Impedance matching design: Reserve positions for series resistors on the I/O signal traces. This allows for impedance matching, which can significantly improve signal integrity and ensure more stable signal transmission.

(5) To ensure the chip operates properly, the I/O load of NCAB0104-Q1 must not exceed 70 pF.

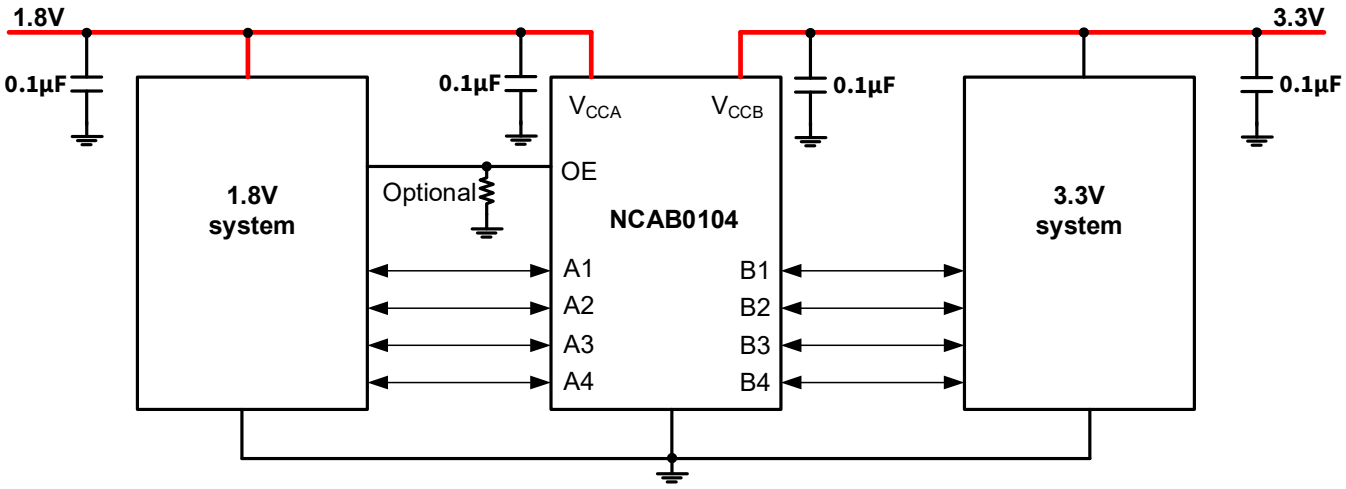
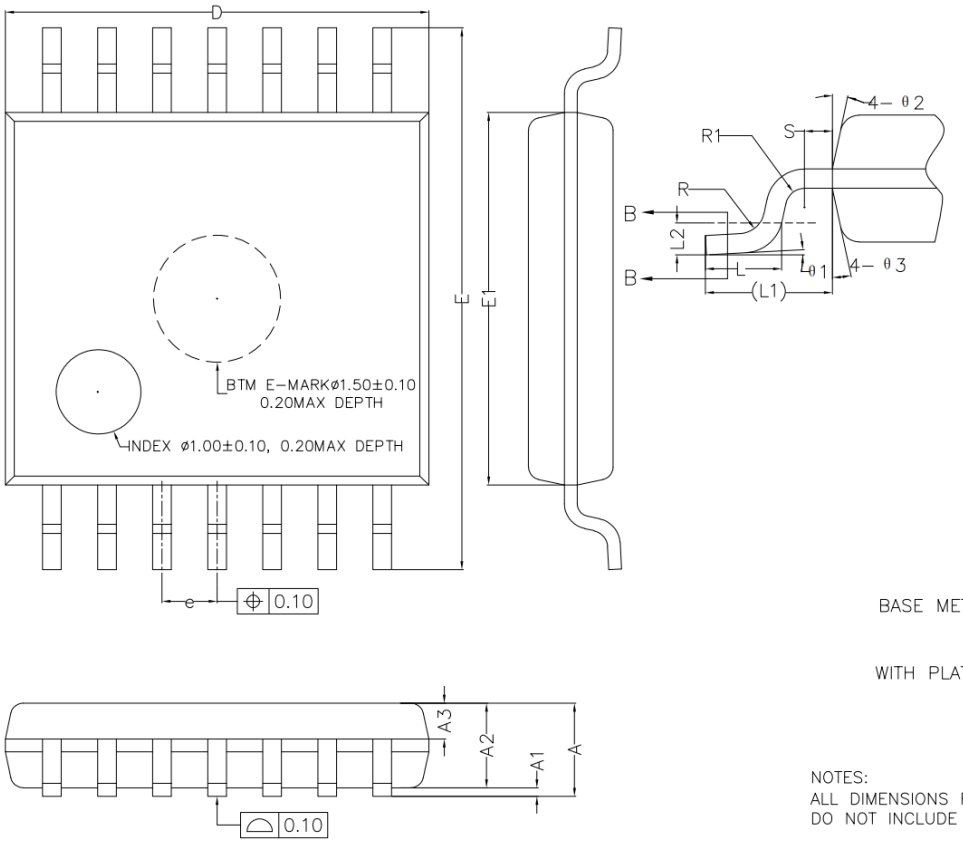


Figure 8.1 Typical application of NCAB0104-Q1

9. Package Information

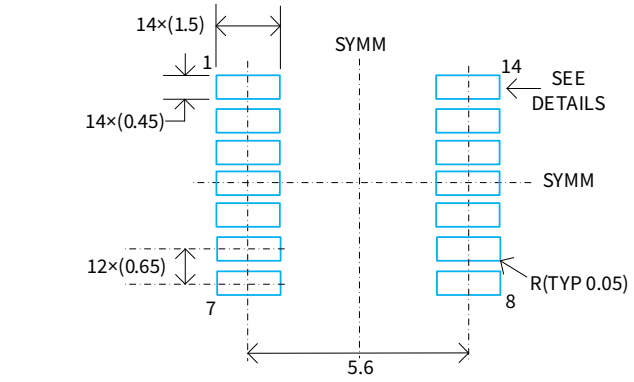


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.32	0.42	0.52
b	0.20	–	0.29
b1	0.19	0.22	0.25
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AB-1
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 9.1 TSSOP14 package shape and dimension in millimeters for NCAB0104-Q1TSKR



LAND PATTERN EXAMPLE(mm)

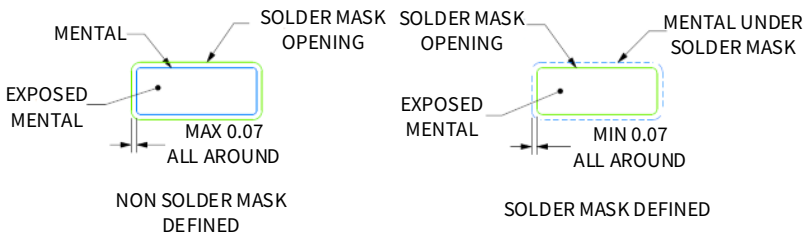
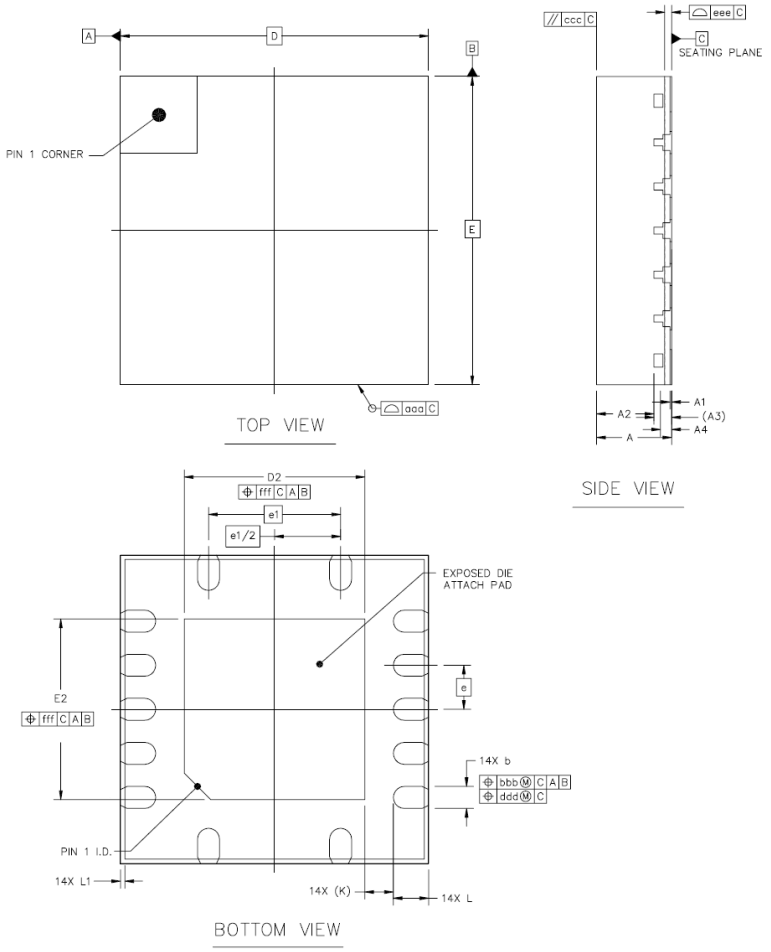


Figure 9.2 TSSOP14 package board layout example for NCAB0104-Q1TSKR



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.8500	0.9
STAND OFF		A1	0	0.02	0.0500
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.1	---	0.1800
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3.5 BSC	
	Y	E		3.5 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		1.5 BSC	
EP SIZE	X	D2	1.95	2.05	2.15
	Y	E2	1.95	2.05	2.15
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.0100	---	0.0900
LEAD TIP TO EXPOSED PAD EDGE		K		0.325 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1000	
MOLD FLATNESS		ccc		0.1000	
COPLANARITY		eee		0.0800	
LEAD OFFSET		bbb		0.1000	
		ddd		0.0500	
EXPOSED PAD OFFSET		fff		0.1000	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP • Sn8~20s

Figure 9.3 VQFN14 package shape and dimension in millimeters for NCAB0104-Q1QBCR

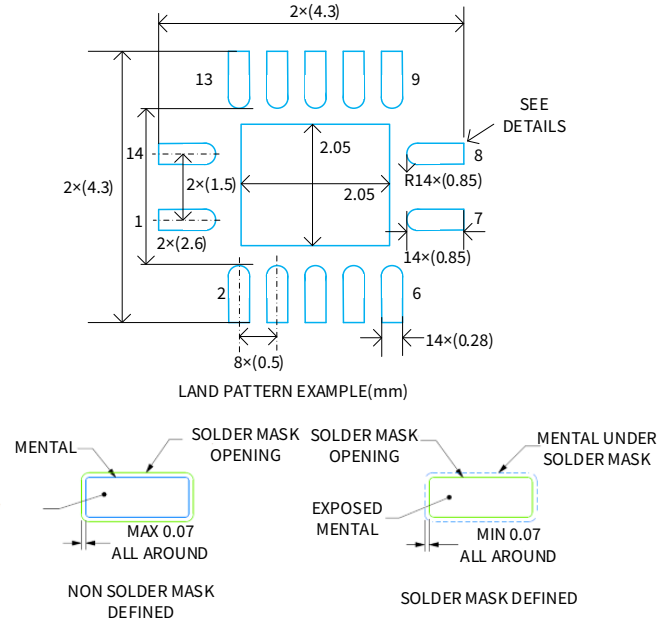
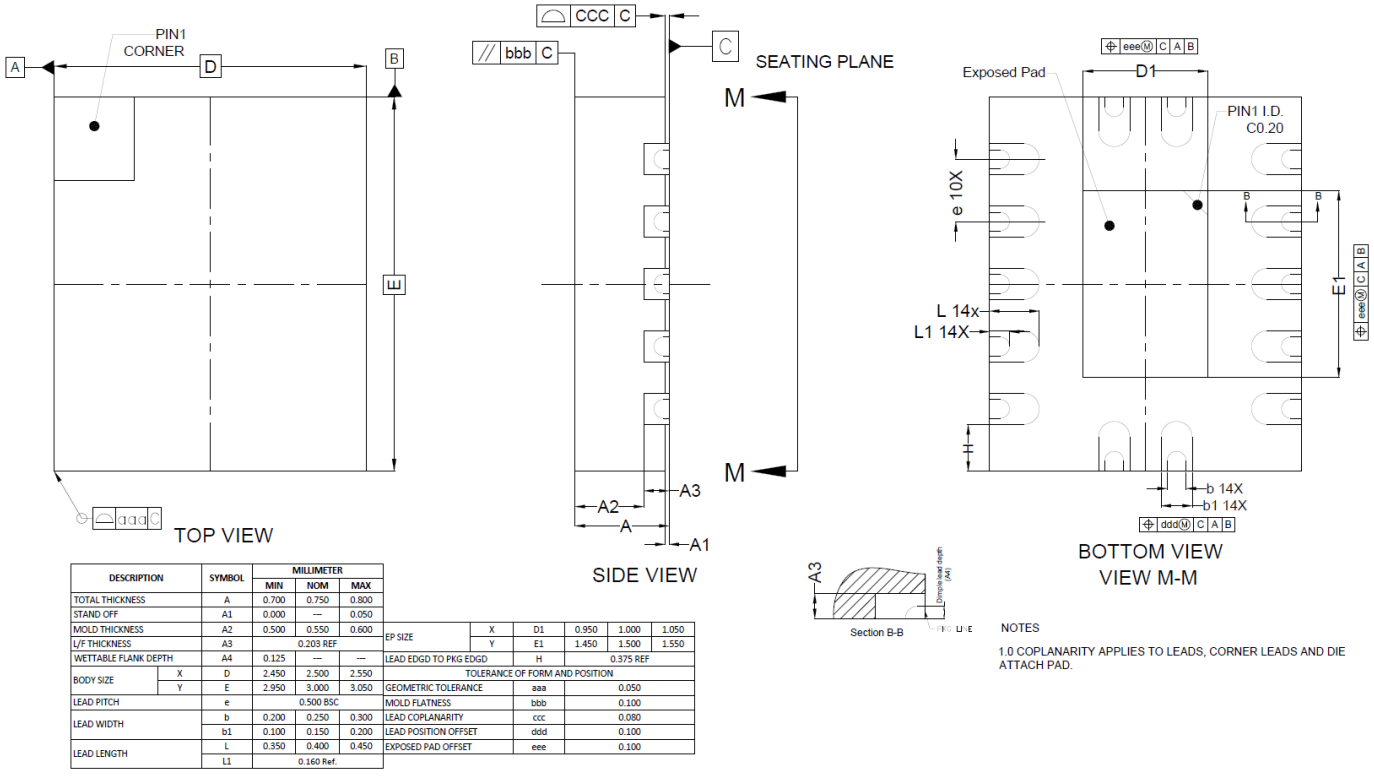


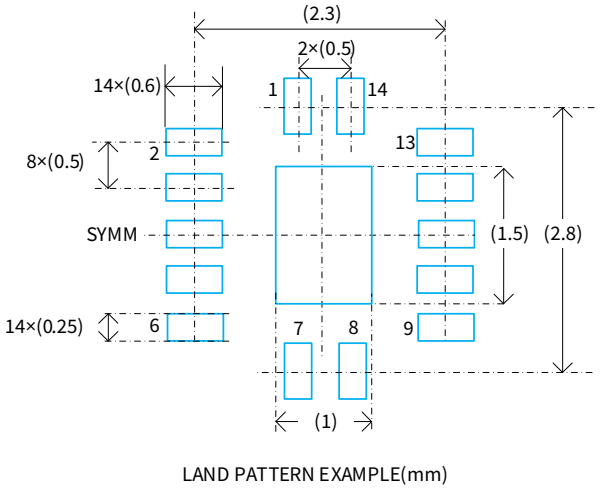
Figure 9.4 VQFN14 package board layout example for NCAB0104-Q1QBCR



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	---	0.050
MOLD THICKNESS		A2	0.500	0.550	0.600
L/F THICKNESS		A3		0.203 REF	
WETTABLE FLANK DEPTH		A4	0.125	---	---
BODY SIZE	X	D	2.450	2.500	2.550
	Y	E	2.950	3.000	3.050
LEAD PITCH		e		0.500 BSC	
LEAD WIDTH		b	0.200	0.250	0.300
		b1	0.100	0.150	0.200
LEAD LENGTH		L	0.350	0.400	0.450
		L1		0.160 Ref.	

EP SIZE	X	D1	0.950	1.000	1.050
	Y	E1	1.450	1.500	1.550
LEAD EDGD TO PKG EDGD		H		0.375 REF	
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa		0.050	
MOLD FLATNESS		bbb		0.100	
LEAD COPLANARITY		ccc		0.080	
LEAD POSITION OFFSET		ddd		0.100	
EXPOSED PAD OFFSET		eee		0.100	

Figure 9.5 WQFN14 package shape and dimension in millimeters for NCAB0104-Q1QDDR



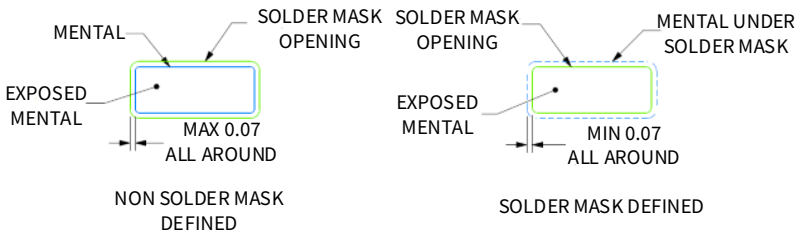
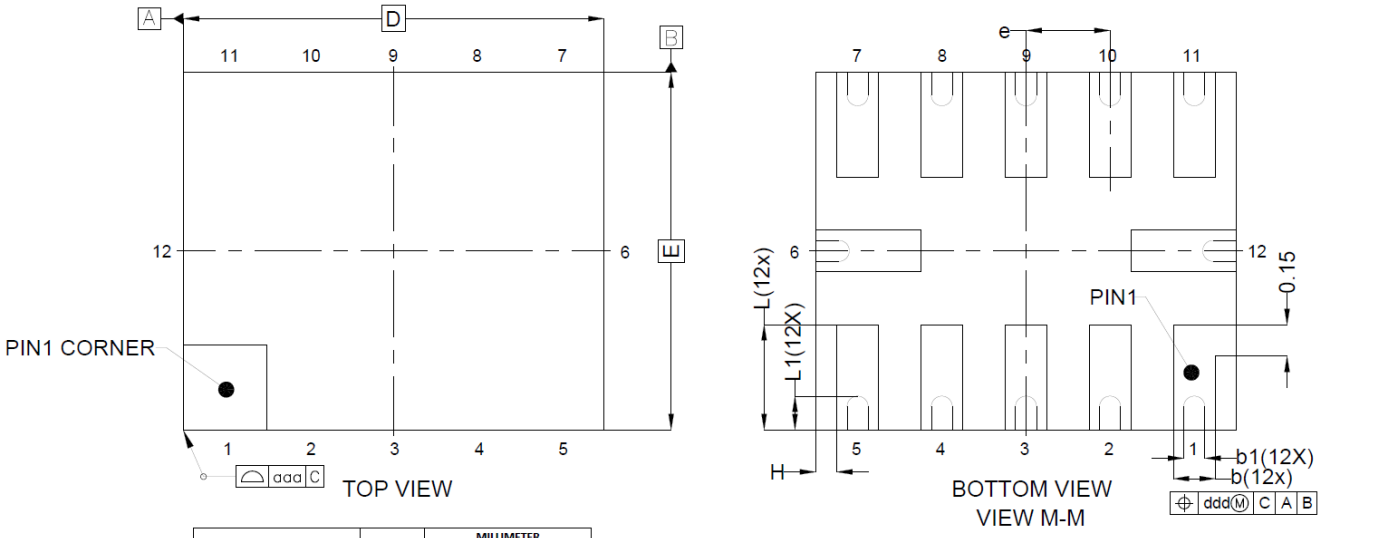


Figure 9.6 WQFN14 package board layout example for NCAB0104-Q1QDDR



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.500	0.550	0.600
STAND OFF		A1	0.000	---	0.050
MOLD THICKNESS		A2	0.350	0.400	0.450
L/F THICKNESS		A3	0.152 REF		
BODY SIZE	X	D	1.950	2.000	2.050
	Y	E	1.650	1.700	1.750
LEAD PITCH		e	0.400 BSC		
LEAD WIDTH		b	0.150	0.200	0.250
		b1	0.050	0.100	0.150
LEAD LENGTH		L	0.450	0.500	0.550
		L1	0.110	0.160	0.210
LEAD EDGD TO PKG EDGE		H	0.100 REF		
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa	0.050		
MOLD FLATNESS		bbb	0.100		
LEAD COPLANARITY		ccc	0.080		
LEAD POSITION OFFSET		ddd	0.100		

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.7 UQFN12 package shape and dimension in millimeters for NCAB0104-Q1QBDR

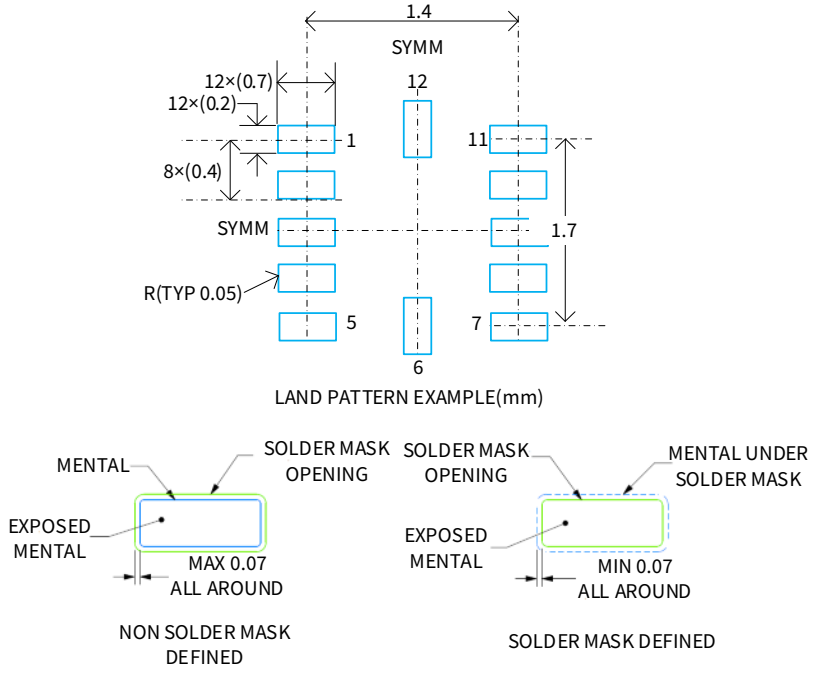
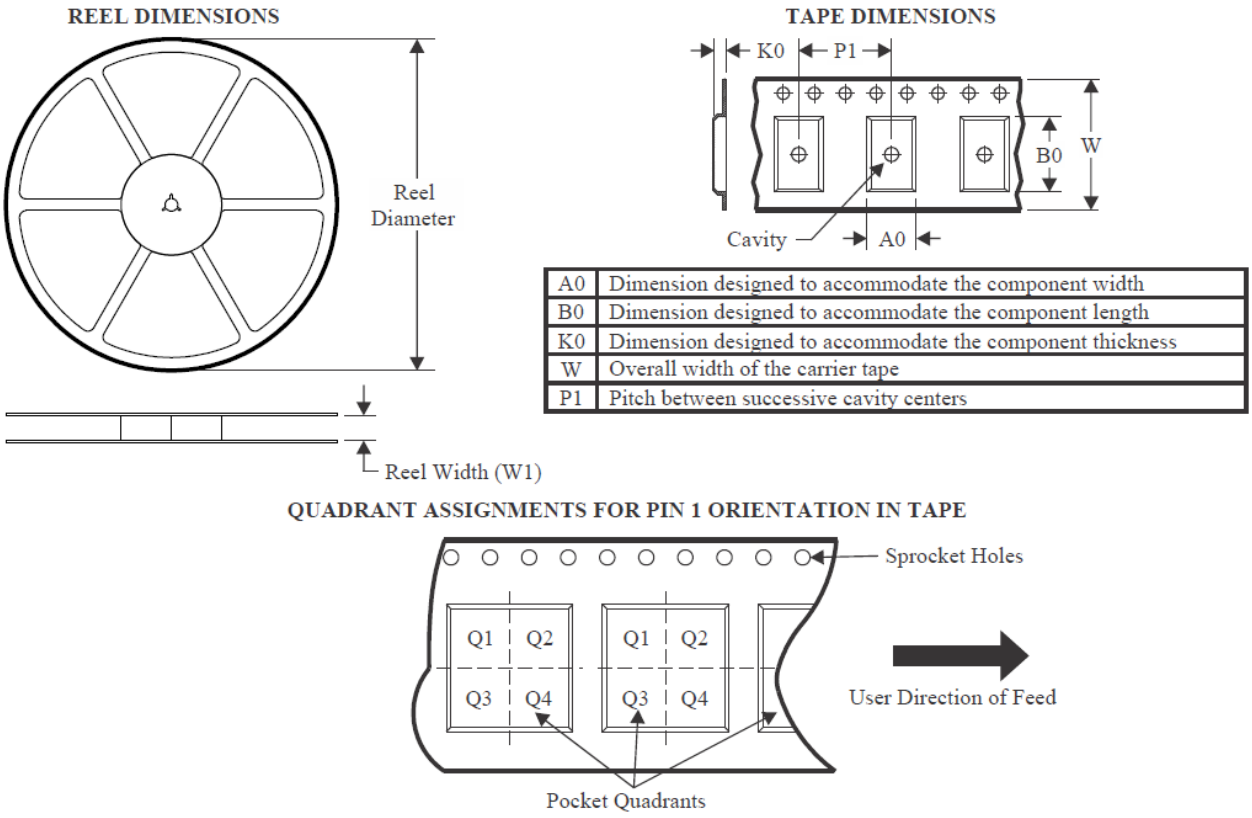


Figure 9.8 UQFN12 package board layout example for NCAB0104-Q1QBDR

10. Ordering Information

Part Number	Operating Temperature	MSL	Package	SPQ	MPQ
NCAB0104-Q1TSKR	-40 °C to 125 °C	3	TSSOP14	4000	4000
NCAB0104-Q1QBCR	-40 °C to 125 °C	3	VQFN14	5000	5000
NCAB0104-Q1QDDR	-40 °C to 125 °C	3	WQFN14	3000	3000
NCAB0104-Q1QBDR	-40 °C to 125 °C	3	UQFN12	3000	3000

11. Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 11.1 Tape and Reel Information in millimeters

Devices	*Package*	*Pins*	*Reel Diameter (mm)*	*Reel Width W1 (mm)*	*A0 (mm)*	*B0 (mm)*	*K0 (mm)*	*P1 (mm)*	*W (mm)*	*Pin1 Quadrant*
NCAB0104-Q1TSKR	TSSOP14	14	330	12.4	6.85	5.45	1.6	8.0	12.0	Q1
NCAB0104-Q1QBCR	VQFN14	14	330	12.4	3.8	3.8	1.1	8.0	12.0	Q1
NCAB0104-Q1QDDR	WQFN14	14	178	13.5	2.8	3.3	1.2	4.0	12.0	Q1
NCAB0104-Q1QBDR	UQFN12	12	178	9.5	1.9	2.2	0.65	4.0	8.0	Q1

12. Revision History

Revision	Description	Date
1.0	Initial version	2026/5/11

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