NOVOSENSE

NCA3176/NCA3492

Half and Full-Duplex RS-485 Transceivers

Datasheet (EN) 1.1

Product Overview

NCA3176 is a half-duplex RS-485 transceiver and NCA3492 is a full-duplex RS-485 transceiver, both with a power supply range of 3.0 to 5.5V. They exceed TIA-485-A specification and industrial applications.

The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The data rate of the device is up to 20Mbps. The devices are slew limited to reduce EMI and reflections with improperly terminated transmission line.

The Bus pins are protected from ±8kV system level ESD to GND. The devices feature fail-safe circuitry, which guarantee a logic-high receiver output when the receiver inputs are open or shorted.

Key Features

- Power supply voltage: 3.0V to 5.5V
- Individual driver and receiver enable
- High system level EMC performance:
  - Bus Pins meet IEC61000-4-2 ±8kV ESD
  - Bus Pins meet ±20kV HBM protection
- Fail-safe protection receiver
- Up to 256 transceivers on the bus
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  - SOP8
  - MSOP8
  - SOP14
- Exceeds TIA-485-A Specifications
- Signaling Rate up to 20 Mbps

Applications

- Industrial automation system
- RS-485 communication
- E-Metering Networks
- Motion Controllers

Device Information

Part Number	*Package*	*Body Size*
NCA3176-DSPR	SOP8	4.90mm × 3.90mm
NCA3176-DMSR	MSOP8	3.00mm × 3.00mm
NCA3492-DSPKR	SOP14	8.65mm × 3.90mm

Functional Block Diagrams

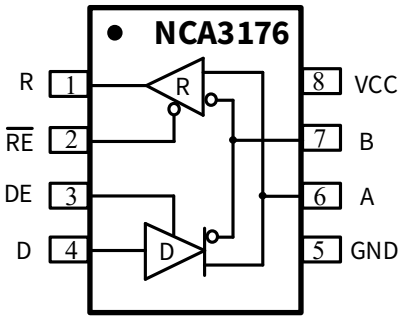


Figure 1. NCA3176 Block Diagram

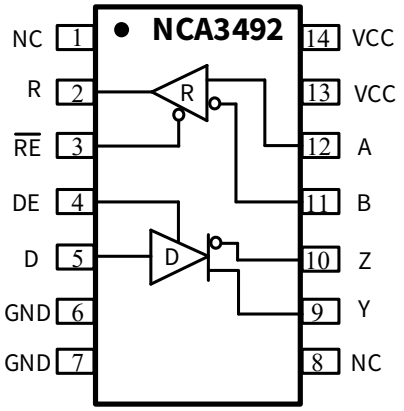


Figure 2. NCA3492 Block Diagram

Copyright © 2025, NOVOSENSE

INDEX

Copyright © 2025, NOVOSENSE

1. Pin Configuration and Functions

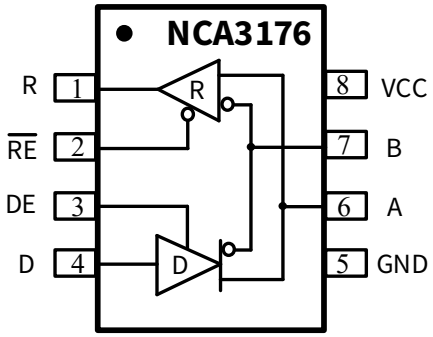


Figure 1.1 NCA3176 Package

Table 1.1 NCA3176 Pin Configuration and Description

NCA3176 PIN NO.	*SYMBOL*	*FUNCTION*
1	R	Receive output
2	/RE	Receive enable input. This is an active low input.
3	DE	Driver enable input. This is an active high input
4	D	Driver transmit data input.
5	GND	Ground.
6	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when VDD is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
7	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
8	VCC	Power Supply.

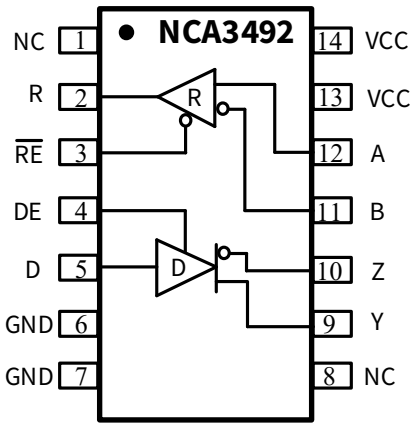


Figure 1.2 NCA3492 Package

Copyright © 2025, NOVOSENSE

Table 1.2 NCA3492 Pin Configuration and Description

NCA3492 PIN NO.	SYMBOL	FUNCTION
1	NC	No Connection.
2	R	Receive output
3	/RE	Receive enable input. This is an active low input.
4	DE	Driver enable input. This is an active high input
5	D	Driver transmit data input.
6	GND	Ground.
7	GND	Ground.
8	NC	No Connection.
9	Y	Noninverting Driver Output. When the driver is disabled, or when VCC is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
10	Z	Inverting Driver Output. When the driver is disabled, or when VCC is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
11	B	Inverting Receiver Input.
12	A	Noninverting Receiver Input.
13	VCC	Power Supply.
14	VCC	Power Supply.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VCC	-0.5		6	V	
Maximum Input Voltage	/RE, DE, D	-0.4		VCC+0.4	V	
Driver Output/Receiver Input Voltage	V_A, V_B, V_Y, V_Z	-18		18	V	
Differential input voltage, A with repect to B	V_{ID}	-18		18	V	
Receiver Output Current	I_o	-15		15	mA	
Operating Temperature	T_{opr}	-40		125	℃	
Storage Temperature	T_{stg}	-40		150	℃	
Junction Temperature	T_j	-40		150	℃	

Copyright © 2025, NOVOSENSE

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins ● Bus pins to GND	 ±8.0 ±20.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	 ±2.0	kV
	IEC61000-4-2 (Bus pins)	±8.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VCC	3		5.5	V	
High-level Input Voltage	V_{IH}	2		VCC	V	
Low-level Input Voltage	V_{IL}	0		0.8	V	
Voltage at any bus terminal (separately or common mode)	V_I	-7		12	V	
Differential input voltage	V_{ID}	-12		12	V	
High-level output current	I_{OH}	-8			mA	
Low-level output current	I_{OL}			8	mA	
Ambient Temperature	T_a	-40		125	℃	

5. Thermal Information

Parameters	Symbol	SOP8	MSOP8	SOP14	Unit
Junction-to-ambient thermal resistance	θ_{JA}	67.9	168.7	96.25	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	27.7	62.2	50	°C/W
Junction-to-board thermal resistance	θ_{JB}	29.4	89.5	61	°C/W

Copyright © 2025, NOVOSENSE

6. Specifications

6.1. Electrical Characteristics

(VCC=3.0V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VCC = 5.0V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power supply voltage	VCC	3.0		5.5	V	
supply current	I_{CC}		900	1800	μA	DE=High, /RE=Low, no load
			600	1000	μA	DE=High, /RE=High, no load
			630	1200	μA	DE=Low, /RE=Low, no load
			0.5	5	μA	DE=Low, /RE=High, no load
Thermal-Shutdown Threshold	T_{TS}		165		℃	
Thermal-Shutdown Hysteresis	T_{TSH}		15		℃	
Logic Side						
Input High Voltage	V_{IH}	2			V	DE, D, /RE
Input Low Voltage	V_{IL}			0.8	V	DE, D, /RE
Input Current	I_{IN}	-2		2	μA	DE, D, /RE
Output Voltage High	V_{OH}	VCC-0.5			V	I_{OH} = -8mA, R
Output Voltage Low	V_{OL}			0.5	V	I_{OL} = 8mA, R
Output Short-Circuit Current	I_{OSR}	-95		95	mA	0 ≤ V_R ≤VCC
Three-State Output Current	I_{OZR}	-15		1	μA	0 ≤ V_R ≤ VCC, /RE = High
Driver						
Input clamp voltage	V_{IK}	-1.5			V	I_I = –18 mA
Differential Output Voltage	| V_{OD} |			VCC	V	No Load
		1.5	3.2		V	see Figure 6. 1, R_L=54Ω(RS-485)
		2	3.6		V	see Figure 6. 2, R_L=100Ω (RS-422), VCC≥3.2V, Tj ≥ 0℃
		1.5	3.2		V	see Figure 6. 3, R_L=60Ω，375Ω on each output to -7V to 12V
Change in magnitude of the differential output voltage	Δ|V_{OD} |	-200		200	mV	See Figure 6. 1,R_L=54Ω, C_L=50pF

Copyright © 2025, NOVOSENSE

Steady-state common-mode output voltage	V_{OC}	1	VCC/2	3	V	See Figure 6. 4
Change in differential driver output common-mode voltage	$\Delta V_{OC(SS)}$	-200		200	mV	See Figure 6. 4
Peak-to-peak driver common-mode output voltage	$V_{OC(PP)}$		450		mV	See Figure 6. 4
Driver Short-Circuit Output Current	I_{OSD}	-250		250	mA	-7V ≤ V_O ≤ +12 V
Output Leakage Current (Y and Z) Full-Duplex	I_I			200	μA	V_I =12V, DE=Low
		-200				V_I =-7V, DE=Low
Receiver						
Positive-going receiver differential input voltage threshold	V_{TH+}			-10	mV	DE=/RE=Low
Negative-going receiver differential input voltage threshold	V_{TH-}	-200			mV	DE=/RE=Low
Receiver differential input voltage threshold hysteresis	V_{hys-}		30		mV	DE=/RE=Low
Bus input current (disabled driver)	I_I			200	μA	V_I =12V, DE=Low
		-200			μA	V_I =-7V, DE=Low
Receiver Input Resistance	R_{IN}	96			kΩ	−7V ≤ V_I ≤ 12V, DE=Low

6.2. Switching Electrical Characteristics

(VDD=3.0V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VCC = 5V Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Driver						
Maximum Data Rate	f_{MAX}			20	Mbps	
Driver Propagation Delay	t_{PLH}		6	15	ns	see Figure 6. 5, R_L=54Ω, C_L=50pF
	t_{PHL}		6	15	ns	see Figure 6. 5, R_L=54Ω, C_L=50pF
Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$			1	4	ns	
Driver Output Falling Time or Rising time	t_f		4.5	10	ns	see Figure 6. 5, R_L=54Ω, C_L=50pF
	t_r		4.5	10	ns	see Figure 6. 5, R_L=54Ω, C_L=50pF
Driver-Output enable time to high level	t_{PZH}			40	ns	See Figure 6. 6，/RE=Low

Copyright © 2025, NOVOSENSE

			1.5	6	μs	see Figure 6. 6，/RE=High
Driver-Output enable time to low level	t_{PZL}			40	ns	see Figure 6. 7，/RE=Low
			1.5	6	μs	see Figure 6. 7，/RE=High
Driver-Output disable time from high level	t_{PHZ}			50	ns	See Figure 6. 6
Driver-Output disable time from low level	t_{PLZ}			50	ns	see Figure 6. 7
Receiver						
Receiver Propagation Delay	t_{PLH}		70	130	ns	See Figure 6. 8,C_L=15pF
	t_{PHL}		70	130	ns	See Figure 6. 8,C_L=15pF
Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				5	ns	
Receiver Output Falling Time or Rising time	t_f		2	5	ns	see Figure 6. 8,C_L=15pF
	t_r		2	5	ns	see Figure 6. 8,C_L=15pF
Receiver Disable to Output High	t_{PHZ}			50	ns	see Figure 6. 9
Receiver Disable to Output Low	t_{PLZ}			50	ns	see Figure 6. 9
Receiver Enable to Output High	$t_{PZH(1)}$			145	ns	see Figure 6. 9,DE=High
	$t_{PZH(2)}$		1	6	μs	see Figure 6. 10,DE=Low
Receiver Enable to Output Low	$t_{PZL(1)}$			115	ns	see Figure 6. 9,DE=High
	$t_{PZL(2)}$		1	6	μs	see Figure 6. 10,DE=Low

6.3. Parameter Measurement Information

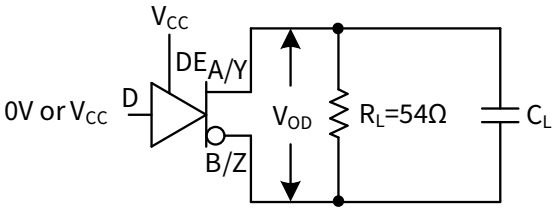


Figure 6. 1 Measurement of Driver Differential Output Voltage With RS-485 Load

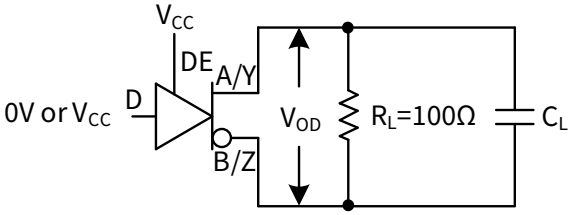


Figure 6. 2 Measurement of Driver Differential Output Voltage With RS-422 Load

Copyright © 2025, NOVOSENSE

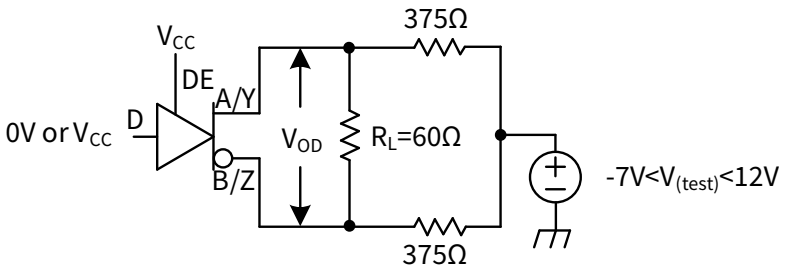


Figure 6. 3 Measurement of Driver Differential Output Voltage With Common-Mode Load

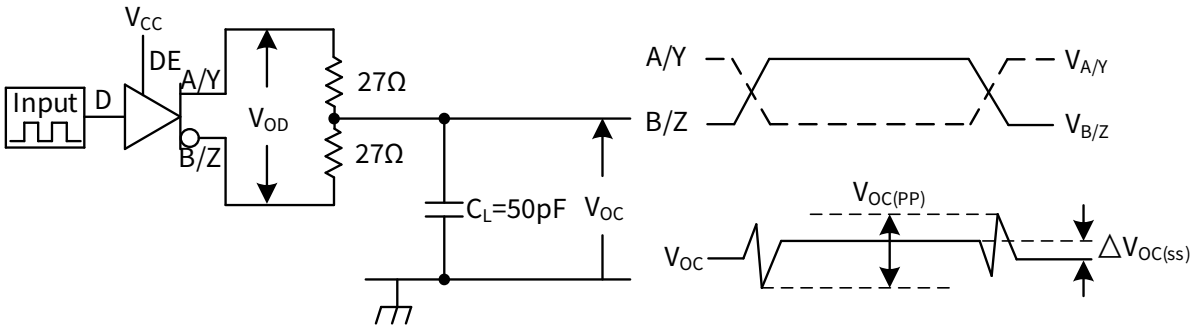


Figure 6. 4 Measurement of Driver Common-Mode Output Voltage With RS-485 Load

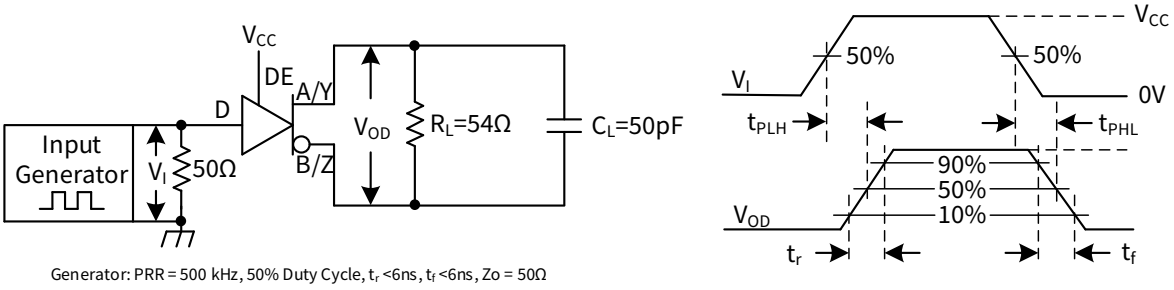


Figure 6. 5 Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays of NCA3176 and NCA3492

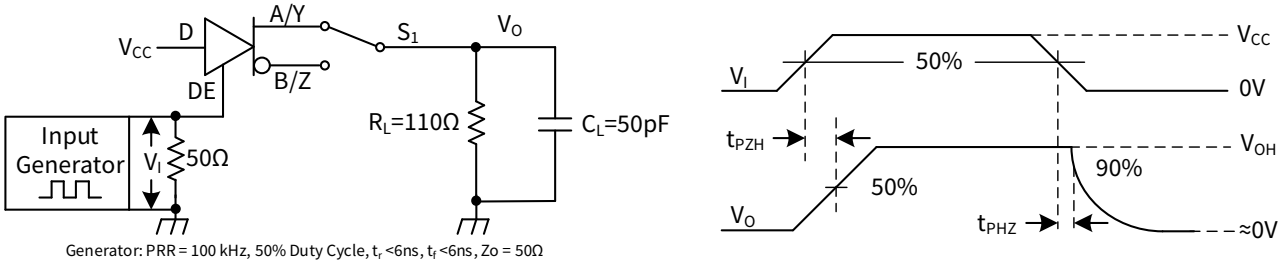


Figure 6. 6 Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load of NCA3176 and NCA3492

Copyright © 2025, NOVOSENSE

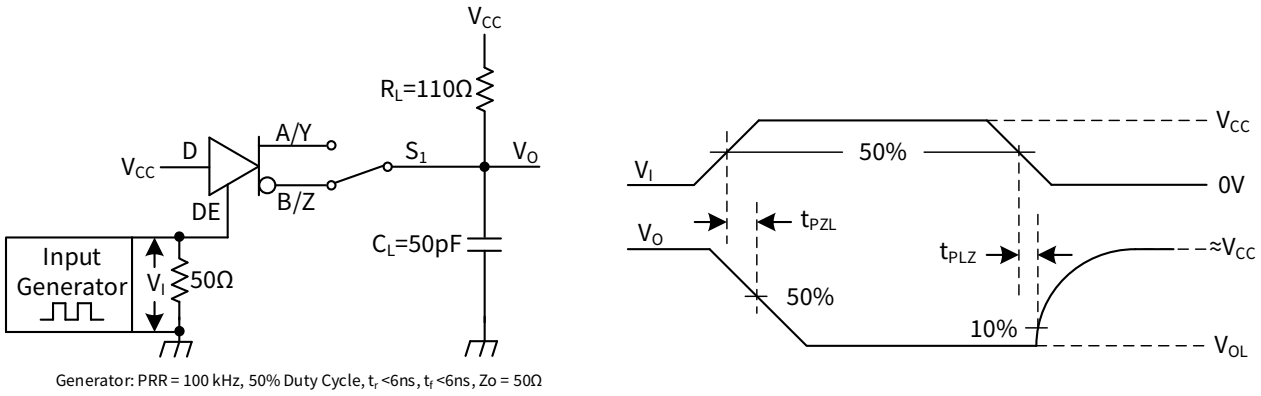


Figure 6. 7 Measurement of Driver Enable and Disable Times With Active Low Output and Pull-Up Load of NCA3176 and NCA3492

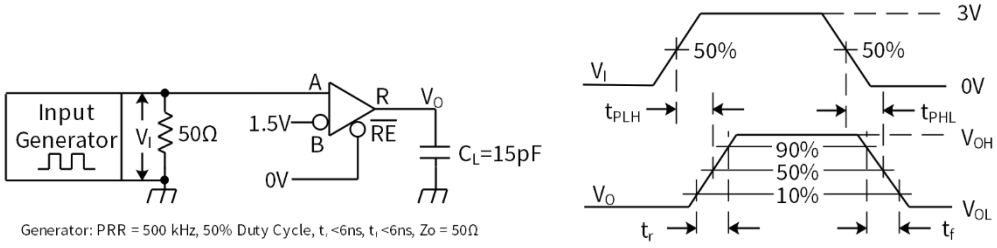


Figure 6. 8 Measurement of Receiver Output Rise and Fall Times and Propagation Delays of NCA3176 and NCA3492

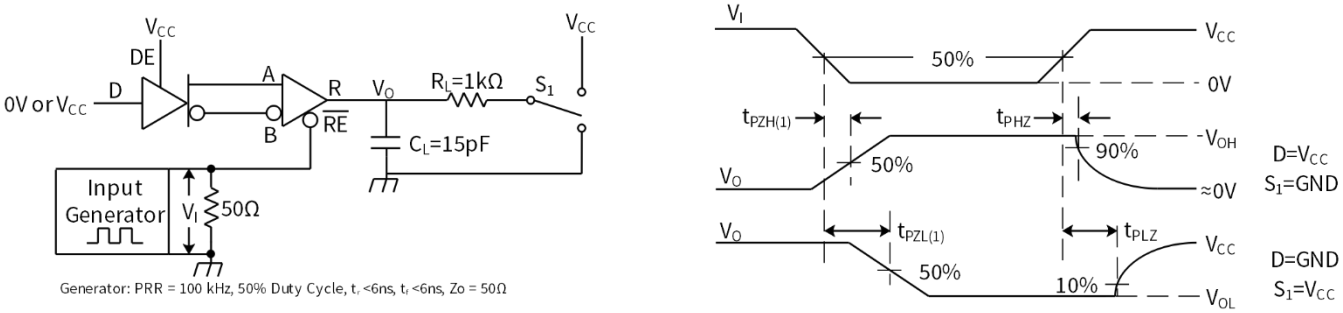


Figure 6. 9 Measurement of Receiver Enable/Disable Times With Driver Enabled of NCA3176 and NCA3492

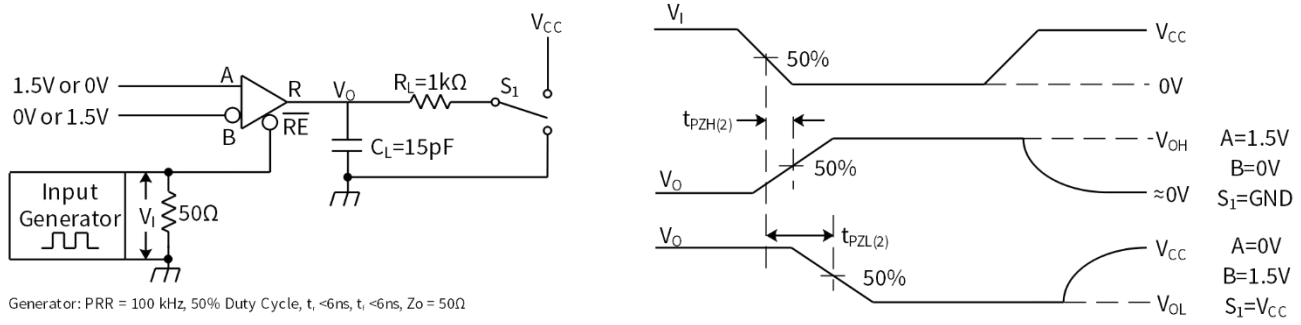


Figure 6. 10 Receiver Enable Time From Standby (Driver Disabled) of NCA3176 and NCA3492

Copyright © 2025, NOVOSENSE

6.4. Typical Performance Characteristics

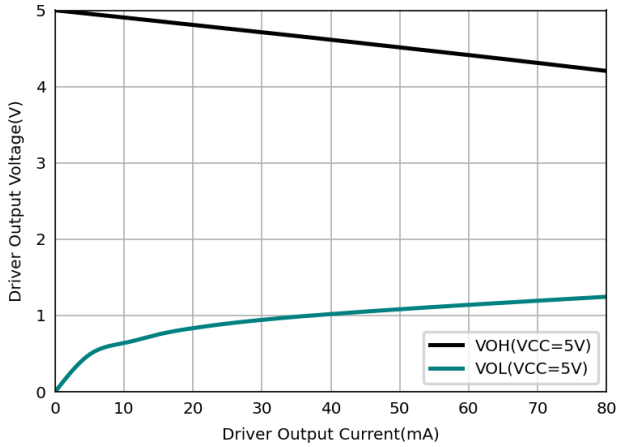


Figure 6.11 Relationship between driver voltage and current

7. Function Description

7.1. Overview

NCA3176 is a half-duplex RS-485 transceiver and NCA3492 is a full-duplex RS-485 transceiver, both with a power supply range of 3.0 to 5.5V. They exceed TIA-485-A specification and industrial applications. The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The data rate of the device is up to 20Mbps. The devices are slew limited to reduce EMI and reflections with improperly terminated transmission line. The Bus pins are protected from ±8kV system level ESD to GND. The devices feature fail-safe circuitry, which guarantee a logic-high receiver output when the receiver inputs are open or shorted.

7.2. Data rate

The data rate of NCA3176 and NCA3492 are 20Mbps. The devices are slew limited to reduce EMI and reflections with improperly terminated transmission line.

7.3. Functional Block Diagram

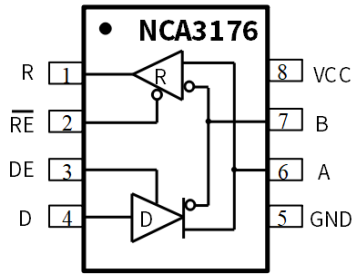


Figure 7. 1 NCA3176 Block Diagram

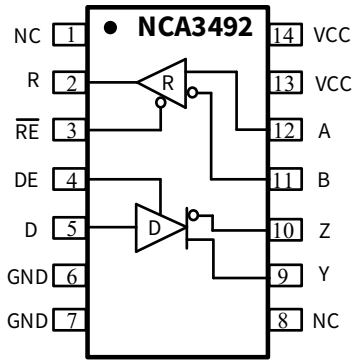


Figure 7.2 NCA3492 Block Diagram

Copyright © 2025, NOVOSENSE

7.4. True Fail-safe receiver inputs

The devices feature fail-safe circuitry, which guarantee a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -10mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage (V_A-V_B) is greater than or equal to -10mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

7.5. Truth tables

Table 7.1 Driver Function Table[1]

Input (D)	*Enable Input (DE)*	*Outputs[1]*	
		A	*B*
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	L	H

H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.

Table 7.2 Receiver Function Table[1]

Differential Input (V_A-V_B)	*Enable Input (/RE)*	*Output (R)*
≥-10mV	L/Open	H
≤-200mV	L/Open	L
Open/Short	L/Open	H
X	H	Z
Idle	L	H

H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.

7.6. Thermal shutdown

The devices are protected from over temperature damage by integrated thermal shutdown circuitry. When the junction temperature (T_j) exceeds +165°C (typ), the driver outputs go high-impedance. The devices resume normal operation when T_j falls below +145°C (typ).

Copyright © 2025, NOVOSENSE

8. Application Note

8.1. Typical Application Circuit

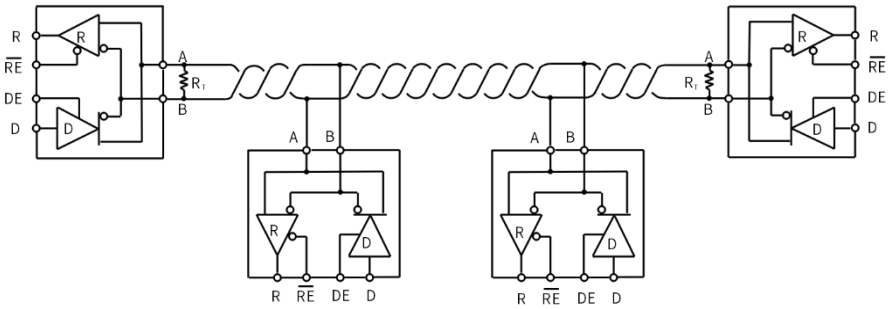


Figure 8.1 Typical RS-485 Network with Half-Duplex Transceivers

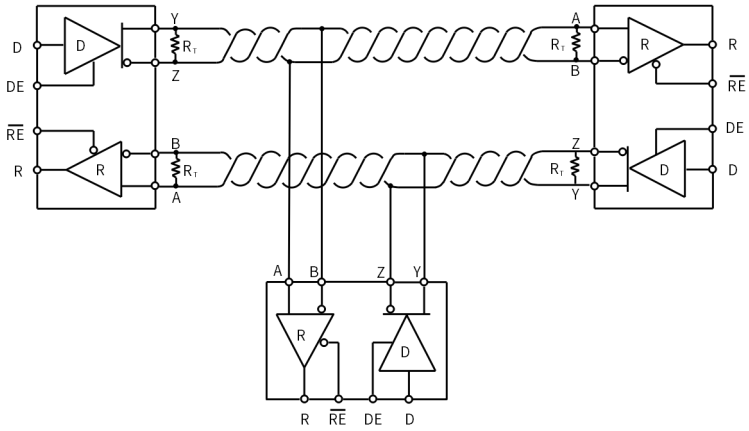


Figure 8.2 Typical RS-485 Network With Full-Duplex Transceivers

8.2. PCB Layout

The devices require a 0.1 μF bypass capacitor between VCC and GND. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to have the bus connectors and termination resistor as close as possible to the A and B Bus pins.

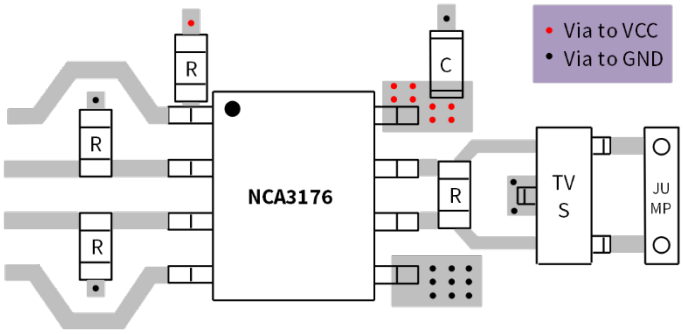


Figure 8.3 NCA3176 Layout Example

8.3. Nodes on the bus

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

Copyright © 2025, NOVOSENSE

8.4. ESD protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handing and assembly.

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- ± 20kV HBM.
- ±8kV using the contact discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±8kV HBM

8.5. Surge protection

If the surge is transient, the high energy content has the characteristics of long pulse duration and slow pulse power attenuation. The transient electrical energy injected into the protective unit inside the transceiver is converted to thermal energy, which heats up and destroys the protective unit, thus destroying the transceiver. Therefore, the following diagram shows a protection circuit against surge transients (IEC 61000-4-5). R_1 and R_2 are current limiting resistors.

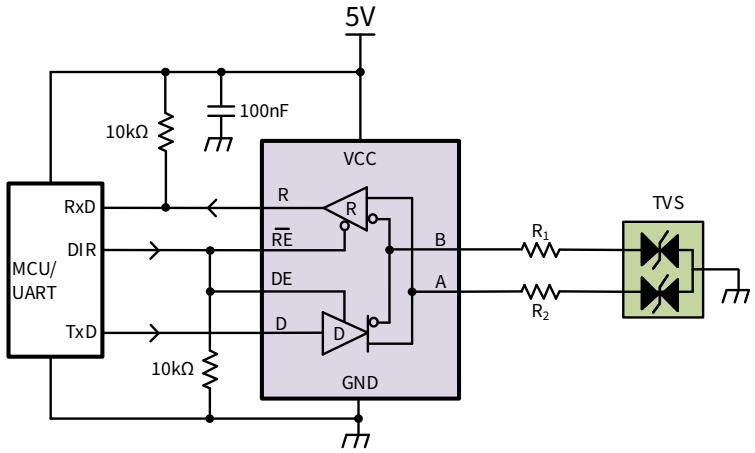
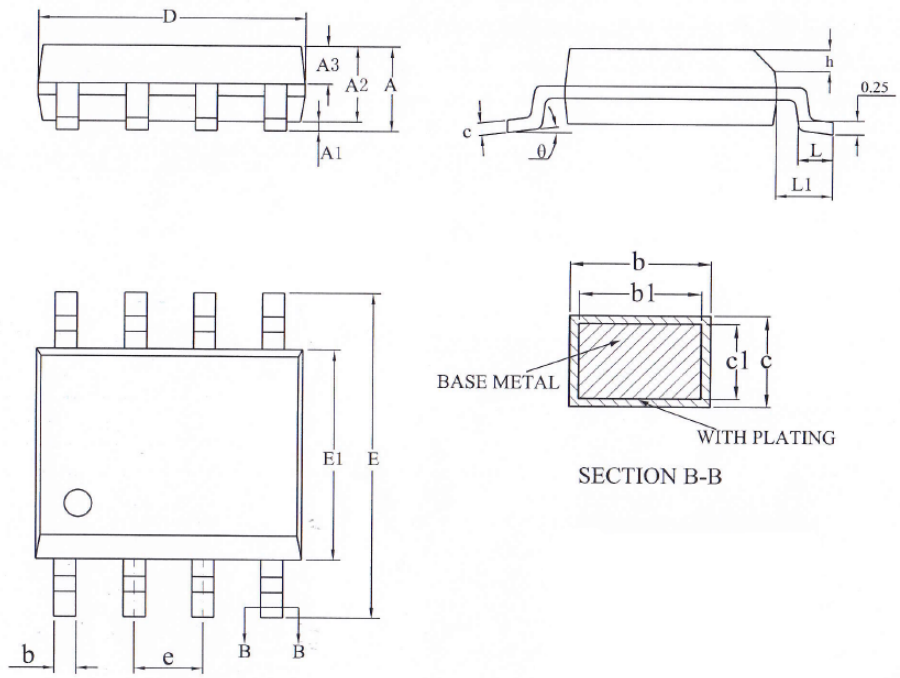


Figure 8.4 Transient protection against surge transients for half-duplex RS-485 transceiver

Copyright © 2025, NOVOSENSE

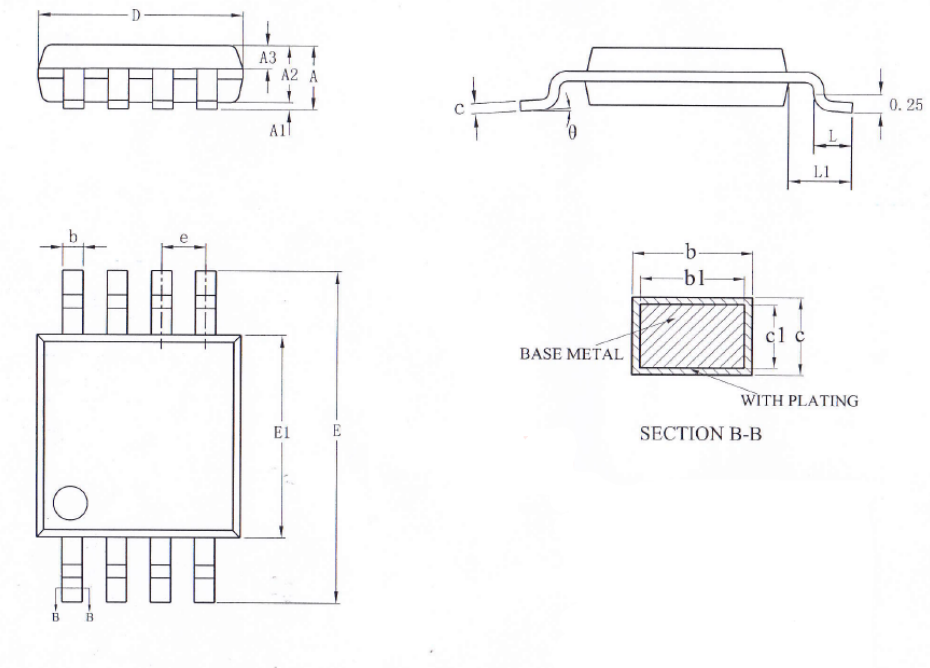
9. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.1 SOP8 Package Shape and Dimension in millimeters

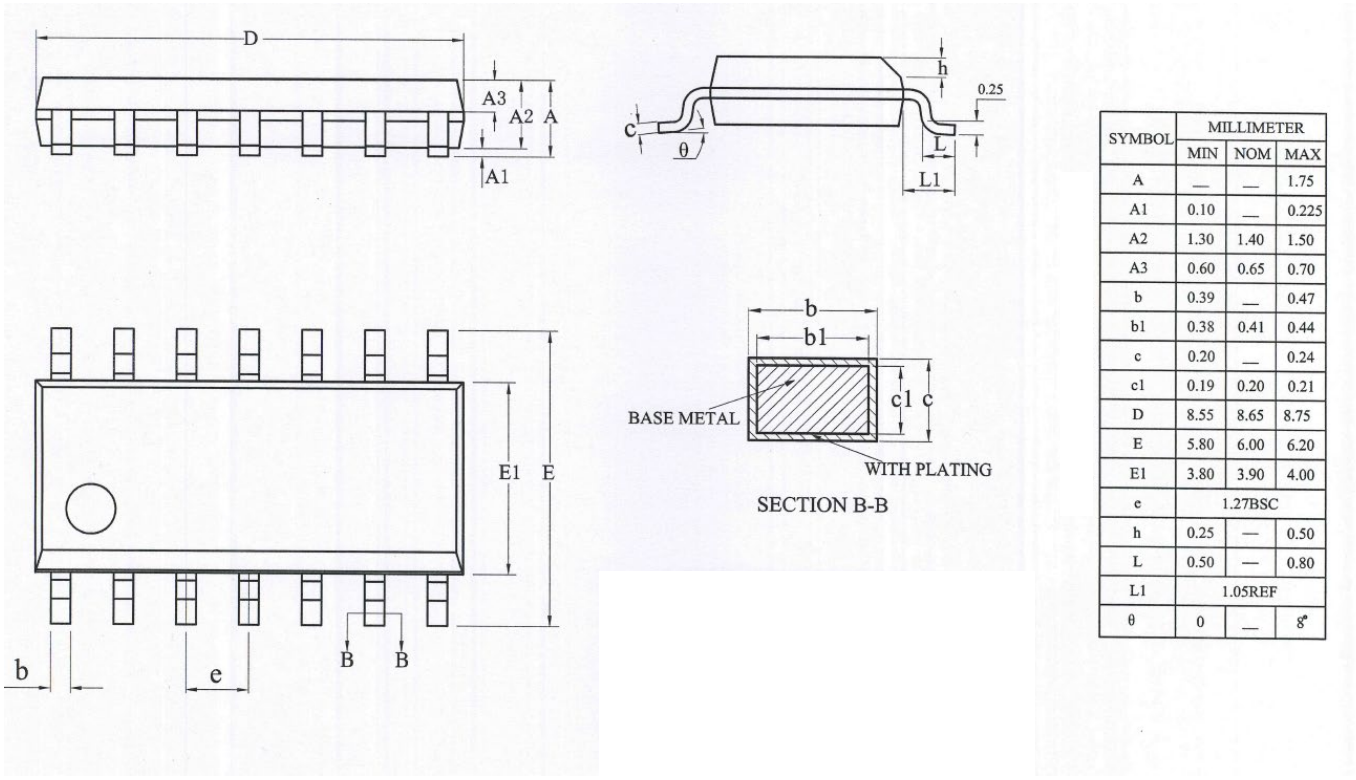


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.2 MSOP8 Package Shape and Dimension in millimeters

Copyright © 2025, NOVOSENSE



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

1

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.3 SOP14 Package Shape and Dimension in millimeters

10. Ordering Information

Part Number	*Duplex*	*Max Data Rate (Mbps)*	*No. of Nodes*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NCA3176-DSPR	Half	20	256	-40 to 125℃	3	SOP8	SOP8	4000
NCA3176-DMSR	Half	20	256	-40 to 125℃	3	MSOP8	MSOP8	4000
NCA3492-DSPKR	Full	20	256	-40 to 125℃	3	SOP14	SOP14	4000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ℃ according to the JEDEC industry standard classifications and peak solder temperatures.								

Copyright © 2025, NOVOSENSE

11. Tape and Reel Information

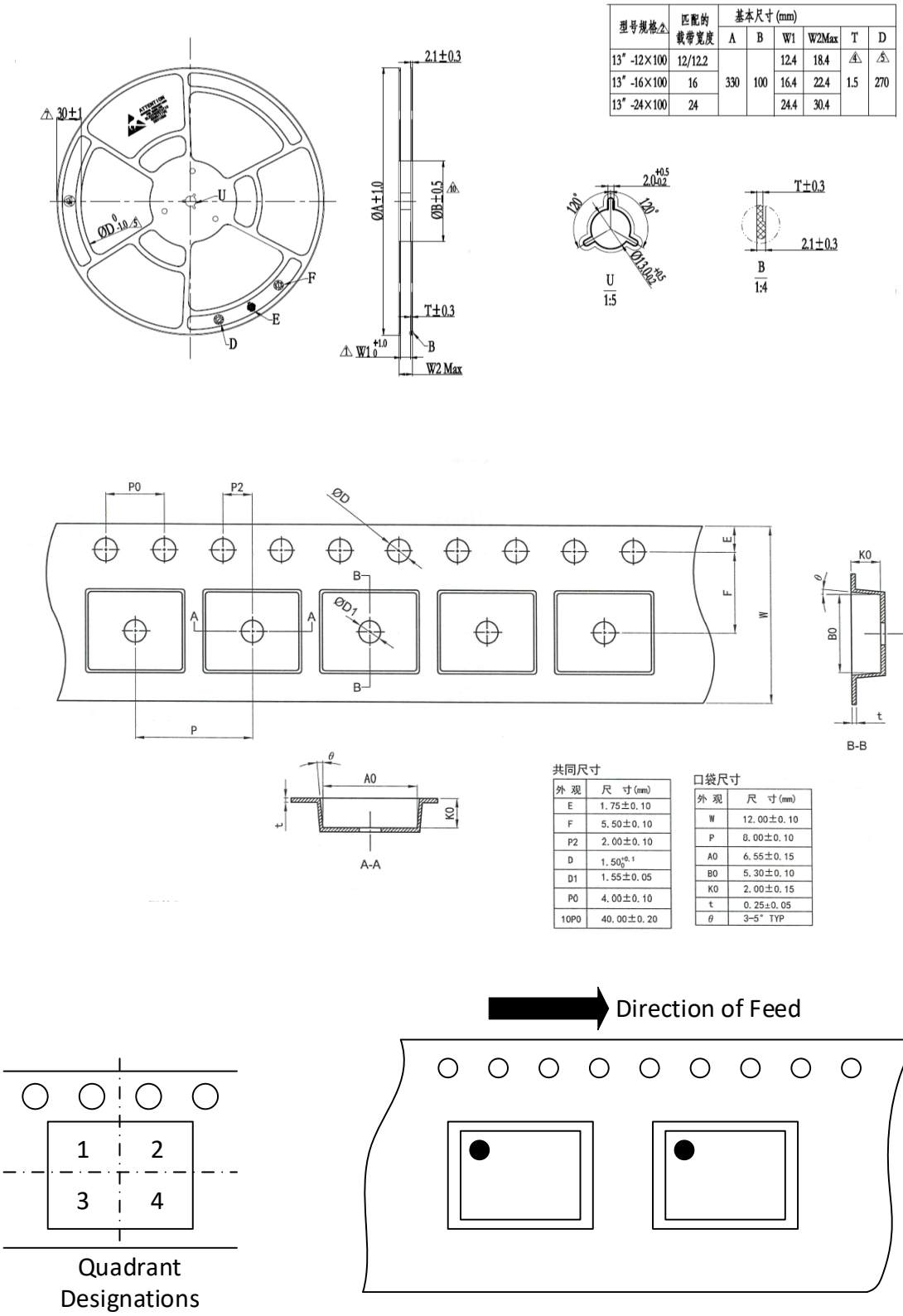
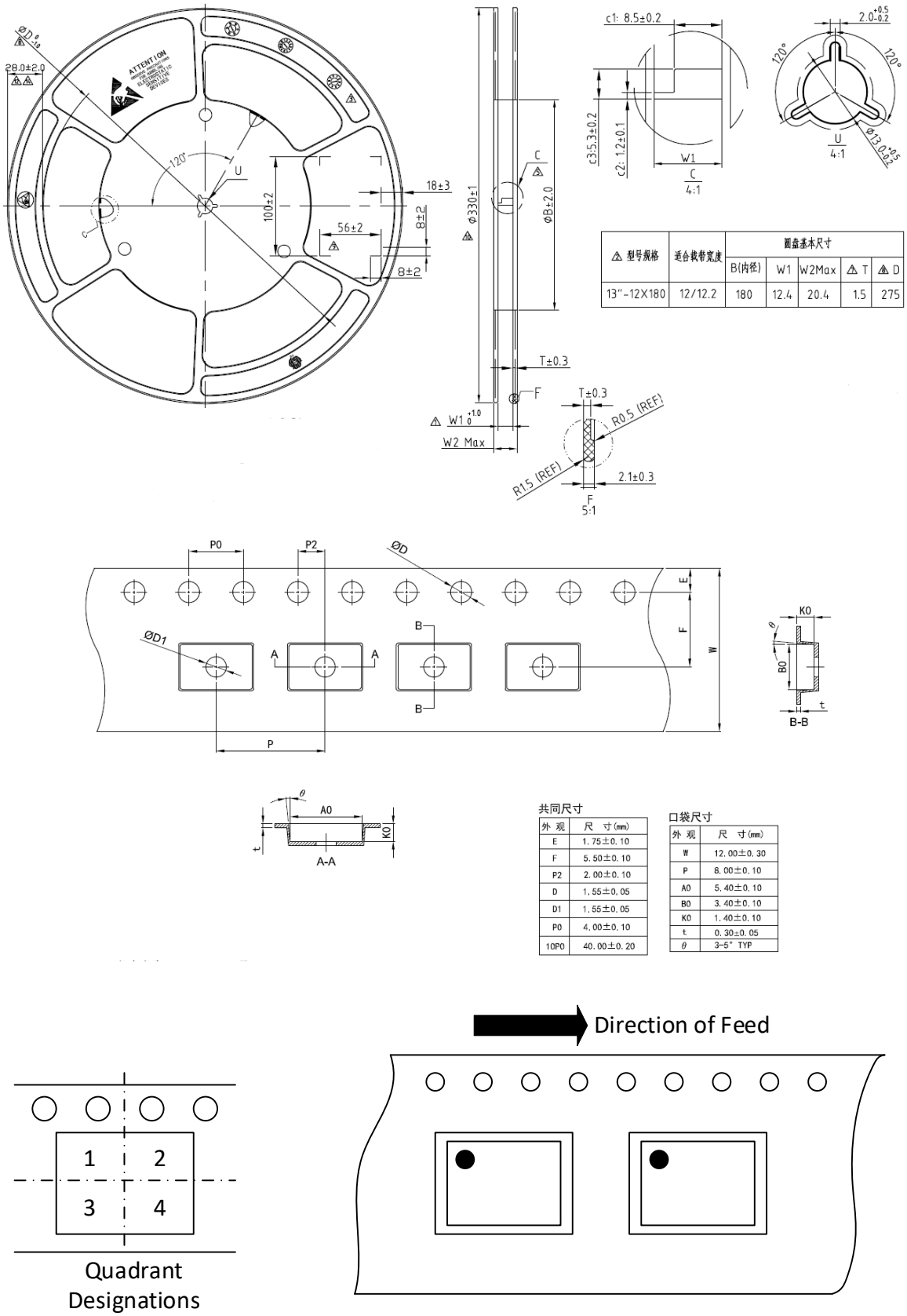


Figure 11.1 Tape and Reel Information of SOP8

Copyright © 2025, NOVOSENSE



⚠ 型号规格	适合载带宽度	圆盘基本尺寸				
		B(内径)	W1	W2Max	⚠ T	⚠ D
13"-12X180	12/12.2	180	12.4	20.4	1.5	275

共同尺寸

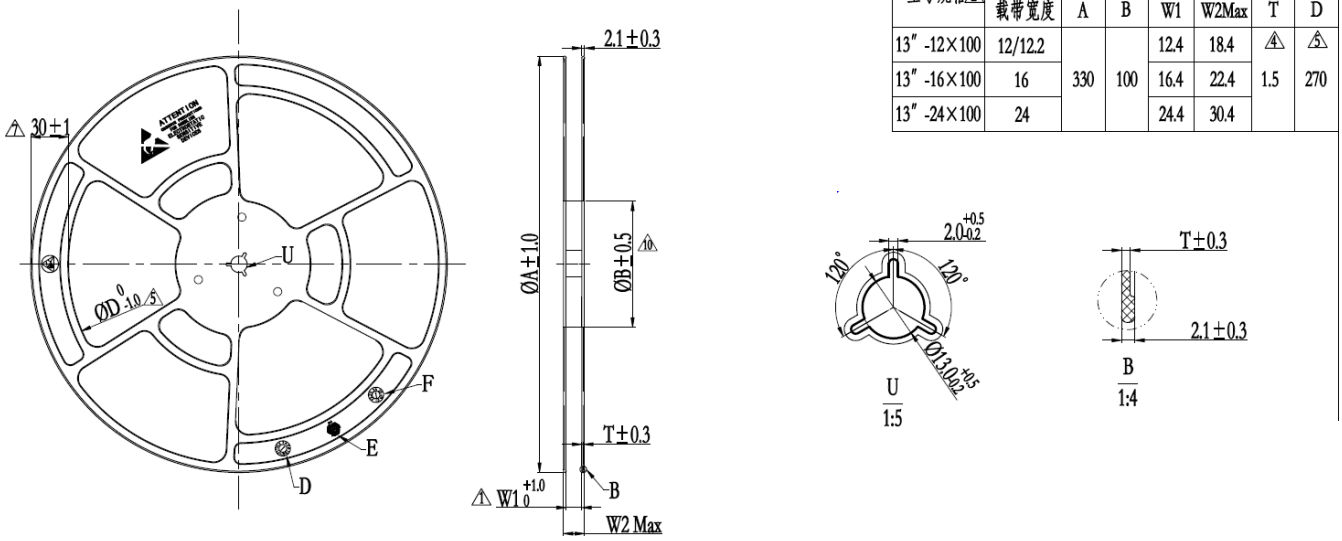
外 观	尺 寸(mm)
E	1.75±0.10
F	5.50±0.10
P2	2.00±0.10
D	1.55±0.05
D1	1.55±0.05
P0	4.00±0.10
10P0	40.00±0.20

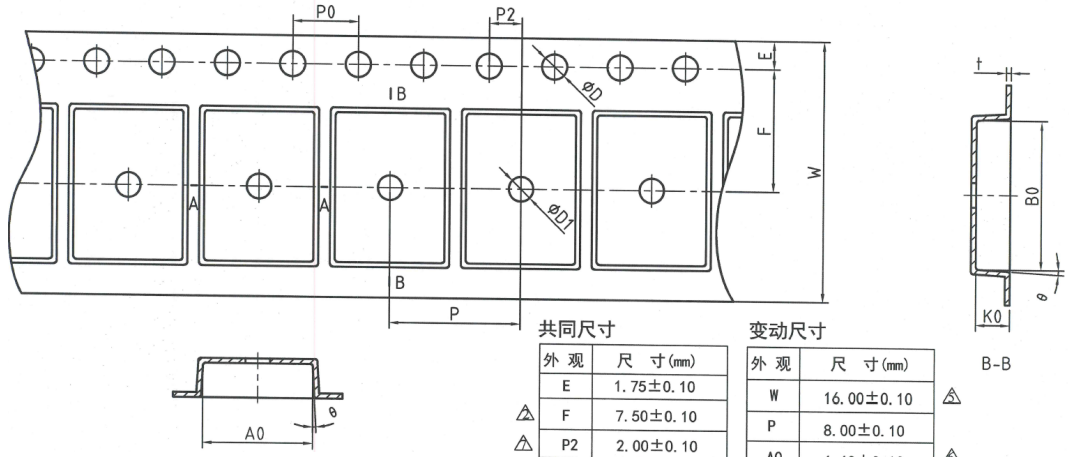
口袋尺寸

外 观	尺 寸(mm)
W	12.00±0.30
P	8.00±0.10
A0	5.40±0.10
B0	3.40±0.10
K0	1.40±0.10
t	0.30±0.05
θ	3-5° TYP

Figure 11.2 Tape and Reel Information of MSOP8

型号规格	匹配的载带宽度	基本尺寸(mm) A	B	W1	W2Max	T	D
13″ -12×100	12/12.2	330	100	12.4	18.4	1.5	270
13″ -16×100	16			16.4	22.4		
13″ -24×100	24			24.4	30.4		





共同尺寸

外观	尺寸(mm)
E	1.75±0.10
F	7.50±0.10
P2	2.00±0.10
D	1.55±0.05
D1	1.55±0.05
P0	4.00±0.10
10P0	40.0±0.20

变动尺寸

外观	尺寸(mm)
W	16.00±0.10
P	8.00±0.10
A0	6.60±0.10
B0	9.15±0.10
K0	1.80±0.10
t	0.24-0.32
θ	5° TYP

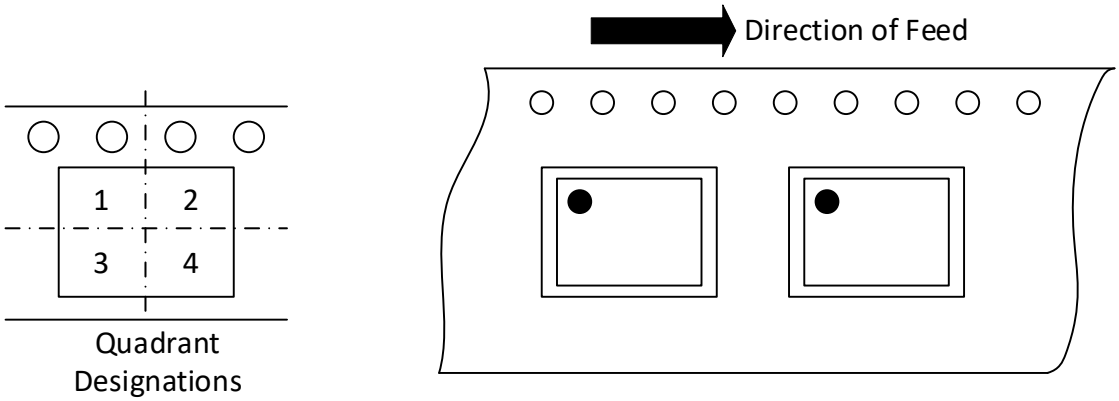


Figure 11.3 Tape and Reel Information of SOP14

Copyright © 2025, NOVOSENSE

12. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/8/15
1.1	Modify the HBM performance; Modify typical values of VOD parameters; Modify the VOC parameter upper limit	2025/11/27

Copyright © 2025, NOVOSENSE

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

You are solely responsible for your use of Novosense' products and applications, and for the safety thereof. You shall comply with all laws, regulations and requirements related to Novosense's products and applications, although information or support related to any application may still be provided by Novosense.

The resources are intended only for skilled developers designing with Novosense' products. Novosense reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided. Novosense authorizes you to use these resources exclusively for the development of relevant applications designed to integrate Novosense's products. Using these resources for any other purpose, or any unauthorized reproduction or display of these resources is strictly prohibited. Novosense shall not be liable for any claims, damages, costs, losses or liabilities arising out of the use of these resources.

For further information on applications, products and technologies, please contact Novosense (www.novosns.com).

Suzhou Novosense Microelectronics Co., Ltd

1

Copyright © 2025, NOVOSENSE