

Product Overview

NCA1463 is a high-speed CAN transceiver. It meets the physical layer and Signal Improvement Capability (SIC) specification requirements of the ISO 11898-2:2024 and is fully interoperable with high-speed Classical CAN and CAN FD transceivers.

The CAN Signal Improvement Capability of NCA1463 helps reduce signal ringing at the dominant-to-recessive edge of unterminated stubs in the network, enabling reliable CAN FD communication in larger and more complex topologies. In addition, the NCA1463 has a much tighter bit timing symmetry, enabling CAN FD communication up to 8 Mbit/s.

The NCA1463 is pin compatible with classical CAN FD transceivers, such as NCA1043B. It is also designed to avoid changes to hardware and software in system applications.

Key Features

- AEC Q-100 Qualified for Grade 1: T_{opr} from -40°C to 125°C
- Compliance with ISO 11898-2:2024 Standard and SAE J2284-1 to SAE J2284-5
- Supports classic CAN and CAN FD up to 8Mbps
- CAN Signal Improvement Capability
- Power supply voltage: V_{BAT} : 4.5V to 28V
 V_{CC} : 4.5V to 5.5V
 V_{IO} : 1.7V to 5.5V
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Transmit data (TXD) dominant time out function
- $\pm 40\text{V}$ CAN bus fault tolerant
- Over temperature protection
- Undervoltage detection on supply pins
- RoHS & REACH compliant

Applications

- Automotive gateway
- Body control modules
- Advanced Driver Assistance Systems (ADAS)
- Infotainment and Cluster

Device Information

Part Number	Package	Body Size
NCA1463-Q1SPKR	SOP14	8.65mm × 3.90mm
NCA1463-Q1DNKR	DFN14	4.50mm × 3.00mm

Functional Block Diagrams

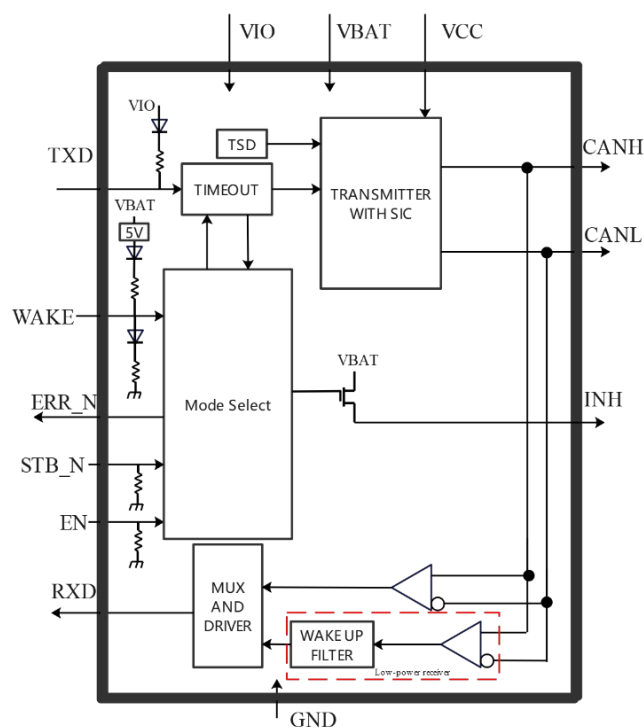


Figure 1. NCA1463 Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS	3
2. ABSOLUTE MAXIMUM RATINGS	4
3. ESD RATINGS	4
4. RECOMMENDED OPERATING CONDITIONS	5
5. THERMAL INFORMATION	5
6. SPECIFICATIONS	6
6.1. ELECTRICAL CHARACTERISTICS	6
6.2. SWITCHING ELECTRICAL CHARACTERISTICS	10
6.3. PARAMETER MEASUREMENT INFORMATION	12
7. FUNCTION DESCRIPTION	15
7.1. OVERVIEW	15
7.2. SYSTEM OPERATING MODES	15
7.2.1. Normal Mode	15
7.2.2. Listen-only Mode	15
7.2.3. Standby Mode	16
7.2.4. Sleep Mode	16
7.2.5. Off Mode	16
7.3. CAN OPERATING MODES	16
7.3.1. CAN Off Mode	17
7.3.2. CAN Offline Mode	17
7.3.3. CAN Wake Mode	17
7.3.4. CAN Active Mode	17
7.3.5. CAN Listen-only Mode	17
7.4. INTERNAL FLAGS	18
7.4.1. Pwon Flag	18
7.4.2. Wake Flag	18
7.4.3. Wake-up Source Flag	18
7.4.4. Local Failure Flag	18
7.5. LOCAL WAKE-UP (VIA WAKE PIN)	19
7.6. REMOTE WAKE-UP (VIA THE CAN BUS)	19
7.7. LOCAL FAILURE EVENTS	19
7.7.1. TXD Dominant Time-out Function	19
7.7.2. TXD-to-RXD Short Circuit	19
7.7.3. Bus Dominant Failures	19
7.7.4. Overtemperature Protection	20
7.8. I/O LEVEL	20
7.9. WAKE PIN	20
7.10. INTERNAL BIASING OF TXD, STB_N AND EN INPUT PINS	20
8. APPLICATION NOTE	21
8.1. TYPICAL APPLICATION CIRCUIT	21
9. PACKAGE INFORMATION	22
10. ORDERING INFORMATION	24
11. TAPE AND REEL INFORMATION	25
12. REVISION HISTORY	27

1. Pin Configuration and Functions

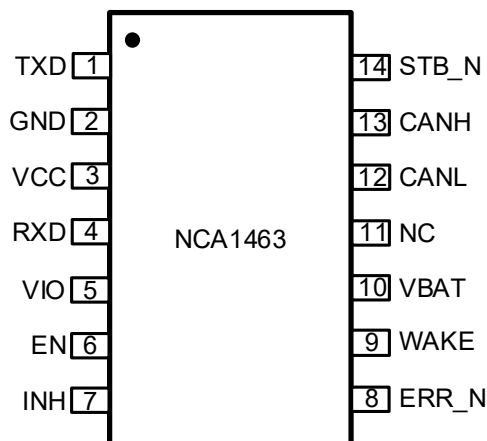


Figure 1.1 NCA1463 SOP Package

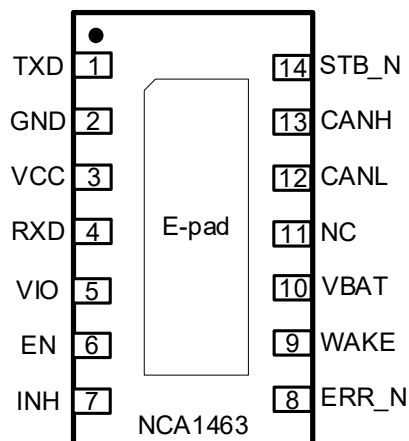


Figure 1.2 NCA1463 DFN Package

Table 1.1 NCA1463 Pin Configuration and Description

NCA1463 Pin No.	Symbol	Function
1	TXD	CAN transmit data input (Internal weak pull-up, LOW for dominant and HIGH for recessive bus states)
2	GND	Ground
3	VCC	Power Supply
4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	VIO	Logic I/O supply voltage
6	EN	enable control input (Internal weak pull-down)
7	INH	inhibit output for switching external voltage regulators
8	ERR_N	error and power-on indication output (open-drain output, active LOW)
9	WAKE	local wake-up input (Internal weak pull-up and pull-down)
10	VBAT	battery supply voltage
11	NC	No connection
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	STB_N	STB (standby mode) select pin (Internal weak pull-down)
/	E-pad	Ground

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VCC, VIO	-0.3		7	V	
	VBAT	-0.3		40	V	
I/O Voltage	V _{TXD} , V _{STB_N} , V _{EN}	-0.3		7	V	
	V _{RXD} , V _{ERR_N}	-0.3		VIO+0.3	V	The maximum voltage must not exceed 7V
	V _{WAKE}	-40		40	V	
	V _{INH}	-0.3		VBAT+0.3	V	
	V _{CANH} , CANL	-40		40	V	
Voltage Between pin CANH and pin CANL	V _(CANH-CANL)	-40		40	V	
Output current on INH	I _{O(INH)}	-6			mA	
Output current on WAKE	I _{O(WAKE)}	-3			mA	
Output current on Logic pins	I _{O(Logic)}	-6			mA	
Transient Voltage	On pins CANH, CANL, WAKE, VBAT; ISO 7637- 2 pulses					
	V _{trt}	-100			V	pulse 1
				75	V	pulse 2a
		-150			V	pulse 3a
				100	V	pulse 3b
Junction Temperature	T _j	-40		150	°C	
Storage Temperature	T _{stg}	-65		150	°C	

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit)		
	● On pins CANH, CANL	±8	kV
	● On pin VBAT with 100nF capacitor	±8	kV
	● On pin WAKE with 33 kΩ resistor	±8	kV
	Human body model (HBM), per AEC-Q100-002-RevD		
	● All pins	±4	kV
	● Bus pins	±8	kV
	Charged device model (CDM), per AEC-Q100-011-RevB		
	● All pins	±2	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VBAT	4.5		28	V	
	VCC	4.5		5.5	V	
	VIO	1.7		5.5	V	
TXD High level input voltage	$V_{IH(TXD)}$	$0.7 \cdot VIO$		$VIO + 0.3$	V	
TXD Low level input voltage	$V_{IL(TXD)}$	-0.3		$0.3 \cdot VIO$	V	
RXD Output High current	I_{OH}	-2			mA	
RXD Output Low current	I_{OL}			2	mA	
INH Output current	$I_{O(INH)}$			2	mA	
Operating Temperature	T_{opr}	-40		125	°C	

5. Thermal Information

Parameters	Symbol	SOP14	DFN14	Unit
Junction-to-ambient thermal resistance	θ_{JA}	78	33.1	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	33.6	30.5	°C/W
Junction-to-board thermal resistance	θ_{JB}	34.7	10.8	°C/W

6. Specifications

6.1. Electrical Characteristics

(VCC=4.5V~5.5V, VIO=1.7V~5.5V, VBAT=4.5V~28V, T_{opr} = -40°C to 125°C. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V, VBAT=12V, R_L=60Ω, T_{opr} = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply VCC						
Supply Voltage	VCC	4.5	5.0	5.5	V	
Undervoltage detection voltage on pin VCC	V _{uvd(VCC)}	3.4		4.3	V	
Undervoltage hysteresis voltage on pin VCC	V _{uvhys(VCC)}	50			mV	[1]
Supply current	I _{cc}		42	65	mA	Normal mode, dominant, TXD = 0, t < t _{to(dom)} TXD
				125	mA	Normal mode, -3V < V _{CANH} = V _{CANL} < 40V
				109	mA	Normal mode, -3V < V _{CANH} = V _{CANL} < 18V
				9	mA	Normal mode, recessive, TXD = VIO
			5	9	mA	Listen-only mode
				2	μA	Standby or sleep mode, T _j < 85°C
				3.5	μA	Standby or sleep mode, T _j < 150°C
Supply VIO						
Supply voltage on pin VIO	VIO	1.7	3.3	5.5	V	
Undervoltage detection voltage on pin VIO	V _{uvd(VIO)}	1		1.68	V	
Undervoltage hysteresis voltage on pin VIO	V _{uvhys(VIO)}		50		mV	[1]
Supply current on pin VIO	I _{io}		90	350	μA	Normal mode, dominant, V _{TXD} = 0
				3	μA	Normal mode, recessive, V _{TXD} = VIO or Listen-only mode
				2	μA	Standby or sleep mode, T _j < 85°C
				4	μA	Standby or sleep mode, T _j < 150°C
Supply VBAT						
Supply voltage on pin VBAT	VBAT	4.5	12	28	V	
Undervoltage detection	V _{uvd(VBAT)}	3.82		4.48	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
voltage on pin VBAT						
Undervoltage hysteresis voltage on pin VBAT	V _{uvd} (VBAT) _{hys}	50			mV	[1]
Supply current on pin VBAT	I _{VBAT}			50	μA	Normal or Listen-only mode, pin INH left open
			23	40	μA	Standby mode, V _{WAKE} = VBAT or GND, pin INH left open, T _j < 150°C, V _{WAKE} = VBAT
			19	40	μA	Sleep mode, V _{WAKE} = VBAT or GND, T _j < 150°C
PIN TXD						
High level input voltage	V _{IH}	0.7*VIO			V	
Low level input voltage	V _{IL}			0.3*VIO	V	
hysteresis voltage	V _{hys}	50			mV	[1]
pull-up resistance	R _{pu}	20		80	kΩ	
High level input current	I _{IH}	-1		1	μA	V _{TXD} = VIO = 5.5V
Low level input current	I _{IL}	-137		-2.5	μA	V _{TXD} = GND, VIO = 5.5V
Unpowered leakage current	I _{LKG} (OFF)	-1		1	μA	V _{TXD} = 5.5V, VCC = VIO = 0V
Input Capacitance	C _{IN}			10	pF	[1]
PIN RXD						
High level output voltage	V _{OH}	VIO - 0.4			V	I _{OH} = -2mA
Low level output voltage	V _{OL}			0.4	V	I _{OL} = 2mA
Unpowered leakage current	I _{LKG} (OFF)	-1		1	μA	V _{RXD} = 5.5V, VBAT = VIO = 0V
PINs STB_N and EN						
High level input voltage	V _{IH}	0.7*VIO			V	
Low level input voltage	V _{IL}			0.3*VIO	V	
hysteresis voltage	V _{hys}	50			mV	[1]
pull-down resistance	R _{pd}	20		80	kΩ	
High level input current	I _{IH}	0.5		137	μA	V _{STB_N} or V _{EN} = VIO = 5.5V
Low level input current	I _{IL}	-1		1	μA	V _{STB_N} or V _{EN} = GND, VIO = 5.5V
Unpowered leakage current	I _{LKG} (OFF)	-1		1	μA	V _{STB_N} or V _{EN} = 5.5V, VIO = 0V
Input Capacitance	C _{IN}			10	pF	[1]
PIN ERR_N						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
High level output voltage	V_{OH}	VIO - 0.4			V	$I_{OH} = -2mA$
Low level output voltage	V_{OL}			0.4	V	$I_{OL} = 2mA$
Unpowered leakage current	$I_{LKG(OFF)}$	-1		1	μA	$V_{ERR_N} = 5.5V$, $V_{BAT} = VIO = 0V$
PIN WAKE						
wake-up threshold voltage	$V_{th(wake)}$	1.8		2.75	V	
hysteresis voltage	V_{hys}	90			mV	[1]
wake pull-up current	I_{pu}	-2.0		-0.3	μA	$4.5V > V_{WAKE} > V_{th(wake)(max)}$ for $t > t_{wake(max)}$; $V_{BAT} > 5V$
wake pull-down current	I_{pd}	0.3		2.0	μA	$V_{WAKE} < V_{th(wake)(min)}$ for $t > t_{wake(max)}$
PIN INH						
High-level voltage drop	ΔV_H		0.5	1	V	$I_{INH} = -2mA$
short-circuit output current	$I_{O(SC)}$	-18			mA	$V_{INH} = 0V^{[1]}$
BUS PINS: CANH/CANL						
dominant output voltage	$V_{O(dom)}$	3		4.26	V	$V_{TXD} = 0V$, $t < t_{to(dom)TXD}$, pin CANH; $R_L = 45\Omega$ to 65Ω ; $VCC = 4.75V$ to $5.25V$
		0.75		2.01	V	$V_{TXD} = 0V$, $t < t_{to(dom)TXD}$, pin CANL; $R_L = 45\Omega$ to 65Ω ; $VCC = 4.75V$ to $5.25V$
transmitter symmetry voltage	V_{TXsym}	$0.9 \cdot VCC$		$1.1 \cdot VCC$	V	$V_{TXsym} = V_{CANH} + V_{CANL}$; $C_{SPLIT} = 4.7 nF$; $f_{TXD} = 250 kHz$, $1 MHz$ or $2.5 MHz$ [1]
common mode voltage step	$V_{cm(step)}$	-150		150	mV	[1]
peak-to-peak common mode voltage	$V_{cm(p-p)}$	-300		300	mV	[1]
differential output voltage	$V_{O(dif)}$	1.5		3	V	Normal mode; $V_{TXD} = 0 V$, $t < t_{to(dom)TXD}$, $R_L = 50\Omega$ to 65Ω ; $VCC = 4.75V$ to $5.25V$
		1.4		3.3	V	Normal mode; $V_{TXD} = 0 V$, $t < t_{to(dom)TXD}$, $R_L = 45\Omega$ to 70Ω ; $VCC = 4.75V$ to $5.25V$
		1.5		5	V	Normal mode; $V_{TXD} = 0$, $t < t_{to(dom)TXD}$, $R_L = 2240\Omega$ [1]
		-50		50	mV	Normal or Listen-only mode; $TXD = HIGH$
		-0.2		0.2	V	Standby or Sleep mode; $TXD = HIGH$

Parameters	Symbol	Min	Typ	Max	Unit	Comments
recessive output voltage	$V_{O(rec)}$	2.256	2.5	2.756	V	Normal or Listen-only mode, $V_{TXD} = V_{IO}$, $R_L = 45\Omega$ to 65Ω ; $V_{CC} = 4.75V$ to $5.25V$, $C_{SPLIT} = 4.7nF$
		2	2.5	3	V	Normal or Listen-only mode, $V_{TXD} = V_{IO}$, no load
		-0.1		0.1	V	Standby or Sleep mode, $V_{TXD} = V_{IO}$, no load
differential receiver threshold voltage	$V_{th(RX)dif}$	0.5	0.7	0.9	V	Normal or Listen-only mode, $-30V \leq V_{CM} \leq 30V$, $V_{CM} = (V_{CANH} + V_{CANL})/2$
		0.4		1.15	V	Standby or Sleep mode, $-30V \leq V_{CM} \leq 30V$
receiver recessive voltage	$V_{rec(RX)}$	-8 ^[1]		0.5	V	Normal or Listen-only mode, $-30V \leq V_{CM} \leq 30V$
		-8 ^[1]		0.4	V	Standby or Sleep mode, $-30V \leq V_{CM} \leq 30V$
receiver dominant voltage	$V_{dom(RX)}$	0.9		9 ^[1]	V	Normal or Listen-only mode, $-30V \leq V_{CM} \leq 30V$
		1.15		9 ^[1]	V	Standby or Sleep mode, $-30V \leq V_{CM} \leq 30V$
differential receiver hysteresis voltage	$V_{hys(RX)dif}$		50		mV	Normal or Listen-only mode, $-30V \leq V_{CM} \leq 30V$ ^[1]
short-circuit output current	$I_{O(sc)}$	-115		115	mA	$-15V \leq V_{CANH} \leq +40V$, $-15V \leq V_{CANL} \leq +40V$
recessive short-circuit output current	$I_{O(sc)rec}$	-3		3	mA	Normal or Listen-only mode, $TXD = HIGH$, $-27V \leq V_{CANH} \leq +32V$, $-27V \leq V_{CANL} \leq +32V$
leakage current	I_L			4.5	μA	$V_{CC} = V_{IO} = V_{BAT} = 0V$ or pins shorted to GND via $47k\Omega$; $V_{CANH} = V_{CANL} = 5V$
input resistance	R_i	25		50	k Ω	$-2V \leq V_{CANH} \leq +7V$; $-2V \leq V_{CANL} \leq +7V$; passive recessive
input resistance deviation	ΔR_i	-1		1	%	$0V \leq V_{CANH} \leq +5V$; $0V \leq V_{CANL} \leq +5V$; passive recessive
differential input resistance	$R_{i(dif)}$	50		100	k Ω	$-2V \leq V_{CANH} \leq +7V$; $-2V \leq V_{CANL} \leq +7V$; passive recessive
common-mode input capacitance	$C_{i(cm)}$			30	pF	^[1]
differential input capacitance	$C_{i(dif)}$			15	pF	^[1]
Bus Differential voltage change rate	dv/dt			95	V/ μs	Normal mode ^[1]
Signal Improvement function on CANH or CANL						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
active recessive phase input resistance	$R_{i(acter)}$	37.5		66.5	Ω	VCC = 4.75V to 5.25V
active recessive phase differential input resistance	$R_{i(dif)acter}$	75		133	Ω	VCC = 4.75V to 5.25V
Temperature detection						
shutdown junction temperature	$T_{j(sd)}$	180	190	200	$^{\circ}\text{C}$	
release shutdown junction temperature	$T_{j(sd)rel}$	170	180	190	$^{\circ}\text{C}$	

[1] Not tested in Production; Guaranteed by design.

6.2. Switching Electrical Characteristics

(VCC=4.5V~5.5V, VIO=1.7V~5.5V, VBAT=4.5V~28V, $T_{opr} = -40^{\circ}\text{C}$ to 125°C . Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V, VBAT=12V, $R_L = 60\Omega$, $T_{opr} = 25^{\circ}\text{C}$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
CAN Timing characteristics						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	-		80	ns	Normal mode, VCC = 4.75V to 5.25V, $t_{bit(TXD)} \geq 125\text{ns}$, up to 8Mbit/s
Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	-		80	ns	Normal mode, VCC = 4.75V to 5.25V, $t_{bit(TXD)} \geq 125\text{ns}$, up to 8Mbit/s
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	-		110	ns	Normal or Listen-only mode, VCC = 4.75V to 5.25V, $t_{bit(TXD)} \geq 125\text{ns}$, up to 8Mbit/s
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	-		110	ns	Normal or Listen-only mode, VCC = 4.75V to 5.25V, $t_{bit(TXD)} \geq 125\text{ns}$, up to 8Mbit/s
Delay from TXD LOW to RXD LOW	$t_{d(TXDL-RXDL)}$	-		190	ns	Normal mode
Delay from TXD HIGH to RXD HIGH	$t_{d(TXDH-RXDH)}$	-		190	ns	Normal mode
CAN FD Signal improvement Characteristics						
Delay time from TXD to bus passive recessive start	$t_{d(TXD-buspasrec)start}$	-		530	ns	$R_L = 45\Omega$ to 65Ω ; VCC = 4.75V to 5.25V
Delay time from TXD to bus active recessive start	$t_{d(TXD-busactrec)start}$	-		120	ns	$R_L = 45\Omega$ to 65Ω ; VCC = 4.75V to 5.25V
Delay time from TXD to bus active recessive end	$t_{d(TXD-busactrec)end}$	355		-	ns	$R_L = 45\Omega$ to 65Ω ; VCC = 4.75V to 5.25V
CAN FD Timing characteristics according to ISO11898-2:2024 parameter set C ($t_{bit(TXD)} \geq 125\text{ns}$, up to 8Mbit/s^[1]), VCC = 4.75V to 5.25V						
transmitted recessive bit width deviation	$\Delta t_{bit(bus)}$	-10		10	ns	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$

Parameters	Symbol	Min	Typ	Max	Unit	Comments
receiver timing symmetry	Δt_{rec}	-20		15	ns	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$
received recessive bit width deviation	$\Delta t_{bit(RXD)}$	-30		20	ns	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$
CAN FD Timing characteristics ($t_{bit(TXD)} \geq 200ns$, up to 5Mbit/s^[2])						
transmitted recessive bit width deviation	$\Delta t_{bit(bus)}$	-30		30	ns	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$
receiver timing symmetry	Δt_{rec}	-45		15	ns	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$
received recessive bit width deviation	$\Delta t_{bit(RXD)}$	-50		40	ns	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$
Dominant time-out times						
TXD dominant time-out time	$t_{to(dom)TXD}$	0.8		9	ms	$V_{TXD} = 0V$; Normal mode ^[3]
bus dominant time-out time	$t_{to(dom)bus}$	0.8		9	ms	$V_{O(dif)} > 0.9 V$; Normal or Listen-only mode ^[3]
Bus wake-up times						
bus dominant wake-up time	$t_{wake(busdom)}$	0.5		1.8	μs	Standby or sleep mode ^[3]
bus recessive wake-up time	$t_{wake(busrec)}$	0.5		1.8	μs	Standby or sleep mode ^[3]
bus wake-up time-out time	$t_{to(wake)bus}$	0.6		9	ms	Standby or sleep mode ^[3]
Mode transitions						
mode change transition time	$t_{t(moch)}$			50	μs	^[3]
start-up time	$t_{startup}$			1.5	ms	start-up time ^[3]
RXD start-up time	$t_{startup(RXD)}$			20	μs	After local or remote wake-up detected ^[3]
INH start-up time	$t_{startup(INH)}$	4		50	μs	After local or remote wake-up detected; transition from Sleep to Standby ^[3]
ERR_N start-up time	$t_{startup(ERR_N)}$			20	μs	After local or remote wake-up detected ^[3]
go-to-sleep hold time	$t_{h(gotosleep)}$	20		50	μs	STB_N = LOW and EN = HIGH, hold time for entering Sleep mode ^[3]
delay time from mode change to ERR_N	$t_{d(moch-ERR_N)}$			20	μs	to ERR_N stable in response to a mode transition ^[3]
Local wake-up input; pin WAKE						
wake-up time	t_{WAKE}	16		50	μs	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode ^[3]
IO filter;						
IO filter time	$t_{ftr(IO)}$	0.5		5	μs	I/O filter time of STB_N & EN pin ^[3]
Undervoltage detection						
undervoltage detection time	$t_{det(uv)}$			30	μs	VBAT/VCC/VIO pin ^[3]

Parameters	Symbol	Min	Typ	Max	Unit	Comments
long undervoltage detection time	$t_{\text{det(}uv\text{)}}\text{long}$	100		350	ms	VCC/VIO pin ^[3]
undervoltage recovery time	$t_{\text{rec(}uv\text{)}}$			50	μs	VCC/VIO pin ^[3]
time for device return to normal operation from a VCC/VIO undervoltage event	$t_{\text{rec(}uv\text{)}}\text{long}$			200	μs	VCC/VIO pin ^[3]

[1] Compliance with parameter set C requirements implies compliance for parameter sets A ($t_{\text{bit(TXD)}} \geq 500$ ns, up to 2 Mbit/s) and B ($t_{\text{bit(TXD)}} \geq 200$ ns, up to 5 Mbit/s).

[2] For reasons related to CAN FD bit timing symmetry, these values are centered around the nominal bit length.

[3] Not tested in Production; Guaranteed by design.

6.3. Parameter Measurement Information

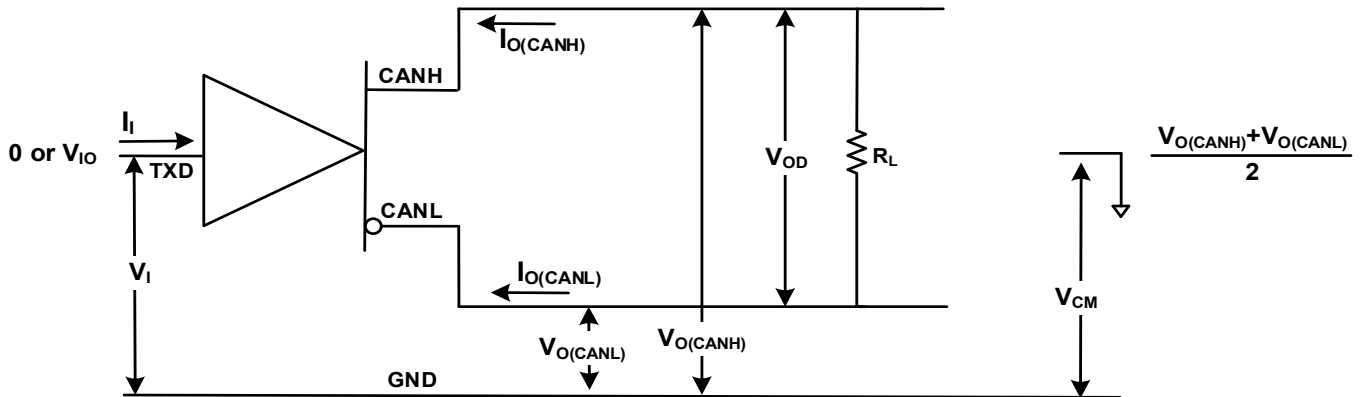


Figure 6. 1 Driver Voltage, Current and Test Definitions

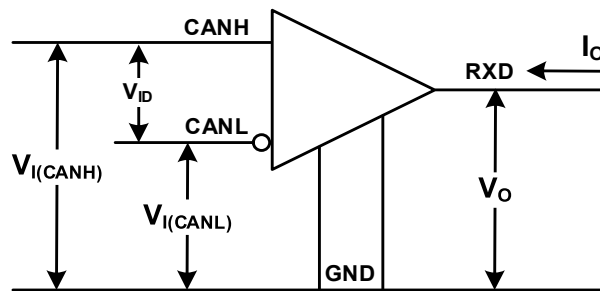


Figure 6. 2 Receiver Voltage and Current Definitions

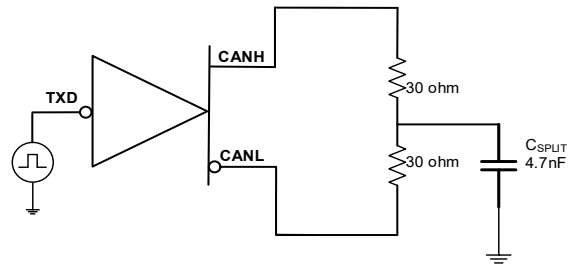


Figure 6. 3 Transceiver Driver Symmetry Test Circuit

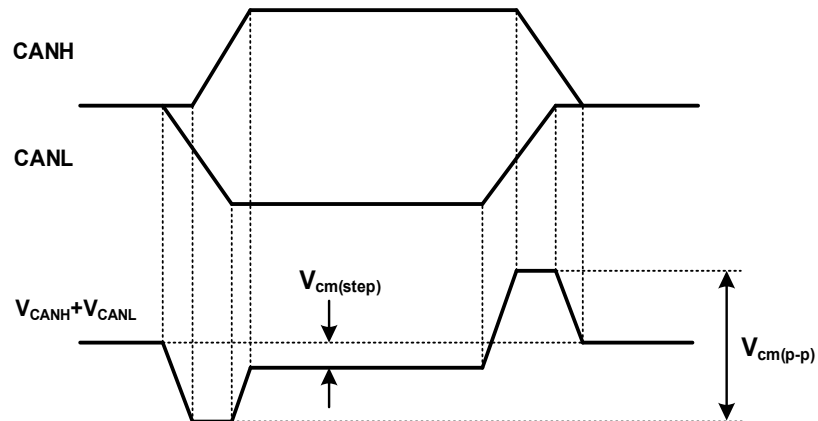


Figure 6. 4 CAN bus common-mode voltage

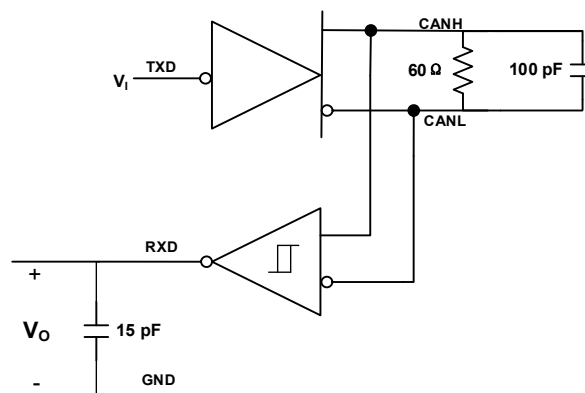


Figure 6. 5 Timing test circuit

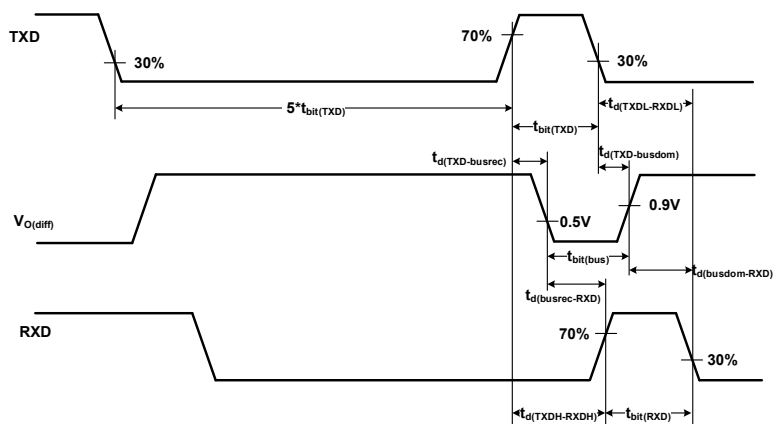
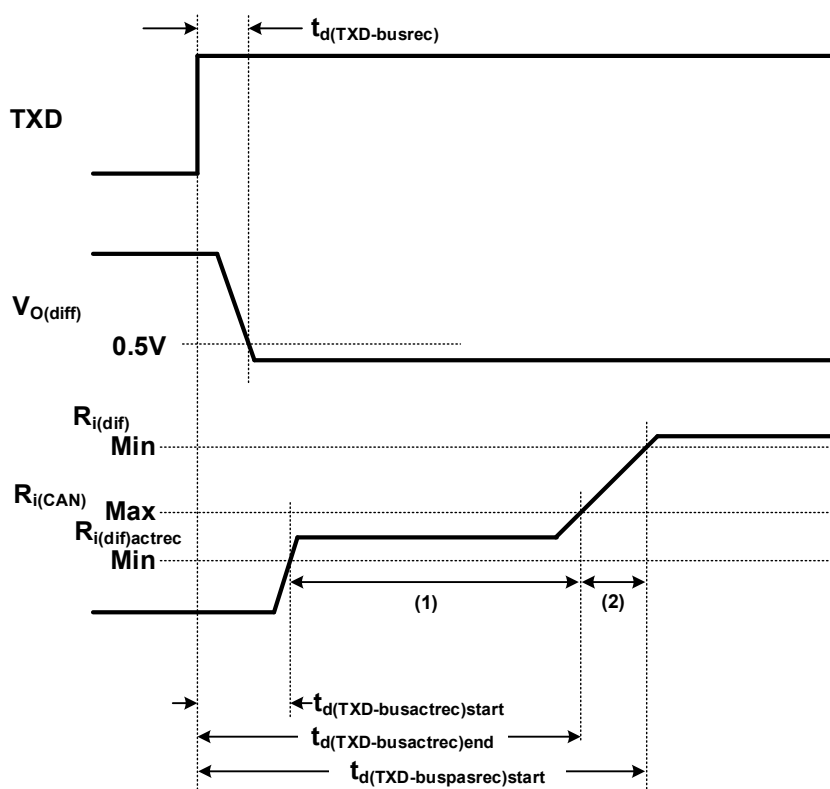


Figure 6.6 Timing definitions



(1) Active recessive phase (2) release phase

Figure 6.7 Transmitter impedance and timing diagram for dominant to passive recessive transition

7. Function Description

7.1. Overview

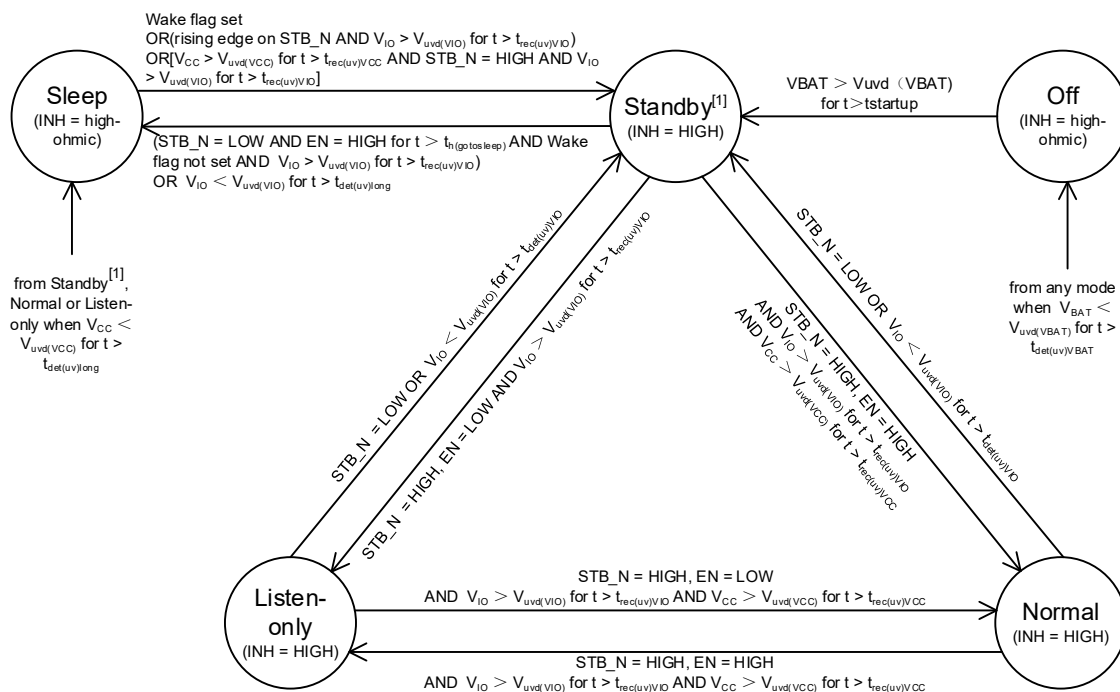
NCA1463 is a high-speed CAN transceiver. It meets the physical layer and Signal Improvement Capability (SIC) specification requirements of the ISO 11898-2:2024 and is fully interoperable with high-speed Classical CAN and CAN FD transceivers.

The CAN Signal Improvement Capability of NCA1463 helps reduce signal ringing at the dominant-to-recessive edge of unterminated stubs in the network, enabling reliable CAN FD communication in larger and more complex topologies. In addition, the NCA1463 has a much tighter bit timing symmetry, enabling CAN FD communication up to 8 Mbit/s.

7.2. System Operating Modes

The NCA1463 contains two independent state machines, a system state machine and a CAN state machine. Two state machines are needed to secure flag handling during undervoltage conditions. These state machines support a number of interdependent operating modes. The system state machine controls the CAN state machine, but both state machines are independently affected by the VCC undervoltage status. For both state machines, undervoltage detection is defined as $V_x < V_{\text{uvd}(x)}$ for $t > t_{\text{det}(uv)}$ and undervoltage recovery is defined as $V_x > V_{\text{uvd}(x)}$ for $t > t_{\text{rec}(uv)}$.

The system state machine in the NCA1463 supports five system operating modes. Control pins STB_N and EN are used to select the operating mode. Figure 7.2 describes how to switch between operating modes. Mode changes are completed after transition time $t_{\text{t(moch)}}$. Fail-safe diagnostic information is available on pin ERR_N with a delay of $t_{\text{d(moch-ERR_N)}}$ after a mode change.



[1] It should be noted that VCC and VIO undervoltage detection is masked at the initial VBAT power-up. The undervoltage detection functions are enabled after VCC and VIO complete power-up successfully (VCC stays above $V_{\text{uvd}(VCC)}$ for $t > t_{\text{rec}(uv)}$, and VIO stays above $V_{\text{uvd}(VIO)}$ for $t > t_{\text{rec}(uv)}$). Following VBAT power-up, the device stays in Standby mode with INH held high when VCC or VIO is unpowered. When only VIO is powered and VCC is off, STB_N and EN control mode transitions, and INH stays high until Sleep mode is entered.

Figure 7. 1 State transition diagram

7.2.1. Normal Mode

In Normal mode, HIGH levels on pin STB_N and pin EN select Normal mode, provided the battery supply voltage VBAT, and VIO are present. Pin INH remains HIGH, so voltage regulators controlled by pin INH will also be active.

7.2.2. Listen-only Mode

In Listen-only mode, a HIGH level on pin STB_N and a LOW level on pin EN select Listen-only mode, provided VBAT

and VIO are present. Pin INH remains HIGH, so voltage regulators controlled by pin INH will also be active. In Listen-only mode the receiver is enabled, but the transmitter is disabled.

7.2.3. Standby Mode

Standby mode is the first-level power-saving mode of the NCA1463. When VBAT rises above the undervoltage detection threshold $V_{\text{uvd}}(\text{VBAT})$, the NCA1463 starts to boot up, triggering an initialization procedure. It switches to Standby mode after t_{startup} , resulting in a HIGH level on pin INH.

When VIO rises above the undervoltage detection threshold $V_{\text{uvd}}(\text{VIO})$, the NCA1463 switches to Normal mode if pins STB_N and EN are HIGH, and to Listen-only mode if STB_N is HIGH and EN is LOW. It will remain in Standby mode if STB_N is LOW.

The NCA1463 will switch to Sleep mode if VIO remains below $V_{\text{uvd}}(\text{VIO})$ for $t_{\text{det(}(\text{uv})\text{)long}}$ and/or VCC remains below $V_{\text{uvd}}(\text{VCC})$ for $t_{\text{det(}(\text{uv})\text{)long}}$. A transition from Standby mode to Sleep mode can also be triggered by holding STB_N LOW and EN HIGH for $t_{\text{h(gotosleep)}}$ (also known as a 'go-to-sleep' command). This 'go-to-sleep' command is overruled if the Wake flag is set, in which case the device remains in Standby mode.

7.2.4. Sleep Mode

Sleep mode is the second-level power-saving mode of the NCA1463. Sleep mode is entered in a number of ways:

- (1) via Standby mode, in response to a 'go-to-sleep' command
- (2) via Standby mode as a result of a VIO undervoltage longer than $t_{\text{det(}(\text{uv})\text{)long}}$
- (3) via all other modes, except Off mode, as a result of a VCC undervoltage longer than $t_{\text{det(}(\text{uv})\text{)long}}$

In Sleep mode, the transceiver behaves as described for Standby mode, with the exception that pin INH is set high-ohmic. Voltage regulators controlled by this pin are switched off and the current into pin VBAT is reduced to a minimum. A number of events will cause the NCA1463 to exit Sleep mode, switching to Standby mode:

- (1) setting the Wake flag
- (2) a rising edge on pin STB_N (if $\text{VIO} > V_{\text{uvd}}(\text{VIO})$)
- (3) $\text{VCC} > V_{\text{uvd}}(\text{VCC})$, $\text{VIO} > V_{\text{uvd}}(\text{VIO})$ and the 'go-to-sleep' command has not been activated. After entering Standby mode, the NCA1463 will enter Normal or Listen-Only if STB_N is HIGH.

7.2.5. Off Mode

In Off mode, the NCA1463 switches to Off mode from any mode when the battery voltage falls below the undervoltage detection threshold $V_{\text{uvd}}(\text{VBAT})$. The device starts up in Off mode when the battery is connected for the first time (cold start). Pins INH and ERR_N are in a high-ohmic state in Off mode.

7.3. CAN Operating Modes

The CAN state machine supports five operating modes.

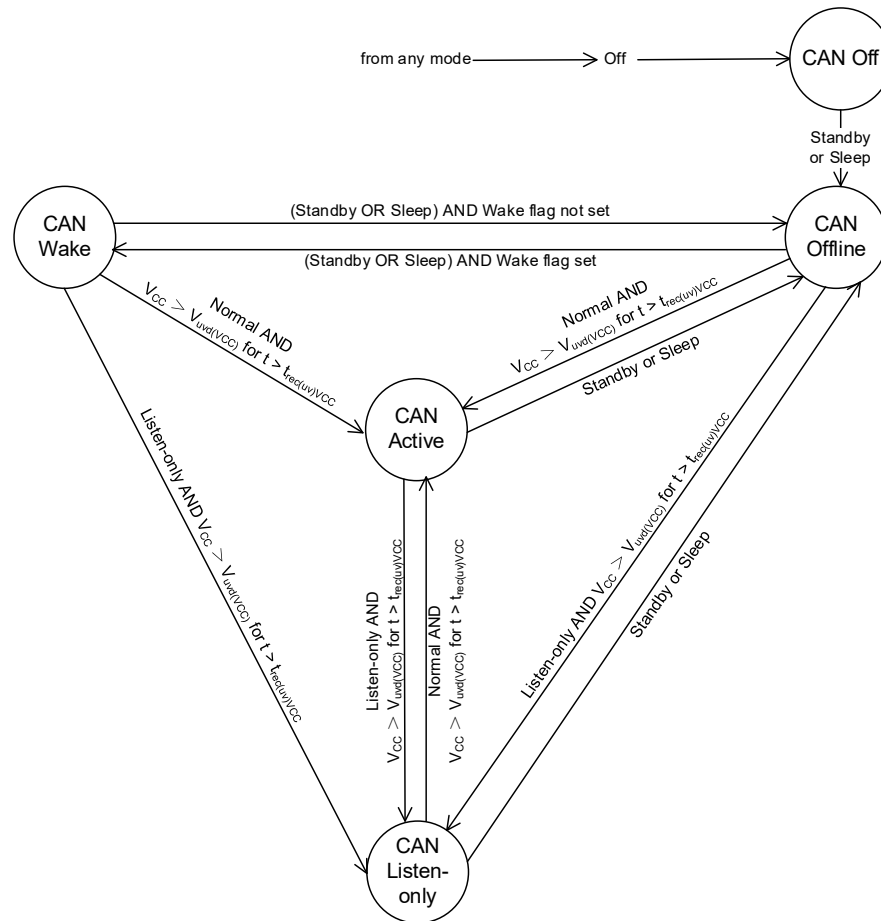


Figure 7.2 State transition diagram

7.3.1.CAN Off Mode

When the NCA1463 system state machine is in Off mode, the CAN state machine will be in CAN Off mode, with the bus pins and pin RXD in a high-ohmic state.

7.3.2.CAN Offline Mode

When the NCA1463 system state machine is in Sleep or Standby mode and the Wake flag has not been set, the CAN state machine will be in CAN Offline mode. The bus pins are biased to ground. The transceiver is unable to transmit or receive data and the low-power receiver is activated to monitor the bus for a wake-up pattern. Pin RXD is HIGH.

7.3.3.CAN Wake Mode

When the NCA1463 system state machine is in Sleep or Standby mode and the wake flag has been set, the CAN state machine will be in CAN Wake mode. Pin RXD will be LOW, reflecting the active wake-up request. The bus pins are biased to ground.

7.3.4.CAN Active Mode

When the NCA1463 system state machine is in Normal mode and VCC is above the undervoltage detection threshold $V_{und}(VCC)$, the CAN state machine will be in CAN Active mode. The transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in CAN Active mode before the first transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is $VCC/2$.

7.3.5.CAN Listen-only Mode

When the NCA1463 system state machine is in Listen-only mode and VCC is above the undervoltage detection threshold $V_{und}(VCC)$, the CAN state machine will be in CAN Listen-only mode. The transmitter is disabled. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. As in CAN Active mode, the bus pins are biased to $VCC/2$.

7.4. Internal Flags

The device makes use of four internal flags for fail-safe fallback control and system diagnosis. These flags can be polled by the controller via pin ERR_N while VIO is active. Which flag is available on pin ERR_N at any time depends on the current system operating mode; see Table 7.1.

Table 7.1 Accessing internal flags via pin ERR_N

Internal flag	Flag is available on pin ERR_N ^[1]	Flag status: set ^[2]	Flag status: not set ^[2]	Flag is cleared
Pwon	in Listen-only mode (coming from Standby mode or Sleep mode)	VBAT has risen above $V_{uvd}(VBAT)$	VBAT has not risen above $V_{uvd}(VBAT)$	On entering Normal mode
Wake	in Standby mode and Sleep mode (provided that VIO and VBAT are present)	remote or local wake-up detected OR Pwon flag has been set	no remote or local wake-up detected	on entering Normal mode
Wake-up source	in Normal mode	local wake-up OR Pwon flag has been set	remote wake-up OR no wake-up	on leaving Normal mode
Local failure	in Listen-only mode (coming from Normal mode)	on occurrence of: 1) TXD dominant failure OR 2) TXD-RXD short circuit OR 3) Bus dominant failure OR 4) Overtemperature	none of the set conditions have been met	when Pwon flag is set or, provided all local failures have been resolved, when: 1) device enters Normal mode OR 2) RXD dominant while TXD recessive OR 3) bus dominant failure resolved AND no other local failure has set the flag

[1] Pin ERR_N is an active-LOW output, so a LOW-level indicates a set flag and a HIGH-level indicates a cleared flag. Allow pin ERR_N to stabilize for at least 8 μ s after changing operating modes.

[2] Status since flag was last cleared.

7.4.1. Pwon Flag

Pwon is the VBAT power-on flag. This flag is set when the voltage on pin VBAT recovers after previously dropping below $V_{uvd}(VBAT)$ (usually because the battery was disconnected). The Pwon flag can be used for cold start diagnosis. The Wake and Wake-up source flags are set to ensure consistent system power-up under all supply conditions. Coming from Sleep or Standby and entering Listen-Only mode, a LOW level on pin ERR_N signals that the Pwon flag has been set. The flag is cleared when the transceiver enters Normal mode.

7.4.2. Wake Flag

The Wake flag is set when the transceiver detects a local or remote wake-up request.

7.4.3. Wake-up Source Flag

Wake-up source recognition is provided via the Wake-up source flag. It is set after the Wake flag has been set by a local wake-up request via the WAKE pin. The Wake-up source flag can be polled via the ERR_N pin in Normal mode. This flag is also set at power-on and cleared when the transceiver leaves Normal mode.

7.4.4. Local Failure Flag

In Normal and Listen-only modes, the transceiver can distinguish four local failure events, any of which will cause the Local failure flag to be set. The four local failure events are:

- (1) TXD dominant failures
- (2) TXD-to-RXD short circuit
- (3) Bus dominant failures
- (4) Overtemperature

The Local failure flag can be polled via the ERR_N pin in Listen-only mode, when coming from Normal mode. This flag is cleared at power-on when the Pwon flag is set or, provided all local failures have been resolved, when:

- (1) The device enters Normal mode OR
- (2) RXD is dominant while TXD is recessive OR
- (3) Bus dominant failure has been resolved AND no other local failure has set the flag.

7.5. Local Wake-up (via WAKE pin)

A local wake-up request is registered when the logic level on pin WAKE changes and the new level remains stable for at least t_{wake} . The system state machine can set the Wake flag in Standby or Sleep mode. Setting the Wake flag clears the timers. Once set, the Wake flag status is immediately available on pins ERR_N and RXD (provided VIO and VBAT are present). This flag is also set at power-on and cleared when the transceiver enters Normal mode.

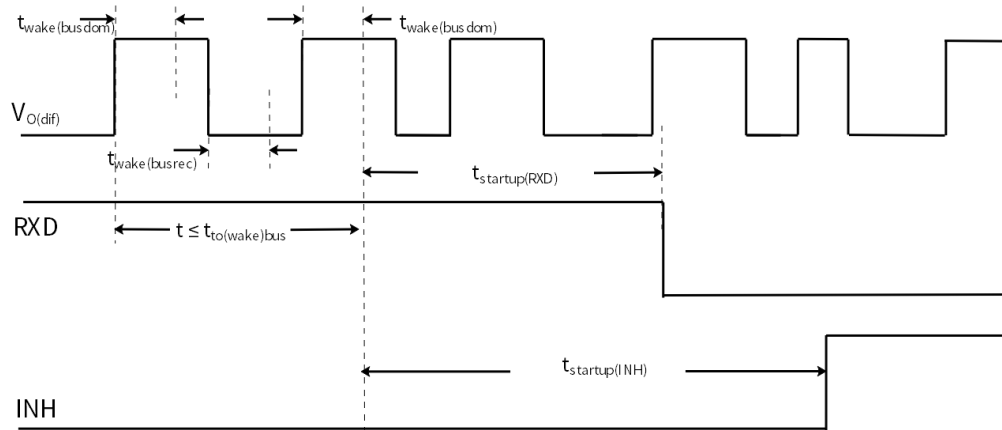
7.6. Remote Wake-up (via the CAN bus)

The NCA1463 wakes up from Sleep to Standby mode when a dedicated wake-up pattern (specified in ISO 11898-2: 2024) is detected on the bus. The wake-up pattern must have a complete dominant-recessive-dominant pattern, in which the dominant phase lasts at least $t_{wake(busdom)}$ and the recessive phase lasts at least $t_{wake(busrec)}$. Otherwise it will be ignored.

At the same time, the complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to prevent recognition as an invalid signal and thus resetting the internal wake-up logic. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event. Pins RXD and ERR_N remain HIGH until the wake-up event has been triggered and then switch LOW after $t_{startup(RXD)}$. Pin INH remains floating until the wake-up event has been triggered and then switches HIGH after $t_{startup(INH)}$.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The NCA1463 switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A VCC or VIO undervoltage is detected



• Figure 7.3 Wake-up timing diagram

7.7. Local Failure Events

The NCA1463 can detect four different local failure conditions, any of which will set the local failure flag. In most cases, the transmitter is disabled.

7.7.1. TXD Dominant Time-out Function

A permanent LOW level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communications. The TXD dominant time-out function prevents such a network lock-up by disabling the transmitter if pin TXD remains LOW for longer than the TXD dominant time-out time $t_{to(dom)TXD}$. The TXD dominant time-out timer is reset when pin TXD goes HIGH.

7.7.2. TXD-to-RXD Short Circuit

A short-circuit between pins RXD and TXD would lock the bus in a permanent dominant state once it has been driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. TXD-to-RXD short-circuit detection prevents such a network lock-up by disabling the transmitter. The transmitter remains disabled until the Local failure flag has been cleared.

7.7.3. Bus Dominant Failures

A CAN bus short circuit (to VBAT, VCC or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not begin to transmit while the bus is dominant, the host controller would not be able to detect this failure condition. However, bus dominant clamping detection

will detect the short circuit. The Local failure flag is set if the dominant state on the bus persists for longer than $t_{to(dom)bus}$. By checking this flag, the controller can determine if a clamped bus is blocking network communications. There is no need to disable the transmitter. Note that the Local failure flag is reset as soon as the bus returns to recessive state.

7.7.4. Overtemperature Protection

If the junction temperature becomes excessive, the transmitter will shut down in time to protect the output drivers from overheating without compromising the maximum operating temperature. The transmitter will remain disabled until the Local failure flag has been cleared.

7.8. I/O Level

Pin VIO should be connected to the same supply voltage used to supply the microcontroller. This adjusts the signal levels on pins TXD, RXD, STB_N, EN and ERR_N to the I/O levels of the microcontroller, allowing for direct interfacing without additional glue logic. Spurious signals from the microcontroller on pins STB_N and EN are filtered out with a filter time of $t_{filtr(IO)}$.

7.9. WAKE Pin

A local wake-up event is triggered by a LOW-to-HIGH or HIGH-to-LOW transition on the WAKE pin when V_{WAKE} crosses the wake-up threshold, $V_{th(wake)}$. After the transition, the new HIGH or LOW level should remain stable for at least t_{WAKE} . This allows for maximum flexibility when designing a local wake-up circuit.

A local wake-up is guaranteed in the case of:

- (1) a LOW-to-HIGH transition from $V_{WAKE} < V_{th(wake)min}$ to $V_{WAKE} > V_{th(wake)max}$, followed by $V_{WAKE} > V_{th(wake)max}$ for $t > t_{WAKE(max)}$
- (2) a HIGH-to-LOW transition from $V_{WAKE} > V_{th(wake)max}$ to $V_{WAKE} < V_{th(wake)min}$, followed by $V_{WAKE} < V_{th(wake)min}$ for $t > t_{WAKE(max)}$

A local wake-up is guaranteed not to occur for a transient (L-H-L or H-L-H) of duration $t < t_{WAKE(min)}$, irrespective of the V_{WAKE} voltage level.

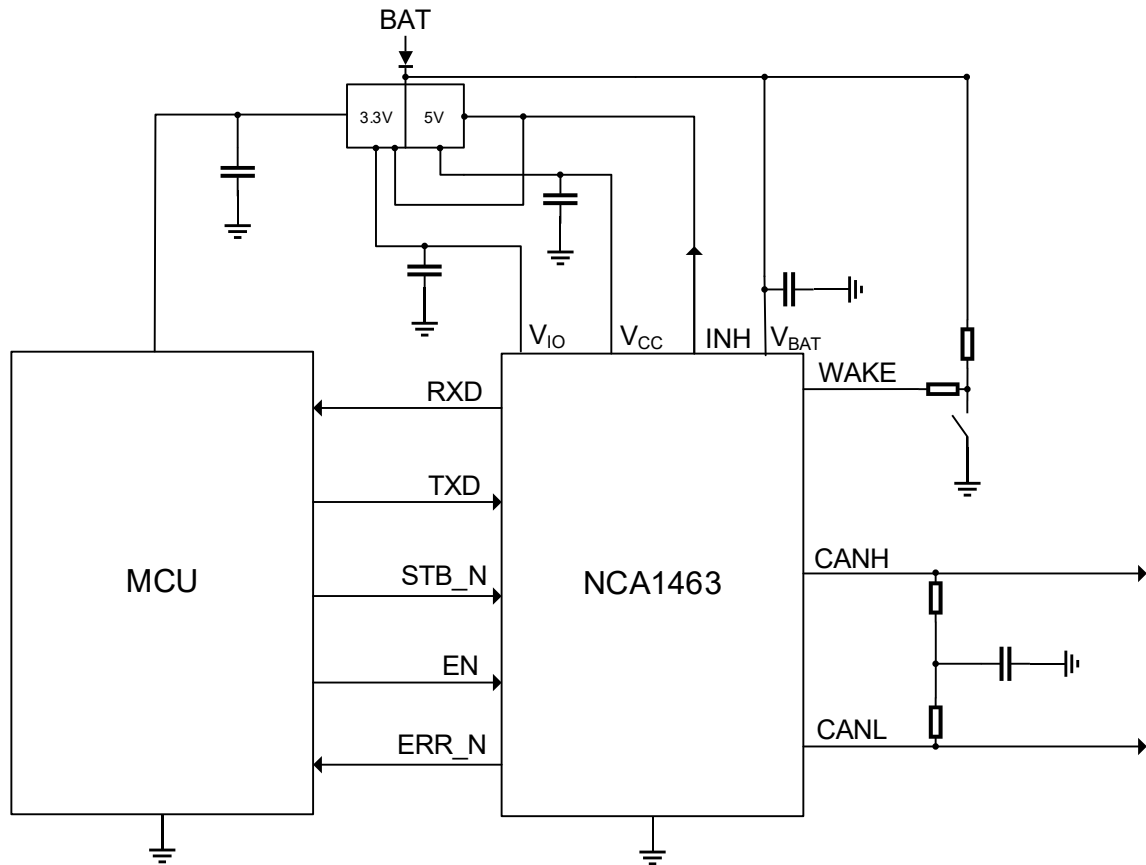
To minimize current consumption, the internal bias voltage follows the logic state on the pin after a delay of t_{WAKE} . A HIGH level on pin WAKE is followed by an internal pull-up to 5 V. A LOW level on pin WAKE is followed by an internal pull-down towards GND. In applications that do not make use of the local wake-up facility, it is recommended to connect the WAKE pin to pin VBAT or GND for optimal EMI performance.

7.10. Internal Biasing of TXD, STB_N and EN Input Pins

Pin TXD has an internal pull-up to VIO and pins STB_N and EN have internal pull-downs to GND to ensure a safe, defined state in case one, or all, of these pins is left floating. Pull-up/pull-down resistors are present on these pins in all states. Pull-down on pin EN is only active when VBAT is present.

8. Application Note

8.1. Typical Application Circuit



• Figure 8.1 Typical Application Circuit

9. Package Information

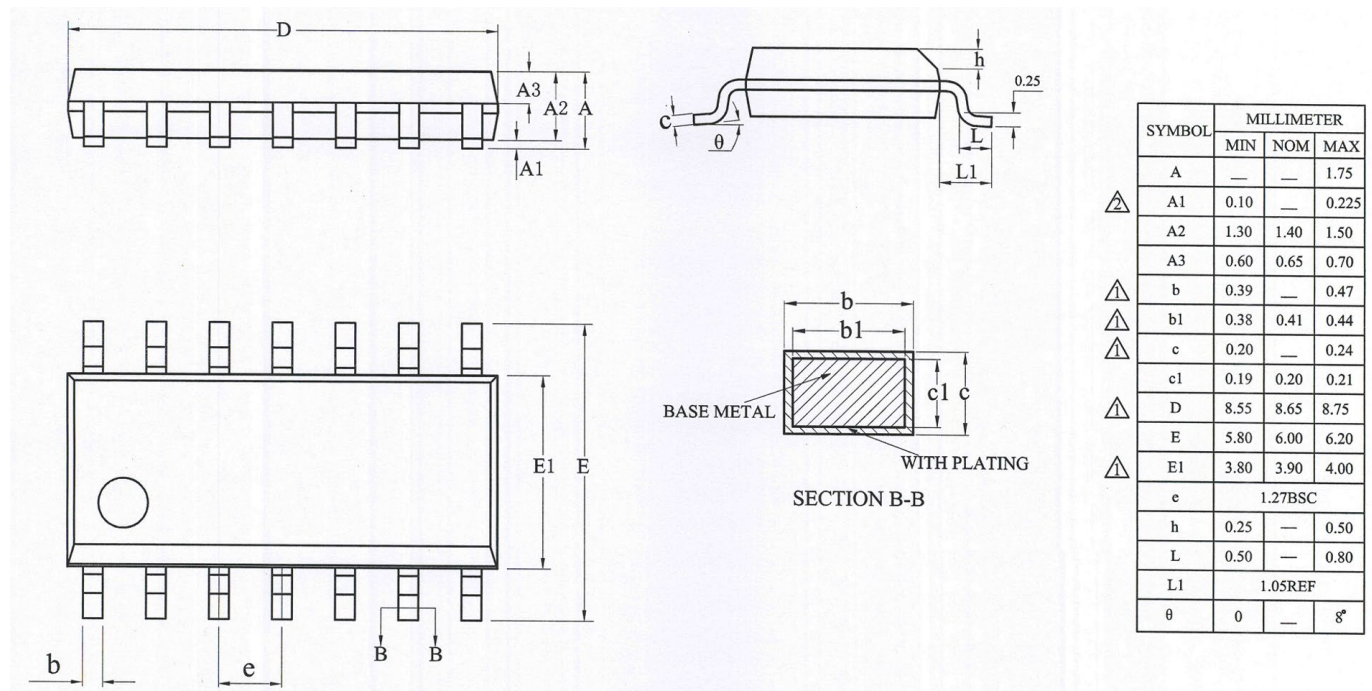
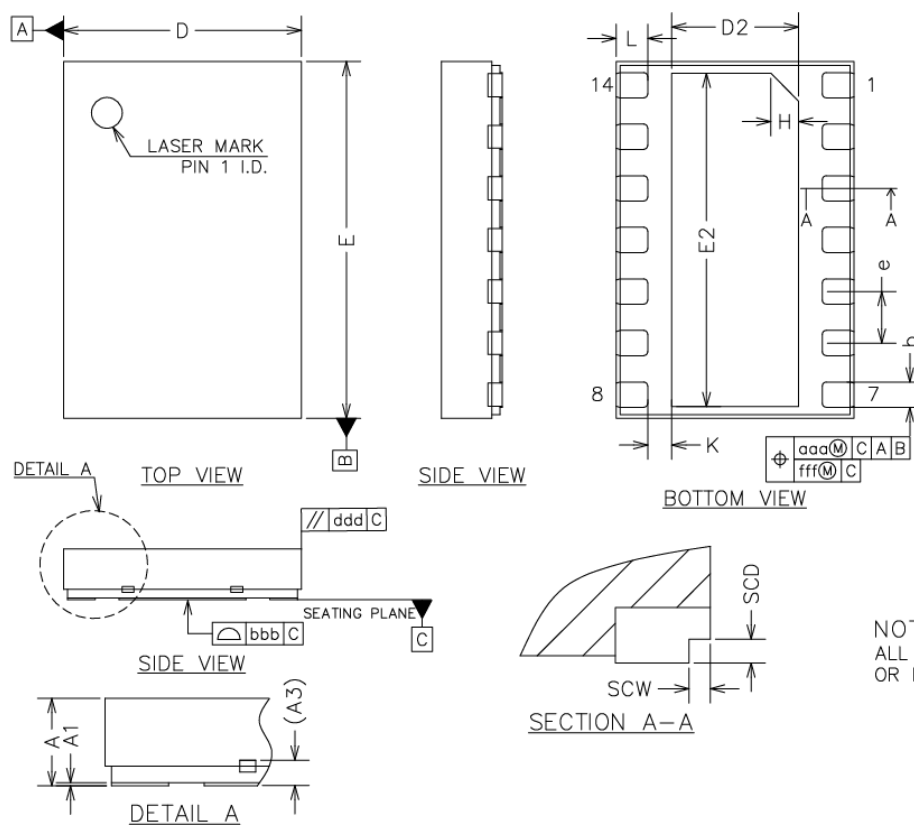


Figure 9.1 SOP14 Package Shape and Dimension

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.27	0.32	0.37
D	2.90	3.00	3.10
E	4.40	4.50	4.60
D2	1.50	1.60	1.70
E2	4.10	4.20	4.30
e	0.65 BSC		
H	0.35REF		
K	0.20	0.30	0.40
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.05		
ddd	0.10		
fff	0.08		
SCW	0.01	—	0.11
SCD	0.10	—	0.18



NOTE:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH
OR PROTRUSIONS.

Figure 9.2 DFN14 Package Shape and Dimension

10. Ordering Information

<i>Part Number</i>	<i>Max Data Rate (Mbps)</i>	<i>Operation Temperature</i>	<i>MSL</i>	<i>Package Type</i>	<i>Package Drawing</i>	<i>Device Marking</i>	<i>MPQ</i>	<i>SPQ</i>
NCA1463-Q1SPKR	8	-40 to 125°C	3	SOP14	SOP14	NCA 1463Q	2500	2500
NCA1463-Q1DNKR	8	-40 to 125°C	2	DFN14	DFN14	NCA 1463Q	6000	6000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.								

11. Tape and Reel Information

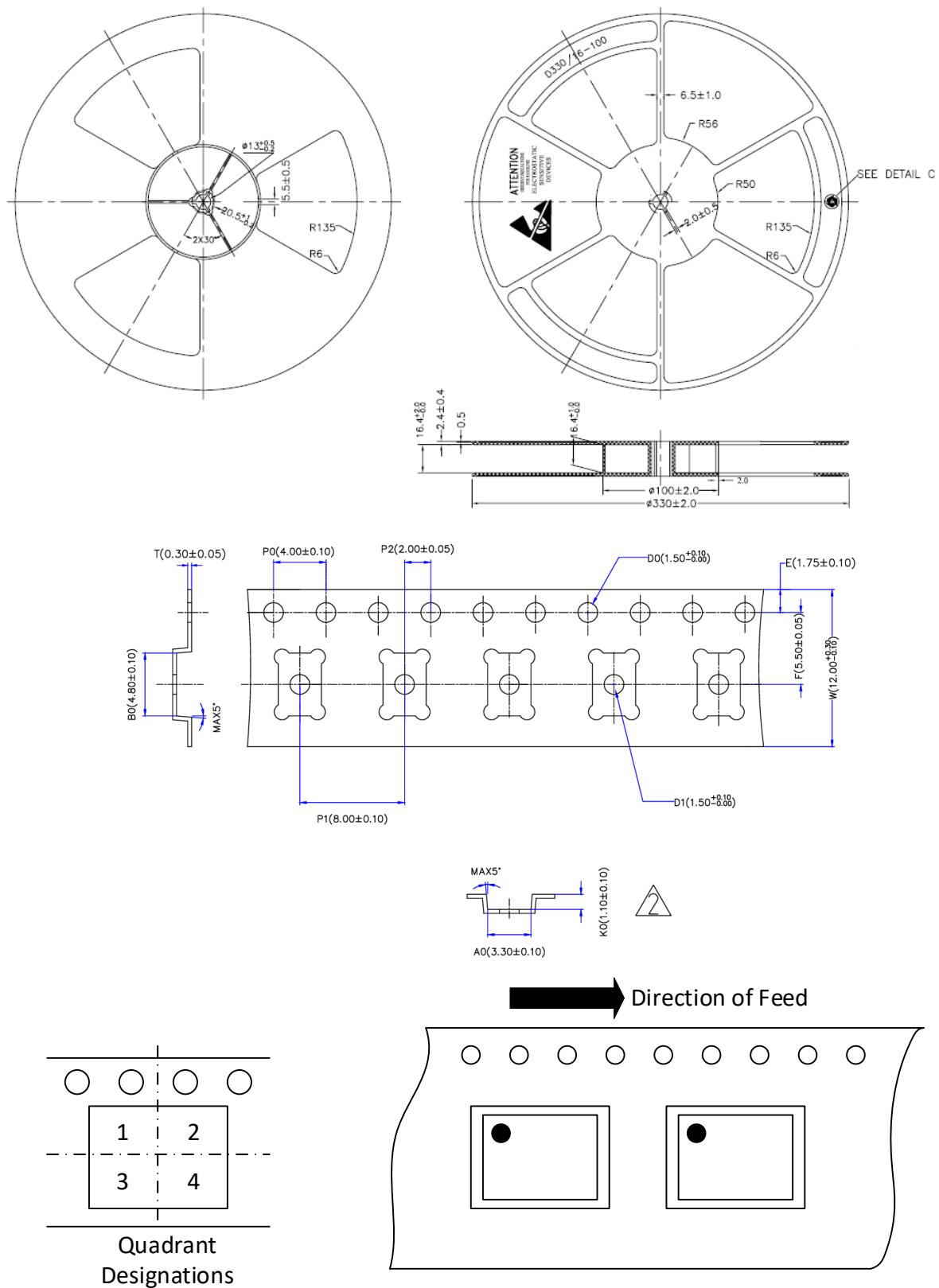


Figure 11.1 Tape and Reel Information of SOP14

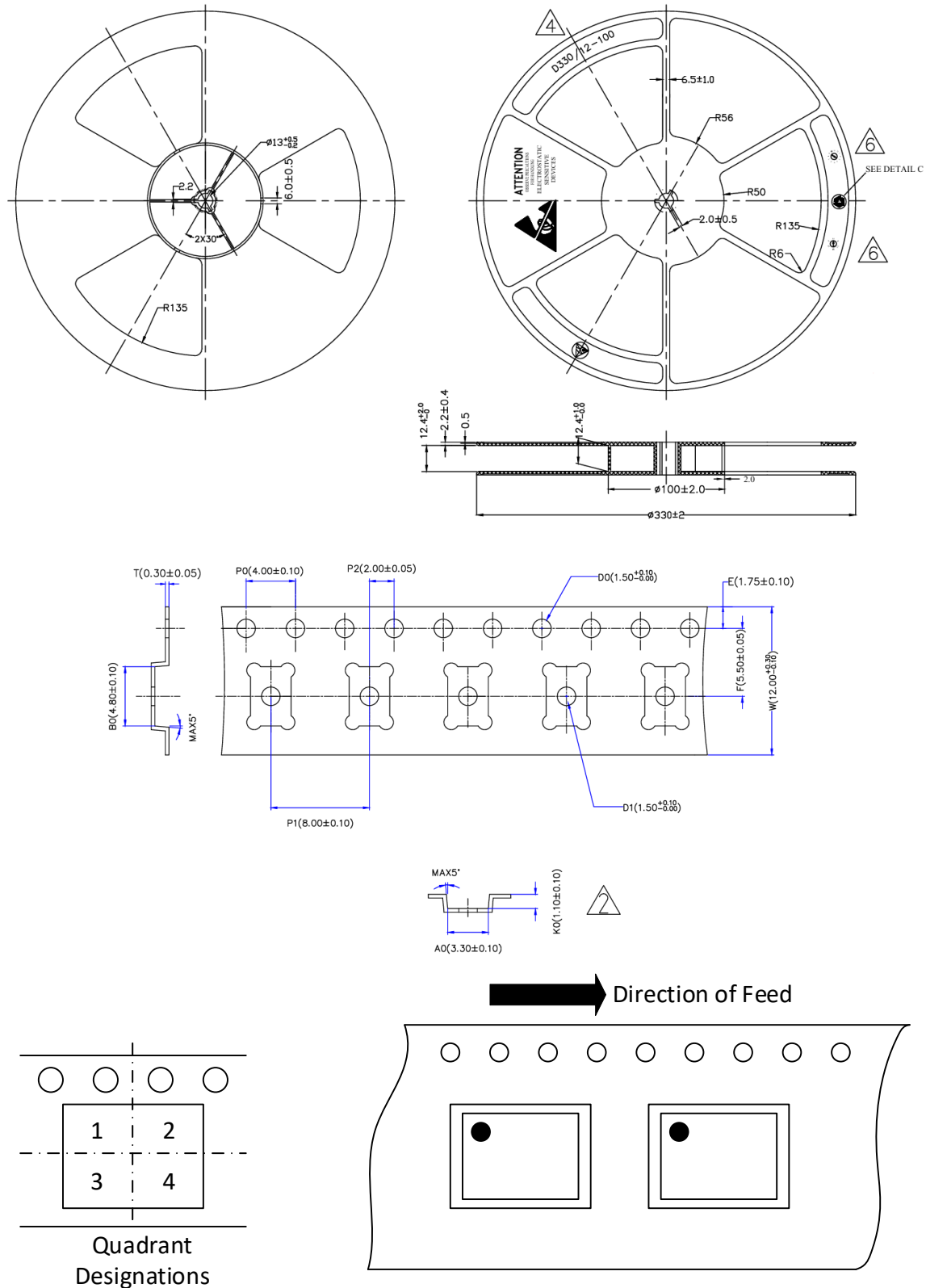


Figure 11.2 Tape and Reel Information of DFN14

12. Revision History

Revision	Description	Date
1.0	Initial Version.	2026/09/15

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE's products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE's products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE's products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE's products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd