

Product Overview

The NCA1021A is a LIN (Local Interconnect Network) transceiver with a low-power mode and multiple wake-up methods. It supports up to 20 kbps for sending and receiving communication and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602 and ISO 17987-4: 2025 (12V LIN systems).

In sleep mode, the power consumption of NCA1021A is extremely low. It supports remote wake-up and local wake-up via LIN bus, pin WAKE_N and pin SLP_N. The device can also use the INH output pin as a sign to control the working state of other devices in the local system, such as the voltage regulator, to achieve low power operation of the system.

The NCA1021A converts the signal received from TXD into a LIN bus signal through waveform shaping and slew rate adjustment to reduce electromagnetic emission (EME). TXD has a dominant time-out protection function to prevent the LIN bus from being stuck dominant.

Key Features

- Compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602 and ISO 17987-4: 2025 standard
- Very low electromagnetic emissions (EME)
- High electromagnetic immunity (EMI)
- Support for 12 V applications
- Input levels compatible with 3.3 V and 5 V devices
- Bus fault protection from -40 V to +40 V
- Wake-up source recognition (local or remote)
- Integrated LIN pull-up resistor
- Transmit data (TXD) dominant time-out function
- K-line compatible
- AEC-Q100 qualified for automotive applications (Grade 1)

- Over temperature protection
- Data rate: up to 20 kbps
- Operating temperature range: -40 °C~125 °C
- RoHS compliance
- Available packages:
 - SOP8
 - DFN8

Applications

- Body sensor and module control
- Automotive steering wheel and instrument cluster
- Powertrain system and electric motors

Device Information

Part Number	Package	Body Size
NCA1021A-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1021A-Q1DNR	DFN8	3.00mm × 3.00mm

Function Block Diagram

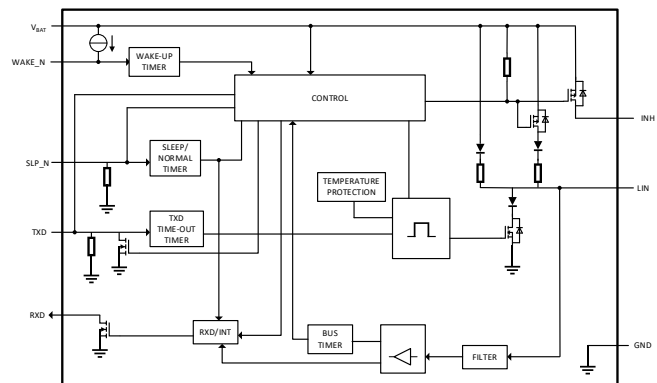


Figure 1. NCA1021A block diagram

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1. Pin Configuration and Functions

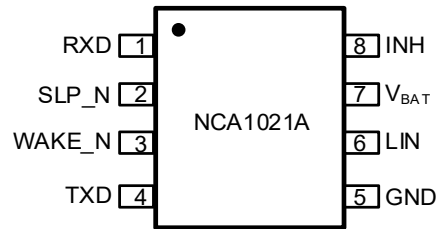


Figure 1.1 NCA1021A SOP8 Package

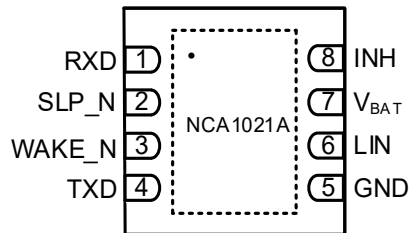


Figure 1.2 NCA1021A DFN8 Package

Table 1.1 NCA1021A Pin Configuration and Description

NCA1021A PIN NO.	SYMBOL	FUNCTION
1	RXD	Receive data output (open-drain); In standby mode, the RXD pin is driven low to indicate a wake-up request.
2	SLP_N	Sleep control input (active low); Integrated pull down.
3	WAKE_N	Local wake-up input, positive or negative edge triggered.
4	TXD	Transmit data input; Integrated pull down; Active low output after a local wake-up event.
5	GND	Ground.
6	LIN	LIN bus line, input/output.
7	V _{BAT}	Battery supply voltage.
8	INH	Battery related inhibit output for controlling an external voltage regulator. Only floating in sleep mode, the rest is high.
Thermal Pad		Not electrically connection, connect the thermal pad to PCB for thermal dissipation.

2. Absolute Maximum Ratings

Current into device pins is defined as positive. Current out of device pins is defined as negative. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Battery supply voltage	V_{BAT}	-0.3		40	V	With respect to GND
Voltage on pin TXD	V_{TXD}	-0.3		6	V	I_{TXD} no limitation
		-0.3		7	V	$I_{TXD} < 500 \mu A$
Voltage on pin RXD	V_{RXD}	-0.3		6	V	I_{RXD} no limitation
		-0.3		7	V	$I_{RXD} < 500 \mu A$
Voltage on pin SLP_N	V_{SLP_N}	-0.3		6	V	I_{SLP_N} no limitation
		-0.3		7	V	$I_{SLP_N} < 500 \mu A$
Voltage on pin LIN	V_{LIN}	-40		40	V	Limiting value with respect to GND, V_{BAT} and V_{WAKE_N}
Voltage on pin WAKE_N	V_{WAKE_N}	-0.3		40	V	
Current on pin WAKE_N	I_{WAKE_N}	-15			mA	Only relevant if $V_{WAKE_N} < V_{GND} - 0.3$, current will flow into pin GND
Voltage on pin INH	V_{INH}	-0.3		$V_{BAT} + 0.3$	V	
Output current on pin INH	$I_{O(INH)}$	-50		15	mA	
Operation ambient temperature	T_a	-40		125	°C	
Virtual junction temperature	T_{vj}	-40		150		
Storage temperature	T_{stg}	-55		150		

3. ESD ratings

Symbol	Ratings	Value	Unit
$V_{ESD-HBM1}$ $V_{ESD-HBM2}$	Human body model (JESD22/A114) - 100pF, 1.5kΩ ● Pins WAKE, INH, LIN and V_{BAT} with respect to ground ● Other pins	±8.0 ±2.0	kV kV
$V_{ESD-CDM}$	Charged device model (JESD22/C101): ● All pins	±2	kV
$V_{ESD-System}$	System, per IEC 61000-4-2 ● Pin LIN ● Pin WAKE_N and V_{BAT} (per IEC 62228-2, Capacitor to GND is 100 nF)	±6 ±15	kV kV

Symbol	Ratings	Value	Unit
V_{Tran}	ISO 7637 ISO Pulse Transients		
	● Pulse 1	-100	V
	● Pulse 2a	75	V
	● Pulse 3a	-150	V
	● Pulse 3b	100	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Battery supply voltage	V_{BAT}	4.5		36	V
LIN bus input voltage	V_{LIN}	0		36	V
Logic pin voltage	V_{LOGIC}	0		5.5	V

5. Thermal Characteristics

Parameters	Symbol	SOP8	DFN8	Unit
Junction-to-air thermal resistance	θ_{JA}	125.3	53.3	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC (top)}$	65.4	60	°C/W
Junction-to-board thermal resistance	θ_{JB}	68.7	25.6	°C/W

6. Specifications

6.1. Electrical Characteristics

($V_{BAT} = 4.5\text{ V}$ to 36 V , $T_a = -40\text{ °C}$ to 125 °C . Unless otherwise noted, typical values are at $V_{BAT} = 12\text{ V}$, $T_a = 25\text{ °C}$, $R_{L(LIN-VBAT)} = 500\text{ }\Omega$).

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Battery supply current	I_{BAT}			20	μA	Sleep mode, $V_{LIN} = V_{BAT} = V_{WAKE_N}$, $V_{TXD} = V_{SLP_N} = 0\text{ V}$
				55	μA	Standby mode, bus recessive $V_{INH} = V_{LIN} = V_{WAKE_N} = V_{BAT}$, $V_{TXD} = V_{SLP_N} = 0\text{ V}$
			500	1000	μA	Standby mode, bus dominant $V_{BAT} = V_{INH} = V_{WAKE_N} = 12\text{ V}$, $V_{LIN} = 0\text{ V}$ $V_{TXD} = 0\text{ V}$, $V_{SLP_N} = 0\text{ V}$
				1700	μA	Standby mode, bus dominant

Parameters	Symbol	Min	Typ	Max	Unit	Comments
						$V_{BAT} = V_{INH} = V_{WAKE_N}$, $V_{LIN} = 0\text{ V}$ $V_{TXD} = 0\text{ V}$, $V_{SLP_N} = 0\text{ V}$
				1200	μA	Normal mode, bus recessive $V_{INH} = V_{LIN} = V_{WAKE_N} = V_{BAT}$ $V_{TXD} = 5\text{ V}$, $V_{SLP_N} = 5\text{ V}$
			1.5	3	mA	Normal mode, bus dominant, no load $V_{BAT} = V_{INH} = V_{WAKE_N} = 12\text{ V}$ $V_{TXD} = 0\text{V}$, $V_{SLP_N} = 5\text{ V}$
				6	mA	Normal mode, bus dominant, no load $V_{BAT} = V_{INH} = V_{WAKE_N}$ $V_{TXD} = 0\text{V}$, $V_{SLP_N} = 5\text{ V}$
Power on reset	$V_{th(POR)L}$	1.6	3.1	3.9	V	Low-level power-on reset threshold voltage
	$V_{th(POR)H}$	2.3	3.4	4.3	V	High-level power-on reset threshold voltage
	$V_{hys(POR)}$	0.01	0.3	1	V	Power-on reset hysteresis voltage
	$V_{th(VBATL)L}$	3		4	V	Low-level V_{BAT} LOW threshold voltage
	$V_{th(VBATL)H}$	3		4	V	High-level V_{BAT} LOW threshold voltage
	$V_{hys(VBATL)}$	0.01	0.3	1	V	V_{BAT} LOW hysteresis voltage
TXD						
High-level input voltage	V_{IH}	2		7	V	
Low-level input voltage	V_{IL}	-0.3		0.8	V	
Hysteresis voltage	V_{hys}		160		mV	Guaranteed by design
Low-level input current	I_{IL}	-5		5	μA	
Output low current	I_{OL}	1.5			mA	Local wake-up request, standby mode, $V_{WAKE_N} = 0\text{ V}$, $V_{LIN} = V_{BAT}$, $V_{TXD} = 0.4\text{ V}$
Pull-down resistance on pin TXD	$R_{PD(TXD)}$	140		1200	$\text{k}\Omega$	
SLP_N						
High-level input voltage	V_{IH}	2		7	V	
Low-level input voltage	V_{IL}	-0.3		0.8	V	
Hysteresis Voltage	V_{hys}		120		mV	Guaranteed by design
Low-Level Input Current	I_{IL}	-5		5	μA	$V_{SLP_N} = 0\text{ V}$

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Pull-down resistance on pin SLP_N	RPD(SLP_N)	140		1200	kΩ	$V_{SLP_N} = 5\text{ V}$
Hold time	$t_h(SLP_N)$	15			μs	Guaranteed by design
RXD (Open-Drain)						
High-level leakage current	I_{LH}	-5		5	μA	Normal mode, $V_{LIN} = V_{BAT}$, $V_{RXD} = 5\text{ V}$
Low-level output current	I_{OL}	1.5			mA	Normal mode, $V_{LIN} = 0\text{ V}$, $V_{RXD} = 0.4\text{ V}$
WAKE_N						
High-level input voltage	V_{IH}	$V_{BAT}-1$		$V_{BAT} + 0.3$	V	
Low-level input voltage	V_{IL}	-0.3		$V_{BAT} - 3.3$	V	
High-level input current	I_{IH}	-5		5	μA	$V_{WAKE_N} = 36\text{ V}$, $V_{BAT} = 36\text{ V}$
Low-level input current	I_{IL}	-30		-1	μA	$V_{WAKE_N} = 0\text{ V}$
INH						
Switch-on resistance Between pins V_{BAT} and INH	$R_{sw}(V_{BAT}-INH)$		20	50	Ω	Switch-on resistance between pins V_{BAT} and INH. Standby, normal, and power-on modes, $I_{INH} = -15\text{ mA}$, $V_{BAT} = 12\text{ V}$
High-level leakage current	I_{LH}	-5		5	μA	Sleep mode, $V_{INH} = 36\text{ V}$, $V_{BAT} = 36\text{ V}$
LIN						
Current limitation for transmitter dominant state	I_{BUS_LIM}	40		100	mA	$V_{BAT} = 18\text{ V}$, $V_{LIN} = 18\text{ V}$, $V_{TXD} = 0\text{ V}$
Pull-up resistance	R_{pu}	50		250	kΩ	Sleep mode, $V_{SLP_N} = 0\text{ V}$
Receiver recessive input leakage current	$I_{BUS_PAS_rec}$			1	μA	$V_{LIN} = 36\text{ V}$, $V_{BAT} = 4.5\text{ V}$, $V_{TXD} = 5\text{ V}$
Receiver dominant input leakage current including pull-up resistor	$I_{BUS_PAS_dom}$	-600			μA	Normal mode, $V_{TXD} = 5\text{ V}$ $V_{LIN} = 0\text{ V}$, $V_{BAT} = 12\text{ V}$
Voltage drop at the serial diode	$V_{SerDiode}$	0.4		1	V	Guaranteed by design
Loss-of-ground bus current	$I_{BUS_NO_GN_D}$	-700		10	μA	$V_{BAT} = 18\text{ V}$, $V_{LIN} = 0\text{ V}$
Loss-of-battery bus current	$I_{BUS_NO_BAT}$			1	μA	$V_{BAT} = 0\text{ V}$, $V_{LIN} = 27\text{ V}$
Receiver dominant state	V_{BUSdom}			$0.4 \cdot V_{BAT}$	V	$V_{BAT} = 5.5\text{ V to } 36\text{ V}$

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Receiver recessive state	V _{BUSrec}	0.6*V _{BAT}			V	V _{BAT} = 5.5 V to 36 V
Receiver center voltage	V _{BUS_CNT}	0.475* V _{BAT}		0.525* V _{BAT}	V	V _{BUS_CNT} = (V _{BUSrec} + V _{BUSdom}) / 2 V _{BAT} = 5.5 V to 36 V
Receiver hysteresis voltage	V _{HYS}			0.175* V _{BAT}	V	V _{HYS} = V _{BUSrec} - V _{BUSdom} V _{BAT} = 5.5 V to 36 V
Slave Resistance	R _{slave}	28		47	kΩ	Connected between pins LIN and V _{BAT} , V _{LIN} = 0 V, V _{BAT} = 12 V
Capacitance on pin LIN	C _{LIN}			30	pF	Guaranteed by design
Dominant output voltage	V _{o(dom)}			1.4	V	Normal mode, V _{TXD} = 0 V, V _{BAT} = 7 V
				2.0	V	Normal mode, V _{TXD} = 0 V, V _{BAT} = 18 V
Thermal shutdown						
Shutdown junction temperature	T _{j(sd)}	150	175	200	°C	Guaranteed by design
Hysteresis temperature	T _{hys}		20		°C	Guaranteed by design

6.2.Switching Characteristics

($V_{BAT} = 4.5 \text{ V to } 18 \text{ V}$, $T_a = -40 \text{ }^{\circ}\text{C to } 125 \text{ }^{\circ}\text{C}$. Unless otherwise noted, typical values are at $V_{BAT} = 12 \text{ V}$, $T_a = 25 \text{ }^{\circ}\text{C}$, $R_{L(LIN-VBAT)} = 500 \text{ }\Omega$).

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Duty cycles (bus load conditions (C_{BUS} / R_{BUS}): 1 nF / 1 k Ω , 6.8 nF / 660 Ω , 10 nF / 500 Ω), see Figure 6. 1						
Duty Cycle 1	D1 ^[1]	0.396				$V_{th(rec)(max)} = 0.744 \times V_{BAT}$ $V_{th(dom)(max)} = 0.581 \times V_{BAT}$ $V_{BAT} = 7 \text{ V to } 18 \text{ V}$, $t_{bit} = 50 \text{ }\mu\text{s}$ ^[2] ISO 17987 Param 27
		0.396				$V_{th(rec)(max)} = 0.76 \times V_{BAT}$ $V_{th(dom)(max)} = 0.593 \times V_{BAT}$ $V_{BAT} = 4.5 \text{ V to } 7 \text{ V}$, $t_{bit} = 50 \text{ }\mu\text{s}$ ^[3]
Duty Cycle 2	D2			0.581		$V_{th(rec)(min)} = 0.422 \times V_{BAT}$ $V_{th(dom)(min)} = 0.284 \times V_{BAT}$ $V_{BAT} = 7.6 \text{ V to } 18 \text{ V}$, $t_{bit} = 50 \text{ }\mu\text{s}$ ISO 17987 Param 28
				0.581		$V_{th(rec)(min)} = 0.41 \times V_{BAT}$ $V_{th(dom)(min)} = 0.275 \times V_{BAT}$ $V_{BAT} = 4.5 \text{ V to } 7.6 \text{ V}$, $t_{bit} = 50 \text{ }\mu\text{s}$
Duty Cycle 3	D3	0.417				$V_{th(rec)(max)} = 0.778 \times V_{BAT}$ $V_{th(dom)(max)} = 0.616 \times V_{BAT}$ $V_{BAT} = 7 \text{ V to } 18 \text{ V}$, $t_{bit} = 96 \text{ }\mu\text{s}$

Parameters	Symbol	Min	Typ	Max	Unit	Comments
						ISO 17987 Param 29
		0.417				$V_{th(rec)(max)} = 0.797 \times V_{BAT}$ $V_{th(dom)(max)} = 0.63 \times V_{BAT}$ $V_{BAT} = 4.5 \text{ V to } 7 \text{ V}, t_{bit} = 96 \mu\text{s}$
Duty Cycle 4	D4			0.59		$V_{th(rec)(min)} = 0.389 \times V_{BAT}$ $V_{th(dom)(min)} = 0.251 \times V_{BAT}$ $V_{BAT} = 7.6 \text{ V to } 18 \text{ V}, t_{bit} = 96 \mu\text{s}$ ISO 17987 Param 30
				0.59		$V_{th(rec)(min)} = 0.378 \times V_{BAT}$ $V_{th(dom)(min)} = 0.241 \times V_{BAT}$ $V_{BAT} = 4.5 \text{ V to } 7.6 \text{ V}, t_{bit} = 96 \mu\text{s}$
Timing characteristics						
Fall Time	t_f			22.5	μs	20 % - 80 %, see Figure 6. 3
Rise Time	t_r			22.5	μs	$C_{BUS} = 1 \text{ nF}$ and $R_{BUS} = 1 \text{ k}\Omega$
Difference between rise and fall time	$t_{(r-f)}$	-6		8	μs	$C_{BUS} = 6.8 \text{ nF}$ and $R_{BUS} = 660 \Omega$ $C_{BUS} = 10 \text{ nF}$ and $R_{BUS} = 500 \Omega$
Transmitter propagation delay of falling edge	t_{tx_pdf}			20	μs	See Figure 6. 3 $R_{BUS} = 500 \Omega$
Transmitter propagation delay of rising edge	t_{tx_pdr}			20	μs	
Transmitter propagation delay symmetry	t_{tx_sym}	-4		4.6	μs	$t_{tx_sym} = t_{tx_pdr} - t_{tx_pdf}$
Receiver propagation delay of falling edge	t_{rx_pdf}			6	μs	See Figure 6. 4 $C_{RXD} = 20 \text{ pF}^{[4]}$ and $R_{RXD} = 2.4 \text{ k}\Omega$
Receiver propagation delay of rising edge	t_{rx_pdr}			6	μs	
Receiver propagation delay symmetry	t_{rx_sym}	-2		2	μs	$t_{rx_sym} = t_{rx_pdr} - t_{rx_pdf}$
LIN dominant wake-up time	$t_{wake(dom)LIN}$	30	80	150	μs	Sleep mode
Dominant wake-up time on pin WAKE_N	$t_{wake(dom)WAKE_N}$	7	55	90	μs	Sleep mode
Go to normal time	$t_{gotonorm}$	2	10	20	μs	Time period for mode change from sleep, power-on or standby mode into normal mode
Normal mode initialization time	$t_{init(norm)}$			25	μs	Normal mode, initialization time, guaranteed by design
Go to sleep time	$t_{gotosleep}$	2	20	30	μs	Time period for mode change from normal mode into sleep mode

Parameters	Symbol	Min	Typ	Max	Unit	Comments
TXD dominant time-out time	$t_{to(dom)TXD}$	27	55	90	ms	Timer started at falling edge on TXD with $V_{TXD} = 0\text{ V}$

- [1] $D1, D3 = t_{bus(rec)(min)} / (2 \cdot t_{bit})$, $D2, D4 = t_{bus(rec)(max)} / (2 \cdot t_{bit})$, as illustrated in Figure 6. 2.
- [2] $t_{bit} = 50\text{ }\mu\text{s}$ (20 kbps), $t_{bit} = 96\text{ }\mu\text{s}$ (10.4 kbps).
- [3] $D1$ meets ISO 17987 Param 88, $D2$ meets ISO 17987 Param 89, $D3$ meets ISO 17987 Param 90, $D4$ meets ISO 17987 Param 91.
- [4] C_{RXD} includes load and jig capacitance.

6.3.Parameter Measurement Information

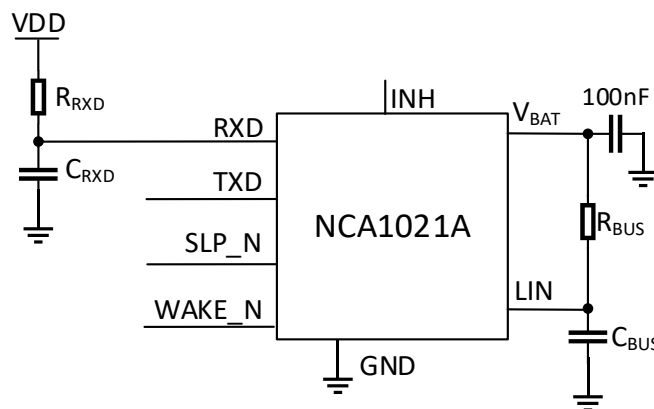


Figure 6. 1 Timing test circuit for LIN transceiver

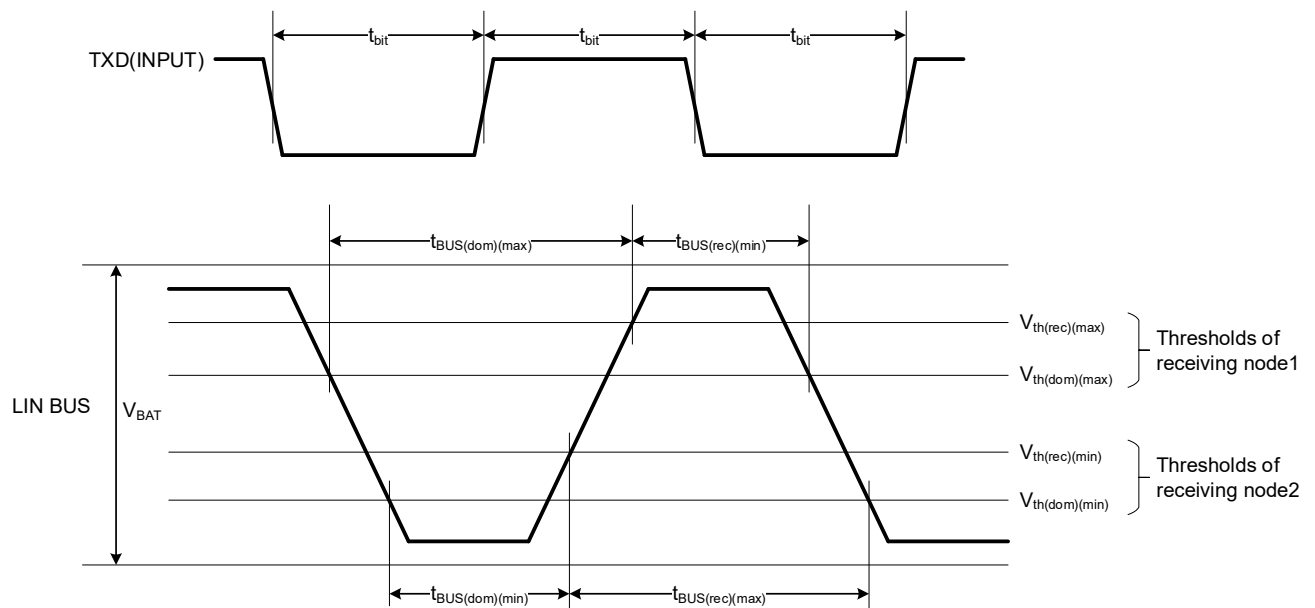


Figure 6. 2 Timing diagram of LIN transceiver

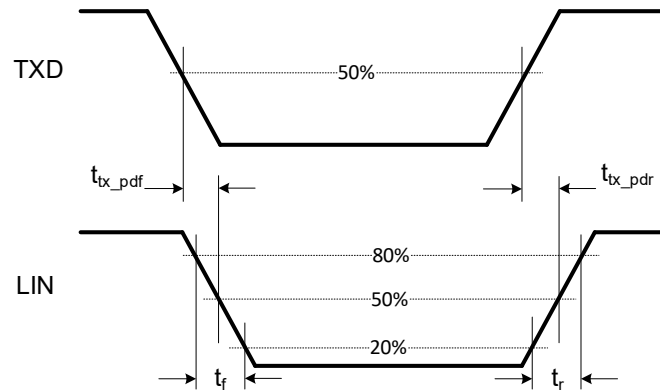


Figure 6. 3 Propagation delay and transition times from TXD to LIN

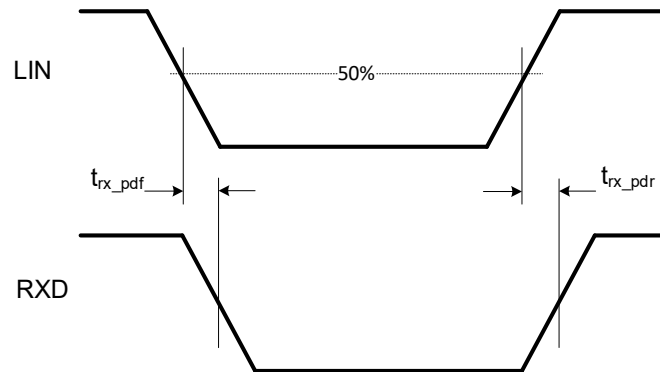


Figure 6. 4 Propagation delay and transition times from LIN to RXD

7. Function Description

7.1. Overview

The NCA1021A is a LIN transceiver with a low-power mode and multiple wake-up methods. The NCA1021A is fully compatible with the ISO 17987-4: 2025 standard. The NCA1021A controls the state of the LIN bus via the TXD pin and reports the state of the bus via its open-drain RXD output pin. The NCA1021A features an optimized wave-shaping transmitter for low electromagnetic emissions. Therefore, it provides high electromagnetic immunity and low emissions.

The data rate of the NCA1021A is up to 20 kbps. No external pull-up components are required for slave applications. For master applications, a resistor in the range of 1 kΩ and a reverse diode must be connected between the LIN bus and the power supply V_{BAT} or the INH pin.

The NCA1021A supports three methods for wake-up from sleep mode via LIN bus, WAKE_N pin or SLP_N pin.

The NCA1021A allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a node through the NCA1021A INH output pin.

The NCA1021A provides thermal protection, undervoltage detection, TXD dominant time-out function and loss of power protection. Digital I/O levels are compatible with 3.3 V and 5 V microcontrollers.

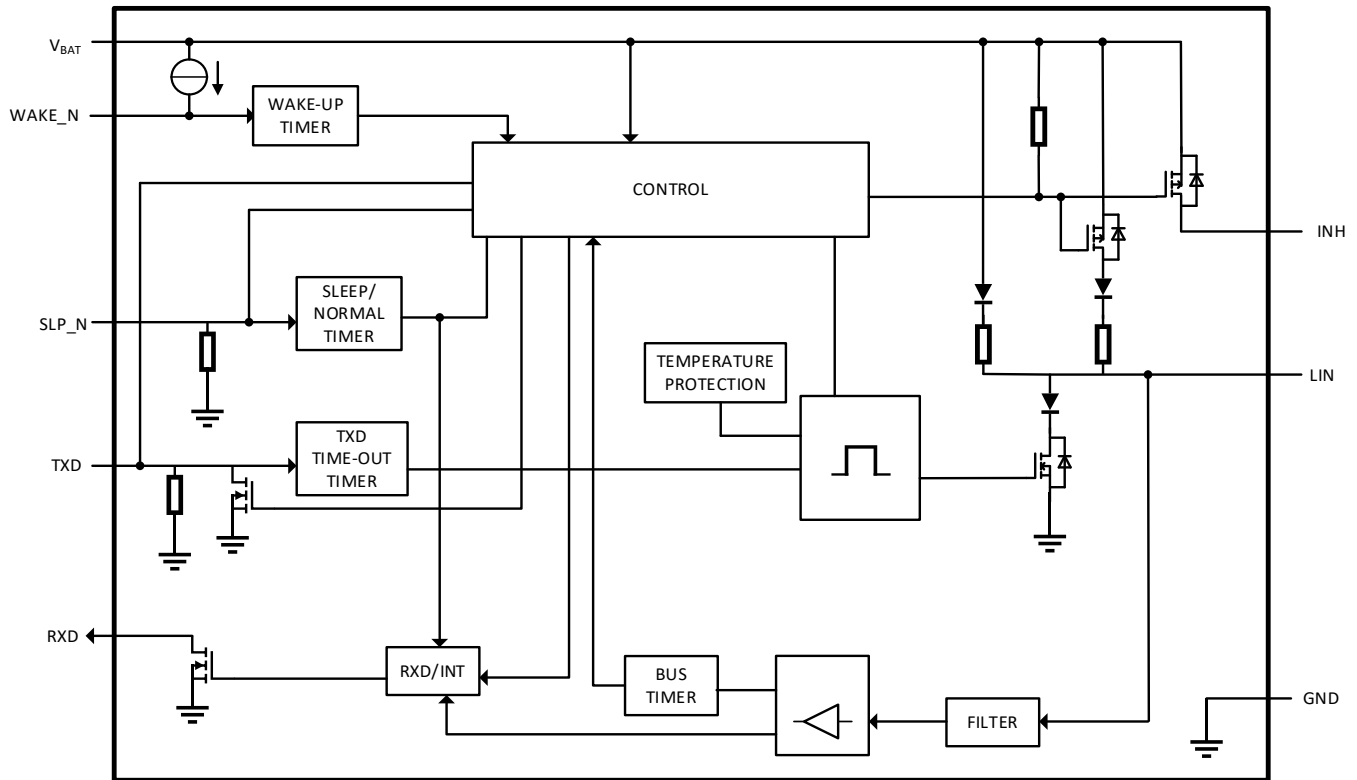


Figure 7. 1 Block diagram of NCA1021A

7.2. Device Functional Modes

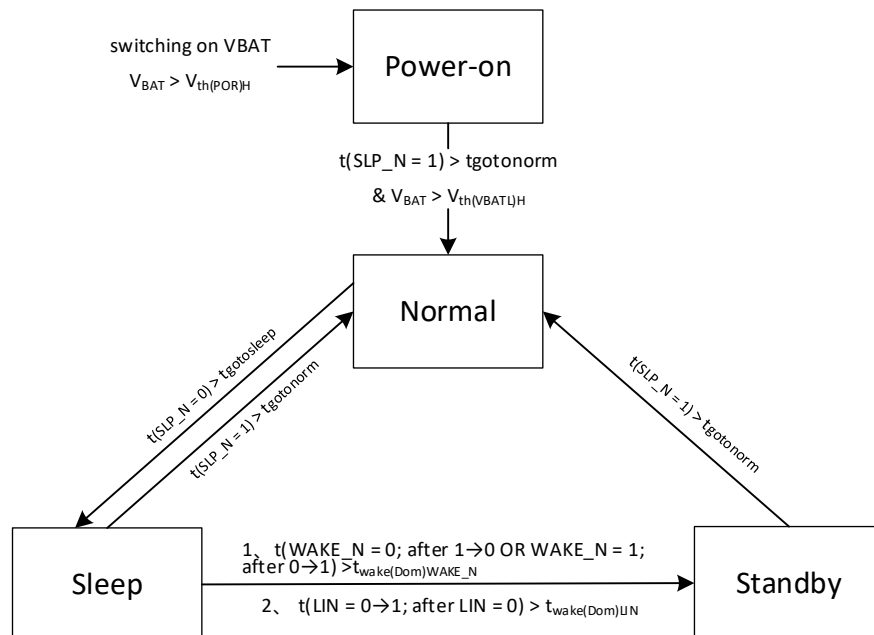


Figure 7. 2 State diagram of NCA1021A

Table 7. 1 Function table

Mode	SLP_N	LIN	TXD	RXD	INH	Transmitter
Power-on ^[1]	low	pulled up by 40 kΩ	weak pull-down	floating	high	OFF
Normal ^[2]	high	pulled up by 40 kΩ	HIGH: recessive state LOW: dominant state	HIGH: recessive state LOW: dominant state	high	ON
Sleep	low	weak pull up	weak pull-down	floating	floating	OFF
Standby	low	pulled up by 40 kΩ	weak pull-down if remote wake-up, strong pull-down if local wake-up ^[4]	LOW ^[5]	high	OFF

- [1] Power-on mode is entered after switching on V_{BAT} .
- [2] Normal mode is entered after a positive edge on SLP_N. If TXD is low, the transmitter is OFF. In the event of a short circuit to ground on pin TXD, the transmitter will be disabled.
- [3] When V_{BAT} is above $V_{th(POR)H}$ but below $V_{th(VBATL)H}$, or below $V_{th(VBATL)L}$ but above $V_{th(POR)L}$, the protection circuit disables the transmitter. The transmitter is enabled again when $V_{BAT} > V_{th(VBATL)H}$ and a recessive level is present at pin TXD.
- [4] The internal wake-up source flag on TXD will be reset after a positive edge on pin SLP_N.
- [5] The wake-up interrupt on pin RXD is released after a positive edge on pin SLP_N.

7.2.1 Power-on Mode

When V_{BAT} exceeds the power-on-reset threshold voltage $V_{th(POR)H}$, the NCA1021A enters power-on mode. Though the NCA1021A is powered-up and INH is high, both the transmitter and receiver are still inactive. If $t_{(SLP_N = 1)} > t_{gotonorm}$, the NCA1021A will enter normal mode.

7.2.2 Normal Mode

In normal mode, the NCA1021A transmits and receives data on the LIN bus. The transmitter receives the signal from the MCU via the TXD, and first determines the dominant timeout, and then converts it into an optimized bus signal with controlled slew rate and waveform shaping to minimize EME. The receiver detects the signal on the LIN bus input and transmits it to the microcontroller through the RXD.

The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). No external pull-up components are required for slave applications. For master application, an external 1kΩ resistor in series with a diode should be connected between pin INH or V_{BAT} and pin LIN, as shown in Figure 8. 1.

7.2.3 Sleep Mode

Sleep mode is the lowest power consumption mode of the NCA1021A. In sleep mode, the transmitter is disabled, releasing INH to a floating state. LIN bus is weakly pulled up, which can minimize the power dissipation in the event that pin LIN is short-circuited to ground.

The INH pin goes high-impedance in sleep mode, turning off any system power devices controlled by INH, thus reducing overall system power consumption

The only way to enter sleep mode is to make $t_{(SLP_N = 0)} > t_{gotosleep}$ in normal mode.

The NCA1021A in sleep mode supports three methods to wake up. They are wake-up remotely via LIN bus, and wake-up locally via pin SLP_N or pin WAKE_N.

7.2.4 Standby Mode

When NCA1021A is in sleep mode, it will enter standby mode upon a local or remote wake-up via LIN bus or pin WAKE_N. When a wake-up event occurs and the NCA1021A enters standby mode, the pin RXD is driven low signaling the wake-up event to the controller.

In standby mode, the INH changes from floating to high, which can be used as a control flag for other devices. In standby mode, the LIN bus slave termination resistance R_{slave} is enabled.

In standby mode, the condition of pin TXD indicates the wake-up source when pin SLP_N is still low. After being remotely awakened by the LIN bus, pin TXD will be in a weak pull-down state. After being woken up locally by the pin WAKE_N, pin TXD will be in a strong pull-down state.

The NCA1021A exits standby mode and enters normal mode when the pin SLP_N is set high for longer than $t_{gotonorm}$.

In standby mode, set the pin SLP_N high ($t_{(SLP_N=1)} > t_{gotonorm}$) to enter the normal mode. Once the device enters normal mode, the wake-up event is cleared, and the RXD output is released. The RXD output is fully operational and reflects the LIN bus state.

7.3. Pin Characteristics

7.3.1 RXD

The receiver detects the data stream at the LIN bus input pin and transfers it via pin RXD to the microcontroller. The pin RXD output structure is an open-drain output structure which allows the device to be used with 3.3 V and 5 V microcontrollers. LIN recessive is represented by a high level on the pin RXD and LIN dominant is represented by a low level on the pin RXD. In standby mode, the pin RXD is driven low which can be used as an interrupt for the microcontroller. The wake-up interrupt on pin RXD is released after a positive edge on pin SLP_N. If the microcontroller's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontrollers IO supply voltage is required.

7.3.2 SLP_N

Pin SLP_N controls the functional modes of NCA1021A. When pin SLP_N is high, NCA1021A operates in normal mode. When SLP_N is low, NCA1021A operates in sleep mode. Pin SLP_N has an internal pull-down resistor to ensure the device remains in low power mode even if SLP_N floats.

7.3.3 WAKE_N

The NCA1021A can be woken up locally via pin WAKE_N, a filter at the pin WAKE_N input prevents unwanted wake-up events due to automotive transients or EMI.

A falling edge at pin WAKE_N followed by $t_{(WAKE_N=0)} > t_{wake(dom)WAKE_N}$ or a rising edge at pin WAKE_N followed by $t_{(WAKE_N=1)} > t_{wake(dom)WAKE_N}$ results in a local wake-up. The pin WAKE_N internally pulls up to V_{BAT} . In order to prevent EMI issues, it is recommended to connect an unused pin WAKE_N to pin VBAT.

7.3.4 TXD

TXD is the interface to the MCU LIN protocol controller that is used to control the state of the LIN output. When TXD is high, the LIN output is recessive. When the TXD is low, the LIN output is dominant. The TXD pin has an internal pull-down to GND to set a default level if the pin is unpowered. In Standby mode, the status of pin TXD indicates the wake-up source: weak pull-down for a remote wake-up request and strong pull-down for a local wake-up request.

After switching to normal mode, the NCA1021A will detect the status of TXD. The LIN driver will be enabled only if a high TXD level is detected.

7.3.5 LIN

LIN has two internal pull-up resistors to V_{BAT} . In sleep mode, the internal slave termination between pins LIN and V_{BAT} is disabled to minimize the power dissipation. Only a weak pull-up between pins LIN and V_{BAT} is present. For master applications, an external 1 kΩ pull-up resistor with series blocking diode can be used.

A falling edge at pin LIN followed by a LOW level maintained for a certain time ($t_{wake(dom)LIN}$) and a rising edge at pin LIN respectively results in a remote wake-up.

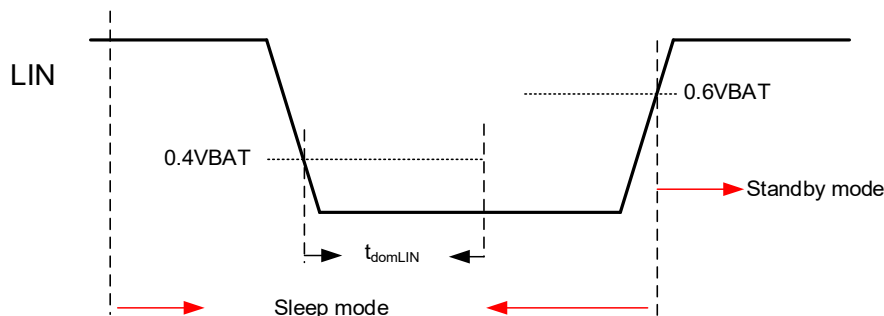


Figure 7. 3 Remote wake-up of NCA1021A

7.3.6 V_{BAT}

V_{BAT} pin is the power supply input. Even if there is a loss of power, the NCA1021A has extremely low leakage from the pin LIN, which will not pull the LIN bus down. The recommended voltage range for V_{BAT} is 4.5 V to 36 V. If V_{BAT} < 4.5 V or V_{BAT} > 36 V, the NCA1021A may remain operational, but parameter values cannot be guaranteed.

7.3.7 INH

Pin INH is a battery-related inhibit output for controlling an external voltage regulator. INH is floating only in sleep mode, otherwise it is high. As a result of the high condition on pin INH the voltage regulator and the microcontroller can be activated. When entering sleep mode, since INH is in a high-impedance state, the INH voltage falls slowly. A pull-down resistor to GND is recommended for fast discharge. Note that the resistor value should not be too low to avoid excessive power loss.

7.4. TXD Dominant Time-out Function

During normal mode, a TXD dominant time-out timer circuit in NCA1021A prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period $t_{to(dom)TXD}$. The timer is triggered by a negative edge on pin TXD. If the duration of the low-level on pin TXD exceeds the internal timer value ($t_{to(dom)TXD}$), the transmitter is disabled, driving the bus line into a recessive state. The timer is reset by a positive edge on pin TXD.

7.5. Fail-safe Features

The current of the transmitter output stage is limited to protect the transmitter against short circuit to pins V_{BAT} or GND.

In automotive applications, some LIN transceivers in a system can be unpowered or ignition supplied, while others in the network remain powered by the battery. A loss of power (pins V_{BAT} and GND) has no impact on the LIN bus line and the microcontroller. There are no reverse currents from the bus.

The transmitter at pin LIN is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the thermal protection circuit disables the transmitter. Once the overtemperature condition is removed and the junction temperature drops below the hysteresis threshold, the transmitter is re-enabled.

If V_{BAT} drops below $V_{th(VBATL)L}$, a protection circuit disables the transmitter. The transmitter is enabled again when V_{BAT} > $V_{th(VBATL)H}$.

8. Application Note

8.1. Typical Application

The Figure 8. 1 shows the typical application schematic of NCA1021A. The NCA1021A requires a 0.1 μ F bypass capacitor between V_{BAT} and GND. To prevent the rectification effect of the diode from affecting the V_{BAT} voltage, it is recommended to add a 1 μ F capacitor in front of the diode. The capacitance value can be adjusted based on system requirements. The capacitor should be placed as close as possible to the package.

For a Master application, an external 1k Ω resistor in series with a diode should be connected between pin INH or V_{BAT} and pin LIN. If RXD on the MCU does not have an internal pull-up, an external pull-up resistor is required.

The LIN external capacitance value is selected according to the actual situation (refer to ISO 17987-4:2025 5.3.6 Line characteristics), generally 220 pF for the slave or 1nF for the master. EMI filtering on the LIN bus is strongly recommended for EMC compliance. In addition to noise radiated by the LIN signal itself from rising/falling edges and asymmetric waveforms, noise from other vehicle systems can also couple onto the LIN bus.

Transient pulse suppression is also important for LIN buses, so it is recommended to add bidirectional TVS diodes.

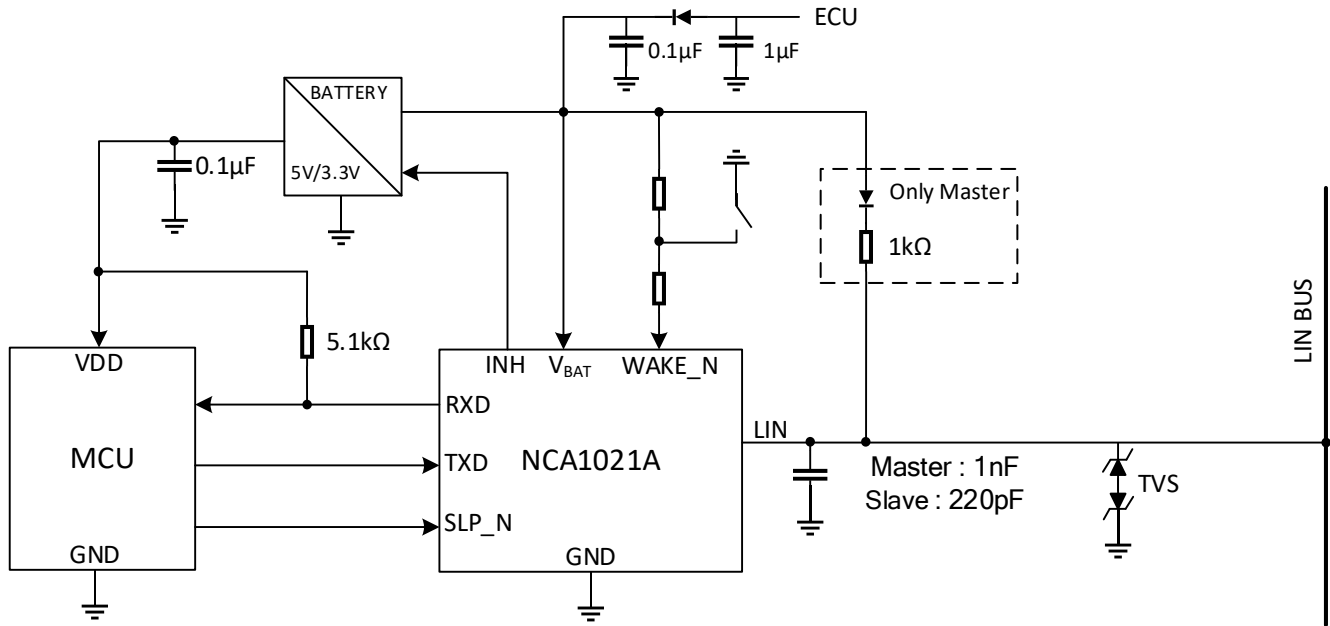


Figure 8. 1 Basic schematic of NCA1021A

9. Package Information

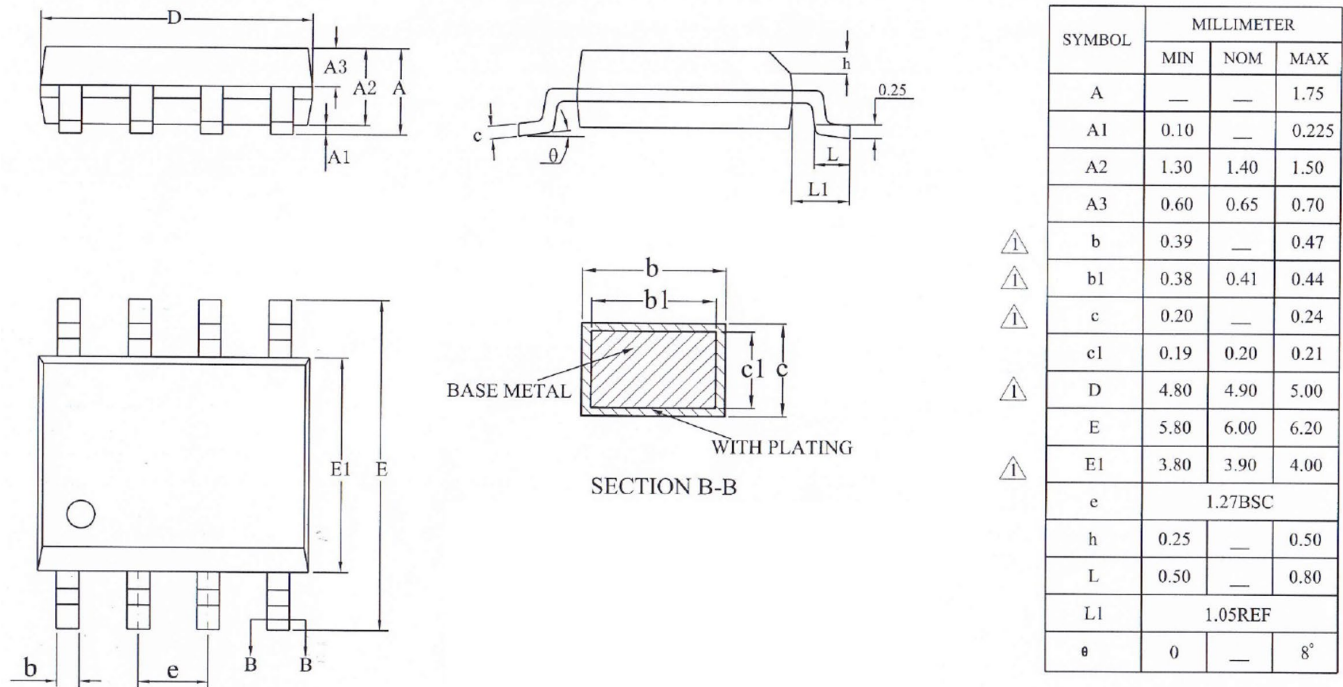


Figure 9. 1 SOP8 package shape and dimension in millimeters

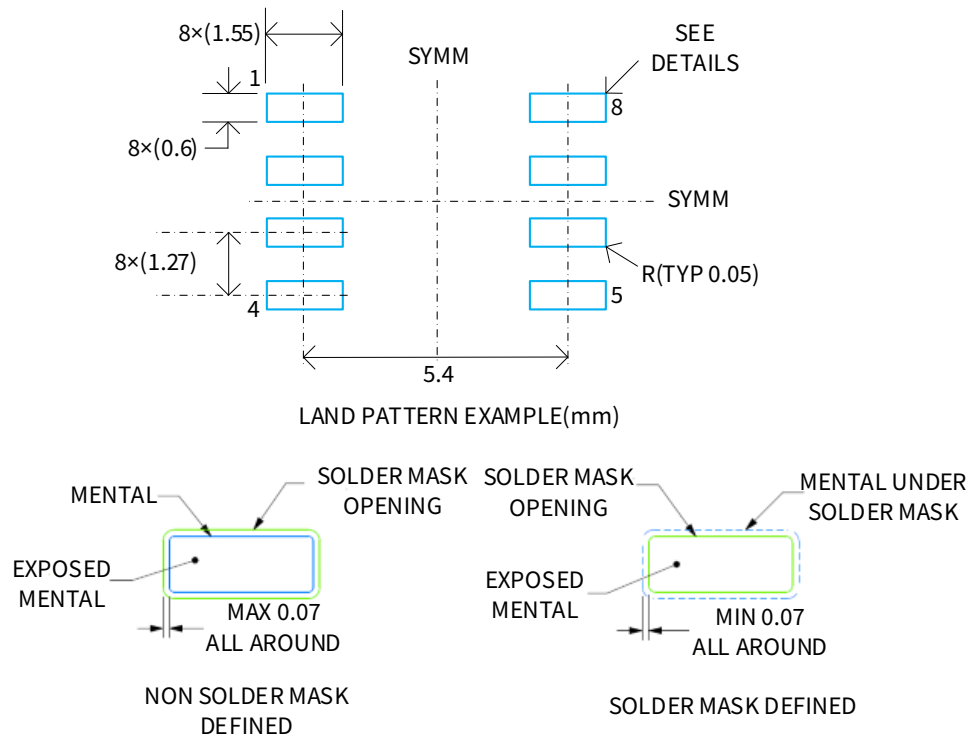
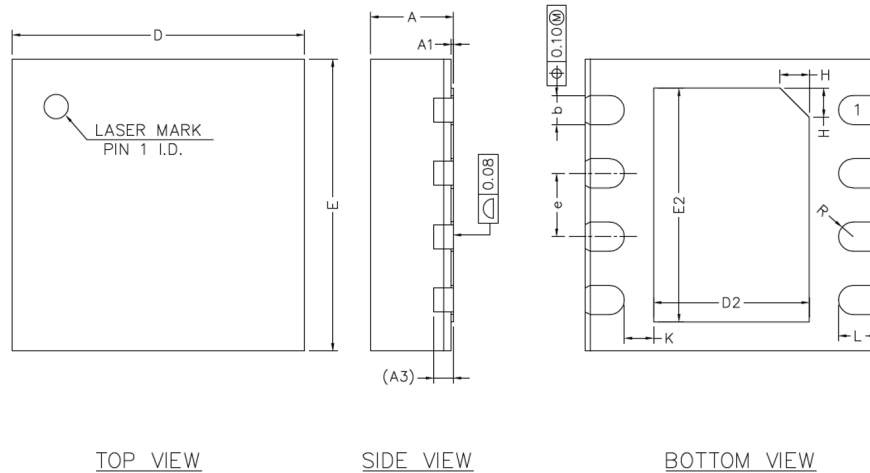
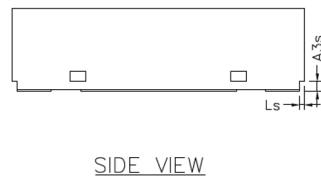


Figure 9. 2 SOP8 package board layout example



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203REF		
A3s	0.10	—	0.18
b	0.25	0.30	0.35
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.50	1.60	1.70
E2	2.30	2.40	2.50
e	0.60	0.65	0.70
K	0.30REF		
L	0.35	0.40	0.45
Ls	0.01	0.05	0.09
R	0.15REF		
H	0.30REF		



NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 9. 3 DFN8 package shape and dimension in millimeters

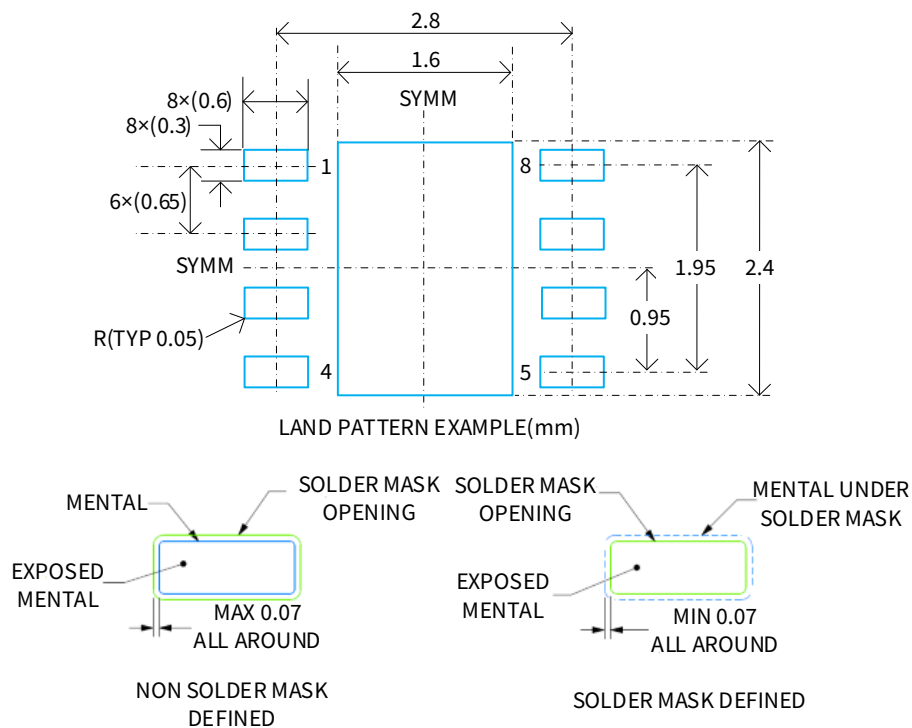
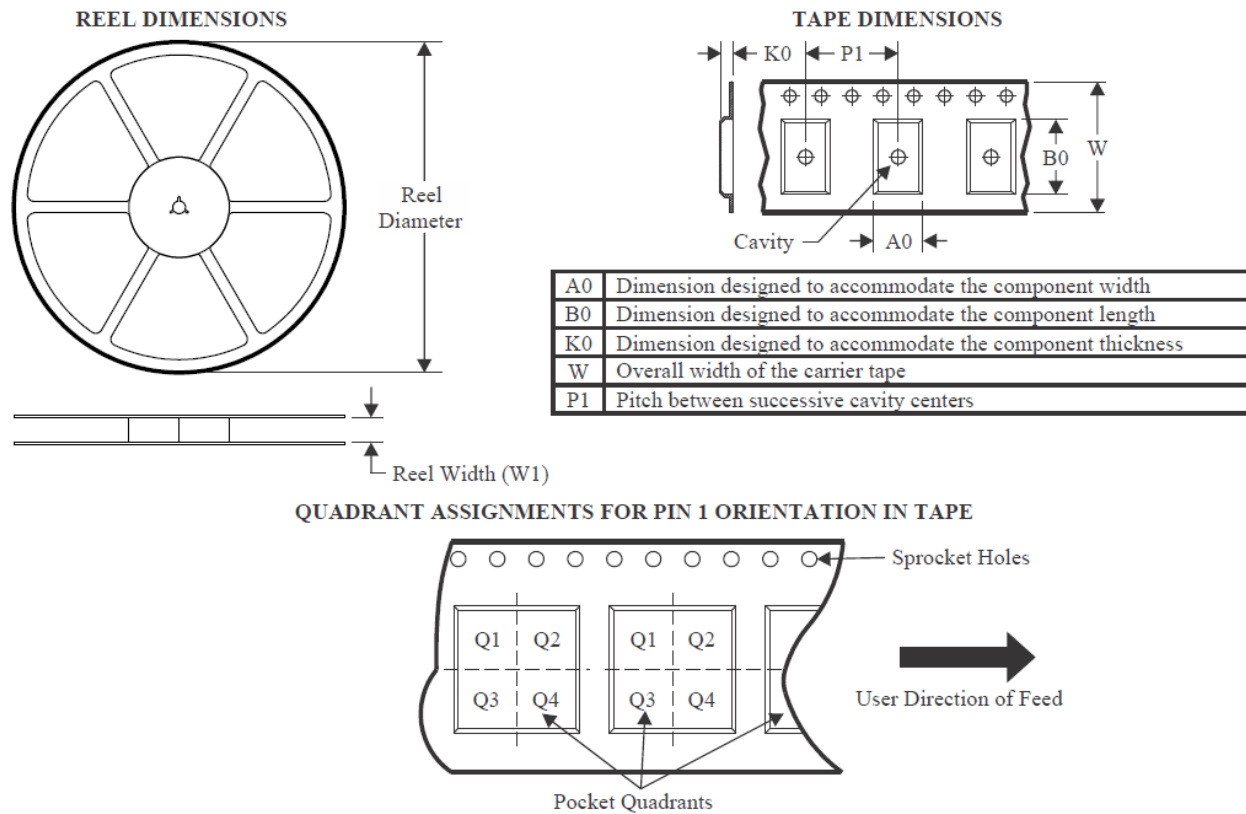


Figure 9. 4 DFN8 package board layout example

10. Order Information

<i>Part Number</i>	<i>Max Data Rate (kbps)</i>	<i>Operation Temperature</i>	<i>MSL</i>	<i>Package</i>	<i>Device Marking</i>	<i>SPQ</i>	<i>MPQ</i>
NCA1021A-Q1SPR	20	-40 °C to 125 °C	3	SOP8	NCA 1021AQ	2500	2500
NCA1021A-Q1DNR	20	-40 °C to 125 °C	2	DFN8	NCA10 21AQ	6000	6000

11. Tape and Reel Information



Devices	Package	Pins	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NCA1021A-Q1SPR	SOP8	8	330	16.4	6.55	5.3	2.0	8.0	12.0	Q1
NCA1021A-Q1DNR	DFN8	8	330	12.4	3.3	3.3	1.1	8.0	12.0	Q1

Figure 11. 1 Tape and Reel Information in millimeters

12. Revision History

Revision	Description	Date
1.0	Initial version	2026/06/30

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