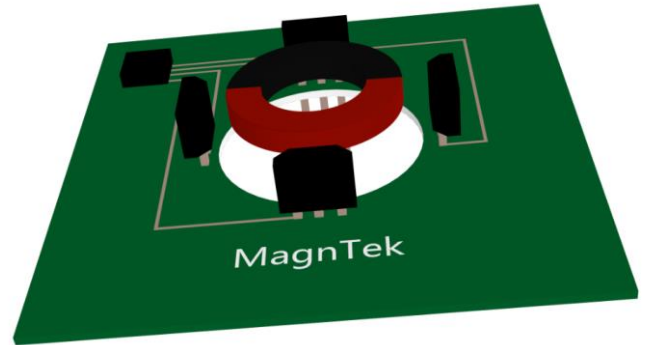
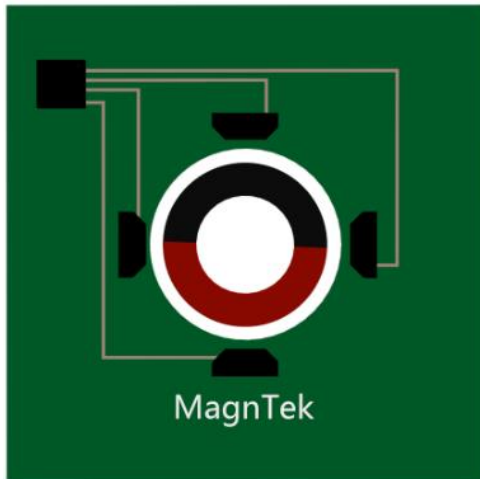


Side-shaft Absolute Interpolator (with External Linear Hall)

Features and Benefits

- Work with a diametrically magnetized permanent one-pair-pole ring magnet and 4 single-ended Halls(or 2 differential-out Halls), provide absolute angle from 0 to 360, side-shaft structure.
- 17-bit Absolute Resolution
- Independent Output Interface: ABZ, UVW, PWM and SPI
- Incremental ABZ Resolution 1~2,500 Pulses per period User Programmable, UVW Output Resolution 1~63 Pole-Pairs per period User Programmable
- Propagation Delay<2us
- 3.3~5.0V、Ambient Temperature -40~125℃
- 3.3~5.0V Programmable EEPROM



General Description

MT6709 is an interpolator work with a diametrically magnetized permanent one-pair-pole ring magnet and 4 single-ended Halls(or 2 differential-out Halls). The maximum ABZ resolution is 2,500 pulses or 10,000 steps per period. And the maximum UVW resolution is 63 pulses per period. The MT6709 provides a 3-Wire SPI interface for a host MCU to read back the 17-bits absolute angle information. PWM output offers 12-bits absolute angle information.

MT6709 offers a user Convenient-Auto-Calibration, which need the signal is sent several periods, to compensate the error in practical operating condition.

Applications

- Side-shaft absolute interpolator
- Sine/cosine interpolation
- Stepping motor angular encoders

Side-shaft Absolute Interpolator (with External Linear Hall)

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Side-shaft Absolute Interpolator (with External Linear Hall)

1. Pin Configuration

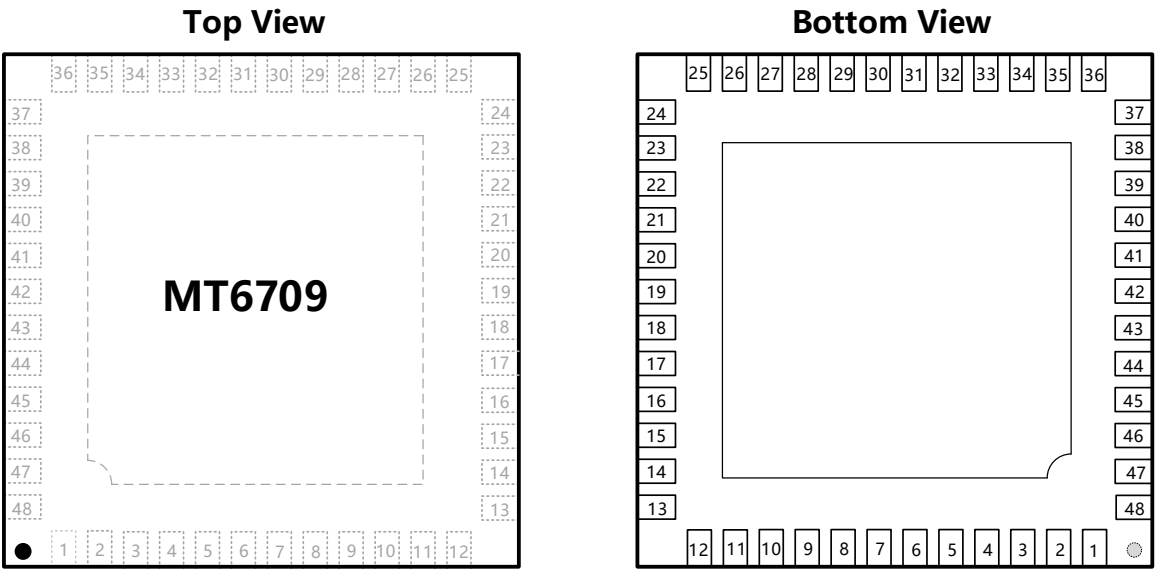


Figure 1: Pin Configuration of MT6709QC (QFN7*7) Package

Table 1: I/O Pin List

I/O Name	#	I/O Type	Description
-	1-2	-	NA
TEST	3	Digital Input	Factory Test Pin(MagnTek use only)
-	4	-	NA
CAL_ENB	5	Digital Input	Auto-Calibration Enable Pin (Low level is valid)
-	6~8	-	NA
SDAT	9	Digital Input/Output	SPI Bi-direction Data Line
-	10	-	NA
SCK	11	Digital Input	SPI Clock
-	12~13	-	NA
CSN	14	Digital Input	SPI Chip Select
VSS	15	Ground	Ground
Z	16	Digital Output	Incremental Signal Z
B	17	Digital Output	Incremental Signal B
A	18	Digital Output	Incremental Signal A
STATUS	19	Digital Output	STATUS Output
FAULT	20	Digital Output	Fault Output
VDD	21	Power Supply	3.3~5.0V Power Supply

Side-shaft Absolute Interpolator (With External Linear Hall)

I/O Name	#	I/O Type	Description
NA	22	-	NA
U	23	Digital Output	Commutation Signal U
V	24	Digital Output	Commutation Signal V
W	25	Digital Output	Commutation Signal W
PG_ZERO	26	Digital Input	Change the zero-position to current position and program EEPROM
-	27~35	-	NA
PWM	36	Digital Output	PWM Output
-	37	-	NA, Don' t connect to anything
-	38	-	NA
SIN_P	39	Analog Input	Differential sine signal input+
SIN_N	40	Analog Input	Differential sine signal input-
COS_P	41	Analog Input	Differential cosine signal input+
COS_N	42	Analog Input	Differential cosine signal input-
-	43~48	-	NA

Table 2: Family Members

Part Number	Description
MT6709QC-STD	QFN7x7-48L Package, Reel (2500 Pcs/Reel)

Side-shaft Absolute Interpolator (with External Linear Hall)

2. Functional Diagram

MagnTek' s MT6709 is a SIN/COS interpolator IC. Figure 2 shows a simplified block diagram of the chip, external devices(usually 4 single-ended Halls or 2 differential-out Halls) generate cosine and sine signals, gain stages, analog-to-digital converters (ADC) for signal conditioning, a digital signal processing (DSP) unit for angle calculation.

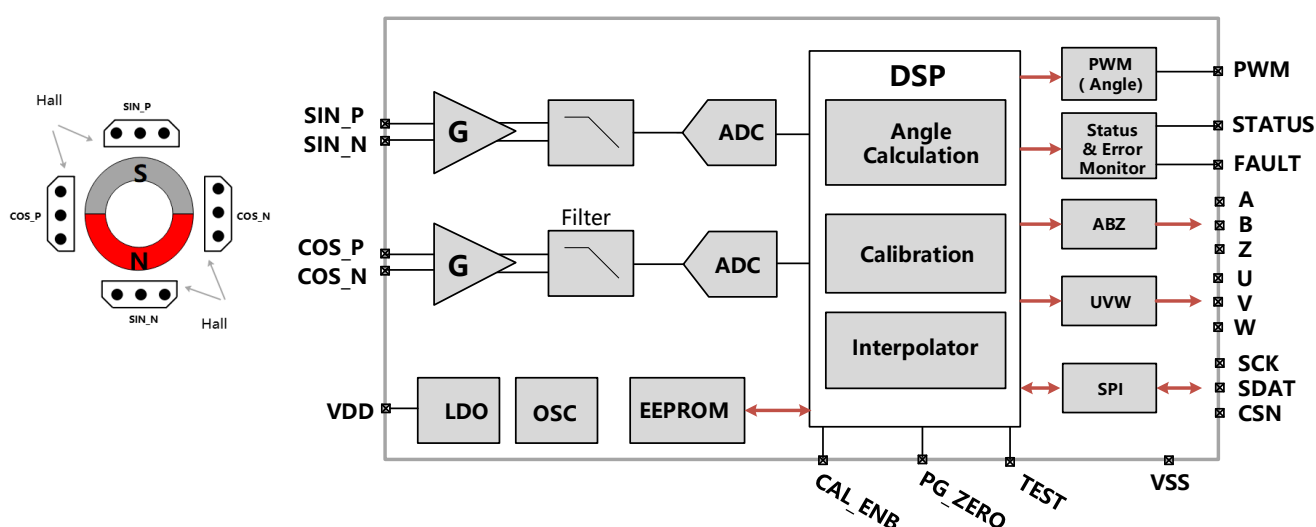


Figure 2: Block Diagram

Side-shaft Absolute Interpolator (With External Linear Hall)

3. Absolute Maximum Ratings (Non-Operating)

Table 3: Non-Operating Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
DC Voltage at Pin VDD	VDD	-0.3	6.5	V	Power Supply
Terminal Voltage at Input and Output Pins		-0.3	VDD	V	
Output Current at Output Pins	I _{OUT}	-25	25	mA	ABZ, UVW, PWM, STATUS, FAULT, SDAT
Ambient Temperature	T _{AMB}	-40	125	°C	-
Junction Temperature	T _J	-40	150	°C	-
Storage Temperature	T _{Storage}	-40	150	°C	-
V _{HBM} (ESD Voltage)	V _{HBM}	-	±4.0	kV	AEC-Q100-002
V _{CDM} (ESD Voltage)	V _{CDM}	-	±1.0	kV	AEC-Q100-011
I _{SCR} (Latch-up Input Current)	I _{Latch-up}		±100	mA	AEC-Q100-004

- 1) Consider current consumption and mounting situation for T_{AMB} and in relation to T_J
- 2) Please contact MagnTek for other temperature requirements

Operation beyond these limits may cause permanent damage to the device. Even if it does not lead to destruction, reliability and life may be adversely affected. Normal operation is not guaranteed at these extremes.

Side-shaft Absolute Interpolator (with External Linear Hall)

4. Electrical Characteristics

Operation conditions: Ta=-40 to 125°C, VDD=3.0~5.5V unless otherwise noted.

Table 4: Electrical Characteristics

Symbol	Description	Conditions/Notes	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	3.0	3.3~5.0	5.5	V
V _{TH_UV}	Undervoltage detection		2.45	2.55	2.65	V
V _{HYS_UV}	Undervoltage Hysteresis		-	100	-	mV
I _{dd}	Supply Current		13	19	25	mA
LSB	Resolution (ABZ Mode)		1	-	2,500	Pulse/Round
	PWM			12		Bit
	SPI			17		Bit
INL	Integral Non-Linearity with User Convenient-Auto-Calibration	Note[1]	-	±1		°
	Integral Non-Linearity with User Constant-Auto-Calibration	Note[2]		±0.5		°
DNL	Differential Non-Linearity (ABZ Mode), Figure 3	@2500 PPR	-	±0.02	-	°
TN	Transition Noise (ABZ Mode)	25°C with 'BW' =3	-	0.01	-	°rms
Hyst	Hysteresis	Programmable	0	0.022	0.7	°
T _{PwrUp}	Power-Up Time (Figure 8)	VDD Ramp<100us	22	32	42	ms
T _{Delay}	Propagation Delay	Constant Speed	-	2	-	us

Note[1]: The typical error value can be achieved at room temperature and without misalignment error.

Note[2]: value is achieved when the offset, amplitude and phase errors of the external input SIN/COS signals are within the calibratable range

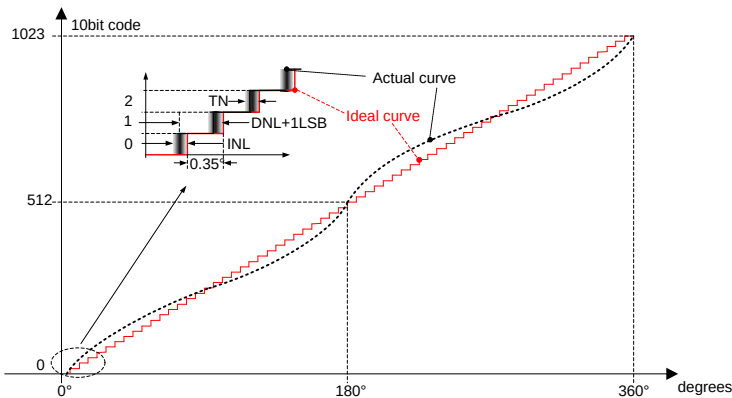


Figure 3 : Drawing Illustration INL, DNL and TN (for 10-bit case)

Side-shaft Absolute Interpolator (With External Linear Hall)

● **Input Signal (SIN_P, SIN_N, COS_P, COS_N)**

Operation conditions: Ta=-40 to 125°C, VDD=3.0~5.5V unless otherwise noted.

Table 5: Analog Input Parameter

Symbol	Description	Min.	Typ.	Max.	Unit
Vin_s	Voltage Range of SIN_P/N, COS_P/N	1.0	-	VDD-0.3	V
Vin_d	Inside Voltage Range of Differential Signal	-	-	1.6	V _{pp}
Vin_s_p	Peak-to peak Voltage of SIN_P/N, COS_P/N	-	-	800	mV
F _{in}	Frequency of input	-	-	32	KHz
Vos	Offset Voltage of Input	-20	-	20	mV
I _{in}	Input Leak Current	-2	-	2	uA
OS_ERR	Calibration Range of Offset Voltage Error	-500	-	500	mV
AM_ERR	Calibration Range of Gain-Mismatch Error	-0.5	-	0.5	
PHASE_ERR	Calibration Range of Phase-Error	-50	-	50	°

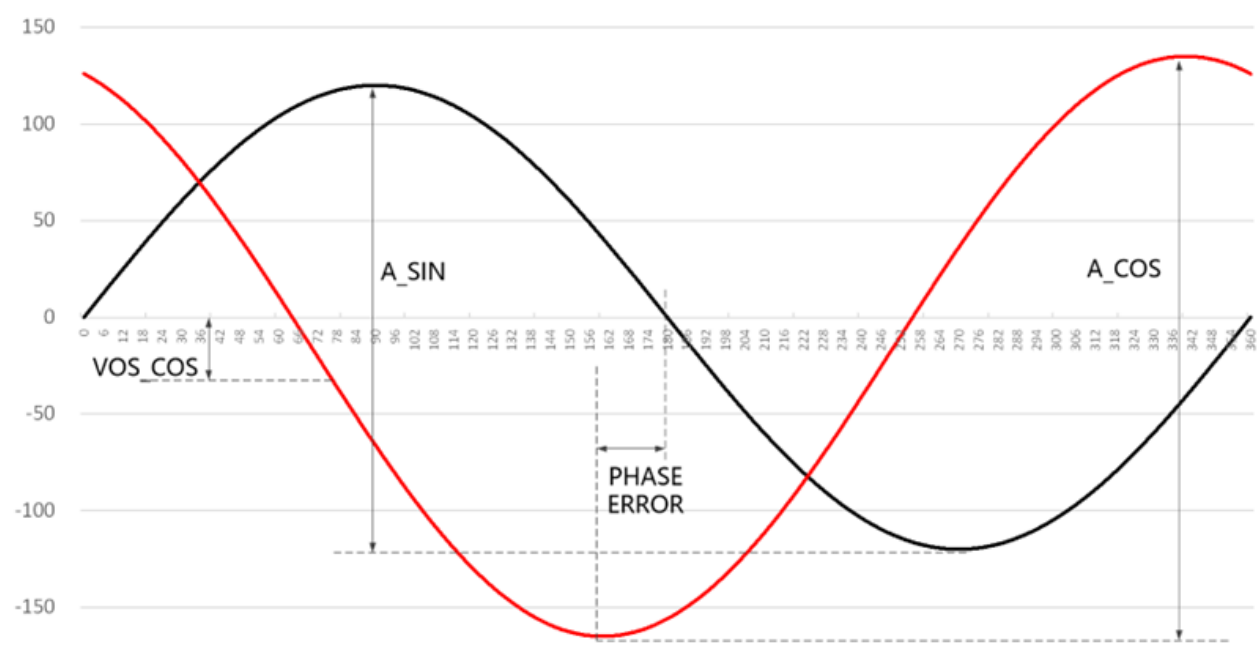


Figure 4: Offset, Gain-Mismatch and Phase

Side-shaft Absolute Interpolator (With External Linear Hall)

ABZ Output Characteristics

Operation conditions: Ta=-40 to 125°C, VDD=3.0~5.5V unless otherwise noted.

Table 6: ABZ Output Parameter

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
AB _{RES}	AB Resolution	Programmable	1	-	2,500	Pulse/period
AB _{Freq}	A or B Frequency	Note(3)	-	-	2	MHz

Note(3): The AB_{Freq} is the product of F_{in}(Speed of single antipolar magnetic ring) and AB_{RES}. So, for maximum AB resolution of 2,500 pulses per period, the maximum frequency of input Fin_{MAX} is:

$$Fin_{MAX} = \frac{AB_{Freq}}{AB_{RES}} = \frac{2MHz}{2,500} = 800Hz = 48,000RPM$$

Even >2MHz AB_{Freq} is available, but the INL could not be guaranteed when AB_{Freq} is >2MHz

PWM Output Characteristics

Operation conditions: Ta=-40 to 125°C, VDD=3.0~5.5V unless otherwise noted.

Table 7: PWM Output Characteristics

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
F _{PWM}	PWM Frequency	Programmable	-5%	125 ~ 2,000	+5%	Hz
T _{Rise}	Rising Time	C _L =1nF	-	-	1	us
T _{Fall}	Falling Time	C _L =1nF	-	-	1	us

Side-shaft Absolute Interpolator (With External Linear Hall)

Digital I/O Characteristics

Operation conditions: Ta=-40 to 125°C, VDD=3.0~5.5V unless otherwise noted.

Table 8: Digital I/O Characteristics

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
V _{IH}	Digital I/O Input Voltage High Level Voltage (CSN, SDAT, SCK, PG_ZERO, CAL_ENB)	-	0.8*VDD	-	-	V
V _{IL}	Digital I/O Input Voltage Low Level Voltage (CSN, SDAT, SCK, PG_ZERO, CAL_ENB)	-	-	-	0.2*VDD	V
V _{OH}	Digital I/O Output High Level Voltage (ABZ, UVW, SDAT, FAULT, STATUS, PWM)	Push-Pull (@Iout=-2mA)	VDD-0.4	-	-	V
V _{OL}	Digital I/O Output Low Level Voltage (ABZ, UVW, SDAT, FAULT, STATUS, PWM)	Push-Pull (@Iout=2mA)	-	-	0.4	V
T _{Rise}	Rising Time	C _L =20pf	-	-	50	ns
T _{Fall}	Falling Time	C _L =20pf	-	-	50	ns

EEPROM Characteristics

Operation conditions: Ta=-40 to 125°C, VDD=3.0~5.5V unless otherwise noted.

Table 9: EEPROM Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Supply Voltage @Erase/Program EEPROM	3.0	-	5.5	V
Endurance	Erase/Program Cycles	100	-	-	Cycles
Data Retention	Data Retention @150°C	10	-	--	Years

Side-shaft Absolute Interpolator (with External Linear Hall)

5. Reference Circuit

The MT6709 is powered by a single supply VDD (3.3~5.0V), so a decoupling capacitor no less than 0.1uf between VDD and GND is necessary. For better EMC performance, we highly recommend adding a TVS between VDD and GND. The MT6709 provides ABZ, UVW and PWM signals at output pins, and the 17-bit absolute angle position data could be transferred by the standard 3-Wire SPI interface. The default reference circuit is shown in Figure. 5.

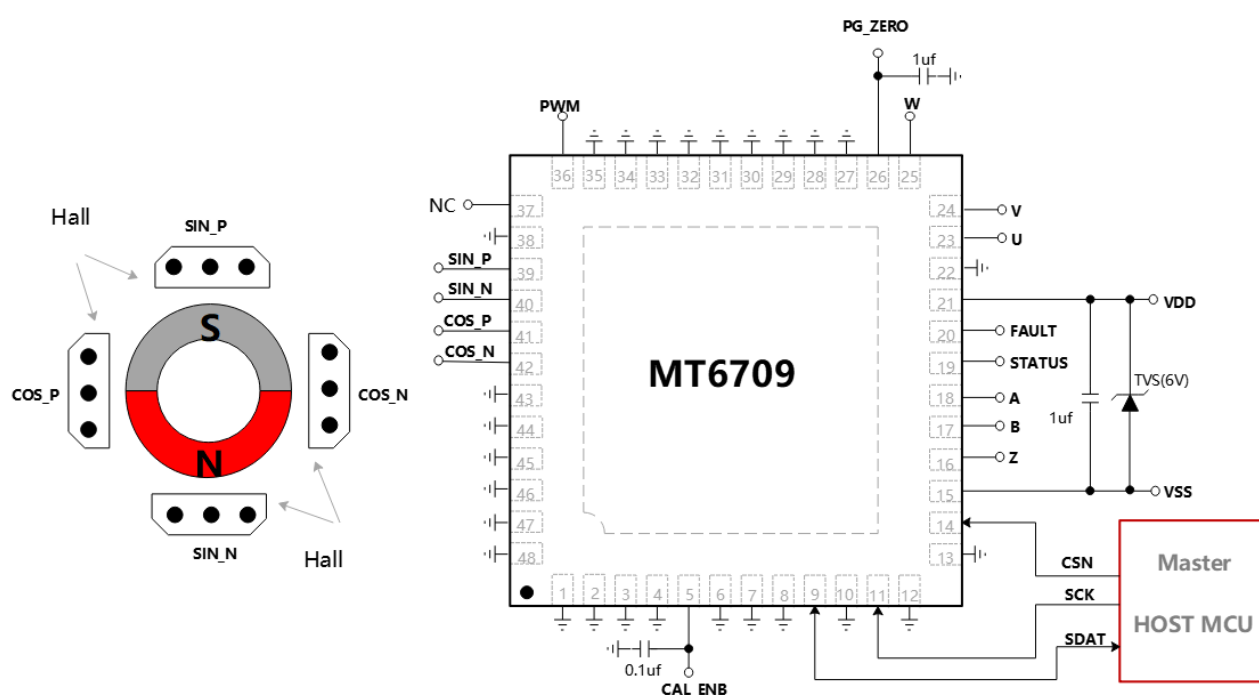


Figure 5: MT6709 Reference Circuit

Side-shaft Absolute Interpolator (With External Linear Hall)

6. External SIN/COS Input

The MT6709 is an interpolator for sine/cosine signal as shown in Figure 6&7. The voltage of input signals (SIN_P, SIN_N, COS_P, COS_N) must be in the range of 1.0V to VDD-0.3V. The peak-to-peak voltage of input signals must be less than 800mV. The calibration function can compensate offset, gain-mismatch and phase-error to improve INL, however, reduce the original error as much as possible is very useful as well.

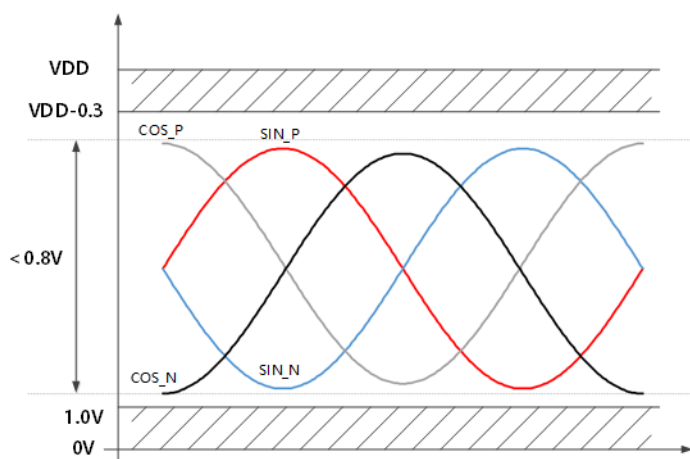


Figure 6: External SIN/COS Input

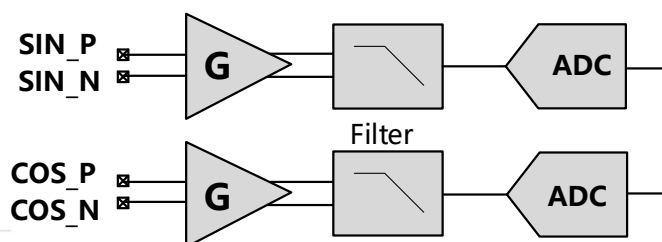


Figure 7: signal chain

PIN_STATUS output represents the signal strength of input and users can change PGA_GAIN REGISTER to set gain. Make sure PIN_STATUS PWM duty is less than 33% in all operation conditions.

Side-shaft Absolute Interpolator (With External Linear Hall)

7. Output Mode

The MT6709 provides ABZ, UVW and PWM signals at output pins, and the 17-bit absolute angle position data could be transferred by the standard 3-Wire SPI interface.

7.1 Quadrature A,B and Zero-Position Output (ABZ Mode)

As shown in Figure 8, when the input signal is CCW ,the rising edge of output B leads output A by 1/4 cycle. When the input signal is CW, the rising edge of output A leads output B by 1/4 cycle.

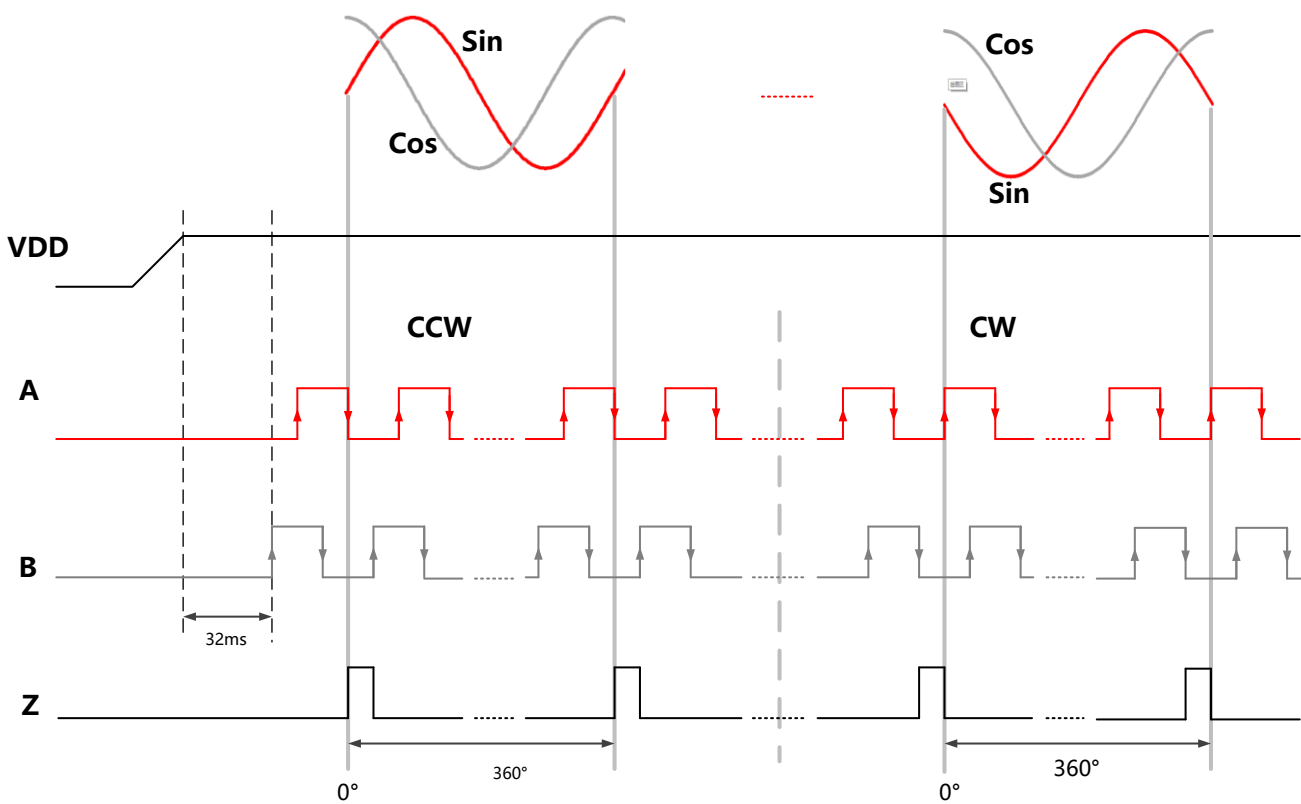


Figure 8: ABZ output with VDD power on

Table 10: ROT_DIR' (CCW or CW) Register (EEPROM)

Register	data	Rotation Direction
ROT_DIR	0	Counter-Clock-wise, Output B leads Output A
	1	Clock-wise, Output A leads Output B

' ROT_DIR' is effective for all output types as ABZ, UVW, PWM and SPI Angle data

Side-shaft Absolute Interpolator (With External Linear Hall)

ABZ resolution is user programmable from 1~2,500 pulses per period. The relationship between binary bits, LSBs and pulses per magnetic period resolution of ABZ output are shown in Figure 9 & Figure 10.

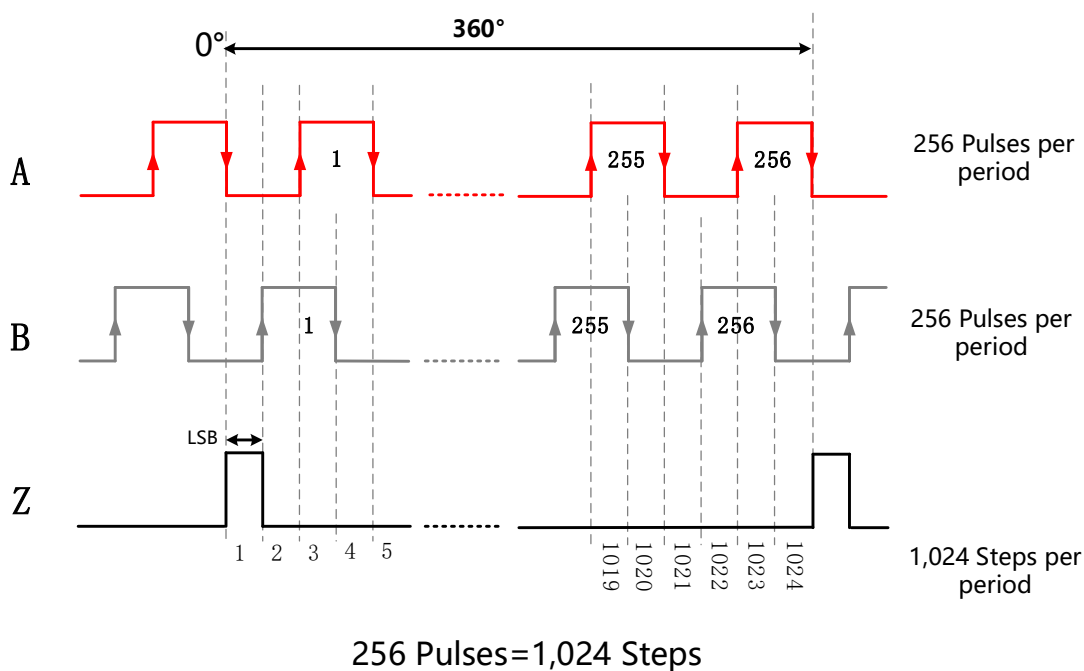


Figure 9: ABZ Output Resolution = 10 bit = 256 pulses per period

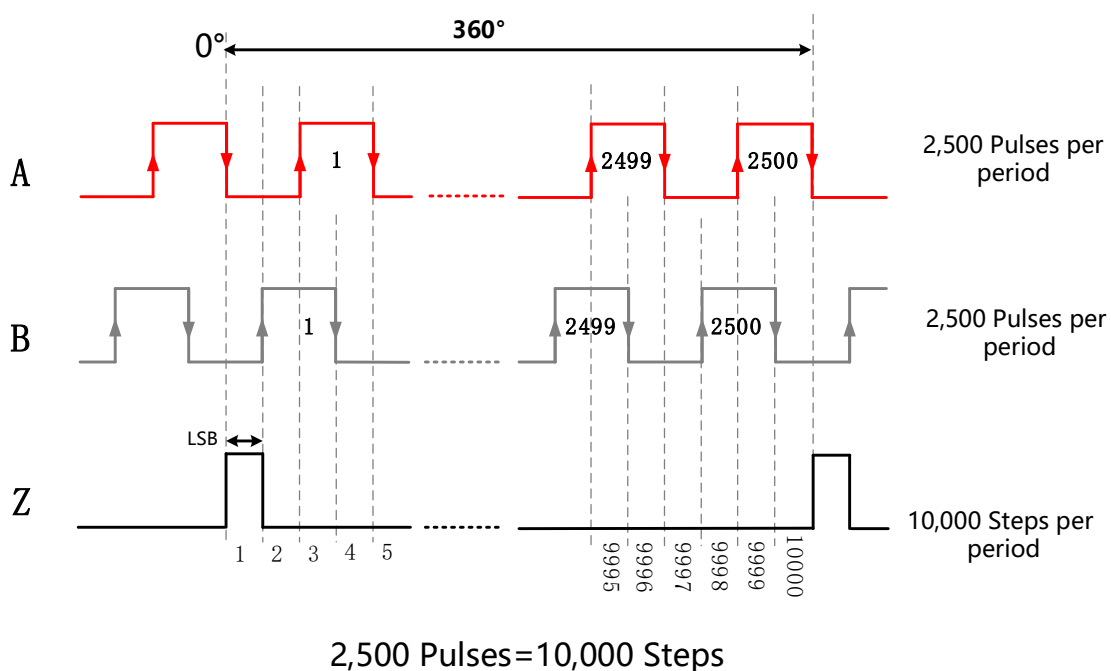


Figure 10: ABZ Output Resolution = 2,500 pulses per period = 10,000 Steps / period

Side-shaft Absolute Interpolator (With External Linear Hall)

The resolution of ABZ is defined by a 12-bit register 'ABZ_RES[11:0]' ;

Table 11: ' ABZ_RES[11:0]' Register (EEPROM)

Register	data	AB Resolution (pulses per period)
ABZ_RES[11:0]	0x000	1
	0x001	2
	0x002	3
	⋮	⋮
	0x9C3	2,500
	0x9C4~0xFFF	2,500

Output Z indicates the zero position of the magnet which is user programmable, and the pulse width of Z is selectable as 1、2、4、8、16、32、64、128LSBs or 60°、120°、180°as shown in Figure 11 and Figure 12.

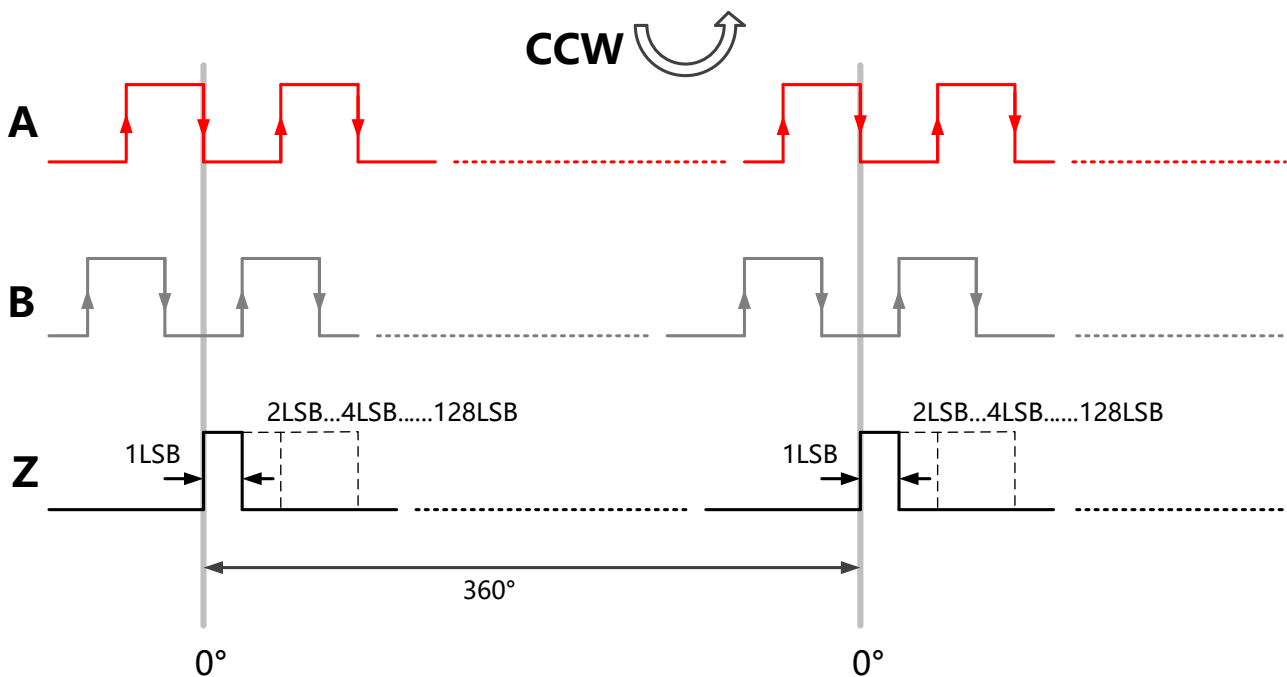


Figure 11: Typical ABZ Output with Z pulse width =1,2,4,8 ,16, 32, 64, 128 LSBs

Side-shaft Absolute Interpolator (With External Linear Hall)

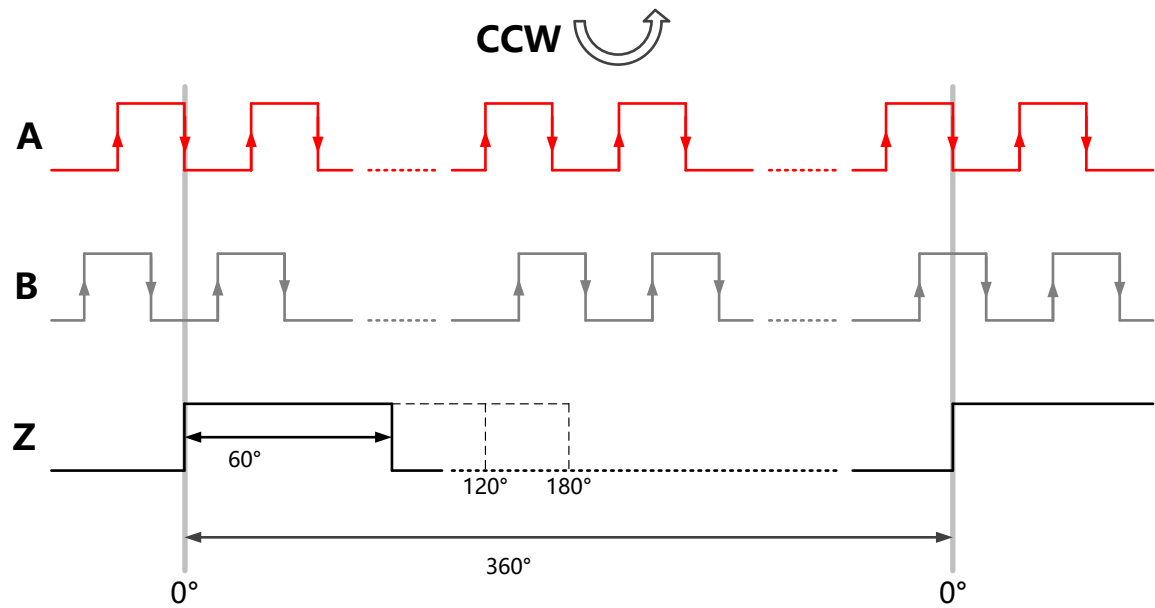


Figure 12: Typical ABZ Output with Z pulse width=60°, 120° and 180°

The width of Z pulse is defined by the 4-bit register 'Z_PUL_WID[3:0]' ;

Table 12: 'Z_PUL_WID[3:0]' Register (EEPROM)

Register	data	Width (LSBs/°)	data	Width (LSBs/°)
Z_PUL_WID[3:0]	0x0	1	0x8	32
	0x1	2	0x9	64
	0x2	4	0xA	128
	0x3	8	0xB	1
	0x4	16	0xC	1
	0x5	60°	0xD	1
	0x6	120°	0xE	1
	0x7	180°	0xF	1

The absolute position of Z pulse is defined by the 12-bit register 'ZERO_POS[11:0]' ;

Table 13: 'ZERO_POS[11:0]' Register (EEPROM)

Register	data	Absolute Position (°)
ZERO_POS[11:0]	0x000	0
	0x001	0.088
	0x002	0.176
	...	...
	0xFFE	359.824
	0xFFF	359.912

Side-shaft Absolute Interpolator (With External Linear Hall)

Also, Z pulse phase could be user programmable by 'Z_PHASE[1:0]' register as shown in Figure 13.

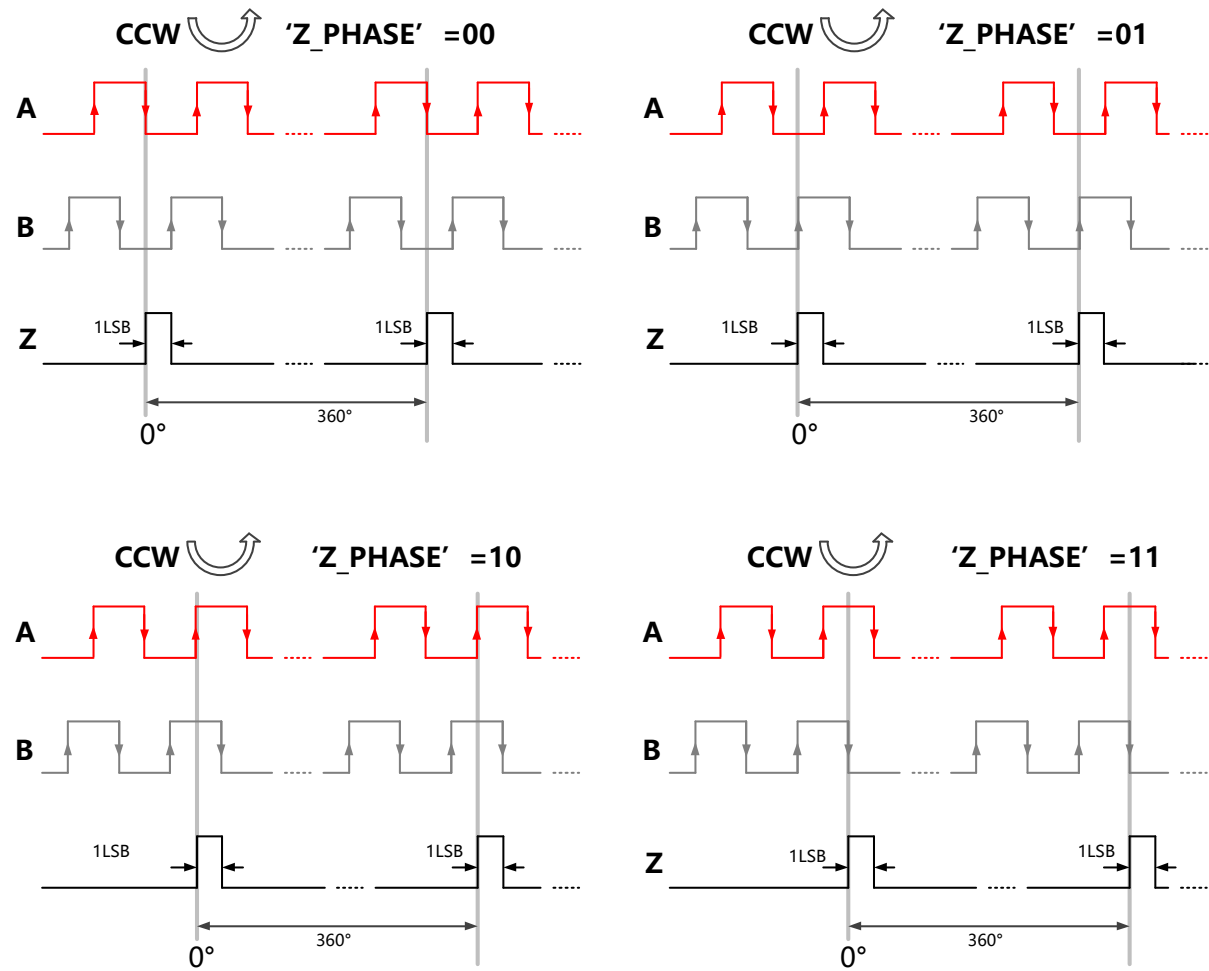


Figure 13: Z Pulse Phase with 'ROT_DIR' = 0, 'SWAP_AB' = 0, 'Z_EDGE' = 0

The relationship of 0° and Z pulse edge is defined by register 'Z_EDGE' .

Table 14: 'Z_EDGE' Register (EEPROM)

Reg. Z_EDGE	Description
0x0	Z Pulse Rising Edge Aligned with Zero-Degree
0x1	Z Pulse Falling Edge Aligned with Zero-Degree

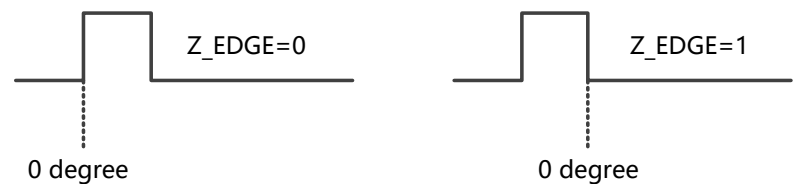


Figure 14: Z Pulse Edge with 0 degree

Side-shaft Absolute Interpolator (With External Linear Hall)

7.2 UVW Output Mode

The MT6709 provides U, V and W pulses which are 120° (electrical angle) out of phase as shown in Figure 15. The cycles of UVW per magnetic period can be programmed as shown in Table 15.

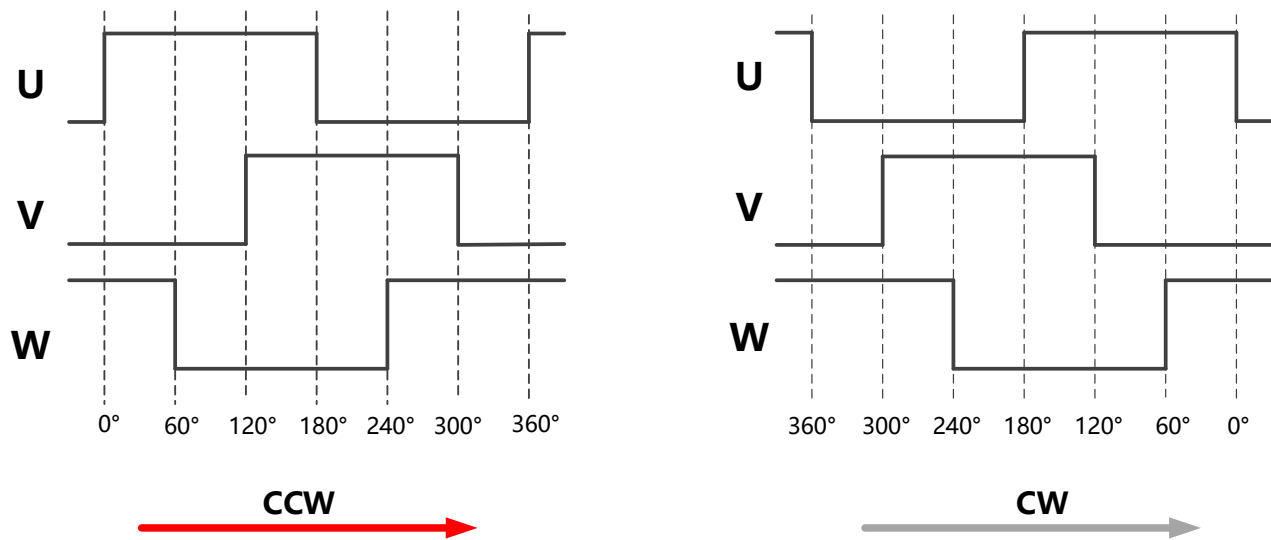


Figure 15: Typical Output Waveform for UVW Mode

Table 15: UVW_RES' Register (EEPROM)

Register	data	UVW Pole Pairs
UVW_RES[5:0]	0x0	1
	0x1	2
	0x2	3
	0x3	4
	0x4	5
	0x5	6
	0x6	7
	0x7	8
	...	...
	0x3B	60
	0x3C	61
	0x3D	62
	0x3E	63
	0x3F	NA

Side-shaft Absolute Interpolator (With External Linear Hall)

7.3 Pulse Width Modulation (PWM) Output Mode

The MT6709 provides a digital Pulse Width Modulation (PWM) output, whose duty cycle is proportional to the measured angle as shown in Figure 16. The PWM output of MT6709 is push-pull type. The PWM signal has the resolution of 12 bits and with programmable frequency and polarity as shown in Figure-16 and Table-16.

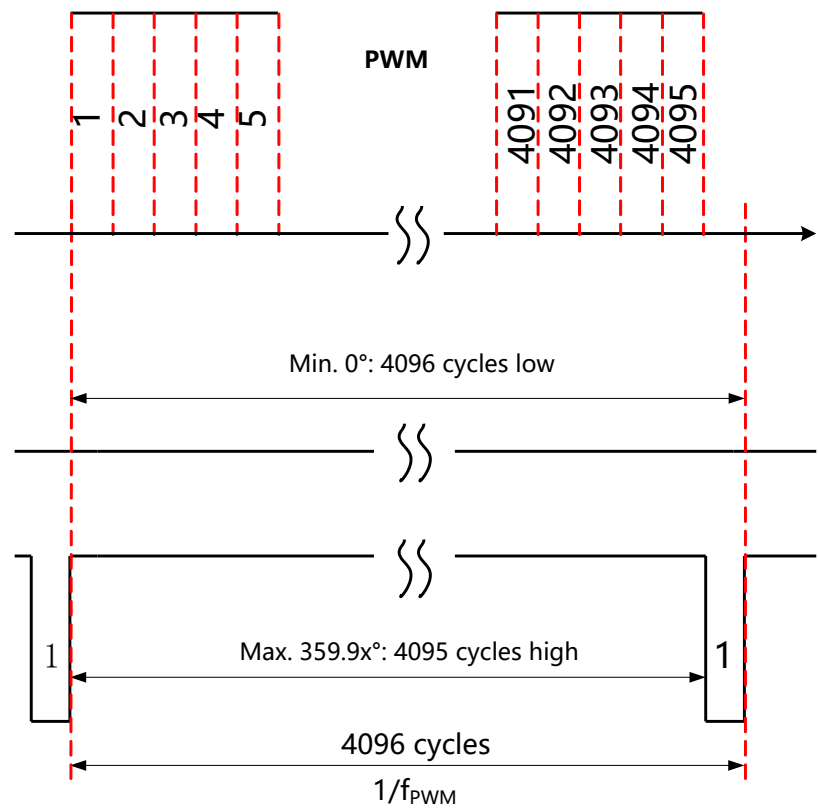


Figure 16: PWM Output Frame

Table 16: PWM_POL' Register (EEPROM)

Register	data	Description
PWM_POL	0	High Level Valid
	1	Low Level Valid

The PWM frequency can be programmed to arbitrary value from 125Hz to 2KHz by setting the 16-bit register 'PWM_N[15:0]' as follows.

$$FPWM = 8,192,000 / PWM_N[15:0] \text{ (Hz)}$$

Where PWM_N is an integer number ranging from 4,096 to 65,535(values below 4,096 is clamped).

Side-shaft Absolute Interpolator (With External Linear Hall)

7.4 SPI Interface(3 wires)

The MT6709 provides a 3-Wire SPI interface for a host MCU to read back the absolute angle information and diagnostic status from its internal registers.

7.4.1 SPI Timing Diagram

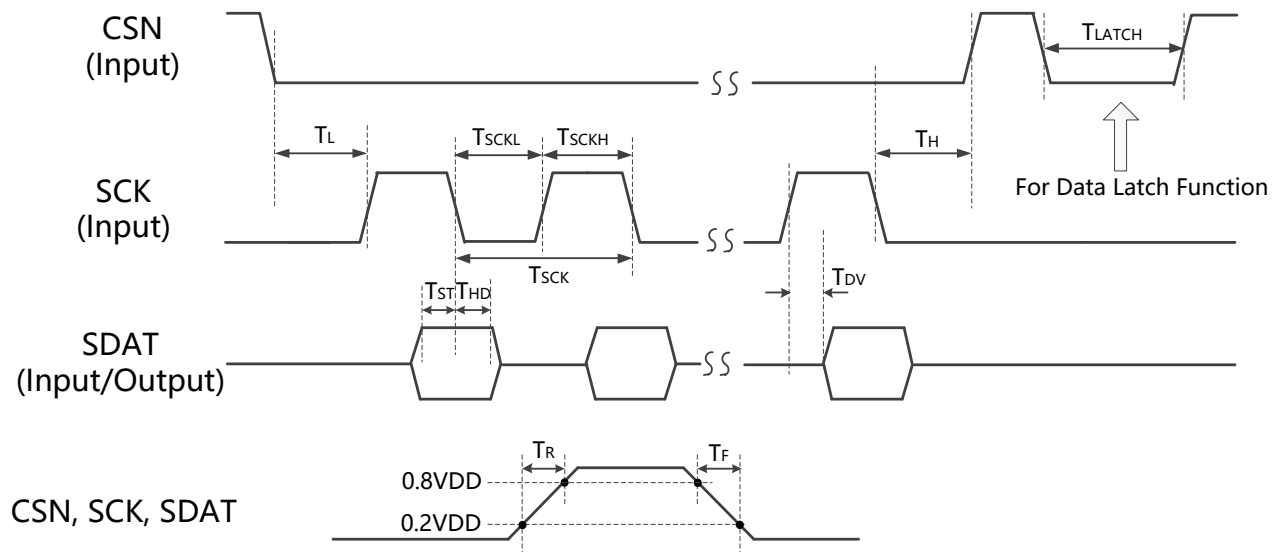


Figure 17: 3-Wire SPI Timing Diagram

Table 17: SPI Timing Specification

Symbol	Description	Min.	Typ.	Max.	Unit
T_L	Time Between CSN Falling Edge and SCK Riseing Edge	100		-	ns
T_{SCK}	Clock Period	125		-	ns
T_{SCKL}	Low Period of Clock	50		-	ns
T_{SCKH}	High Period of Clock	50		-	ns
T_H	Time Between SCK Last Falling Edge and CSN Rising Edge	$0.5 \cdot T_{SCK}$		-	ns
T_R	Rise Time of Digital Signal (with 20pf Loading Condition)	-	10	-	ns
T_F	Fall Time of Digital Signal (with 20pf Loading Condition)	-	10	-	ns
T_{DV}	Data Valid Time of SDAT (with 20pf Loading Condition)	-	-	15	ns
T_{ST}	Setup Time of SDAT Data	10	-	-	ns
T_{HD}	Hold Time of SDAT Data	10	-	-	ns
T_{LATCH}	Effective CSN Low Period Time for Latch Angle Function	1	-	-	us
T_W	SDAT Input Output Transition Time	-	$2 \cdot T_{SCK}$	-	ns

Side-shaft Absolute Interpolator (With External Linear Hall)

7.4.2 SPI Protocol

The Reading-Mode and Writing-Mode of the 3-Wire SPI protocol is shown in Figure-18 and Figure-19. An SPI data transfer starts with the falling edge of CSN and stops at the rising edge of CSN; SCK is the serial port clock, and it is always driven by the SPI master, it is low when there is no SPI transmission. And SDAT is the serial port data input and output, it is driven at the rising edge of SCK and should be captured at the falling edge of SCK. The I/O pin 'SDAT' of MT6709 keeps Hi-Z (as input) unless it drives data out.

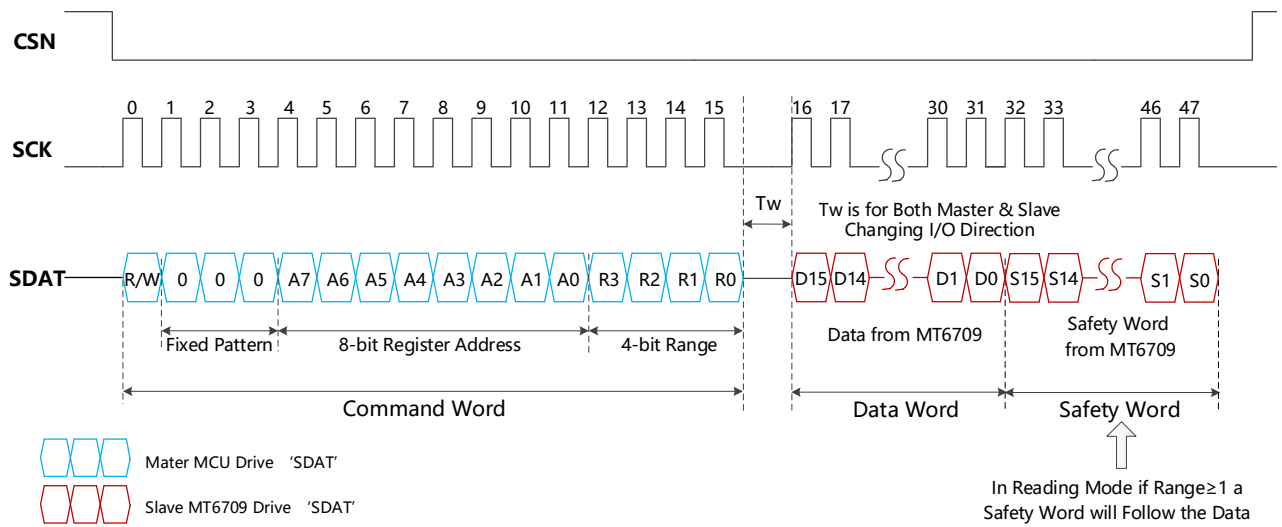


Figure 18: 3-Wire SPI Reading Mode

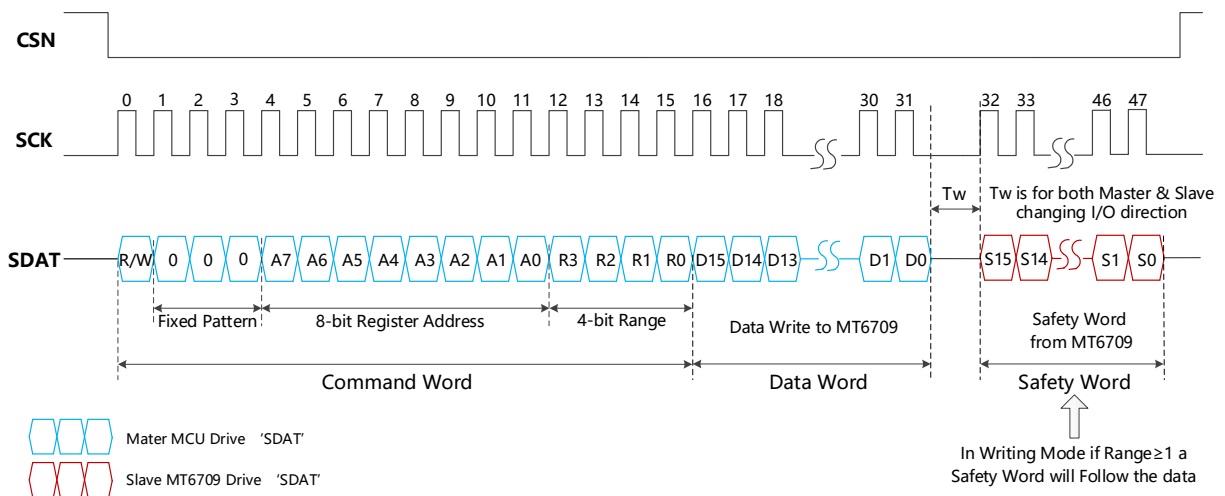


Figure 19: 3-Wire SPI Writing Mode

Side-shaft Absolute Interpolator (With External Linear Hall)

Table 18: The SPI Command Word Structure

Bit	Name	Description
Bit[15]	R/W	Command Read ('1') or Write ('0')
Bit[14:12]	Fixed '000'	
Bit [11:4]	Register Address	Register Address for Read or Write
Bit[3:0]	Read/Write Range N	N=0: Read/Write 1 Word (16 bits) without Safety-Word N=1: Read/Write 1 Word (16 bits) with Safety-Word N=2~15: Read/Write N Words with Safety-Word

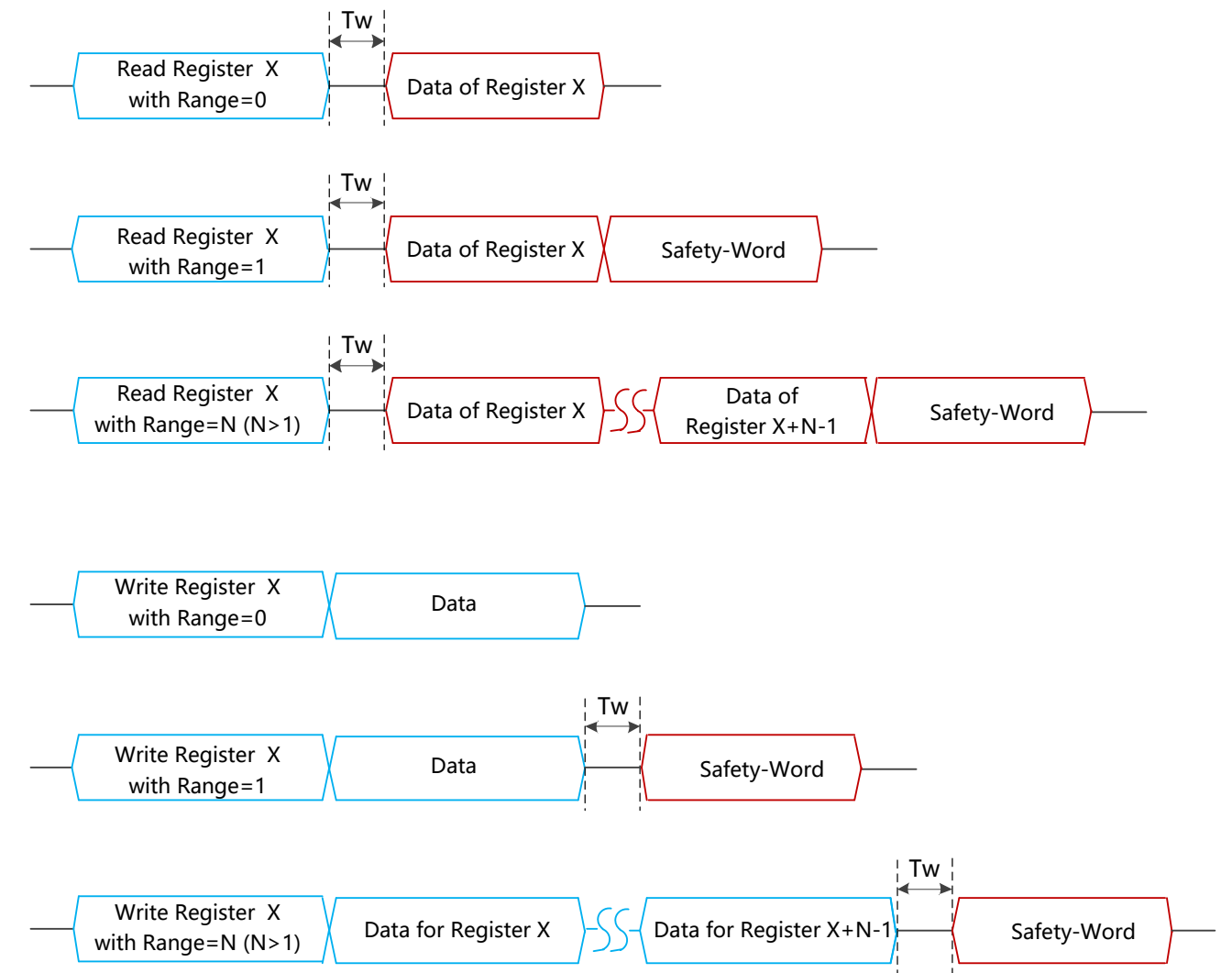


Figure 20: SPI Read/Write with different Range

Side-shaft Absolute Interpolator (With External Linear Hall)

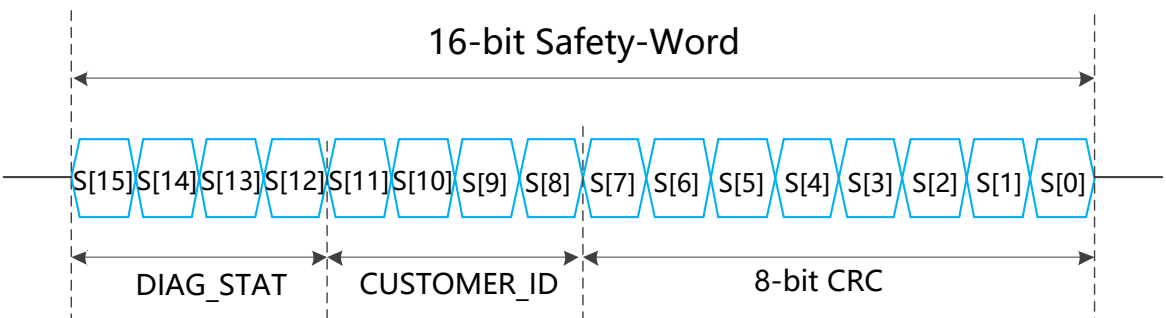


Figure 21: Safety-Word Structure

Table 19 : Safety-Word Structure

Name	Bit	Description
DIAG_STAT Note [4]	S[15]	Magnetic Field too Weak/Magnetic Field too Strong
	S[14]	Loss of Tracking (Angle Velocity Over Speed) /Calibration failed
	S[13]	EEPROM Data Loading CRC Failure
	S[12]	Under-Voltage Detection
CUSTOMER_ID	S[11:8]	4-bit ID for the chip which can be programmed by Register 'CUSTOMER_ID'
CRC	S[7:0]	CRC Redundancy Check

Note[4]: DIAG_STAT bit is set to 0 in normal operation and 1 in case of diagnostic failure

CRC

- CRC data range:
- (1) Default with register 'SPI_CRC_SEL' =0, including command word and data words;
- (2) With register 'SPI_CRC_SEL' =1, including command word, data words and S[15:8];
- CRC polynomial: $X^8+X^4+X^3+X^2+1$, the 'R/W' bit of command word shifts in first;
- CRC seed value: '11111111B' ;
- The remainder is inverted before transmission;

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7.4.3 SPI Read Angle

Customer can read the angle register inside MT6709 through the 3-wire SPI interface as shown in Figure 22. A separate CSN low level can latch the value of the angle register, as shown in Figure-23.

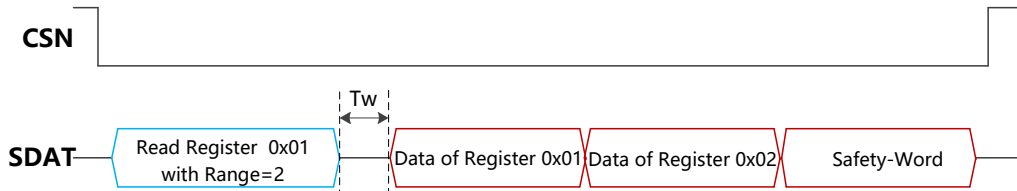


Figure 22: SPI Reading Current Angle Data

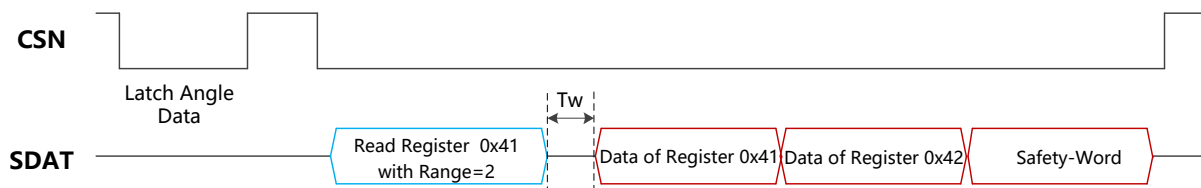


Figure 23: SPI Reading Latched Angle Data

Table 20: Angle Data Related Register

Address	Bit15	Bit14~0
0x01	ANGLE[16:1] (data of angle)	
0x02	ANGLE [0] (data of angle)	
0x41	ANGLE_Latched[16:1] (latched data of angle)	
0x42	ANGLE_Latched[0]	

0~360° absolute angle θ could be calculated by the below formula with ANGLE[16:0]:

$$\theta = \frac{\sum_{i=0}^{16} \text{ANGLE}[i] \cdot 2^i}{2^{17}} \cdot 360^\circ$$

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7.5 STATUS and FAULT Output

STATUS OUTPUT

The output of STATUS is a PWM signal and the duty ratio represents the magnetic field intensity. The frequency is 2KHz and the polarity is high level valid by default. The frequency and polarity can be programmed as describe in chapter 7.3. It is suitable if the duty ratio between 10% and 33%. Less than 10% means the magnetic field intensity is too weak and greater than 33% means the magnetic field intensity is too strong.

In addition, when the chip work in the Convenient-Auto-Calibration mode, the output of STATUS represents the status of calibration(success, fail or in the process), please refer to chapter 8.

FAULT OUTPUT

The FAULT output is the fault information of the chip. The failure mode is shown in Table 21. The default output of FAULT is logic low, and any of the failure mode in Table 21 will turn the FAULT to logic high.

Table 21: Failure Mode of FAULT

Failure Mode	Description
Magnetic Field too Weak	The Duty-Cycle of STATUS is less than 10%
Magnetic Field too Strong	The Duty-Cycle of STATUS is greater than 44%
Loss of Tracking	The frequency of SIN/COS>25KHz
EEPROM Data Loading CRC Failure	EEPROM Data Loading CRC Failure when power on
Auto-Calibration Failure	Result of Auto-Calibration can not converge
Under-Voltage Detection	The power supply voltage is too low

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8. Calibration

8.1 User Convenient-Auto-Calibration

MT6709 offers a user Convenient-Auto-Calibration, which need magnet ring rotate a few periods, to compensate the error in practical operating condition, as shown in Figure 24.

Please follow these steps:

- (1) Install the PCB and magnet ring.
- (2) rotate with the speed from 40rpm to 3000rpm.
- (3) Pull down CAL_ENB to GND (or write 0x01 to register_ 'SOFT_AUTOCAL') to enable the calibration function at least 16 periods. Monitor the status of calibration from PIN_STATUS (shown in Table 22) , or register_ 'CAL_STATE' (shown in Table 23). If the calibration succeed, the data will be programmed into the EEPROM. Please wait for 500ms and then pull up CAL_ENB to VDD (or write 0x00 to register_ 'SOFT_AUTOCAL') .
- (4) If the calibration failed, please power on again before next calibration.

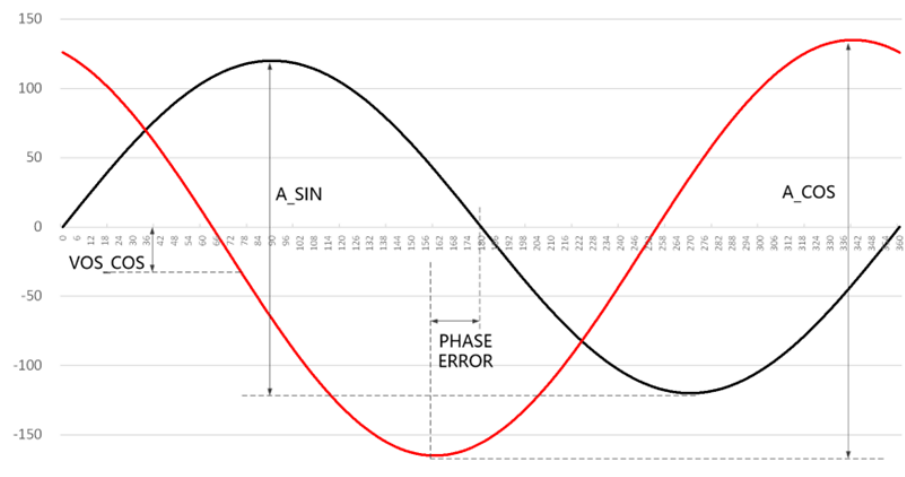


Figure 24: Offset, Gain-Mismatch and Phase-Error

Table 22: Description of STATUS Output in User Convenient-Auto-Calibration

STATUS Duty-Cycle	Status
50%	In Calibration Process
25%	Calibration Failed
>99%	Calibration Succeed

Table 23: 'CAL_STATE'

Register: CAL_STATE [1:0]	Status
0x0	Not in Calibration Mode
0x1	In Calibration Process
0x2	Calibration Failed
0x3	Calibration Succeed

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8.2 User Constant-Auto-Calibration

MT6709 offers a user Constant-Auto-Calibration, which need magnet ring rotate with a constant speed, to compensate the error in practical operating condition. Please follow these steps:

- (1) Install the PCB and magnet ring.
- (2) Use register 'AUTO_CAL_MODE' (Table 24) to set the calibration mode (Convenient-Auto-Calibration default).

Table 24: 'AUTO_CAL_MODE'

Register	Data	Description
AUTO_CAL_MODE[2:0]	0x3	Convenient-Auto-Calibration (default)
	0x1	Constant-Auto-Calibration

- (3) Use 'AUTO_CAL_FREQ' to set the speed range of Constant-Auto-Calibration, as shown in Table 25. Make the ring rotate constant with the angle increased direction

Table 25: 'CAL_FREQ'

CAL_FREQ[2:0]	Constant-Auto-Calibration speed (Pole-Pairs/Minute)
0x0	$3200 \leq \text{speed} < 6400$
0x1	$1600 \leq \text{speed} < 3200$
0x2	$800 \leq \text{speed} < 1600$
0x3	$400 \leq \text{speed} < 800$
0x4	$200 \leq \text{speed} < 400$
0x5	$100 \leq \text{speed} < 200$
0x6	$50 \leq \text{speed} < 100$
0x7	$25 \leq \text{speed} < 50$

- (4) Pull down CAL_ENB to GND (or write 0x01 to register_ 'SOFT_AUTOCAL') to enable the calibration function at least 16 periods. Monitor the status of calibration from PIN_STATUS (shown in Table 22) , or register_ 'CAL_STATE' (shown in Table 23). If the calibration succeed, the data will be programmed into the EEPROM. Please wait for 500ms and then pull up CAL_ENB to VDD (or write 0x00 to register_ 'SOFT_AUTOCAL') .
- (5) If the calibration failed, please power on again before next calibration.

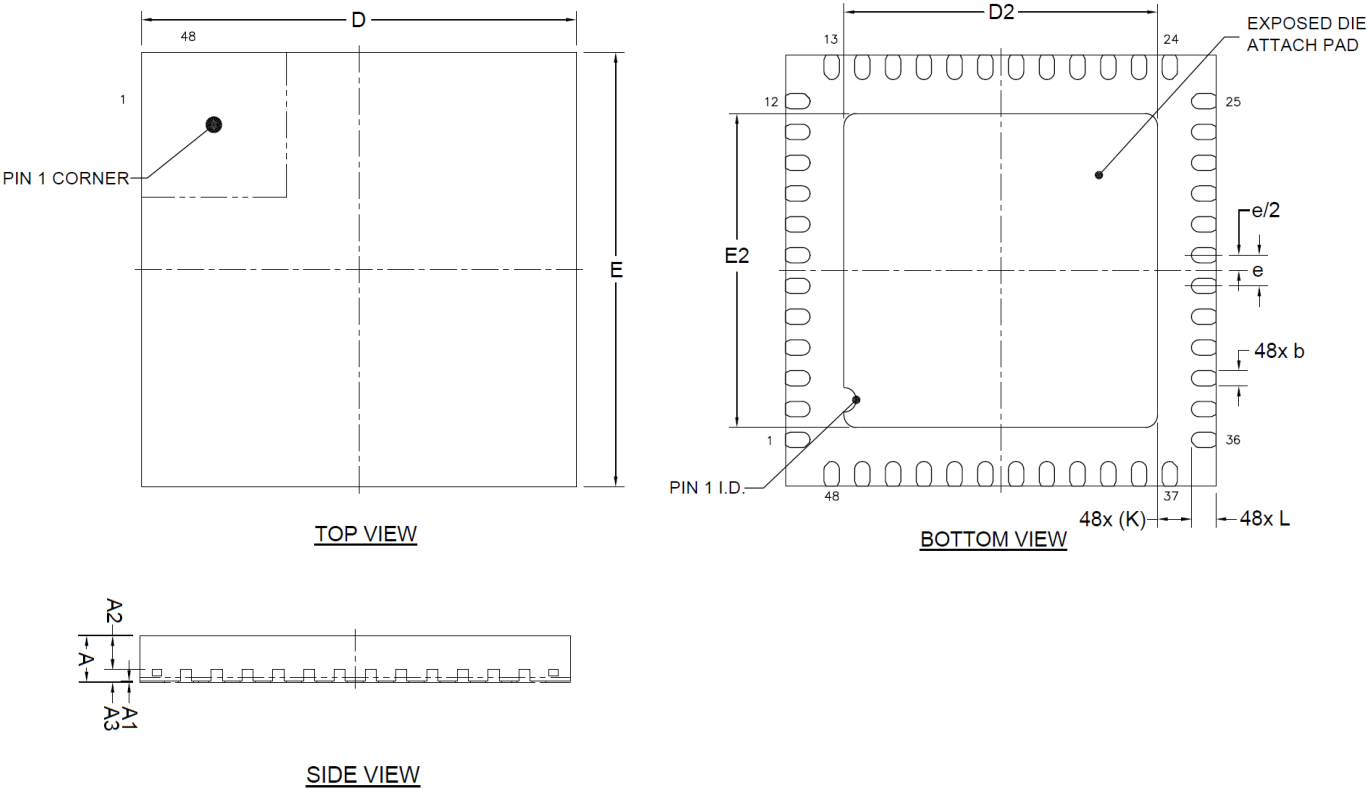
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9. Register Map

Please contact MagnTek to get Register Map.

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10. Package Information



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0	0.050	0	0.002
A2	0.550		0.022	
A3	0.203 (REF)		0.008 (REF)	
b	0.200	0.300	0.008	0.012
D	7.000 (BSC)		0.276 (BSC)	
E	7.000 (BSC)		0.276 (BSC)	
e	0.500 (BSC)		0.020 (BSC)	
D2	5.000	5.200	0.197	0.205
E2	5.000	5.200	0.197	0.205
L	0.300	0.500	0.012	0.020
K	0.550 (REF)		0.022 (REF)	

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12. Revision History

Revision	Date	Comments
0.5	2023.05	Initial Release as Draft
1.0	2024.01	Formal Release