Application Note

NOVOSENSE

Application of Solid-State Relay NSI7258 in Insulation Monitoring for High-Reliability BMS

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Author: Kaijie Zheng, Ning Zhang

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ABSTRACT

The operating voltage of a Battery Management System (BMS) generally exceeds the safe voltage threshold for the human body. A degradation in insulation performance may lead to increased leakage current, posing a threat to personal safety. The insulation monitoring circuit described in this article utilizes the NSI7258 from NOVOSENSE to calculate and monitor the insulation resistance between the positive bus-to-ground and negative bus-to-ground of the battery, thereby enabling high-precision and high-reliability insulation monitoring.

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1.Principle of the Solution

1.1.Implementation of Insulation Monitoring

According to China's national standard: GB 18384 Safety Requirements for Electric Vehicles, the insulation resistance must be greater than 500 Ω/V at the maximum operating voltage. Therefore, for a system with a bus voltage of V_{BUS}, the insulation resistance must be greater than 500 · V_{BUS} to ensure personnel safety. When the insulation resistance degrades, the insulation monitoring circuit should promptly detect the change and trigger an alarm.

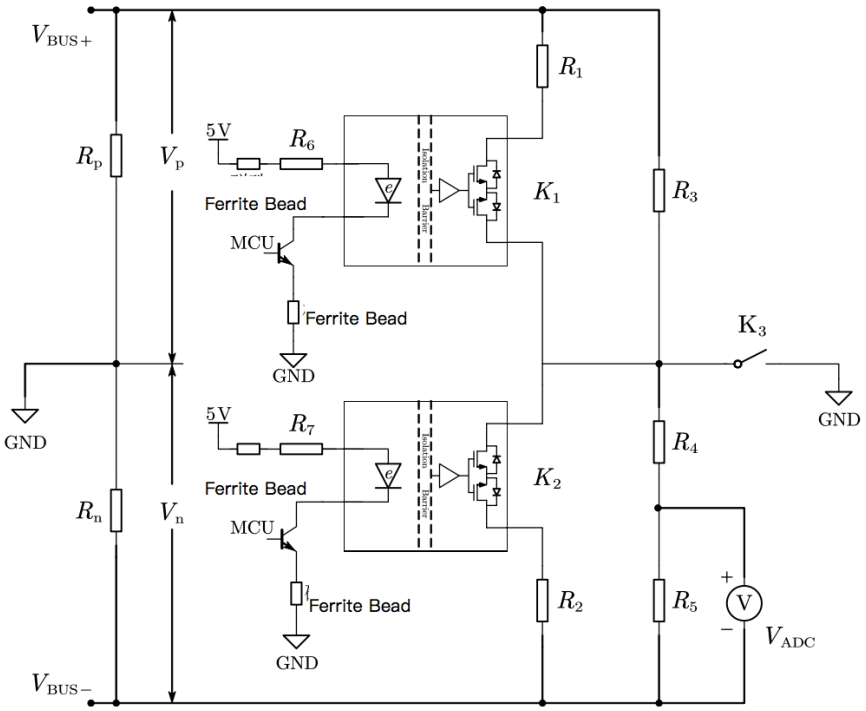

Figure 1.1 Recommended Insulation Monitoring Circuit

The recommended insulation monitoring circuit is illustrated in Figure 1.1. K1 and K2 represent the main application positions of NOVOSENSE Solid-State Relays (SSRs) in the insulation monitoring circuit. The chip adopts a low-side control approach, where the low-side reference ground is the vehicle chassis ground. This circuit performs insulation resistance measurements (R_p, R_n) every 2-3 seconds by switching K1 and K2, while K3 switching controls whether the insulation monitoring circuit is active. During insulation monitoring, K3 remains normally closed.

In this article, the bus voltage is defined as V_{BUS}, the positive bus-to-chassis ground voltage as V_p, and the chassis ground-to-negative bus voltage as V_n.

When K1 is open and K2 is open, the voltage across R5 is V0, then Vn0 = V0*(R4+R5)/R5, $V_{p0} = V_{bus} - V_{n0}$, and the calculation formula (1) is derived:

$$\frac{V_{p0}}{V_{n0}} = \frac{R_p // R_3}{R_n // (R_4 + R_5)} \quad (1)$$

When K1 is closed and K2 is open, the voltage across R5 is V1, then Vn1 = V1*(R4+R5)/R5, Vp1 = Vbus - Vn1, and the calculation formula (2) is derived:

$$\frac{V_{p1}}{V_{n1}} = \frac{R_p // R_3 // R_1}{R_n // (R_4 + R_5)} \quad (2)$$

From equations (1) and (2), we derive calculation formula (3):

$$R_n // (R_4 + R_5) = \left(\frac{V_{n1}}{V_{p1}} - \frac{V_{n0}}{V_{p0}}\right) \times R_1 \quad (3)$$

When K1 is open and K2 is closed, the voltage across R5 is V2, then Vn2 = V2*(R4+R5)/R5 and Vp2 = Vbus - Vn2, and the calculation formula (4) is derived:

$$\frac{V_{p2}}{V_{n2}} = \frac{R_p // R_3}{R_n // (R_4 + R_5) // R_2} \quad (4)$$

From equations (1) and (4), we derive calculation formula (5):

$$R_p // R_3 = \left(\frac{V_{p2}}{V_{n2}} - \frac{V_{p0}}{V_{n0}}\right) \times R_2 \quad (5)$$

Equations (3) and (5) are the results for insulation resistance calculation.

2.Component Selection

2.1.Resistor Selection

2.1.1. Considerations for Resistor Selection

In a typical circuit design, it is common to set R_1=R_2<R_3=R_4, with the following design considerations:

ADC Input Voltage Consideration: The voltage across R5 must always remain below the maximum input voltage of the ADC, ideally close to its full-scale range to ensure high output accuracy of the ADC. Therefore, R5/(R4+R5)*VBUS should be near the ADC's maximum input voltage, determining the ratio between R5 and R4.

ADC Internal Impedance Consideration: Since R5 serves as the ADC sampling input, its resistance should be significantly lower than the internal impedance of the ADC (e.g., R5 < RADC/10) to ensure negligible effects from the ADC's internal impedance.

Impact on Insulation Resistance: During switching of K1 and K2, R1 and R2 are respectively connected in parallel with Rp and Rn. If R1 and R2 are too small, the measured insulation resistance values (Rp // R1 and Rn // R2) may drop significantly.
Detection Accuracy Consideration: As can be concluded from Equation (4), when Rp//R3 degrades below the critical threshold $500 \cdot V_{BUS}$, the MCU should detect this degradation and trigger an alarm if $\left(\frac{V_{p2}}{V_{n2}} - \frac{V_{p0}}{V_{n0}}\right) \times R_2 < 500 \cdot V_{BUS}$. To compensate for ADC measurement accuracy errors, R2 should be relatively smaller to allow sufficient voltage differences between Vp2 and Vn2.
Settle Time Consideration: In real-world applications, some customers connect a Y-capacitor between chassis ground and battery ground (parallel to Rn), introducing RC charge/discharge behaviors. Smaller R1 and R2 reduce the settle time. However, excessively small values can cause too small equivalent parallel impedances – $R_p//R_3//R_1$ and $R_n//(R_4+R_5)//R_2$, potentially compromising personnel safety.

2.1.2. Recommended Resistor Values for 400V/800V Systems

Based on the analysis above, the following resistor configurations are recommended for insulation monitoring circuits.

R_1、R_2	500 kΩ
R_3、R_4	3 MΩ
R_5	12 kΩ

Table 2.1 Recommended Resistor Values for 400V Systems

R_1、R_2	1 MΩ
R_3、R_4	6 MΩ
R_5	12 kΩ

Table 2.2 Recommended Resistor Values for 800V Systems

2.2.Relay Selection

2.2.1. Impact of Relay Leakage Current on Measurement Accuracy

When the insulation resistance degrades below $500 \cdot V_{BUS}$, the system must detect this condition and trigger an alarm. Taking a system with VBUS = 800V as an example, the insulation resistance must be greater than 400 kΩ per industry standards. If the leakage current through K1 and K2 is less than 1 μA, their equivalent impedance exceeds 800 MΩ, far higher than the insulation resistances Rp and Rn, introducing a measurement error of less than 0.05%. If the leakage current increases to 10 μA, the equivalent impedance drops to 400 MΩ, causing a measurement error of approximately 0.5%.
Therefore, higher leakage currents introduce larger measurement errors. Using NOVOSENSE SSR products with small leakage current (<1 μA) to enable turn-on and turn-off functions of K1 and K2, will help enhance measurement accuracy and avoid false alarms.

2.2.2. Impact of Relay Reliability on System Safety

Traditional mechanical relays suffer from limited switching cycles. Once the maximum number of switching cycles is reached, the insulation monitoring function fails, posing significant personal safety risks. As a result, mechanical relays have largely been obsoleted in this application.

Currently, traditional PhotoMOS relays are widely used. In a PhotoMOS relay, when current flows through the LED on the control side, the photodiode receives the emitted light and generates current via the photoelectric effect, thereby controlling the conduction of the high-side MOSFET.

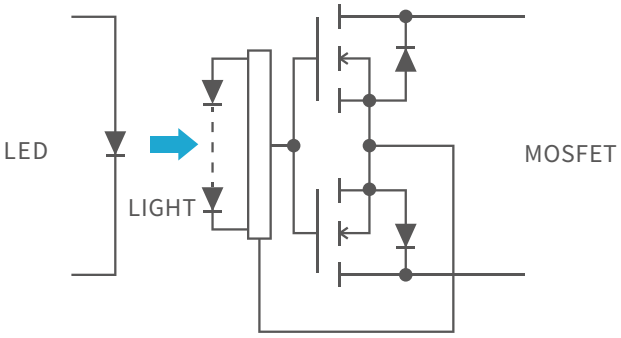

Figure 3.1 PhotoMOS Operating Principle

The luminous intensity of LEDs will degrade over time. According to service life predictions by major optocoupler suppliers, after 1000 hours of operation, the threshold current will increase by 10%; after 11 years, the threshold current may rise by a factor of over 5. If the design strictly follows the threshold current specified in the datasheet, insufficient optical energy received by the photodiode will lead to bit-error failures. The only solution is to increase the input current to compensate for LED aging. However, this introduces another challenge – higher current means elevated temperatures, which degrade both the LED's electro-optical conversion efficiency and the photodiode's optical-to-electrical conversion performance. Additionally, due to thermal stress and aging, PhotoMOS devices are typically limited to a maximum operating temperature of 85°C. These factors pose significant reliability challenges for optocoupler products.

Replacing PhotoMOS relays (similar to optocouplers) with SSRs that adopt capacitive or magnetic isolation mechanism, can significantly improve system reliability. The NSI7258 from NOVOSENSE is a high-reliability isolation device that meets the EMI CISPR25 CLASS5 standard. Combining robust technological innovation with automotive quality management systems, the NSI7258 offers a high-performance, high-reliability solution for insulation monitoring systems.

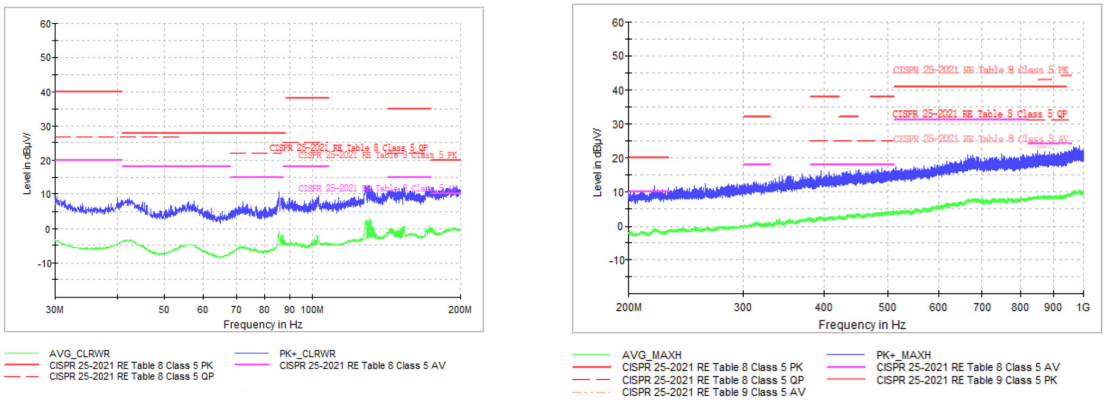

Figure 3.2 NSI7258 EMI Test Results

3.EMS Considerations and Recommended Solutions for Insulation Monitoring Applications

3.1.Potential EMS Issues in Insulation Monitoring Applications

In new energy vehicles (NEVs), the reliability of electronic components is critical to overall vehicle performance. Particularly in environments with harsh electromagnetic interference (EMI), ensuring that integrated units operate normally and meet electromagnetic compatibility (EMC) standards becomes a key challenge.

Some EMS tests, such as radiated immunity (RI), bulk current injection (BCI), and portable transmitter immunity (PTI), can be equivalently modeled as applying a high-frequency current source across the high- and low-voltage sides of the chip, as shown in Figure 4.1. Despite parasitic capacitances on the PCB and in space providing paths for high-frequency current discharge, some currents may still be directly injected into the chip. At higher frequencies (e.g., several hundred MHz), isolation capacitors exhibit relatively low impedance, creating potential current paths. When no other high-frequency current discharge paths are designed, these currents may flow through the isolation capacitors and flow from the high-voltage side back to the low-voltage side, forming a current loop that could interfere with normal chip operation.

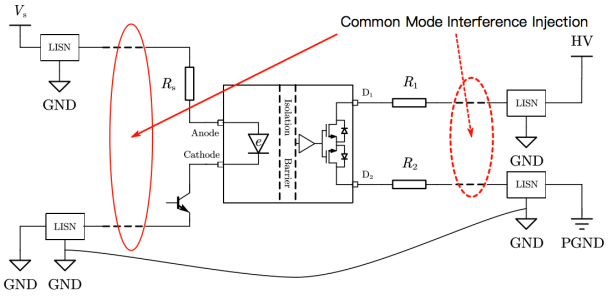

Figure 4.1 Equivalent Model for Some EMS Tests

During the design validation phase of BMS products, system-level ESD tests are required, including power-off mode test, which simulate electrostatic discharge (ESD) events caused by human contact during manufacturing, assembly, testing, storage, and handling to evaluate the product's resistance to ESD damage. In this test, the ESD gun's ground must be connected to the equipment enclosure ground, and discharge points include exposed components (e.g., enclosure, screws) and every pin of accessible connectors. Typically, ±8 kV test is required. Since SSRs bridge the high-voltage and low-voltage domains of the BMS, improper chip placement may expose the isolation barrier to the ±8kV ESD voltage without alternative ESD current discharge paths. The equivalent model of the test is shown in Figure 4.2.

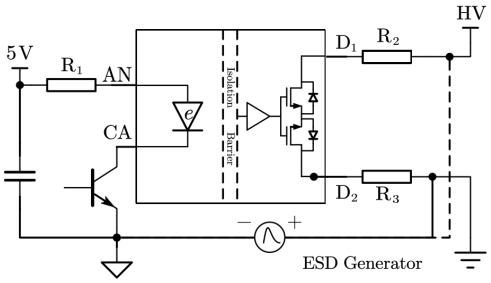

Figure 4.2 Equivalent Model for System ESD Test

To prevent the aforesaid EMC issues from affecting or damaging the chip, the following recommended schematic and layout designs are provided.

3.2.Recommended Application Circuit Analysis

As shown in Figure 2.1, in insulation monitoring applications, it is recommended to place SSRs at both sides of the midpoint of the bridge, and connect them to the high-voltage bus V_{BUS+} and V_{BUS-} via large voltage divider resistors R1 and R2. Taking K1 as an example, due to the presence of large voltage divider resistors on the lines between the D1 and D2 pins of K1 and the high-voltage bus HV_+ and HV_-, high-frequency interference currents find it difficult to enter the SSR. Additionally, when K3 is turned on, it provides an additional path for high-frequency interference currents to discharge. During interference injection, the current flow path would be: V_{BUS+} →R_1 →K_1 's on-resistance R_{dson} →K_3 's on-resistance R_{dson} → chassis ground GND, avoiding flow through the SSR isolation capacitor, thus reducing the SSR's malfunction risk due to interference. It is also recommended to add ferrite beads in series with the low-voltage side of the chip to increase the impedance of the line, thereby hindering high-frequency currents from entering the chip. Considering that isolation capacitors have lower impedance at higher frequencies, ferrite beads with higher impedance in the 100 MHz - 400 MHz range are recommended to effectively block interference currents. During system ESD test in power-off mode, ESD voltages are applied between VBUS+, VBUS-, and the chassis ground GND. For K1, K2, and K3, the megaohm-level current-limiting resistors in the ESD path protect the chip.

In the suboptimal circuit design illustrated in Figure 4.2, unlike the design in Figure 2.1, K2 and R2 positions are swapped, directly connecting K2 to HV_-. This results in different EMS and ESD performances for K1 and K2. Without the blocking effect of large voltage divider resistors, high-frequency currents directly inject into K2 via the D2 pin. Due to the presence of large voltage divider resistor R2 between the D1 pin of K2 and the midpoint of the bridge, the impedance of the isolation capacitor becomes relatively smaller, preventing interference currents from discharging through K3 to the chassis ground GND. Instead, they flow through the isolation capacitor of K2 back to the chassis ground. The current flow path is: HV_- → K2's isolation capacitor C_{ISO} → chassis ground GND. Since the interference current flows through the SSR's isolation capacitor, there is a SSR malfunction risk. Moreover, during the system ESD test, the ESD voltage is directly borne by the isolation capacitor of K2, potentially leading to chip damage if the applied ESD voltage is too high.

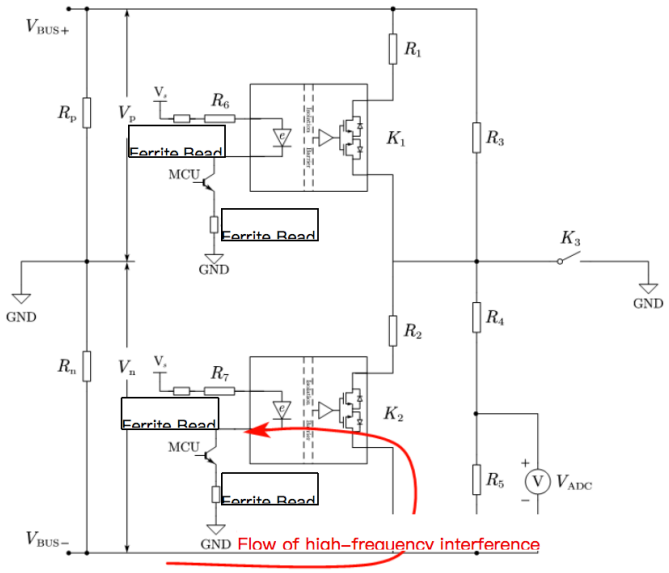

Figure 4.3 Suboptimal Insulation Monitoring Design

3.3.Recommended PCB Layout

PCB layout is crucial for EMS performance. Based on the optimized circuit design discussed in Section 4.1, the following PCB circuit design reference is provided. See Figure 4.4 Recommended Schematic Diagram, Figure 4.5 Recommended PCB Layout and the PCB layout guidelines below.

1. To meet the isolation and safety requirements, the primary and secondary sides must be physically isolated. Creepage distances and clearances must meet the applicable safety standards for the application. Given that typical PCB boards are of CTI Class III, slots should be made to ensure adequate creepage.

2. Special attention should be paid to PCB traces to ensure sufficient common-mode interference rejection. Considering the effects of distributed parasitic capacitance, placing traces too close within the same layer or across layers should be avoided to prevent the generation of parasitic low-impedance paths that allow interference currents to directly enter the chip's high-voltage side D1 and D2 pins. Additionally, large ground planes near ferrite beads should be avoided to prevent currents from bypassing the beads through stray capacitance, which would compromise their effectiveness.

Experimental verification shows that the recommended circuit passes the ISO11452-4 Level 4 BCI test in the 100 kHz - 400 MHz frequency range and meets the ±10 kV system ESD test requirements.

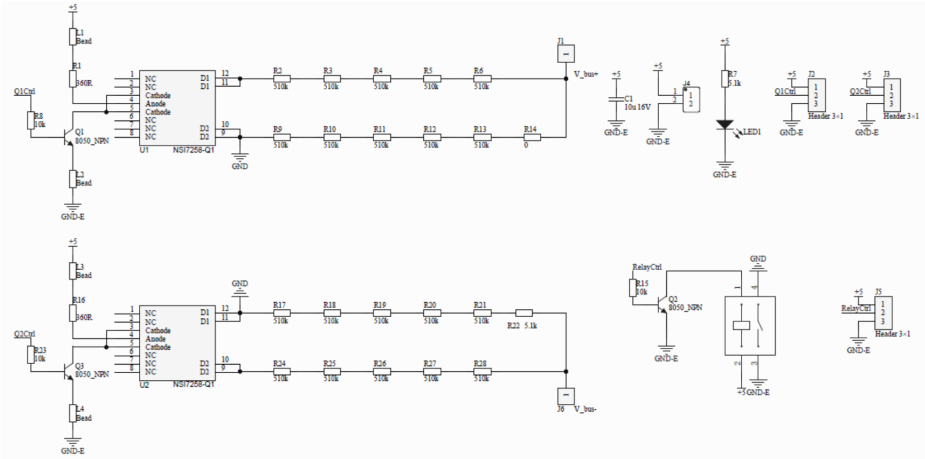

Figure 4.4 Recommended Schematic Diagram for Insulation Monitoring

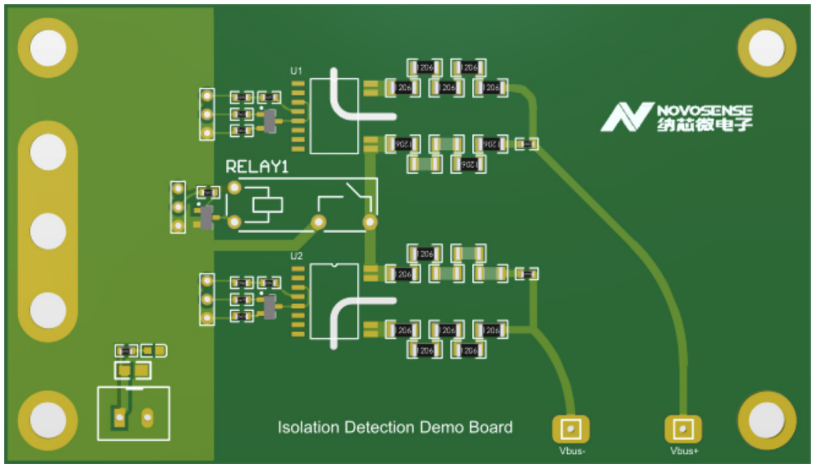

Figure 4.5 Recommended PCB Layout for Insulation Monitoring

4.Revision History

Revision	Description	Author	Date
1.0	Application Note created	Kaijie Zheng, Ning Zhang	2025/4/10

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