NOVOSENSE

NSD56008-Q1

8CH, 1Ω, 40V, Fully Protected Automotive Low-side Switch

Datasheet (EN) 1.1

Product Overview

The NSD56008 is an eight-channel low-side switch specifically designed to control relays and LEDs in automotive and industrial applications.

The 16-bit serial peripheral interface (SPI) is utilized to control and diagnose the device and the loads. The SPI interface also provides daisy chain capability.

This device is designed for low supply voltage operation, therefore being able to keep its state at low battery voltage ($V_S \geq 4.1$ V) when V_S falls down.

The NSD56008 is equipped with two input pins that are connected to two outputs. With the Input Mapping it is possible to connect the input pins to different outputs, or assign more outputs to the same input pin. In this case more channels can be controlled with one signal applied to one input pin.

In Limp Home mode (Fail-Safe mode) the input pins are directly routed to channels 2 and 3.

The device provides diagnosis of the load via Open Load at OFF state and short circuit detection. Temperature sensors are available for each channel to protect the device against Over Temperature.

Applications

- Relays
- LEDs
- Motors
- Solenoids

Key Features

- 16-bit serial peripheral interface for control and diagnosis
- Daisy Chain capability SPI also compatible with 8-bit SPI devices
- 2 CMOS compatible parallel input pins with Input Mapping functionality
- Cranking capability down to $V_S = 4.1$ V
- Digital supply voltage range compatible with 3.3 V and 5 V microcontrollers
- Very low quiescent current
- Limp Home mode
- AEC-Q100 (Grade 1) qualified for automotive application

Protection and Diagnostic Features

- Short circuit to battery protection
- Over Current latch OFF
- Thermal shutdown latches OFF
- Latched diagnostic information via SPI register
- Over Load detection at ON state
- Open Load detection at OFF state using Output Status Monitor function
- Output Status Monitor
- Input Status Monitor

Device Information

Part Number	Package	Body Size
NSD56008-Q1HTSBR	HTSOP24	8.65mm x 3.9mm

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1. Pin Configuration and Functions

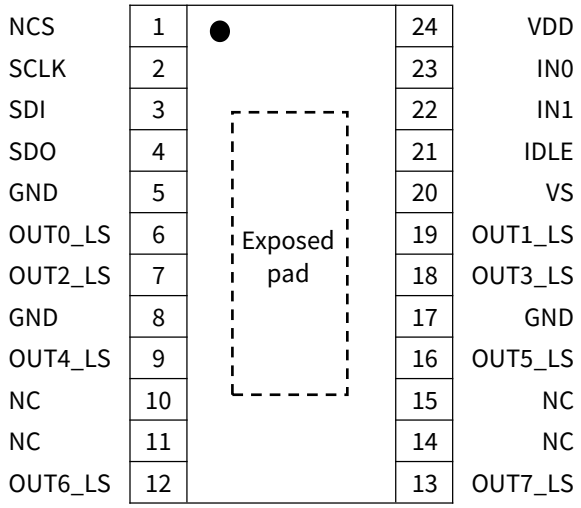
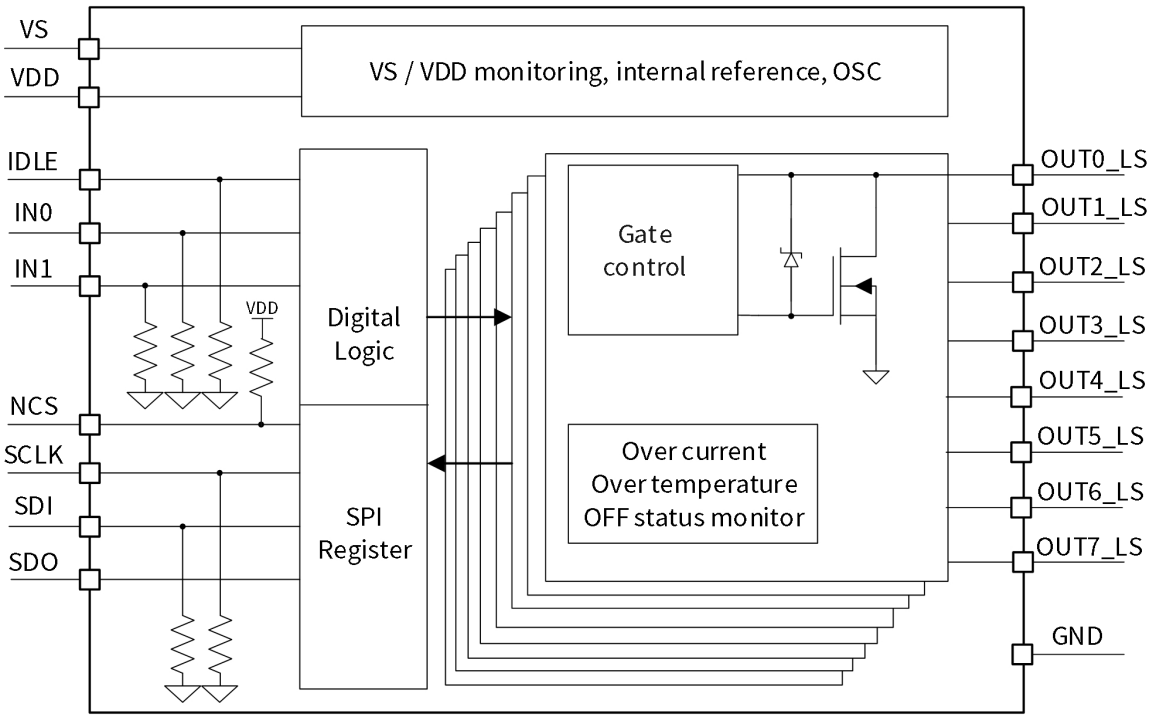


Figure 1.1 NSD56008 Pinout

Table 1.1 NSD56008 Pin Configuration and Description

SYMBOL	PIN NO.	TYPE	DESCRIPTION
NCS	1	Input	Chip Select, "low" active, integrated pull-up to V_{DD}
SCLK	2	Input	Serial Clock, "high" active, integrated pull-down to ground
SDI	3	Input	Serial Input, "high" active, integrated pull-down to ground
SDO	4	Output	Serial Output, "Z" (tri-state) when NCS is "high"
GND	5, 8, 17	Ground	Ground connection
OUT0_LS	6	Output	Drain of low-side power transistor (channel 0)
OUT2_LS	7	Output	Drain of low-side power transistor (channel 2)
OUT4_LS	9	Output	Drain of low-side power transistor (channel 4)
NC	10, 11, 14, 15		Not Connected, internally not bonded
OUT6_LS	12	Output	Drain of low-side power transistor (channel 6)
OUT7_LS	13	Output	Drain of low-side power transistor (channel 7)
OUT5_LS	16	Output	Drain of low-side power transistor (channel 5)
OUT3_LS	18	Output	Drain of low-side power transistor (channel 3)
OUT1_LS	19	Output	Drain of low-side power transistor (channel 1)
VS	20	Power	Power supply V_S for power switches gate control and protections
IDLE	21	Input	Idle mode control, "high" activates Idle mode, integrated pull-down to ground
IN1	22	Input	Input pin 1, connected to channel 3 by default and in Limp Home mode, "high" active, integrated pull-down to ground
IN0	23	Input	Input pin 0, connected to channel 2 by default and in Limp Home mode, "high" active, integrated pull-down to ground
VDD	24	Power	Digital supply V_{DD}, Supply voltage for SPI with support function to V_S
Exposed pad		—	It is recommended to connect it to PCB ground for cooling and EMC - not usable as electrical GND pin. Electrical ground must be provided by pins 5, 8 and 17.

2. Block Diagram



3. Application information

Note1: Recommended components may depend on the requirements at system levels and shall be confirmed by specific tests on the final application.

Note2：There is no reverse polarity protection function in VS pin. A reverse protection diode or ideal diode must be added before VS pin.

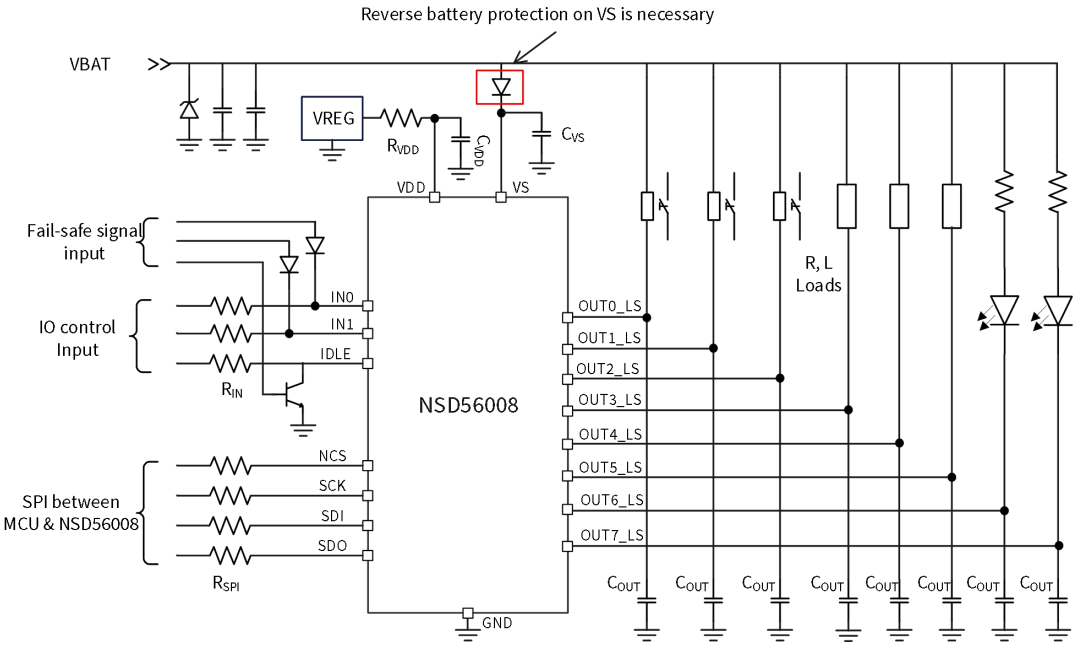


Figure 3.1 NSD56008 Application Diagram

Table3.1 Suggested Component values

Reference	Value	Purpose
R_{IN}	4.7 kΩ	Protection of the micro-controller during Over Voltage and Reverse Polarity Guarantee NSD56008 channels OFF during Loss of Ground
R_{SPI}	500 Ω	Protection of the micro-controller during Over Voltage and Reverse Polarity
R_{VDD}	100 Ω	Logic supply voltage spikes filtering
C_{VDD}	100 nF	Logic supply voltage spikes filtering
C_{VS}	68 nF	Analog supply voltage spikes filtering
TVS	P6SMB30	Transient voltage suppressor
C_{OUT}	22 nF	Protection of NSD56008 against ESD and BCI

Note： When $f_{SCLK} \geq 2MHz$ or VDD = 3.3V, resistor in SPI line is suggested 100R, and MCU I/O is suggested to set in strong mode

4. General Product Characteristics

Table4.1 Suggested Component values

SYMBOL	PARAMETER	VALUES
V_S	Analog supply voltage	4.5 V … 28 V
V_{DD}	Digital supply voltage	3.0 V … 5.5 V
$R_{DS(ON)}$	Typical on-state resistance at T_J = 25 °C	1Ω
$I_{L(NOM)}$	Nominal load current (T_A = 85 °C, all channels)	330 mA
E_{AR}	Maximum Energy dissipation - repetitive	10 mJ @ $I_{L(EAR)}$ = 220 mA
$V_{DS(CL)}$	Minimum Drain to Source clamping voltage	42 V
$I_{L(OVL1)}$	Minimum overload switches OFF threshold	500 mA
I_{SLEEP}	Typical V_S quiescent current at $T_J \leq 85$ °C	1.1µA
f_{SCLK}	Maximum SPI clock frequency	5MHz

4.1. Absolute Maximum Ratings

Absolute Maximum Ratings [1] T_J = -40 °C to +150 °C, all voltages with respect to ground

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_S	Analog Supply voltage	-0.3	28	V
V_{DD}	Digital Supply voltage	-0.3	5.5	V
$V_{S(LD)}$	Supply voltage for load dump protection		42	V
V_{DS}	Voltage at power transistor	-0.3	42	V
V_{IDLE}	Voltage at IDLE pin	-0.3	5.5	V
V_{IN}	Voltage at input pins	-0.3	5.5	V
V_{NCS}	Voltage at chip select pin	-0.3	5.5	V
V_{SCLK}	Voltage at serial clock pin	-0.3	5.5	V
V_{SDI}	Voltage at serial input pin	-0.3	5.5	V
V_{SDO}	Voltage at serial output pin SDO	-0.3	V_{DD}+0.3	V
T_J	Junction Temperature	-40	150	°C
T_{stg}	Storage Temperature	-55	150	°C

1) Not subject to production test，specified by design

4.2. Functional Range

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{S(NOR)}$	Supply Voltage Range for Normal Operation	7	18	V
$V_{S(EXT,UP)}$ [1]	Upper Supply Voltage Range for Extended Operation	18	28	V
$V_{S(EXT,LOW)}$ [1]	Lower Supply Voltage Range for Extended Operation	4.5	7	V
T_J	Junction Temperature	-40	150	°C
V_{DD}	Logic supply voltage	3	5.5	V

1) Parameter deviation possible

4.3. Thermal Resistance

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
R_{thJC}	1) Junction to Case(bottom) Thermal Resistance		5.5		K/W
R_{thJA}	1) Junction to Ambient Thermal Resistance		30		K/W
ψ_{JT}	1) Junction-to-top characterization parameter		2.6		K/W

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four-layer board.

1) Not subject to production test，specified by design

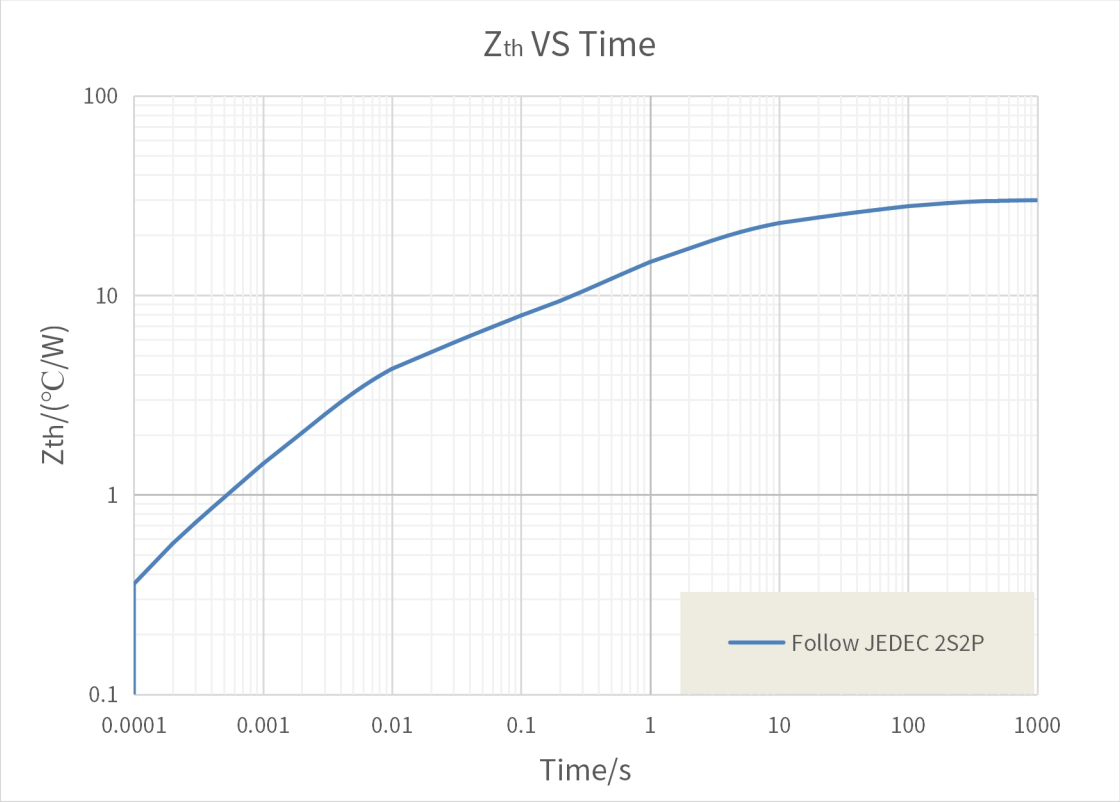


Figure 4.1 Typical Thermal Impedance

4.4. ESD Ratings

SYMBOL	PARAMETER	VALUE	UNIT
Electrostatic discharge	Human-body model, per AEC-Q100-002-RevD ， $V_{ESD-HBM}$	±4000	V
	Charged-device model, per AEC-Q100-011-RevB ， $V_{ESD-CDM}$	±750	V

5. Power Supply

The NSD56008 is fed by two supply voltages:

- V_S (analog supply voltage used also for the logic)
- V_{DD} (digital supply voltage)

The V_S supply line is connected to a battery feed, and outputs V_{reg} by LDO. V_{reg} is used, in combination with V_{DD} supply, for the driving circuitry of the power stages. An increased current consumption may be observed at VDD pin, when V_S voltage drops below V_{DD} voltage (for instance during cranking events down to 4.1 V).

V_S and V_{DD} supply voltages have an undervoltage detection circuit. Function of the UV circuit is shown in **Table 5.1**.

Figure 5.1 shows a basic interaction between supply pins VS and VDD, the output stage drivers and SDO supply line.

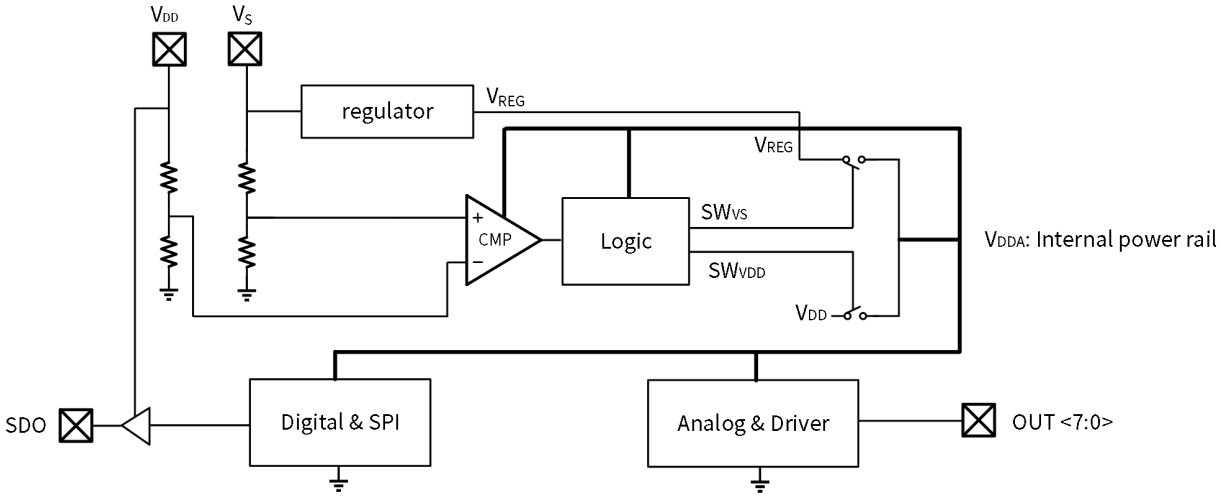


Figure 5.1 NSD56008 Internal Power Supply concept

When $V_S \le V_{DD}$ +0.7 ± V_{SDIFF} (V_{SDIFF} is hysteresis between V_{DD} and V_S) NSD56008 operates in “Cranking Operative Range” (COR). The current consumption from VDD pin increases while it decreases from VS pin where the total current consumption remains within the specified limits in this condition. **Figure 5.2** shows the voltage levels at VS pin where the device goes in and out of COR.

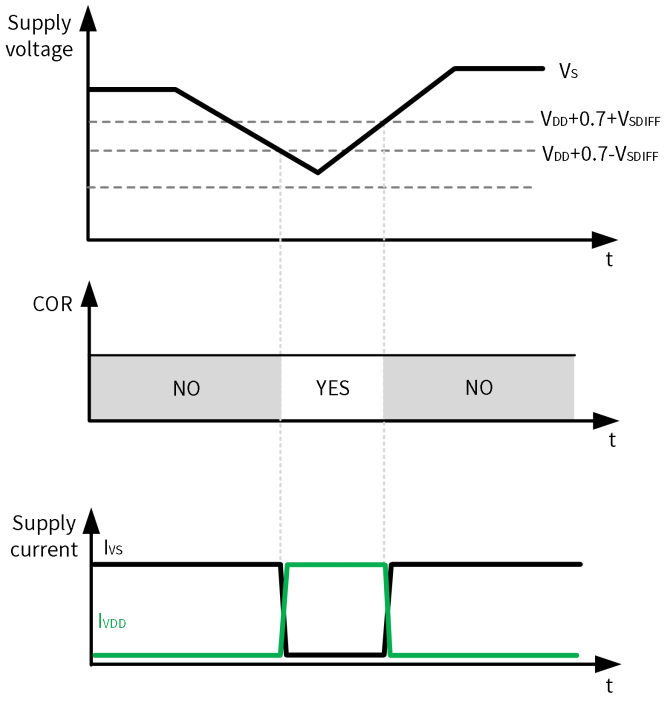


Figure 5.2 “Cranking Operative Range”

An overview of channel behavior according to different V_S and V_{DD} supply voltages is shown in **Table 5.1** (the Table is valid after a successful power-up, see **Chapter 5.1.1** for more details).

Table 5.1 Device capability as function of V_S and V_{DD}

	$V_{DD}<V_{DD(UV)}$	$V_{DD}\geq V_{DD(UV)}$
$V_S<V_{S(UV)}$	channels cannot be controlled	channels can be switched ON and OFF (SPI control) ($R_{DS(ON)}$ deviations possible)
	SPI registers reset	SPI registers available
	SPI communication not available	SPI communication possible (f_{SCLK} = 5 MHz)
	Limp Home mode not available	Limp Home mode available ($R_{DS(ON)}$ deviations possible)
$V_S \geq V_{S(UV)}$	channels cannot be controlled by SPI	channels can be switched ON and OFF (SPI control) ($R_{DS(ON)}$ deviations possible)
	SPI registers reset	SPI register available
	SPI communication not available	SPI communication possible (f_{SCLK} = 5 MHz)
	Limp Home mode available ($R_{DS(ON)}$ deviations possible)	Limp Home mode available ($R_{DS(ON)}$ deviations possible)

5.1. Operation Modes

NSD56008 has the following four operation modes: Sleep mode, Idle mode, Active mode and Limp Home mode.

The transition between operation modes is determined according to following levels and states:

- IDLE pin logic level
- INn pins logic level
- **OUT.OUTn** bits state
- **HWCR.ACT** bit state

The operation mode of the NSD56008 can be observed by:

- status of output channels
- status of SPI registers
- current consumption at VDD pin (I_{VDD}) and VS pin (I_{VS})

The state diagram including the possible transitions is shown in **Figure 5.3**.

The default operation mode to switch ON the loads is Active mode. Output turn-on time t_{ON} will be extended due to the mode transition latency.

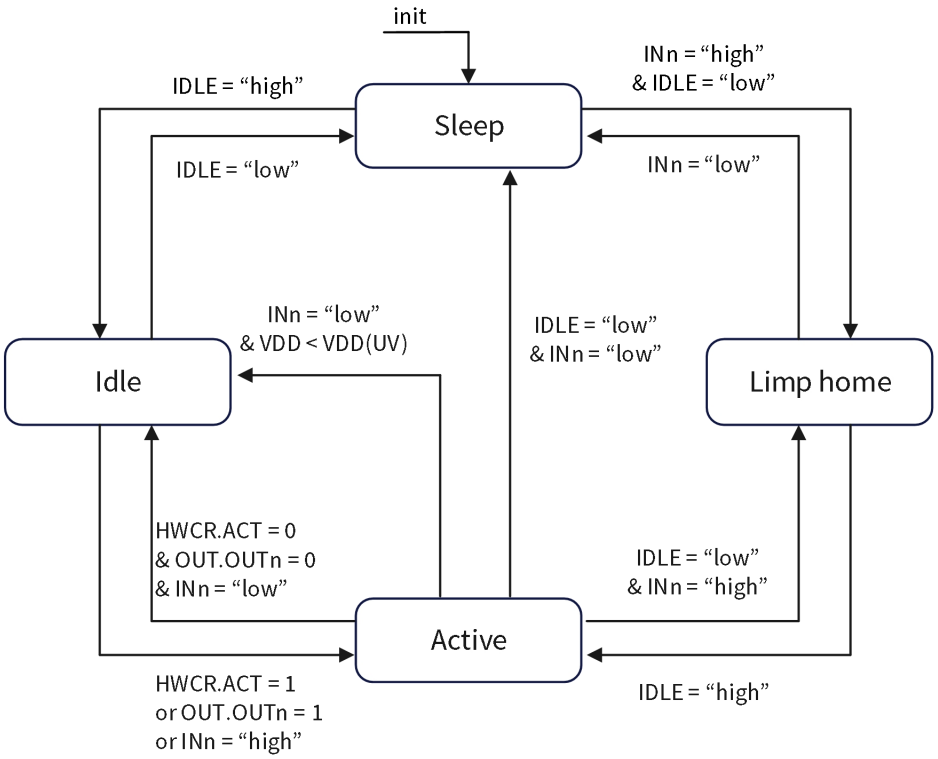


Figure 5.3 Operation Mode state diagram

Table 5.2 shows the correlation between device operation modes, V_S and V_{DD} supply voltages, and state of the important functions (channels operativity, SPI communication and SPI registers).

Table 5.2 Device function in relation to operation modes, V_S and V_{DD} voltages

Operation Mode	Function	Undervoltage condition on V_S $V_{DD} \le V_{DD(UV)}$	Undervoltage condition on V_S $V_{DD} > V_{DD(UV)}$	V_S not in undervoltage $V_{DD} \le V_{DD(UV)}$	V_S not in undervoltage $V_{DD} > V_{DD(UV)}$
Sleep	Channels	not available	not available	not available	not available
	SPI comm.	not available	not available	not available	not available
	SPI registers	reset	reset	reset	reset
Idle	Channels	not available	not available	not available	not available
	SPI comm.	not available	√	not available	√
	SPI registers	reset	√	reset	√
Active	Channels	not available	√	√ (IN pins only)	√
	SPI comm.	not available	√	not available	√
	SPI registers	reset	√	reset	√
Limp Home	Channels	not available	√ (IN pins only)	√ (IN pins only)	√ (IN pins only)
	SPI comm.	not available	√ (read-only)	not available	√ (read-only)
	SPI registers	reset	√ (read-only)	reset	√ (read-only)

5.1.1. Power-up

The IC performs Power-up procedure when one of the supply voltages (V_S or V_{DD}) is applied to the device and the INn or IDLE pins are set to "high".

5.1.2. Sleep mode

In sleep mode, the outputs of the device are OFF and the SPI registers are reset to default values. The current consumption is minimum.

5.1.3. Idle mode

The current consumption of the device can reach the parameter I_{IDLE} in Idle mode. The internal voltage regulator is still working. Diagnosis functions are not available. The output channels are disabled. The SPI registers are working and SPI communication is possible when VDD is available. **ERRn** bits are not cleared for functional safety reasons in Idle mode.

5.1.4. Active mode

Device current consumption is specified with I_{ACTIVE}. When IDLE pin is set to "high" and one of the input pins is set to "high" or one **OUT.OUTn** bit is set to "1", the device enters Active mode. The device returns to Idle mode as soon as all inputs pins are set to "low", **OUT.OUTn** bits are set to "0" and **HWCR.ACT** is set to "0". If all input pins are set to "low", an undervoltage condition on V_{DD} supply brings the device into Idle mode.

5.1.5. Limp Home mode

When IDLE pin is "low" and one of the input pins is set to "high", the device is brought into Limp Home mode switching ON the channel connected to it. All other channels are OFF.SPI registers can be read but cannot be written. More in detail:

- **VSUV** and **LOPVDD** are set to "1"
- **OLOFF** bits are set to "0"
- **ERRn** bits work normally
- **DIAG_OSM.OUTn** bits can be read and work normally
- **MODE** bits are set to "01_B" (Limp Home mode)
- **TER** bit is set to "1" on the first SPI command after entering Limp Home mode. Afterwards it works normally
- When the device is in Limp Home mode, all other registers are set to their default value and cannot be programmed.

5.1.6. Power Supply modes transition

When the device is in Active mode or in Limp Home mode the channel turn-on time is as defined by parameter t_{ON}. In all other cases, it is necessary to add the transition time required to reach Active mode or Limp Home mode (as shown in **Figure 5.4**).

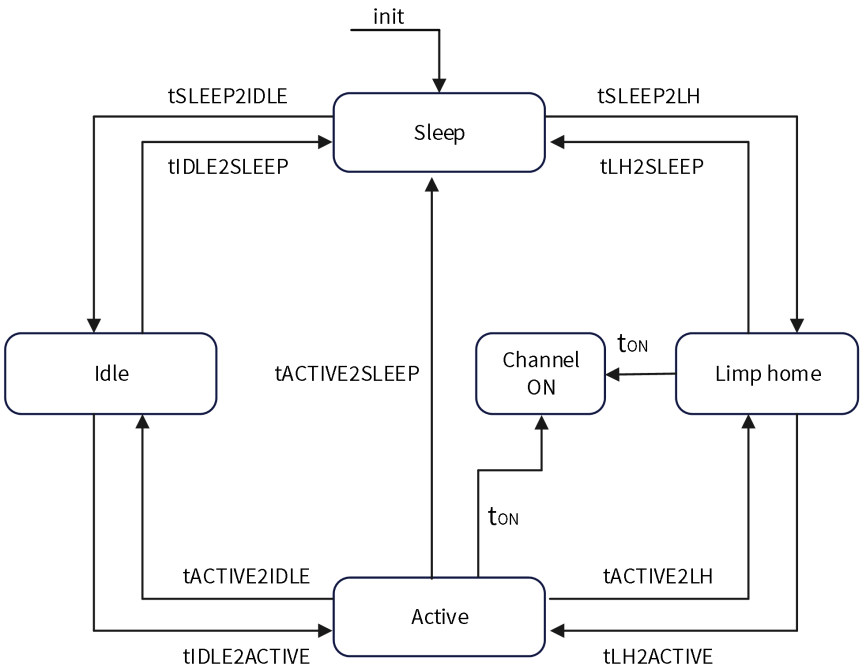


Figure 5.4 Transition Time diagram

5.2. Reset condition

The following 3 conditions reset the SPI registers to the default value:

- V_{DD} is not present or below the undervoltage threshold $V_{DD(UV)}$
- IDLE pin is set to “low” (in Limp home mode, see **Chapter 5.1.5** for more details).
- A reset command (HWCR.RST set to “1”) is executed
  - **ERRn** bits are not cleared by a reset command (for functional safety)
  - **VSUV** and **LOPVDD** bits are cleared by a reset command

If there are no input pin set to “high”, all channels are switched OFF. And the Input Mapping configuration is reset.

5.2.1. Undervoltage on V_S

Undervoltage behavior is shown in **Figure 5.5.**

Between $V_{S(UV)\_FALL}$ and $V_{S(UV)\_RISE}$ the undervoltage mechanism is triggered. the logic will set the bit **VSUV** to "1" if the device is operative and the supply voltage drops below the undervoltage threshold $V_{S(UV)\_FALL}$. The bit **VSUV** is set to "0" after the first Standard Diagnosis readout as soon as the supply voltage V_S is above the minimum voltage operative threshold $V_{S(UV)\_RISE}$.

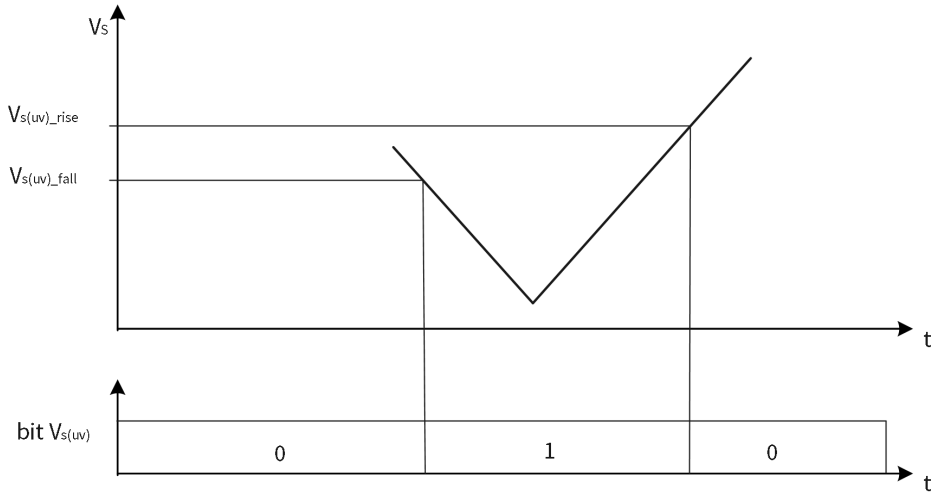


Figure 5.5 V_S Undervoltage Behavior

5.2.2. Low Operating Power on V_{DD}

In V_{DD} rise condition, when $V_{DD} \le V_{DD(LOP)\_RISE}$, the bit **LOPVDD** remains "1", As soon as $V_{DD} > V_{DD(LOP)\_RISE}$ the bit **LOPVDD** is set to "0" after the first Standard Diagnosis readout.

In V_{DD} fall condition, when $V_{DD} > V_{DD(LOP)\_FALL}$, the bit **LOPVDD** remains "0", As soon as $V_{DD} \le V_{DD(LOP)\_FALL}$ the bit **LOPVDD** is set to "1" after the first Standard Diagnosis readout.

5.3. Electrical Characteristics Power Supply

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground. Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VS pin						
$V_{S(UV)\_FALL}$	Analog supply undervoltage shutdown falling	V_M falls until **VSUV** triggers	3.3	3.7	4.1	V
$V_{S(UV)\_RISE}$	Analog supply minimum operative voltage rising	V_M rises until operation recovers	3.7	4.2	4.7	V
$V_{S(HYS)}$	Undervoltage shutdown hysteresis			0.5		V
$I_{VS(SLEEP)}$	Analog supply current consumption in Sleep mode with loads	V_{DD}=V_{NCS}		1.1	20	µA
$I_{VS(IDLE)}$	Analog supply current consumption in Idle mode with loads	f_{SCLK} = 0 MHz V_{NCS} =V_{DD}		1.2	2.2	mA
$I_{VS(IDLE)}$	Analog supply current consumption in Idle mode with loads (COR)	f_{SCLK} = 0 MHz V_{NCS} =V_{DD}			0.3	mA
$I_{VS(ACTIVE)}$	Analog supply current consumption in active mode with loads	f_{SCLK} = 0 MHz, **DIAG_IOL.OUTn** = 0_B V_{NCS} =V_{DD}		2	4.2	mA
$I_{VS(ACTIVE)}$	Analog supply current consumption in active mode with loads (COR)	f_{SCLK} = 0 MHz, **DIAG_IOL.OUTn** = 0_B V_{NCS} =V_{DD}			0.3	mA
VDD pin						
$V_{DD(OP)}$	Logic Supply Operating voltage	f_{SCLK} = 5 MHz	3.0		5.5	V
V_{DDUV_FALL}	Logic supply undervoltage shutdown falling	V_{SDI} = 0 V, V_{SCLK} = 0 V, V_{NCS} = 0 V SO from “low” to high impedance	2	2.4	2.7	V
V_{DDUV_RISE}	Logic supply minimum operative voltage rising	V_{SDI} = 0 V, V_{SCLK} = 0 V, V_{NCS} = 0 V SO from high impedance to “low”	2.2	2.65	3	V
V_{DDUV_HYS}	VDD Undervoltage shutdown hysteresis			0.25		V
$V_{DD(LOP)}$	Logic Supply Lower Operating Voltage		3.0		4.5	V
$V_{DD(LOP)\_FALL}$	Logic Supply Lower Operating Voltage falling	V_{DDLOP} from “0” to “1”		4		V
$V_{DD(LOP)\_RISE}$	Logic Supply Lower Operating Voltage rising	V_{DDLOP} from “1” to “0”		4.2		V
$I_{VDD(SLEEP)}$	Logic supply current in Sleep mode	V_{NCS} =V_{DD}, $T_J \le 85$ °C		0.1	2.5	µA
$I_{VDD(SLEEP)}$	Logic supply current in Sleep mode	V_{NCS} =V_{DD}, T_J = 150 °C			10	µA
$I_{VDD(IDLE)}$	Logic supply current in Idle mode	f_{SCLK} = 0 MHz, V_{NCS} =V_{DD}			0.3	mA
$I_{VDD(IDLE)}$	Logic supply current in Idle mode (COR)	f_{SCLK} = 0 MHz, V_{NCS} =V_{DD}		1.2	2.2	mA
$I_{VDD(ACTIVE)}$	Logic supply current in Active mode	f_{SCLK} = 0 MHz, **DIAG_IOL.OUTn** = 0_B V_{NCS} =V_{DD}			0.3	mA
$I_{VDD(ACTIVE)}$	Logic supply current in Active mode (COR)	f_{SCLK} = 0 MHz, **DIAG_IOL.OUTn** = 0_B V_{NCS} =V_{DD}		2	4.2	mA

Overall current consumption						
I_{SLEEP}	Overall current consumption in Sleep mode $I_{VS(SLEEP)}$ +$I_{VDD(SLEEP)}$	V_{NCS} =V_{DD}, $T_J \le 85$ °C			5	µA
I_{SLEEP}	Overall current consumption in Sleep mode $I_{VS(SLEEP)}$ +$I_{VDD(SLEEP)}$	V_{NCS} =V_{DD}, $T_J = 150$ °C			30	µA
I_{IDLE}	Overall current consumption in Idle mode $I_{VS(IDLE)}$ +$I_{VDD(IDLE)}$	f_{SCLK} = 0 MHz, **DIAG_IOL.OUTn** = 0_B V_{NCS} =V_{DD}			2.5	mA
I_{ACTIVE}	Overall current consumption in Activemode $I_{VS(ACTIVE)}$ +$I_{VDD(ACTIVE)}$	f_{SCLK} = 0 MHz, **DIAG_IOL.OUTn** = 0_B V_{NCS} =V_{DD}			4.5	mA
V_{SDIFF}	Voltage difference between, V_S and V_{DD} supply lines	1)		100		mV
Timings						
$t_{SLEEP2IDLE}$	Sleep to Idle delay	1) from IDLE pin to **TER** + **ISM** register = 8680_H		200	400	µs
$t_{IDLE2SLEEP}$	Idle to Sleep delay	1) from IDLE pin to Standard Diagnosis = 0000_H, external pull-down SDO to GND required		100	200	µs
$t_{IDLE2ACTIVE}$	Idle to Active delay	1) from INn or NCS pins to MODE = 10_B		100	200	µs
$t_{ACTIVE2IDLE}$	Active to Idle delay	1) from INn or NCS pins to MODE = 11_B		100	200	µs
$t_{SLEEP2LH}$	Sleep to Limp Home delay	1) from INn pins to VDS = 10% VS		300 +t_{ON}	600 +t_{ON}	µs
$t_{LH2SLEEP}$	Limp Home to Sleep delay	1) from INn pins to Standard Diagnosis = 0000_H, External pull-down SDO to GND required		200 +t_{OFF}	400 +t_{OFF}	µs
$t_{LH2ACTIVE}$	Limp Home to Active delay	1) from IDLE pin to MODE = 10_B		50	100	µs
$t_{ACTIVE2LH}$	Active to Limp Home delay	1) from IDLE pin to TER + ISM register = 8683_H (IN0 = IN1 = “high”) or 8682_H (IN1 = “high”, IN0 = “low”) or 8681_H (IN1 = “low”, IN0 = “high”)		50	100	µs
$t_{ACTIVE2SLEEP}$	Active to Sleep delay	1) from IDLE pin to Standard Diagnosis = 0000_H, external pull-down SDO to GND required.		50	100	µs

1) Not subject to production test, specified by design

6. Control Pins

The device has three pins (IN0, IN1 and IDLE) to directly control the device operation without using SPI.

6.1. Input pins (IN0, IN1)

The device has two input pins IN0 & IN1. Each input pin is connected to one channel in default (IN0 to channel 2, IN1 to channel 3). In idle & active mode, input mapping registers **MAP_IN0** and **MAP_IN1** can be programmed to connect other channels to the corresponding input pin, as shown in **Figure 6.1**. The signals to drive the channels are generated by an OR combination between **OUT** control registers, IN0 and IN1.

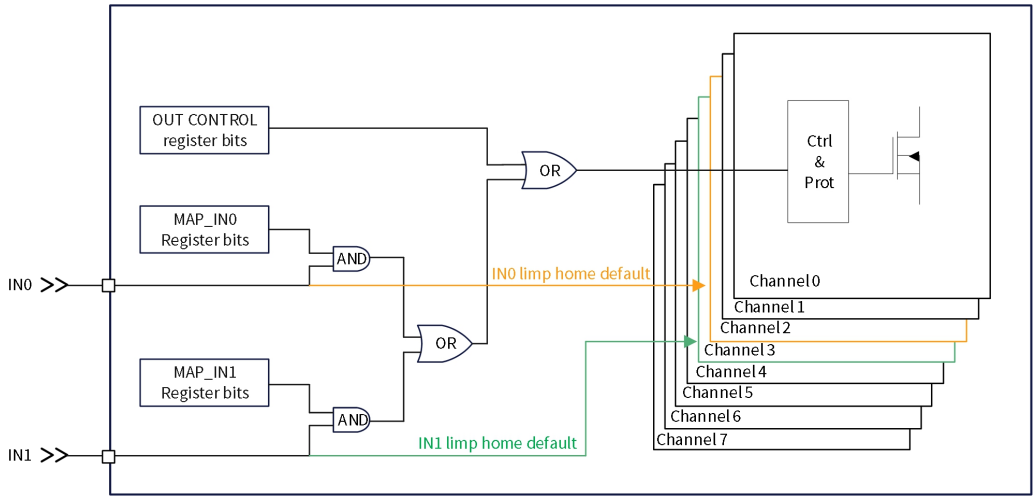


Figure 6.1 Input Mapping

The logic level of the input pins can be monitored via the Input Status Monitor Register (**ISM**). The input status monitor register is also operative and available for SPI read when NSD56008 is in Limp Home mode.

6.2. IDLE pin

The IDLE pin is used to bring the device into Sleep mode or Limp Home mode, depends on the logic combination of IDLE and INx pins. See **Chapter 5.1 Operation Modes** for further details.

To ensure a proper mode transition, IDLE pin must be set for at least $t_{IDLE2SLEEP}$ (IDLE pin transition from “high” to “low”) or $t_{SLEEP2IDLE}$ (IDLE pin transition from “low” to “high”).

After setting the IDLE pin to “low”, the following behavior are as below:

- All registers in the SPI are reset to default values
- If both inputs IN0 & IN1 are also set to “low”, then
  - V_{DD} and V_S Undervoltage detection circuits are disabled to decrease current consumption
  - SPI communication is not available, SDO pin remains in high impedance state

6.3. Electrical Characteristics Control Pins

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDLE pin						
$V_{IDLE(L)}$	Low input level		0		0.8	V
$V_{IDLE(H)}$	High input level		2.0		5.5	V
$I_{IDLE(L)}$	Low input current	V_{IDLE} = 0.8 V	5	12	20	μA
$I_{IDLE(H)}$	High input current	V_{IDLE} = 2.0 V	14	28	45	μA
R_{IDLE}	Idle pin input pull-down resistor			70		kΩ
Input Pins (IN0 & IN1)						
$V_{IN(L)}$	Low input level		0		0.8	V
$V_{IN(H)}$	High input level		2.0		5.5	V
$I_{IN(L)}$	Low input current	V_{IN} = 0.8 V	5	12	20	μA
$I_{IN(H)}$	High input current	V_{IN} = 2.0 V	14	28	45	μA

7. Power Stages

The NSD56008 is an eight channels low-side switch. The power stages are built by N-channel lateral power MOSFET.

$R_{DS(ON)}$ depends on the supply voltage and junction temperature T_J.

7.1. Operating modes

7.1.1. Switching Resistive Loads

In the case of resistive loads switching, refer to the following switching times and slew rates.

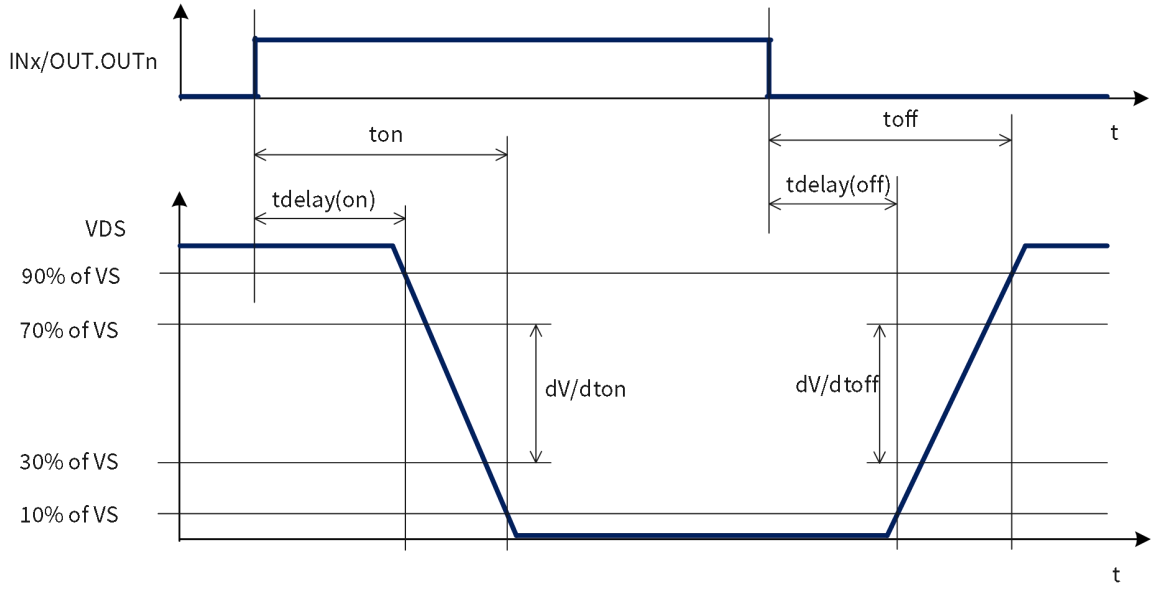


Figure 7.1 Switching ON/OFF timing using resistive Load

7.1.2. Inductive Output Active Clamp

In order to avoid avalanche condition during switching-off an inductive load, the NSD56008 integrates an internal active clamp, which limits the voltage across the output power switch up to $V_{DS(CL)}$.

Figure 7.2 shows a concept drawing of the implementation. The clamping structure protects the device in all operative modes (Sleep, Idle, Active, Limp Home).

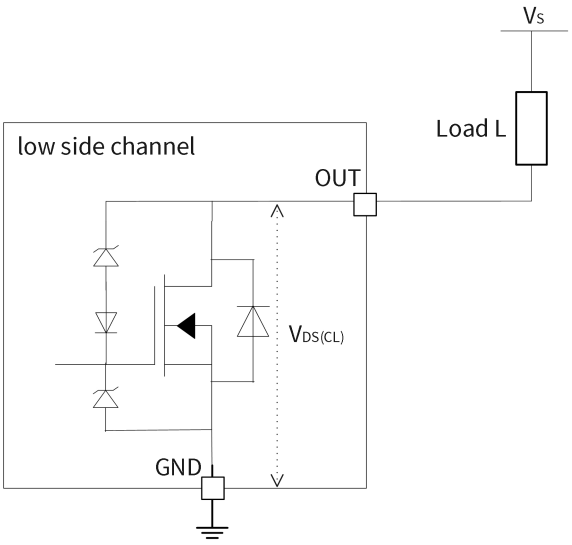


Figure 7.2 Output Clamp concept

7.1.3. Clamping Energy Calculation Method

During demagnetization of inductive loads, energy has to be dissipated in the NSD56008. Equation below shows how to calculate the energy for low-side switches:

$$E = \int (V_{DS} * ID)dt = \int (C1 * C4)dt$$

C1: V_{DS} C4: ID

F1: P=C1*C4=V_{DS}*ID

F2: $E = \int (V_{DS} * ID)dt = \int (C1 * C4)dt$

The maximum energy, which is converted into heat, is limited by the thermal design of the component. The E_{AR} value provided in **Chapter 4 General Product Characteristics** assumes that all channels can dissipate the same energy when the inductances connected to the outputs are demagnetized at the same time.

7.2. Switching Channels in parallel

During switching channels in parallel application, it may happen that the two channels switch OFF not fully synchronously, therefore bringing an additional thermal stress to the channel that switches OFF last. In order to avoid this condition, NSD56008 provides in the SPI registers (bits **HWCR.PAR**) the parallel operation of two neighbor channels. It is possible to synchronize the following couples of channels:

- channel 0 and channel 2 → **HWCR.PAR** (0) set to "1"
- channel 1 and channel 3 → **HWCR.PAR** (1) set to "1"
- channel 4 and channel 6 → **HWCR.PAR** (2) set to "1"
- channel 5 and channel 7 → **HWCR.PAR** (3) set to "1"

When operating in this mode, the fastest channel to react to an Over Load or Over Temperature condition will also deactivate the other of parallel group. The inductive energy that two channels can handle once set in parallel is lower than twice the single channel energy.

Note:

The synchronization bits only influence how the channels react to Over Load or Over Temperature conditions. Synchronized channels ON/OFF have to be controlled by the micro-controller.

7.3. Electrical Characteristics Power Stages

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Characteristics						
$R_{DS(ON)}$	On-State Resistance	T_J = 25 °C		1		Ω
$R_{DS(ON)}$	On-State Resistance	T_J = 150 °C $I_L = I_{L(EAR)}$ = 220 mA		1.5	2	Ω
$I_{L(NOM)}$	Nominal load current (all channels active)	1) T_A = 85 °C, $T_J \leq$ 150 °C		330	500	mA
$I_{L(NOM)}$	Nominal load current (all channels active)	1) T_A = 105 °C, $T_J \leq$ 150 °C		260	500	mA
$I_{L(EAR)}$	Load current for maximum energy dissipation - repetitive (all channels active)	1) T_A = 85 °C, $T_J \leq$ 150 °C		220		mA
E_{AS}	Maximum energy dissipation single pulse	1) T_J = 25 °C, I_L = 2 x $I_{L(EAR)}$			50	mJ
E_{AS}	Maximum energy dissipation single pulse	1) T_J = 150 °C, I_L = 2 x $I_{L(EAR)}$			25	mJ
E_{AR}	Maximum energy dissipation repetitive pulses- $I_{L(EAR)}$	1) T_J = 85 °C, $I_L = I_{L(EAR)}$, $2*10^6$ cycles			10	mJ
E_{AR}	Maximum energy dissipation repetitive pulses- $2*I_{L(EAR)}$ (two channels in parallel)	1) T_J = 85 °C $I_L = 2*I_{L(EAR)}$ $2*10^6$ cycles **HWCR.PAR** = "1" for affected channels			15	mJ
$V_{DS(CL)}$	Drain to Source Output clamping voltage	I_L = 20 mA	42	47	55	V
$I_{L(OFF)}$	Output leakage current (each channel)	V_{IN} = 0 V or floating V_{DS} = 28V **OUT.OUTn** = 0		0.1	5	µA
Timings						
$t_{DELAY(ON)}$	Turn-ON delay, (from INx pin or bit to V_{OUT} = 90% V_S)	R_L = 50 Ω V_S = 13.5V Active mode or Limp Home mode	1	6	12	µs
$t_{DELAY(OFF)}$	Turn-OFF delay, (from INx pin or bit to V_{OUT} = 10% V_S)	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	1	9	16	µs
t_{ON}	Turn-ON time, (from INx pin or bit to V_{OUT} = 10% V_S)	R_L = 50 Ω V_S = 13.5 V	6	17	35	µs

		Active mode or Limp Home mode				
t_{OFF}	Turn-OFF time, (from INx pin or bit to V_{OUT} = 90% V_S)	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	6	20	35	µs
dV/dt_{ON}	Turn-ON slew rate, V_{DS} = 70% to 30% V_S	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	0.7	1.1	1.8	V/µs
$-dV/dt_{OFF}$	Turn-OFF slew rate, V_{DS} = 30% to 70% V_S	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	0.7	1.1	1.8	V/µs

1) Not subject to production test, specified by design

8. Protection Functions

8.1. Over Load Protection

The device has two different overload current thresholds that preserve itself in case of overload or short-circuit of the load (see **Figure 8.1**):

- $I_{L(OVL0)}$ between channel switch ON and t_{OVLIN}
- $I_{L(OVL1)}$ after t_{OVLIN}

Every time the channel is switched OFF, the over load current threshold is set back to $I_{L(OVL0)}$

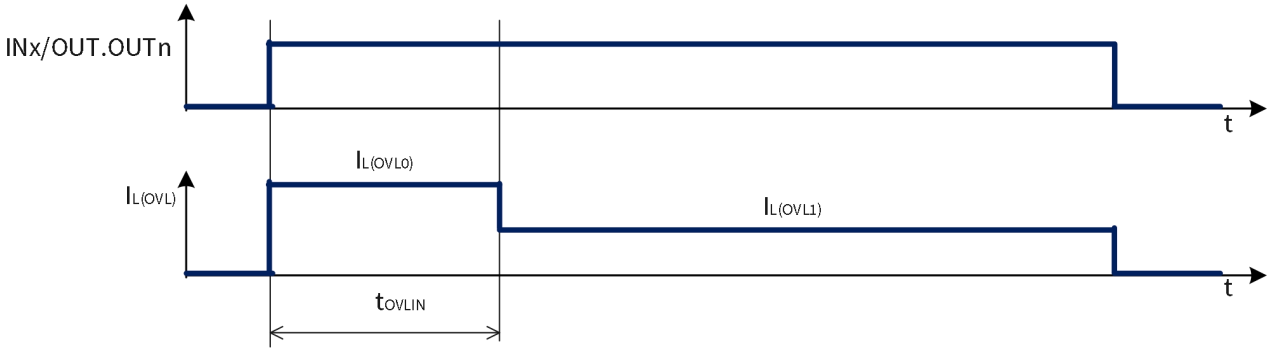


Figure 8.1 Over Load current thresholds

In case the load current is higher than $I_{L(OVL0)}$ or $I_{L(OVL1)}$ and $t_{OFF(OVL)}$ elapsed, the over loaded channel is switched OFF and the corresponding diagnosis bit **ERRn** is set.

The channel can be switched ON after clearing the protection latch by setting the corresponding **COEL.OUTn** bit to "1". This bit is automatically set back to "0" internally after clearing latching status of the channel. Please refer to **Figure 8.2** for details.

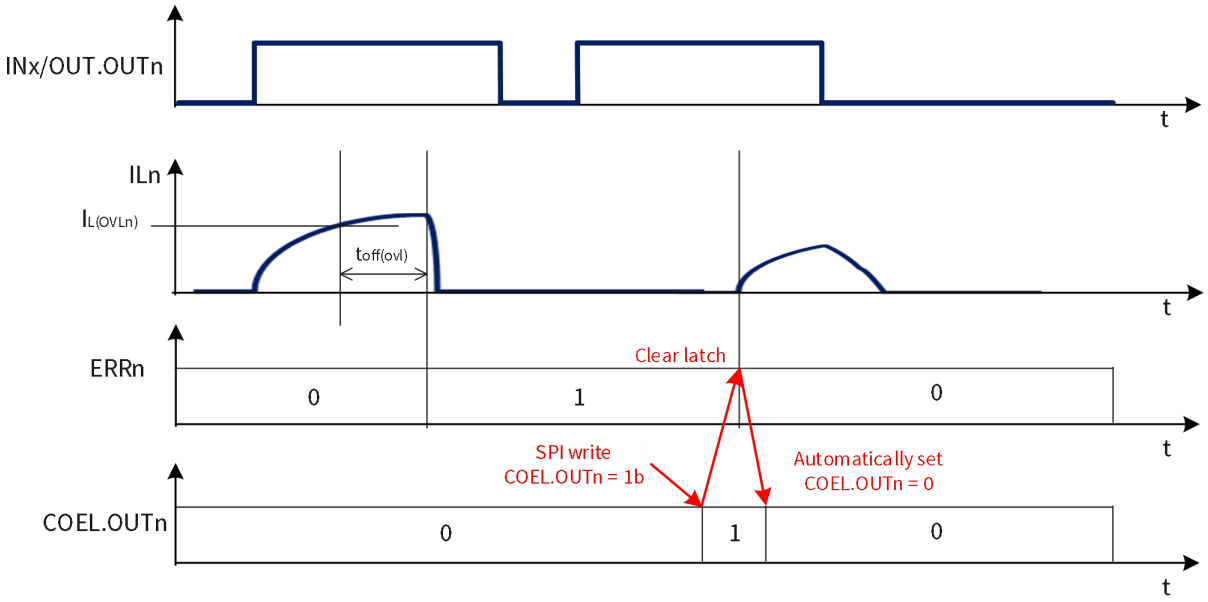


Figure 8.2 Latch OFF at Over Load

8.2. Over Temperature Protection

A temperature sensor is integrated for each channel, which switch off the channel in over temperature in order to prevent output stage overheat.

Once the temperature increases above the $T_{J(SC)}$ The according diagnosis bit **ERRn** is set (combined with Over Load protection). The channel can be switched ON after clearing the protection latch by setting the corresponding **COEL.OUTn** bit to “1”. This bit is set back to “0” internally after de-latching the channel.

8.3. Over Temperature and Over Load Protection in Limp Home mode

In limp-home mode, through the input pin IN0 and IN1, the channels 2 and 3 can be switched on. In case of overload, short-circuit or overtemperature the channels are switched off.

In the meanwhile, NSD56008 provides auto-retry mechanism If the input pins remain “high” in limp home mode, the channels restart with the following timings (See **Figure 8.3** for details):

- 9 ms (first 8 retries)
- 18 ms (following 8 retries)
- 35 ms (following 8 retries)
- 70 ms (as long as the input pin remains “high” and the error is still present)

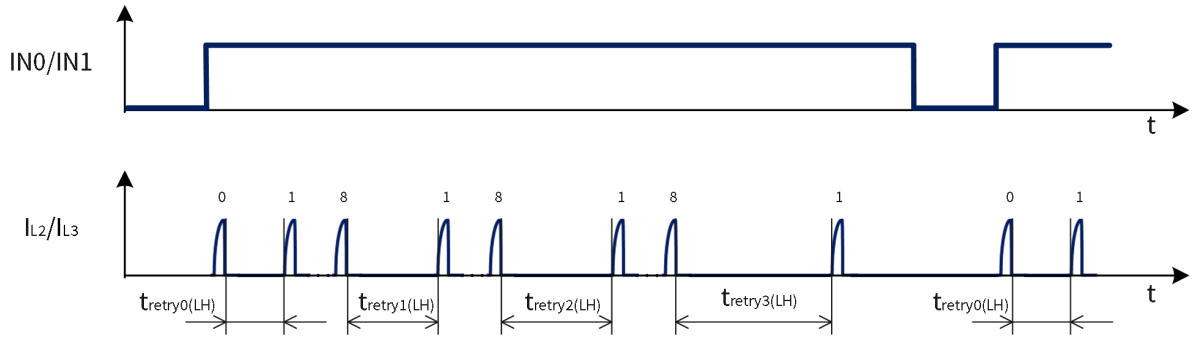


Figure 8.3 Restart timer in Limp Home mode

Note:

Every time the input pin is set to “low”, the restart timer is reset. And the timer starts from 10 ms again for the next over temperature / load protection while in Limp Home mode

8.4. Reverse Polarity Protection

There is no reverse polarity protection function in VS pin. A reverse protection diode or ideal diode is must added before VS pin.

For low side, the reverse current through the channels is limited by the connected loads, so there is no need to add reverse protection diode or ideal diode before them.

See **Figure 3.1** Application Diagram for details.

8.5. Electrical Characteristics Protection

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Over Load						
$I_{L(OVL0)}$	Over Load detection current	T_J = -40 °C	1.3	1.7	2.3	A
$I_{L(OVL0)}$	Over Load detection current	T_J = 25 °C	1.25	1.6	2.3	A
$I_{L(OVL0)}$	Over Load detection current	T_J = 150 °C	1	1.5	2	A
$I_{L(OVL1)}$	Over Load detection current	T_J = -40 °C	0.7	1	1.3	A
$I_{L(OVL1)}$	Over Load detection current	T_J = 25 °C	0.65	0.9	1.3	A
$I_{L(OVL1)}$	Over Load detection current	T_J = 150 °C	0.5	0.85	1.25	A
t_{OVLIN}	Over Load threshold switch delay time	Guaranteed by digital SCAN	80	170	270	µs
$t_{OFF(OVL)}$	Over Load shut-down delay time		2	7	11	µs
Over Temperature						
$T_{J(SC)}$	Thermal shut-down temperature	1)	150	175	195	°C
Reverse Polarity						
$V_{DS(REV)}$	Drain Source diode during reverse polarity	I_L = -10 mA Sleep mode		650		mV
Timings						
$t_{RETRY0(LH)}$	Restart time in Limp Home mode	1) Guaranteed by digital SCAN	6	9	12	ms
$t_{RETRY1(LH)}$	Restart time in Limp Home mode	1) Guaranteed by digital SCAN	12	18	24	ms
$t_{RETRY2(LH)}$	Restart time in Limp Home mode	1) Guaranteed by digital SCAN	23	35	47	ms
$t_{RETRY3(LH)}$	Restart time in Limp Home mode	1) Guaranteed by digital SCAN	46	70	94	ms

1) Not subject to production test, specified by design

9. Diagnosis

The SPI communication provides diagnosis information about the device and the load status. Diagnosis information of each channel is independent from other channels. An error condition on one channel has no influence on the diagnostic of other channels in the device (unless two neighbor channels are configured to work in parallel, see **Chapter 7.2** for more details).

9.1. Over Load and Over Temperature

When either an Over Load or an Over Temperature occurs on one channel, the diagnosis bit **ERRn** is set accordingly. The channel latches OFF and must be reactivated setting corresponding **COEL.OUTn** bit to "1".

9.2. Output Status Monitor

To monitor the output pin and load status, the device integrates dedicated voltage comparator for each channel. It compares VDS with VDS(OL) and sets the corresponding **DIAG_OSM.OUTn** bits accordingly, based on the below logic.

$V_{DS} < V_{DS(OL)} \rightarrow$ **DIAG_OSM.OUTn**= "1"

The bits are updated every time **DIAG_OSM** register is read.

Additionally, a diagnosis current IOL in parallel to the power switch can be enabled by programming the **DIAG_IOL.OUTn** bit. With I_{OL} enabled and power switch OFF, open Load in OFF state can be detected when **DIAG_OSM.OUTn**= "1".

Note:

1. *If the diagnosis current I_{OL} is enabled or if the channel changes state (ON → OFF or OFF → ON), it is necessary to wait a time t_{OSM} for a reliable diagnosis.*
2. *Due to output status monitor checks the voltage level at the outputs in real time, for Open Load in OFF diagnostic, it is necessary to read DIAG_OSM register after the channels switch off.*
3. *In Standard Diagnosis the bit OLOFF represents the OR combination of all DIAG_OSM.OUTn bits for all channels in OFF state which have the corresponding current source I_{OL} activated*
4. *Enabling I_{OL} current sources increases the current consumption of the device.*
5. *Even if an Open Load is detected, the channel is not latched OFF.*

Output Status Monitor diagnostic is available when $V_S = V_{S(NOR)}$ and $V_{DD} \geq V_{DD(UV)}$.

See **Figure 9.1** for DIAG_OSM timing overview and **Figure 9.2** for DIAG_OSM internal structure

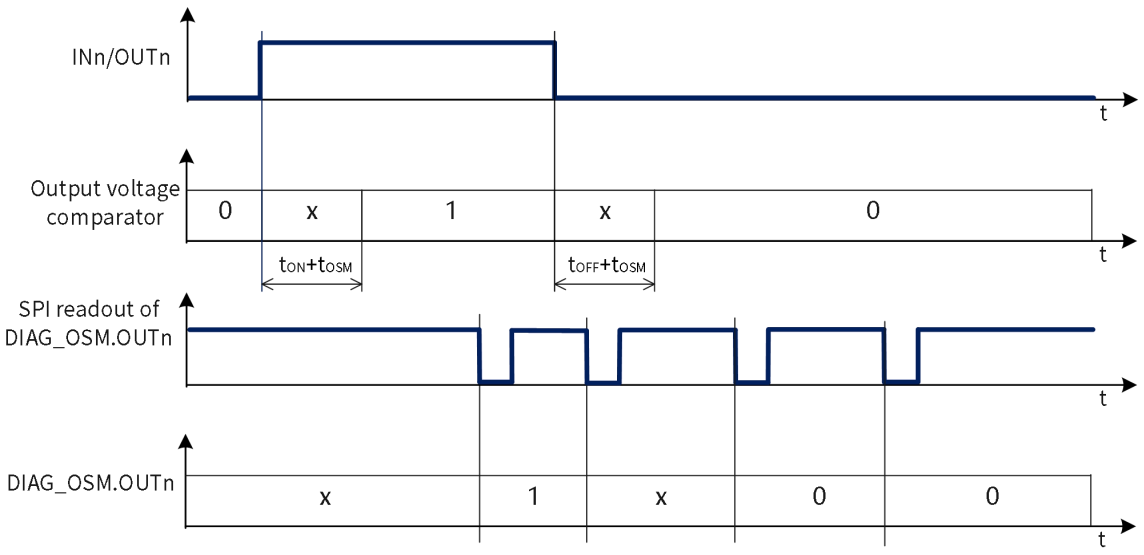


Figure 9.1 Output Status Monitor timing

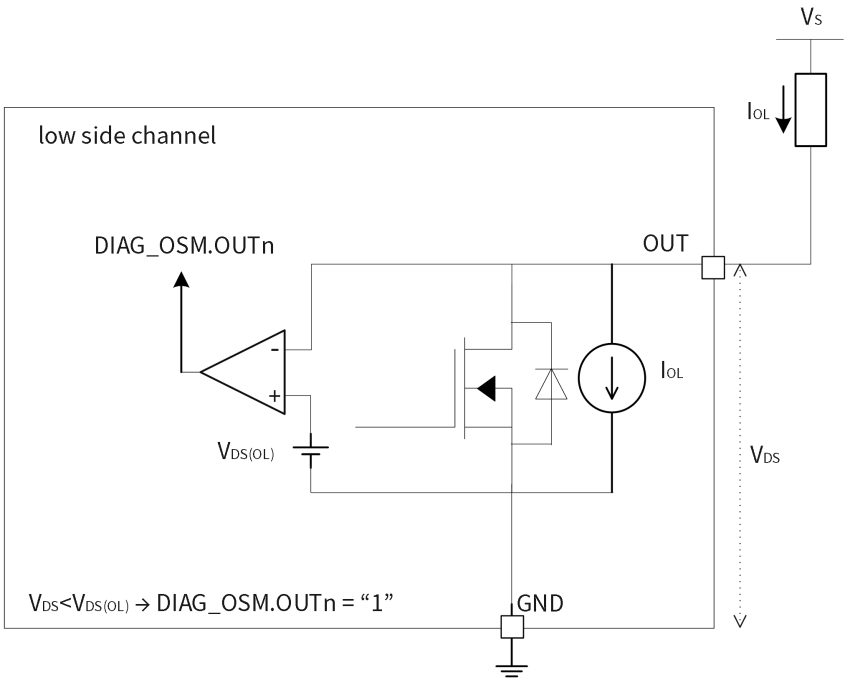


Figure 9.2 Output Status Monitor - concept

9.3. Electrical Characteristics Diagnosis

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Status Monitor						
t_{OSM}	Output Status Monitor comparator settling time	1)			20	µs
$V_{DS(OL)}$	Output Status Monitor threshold voltage		2.9	3.3	3.7	V
I_{OL}	Output diagnosis current	V_{DS} = 3.3 V	65	85	105	µA
R_{OL}	Open Load equivalent resistance	1) Application information	30		300	kΩ

1) Not subject to production test, specified by design

10. Serial Peripheral Interface (SPI)

The SPI version of the device has full duplex, 4-wire synchronous communication. This section describes the SPI protocol, the command structure, and the control and status registers. The device can be connected with the MCU in the following configurations:

- One slave device
- Multiple slave devices in parallel connection
- Multiple slave devices in series (daisy chain) connection

The falling edge of NCS indicates the beginning of an access. Data is sampled in on line SDI at the falling edge of SCLK and shifted out on line SDO at the rising edge of SCLK. Each access must be terminated by a rising edge of NCS.

A modulo 8/16 counter ensures that data is taken only when a multiple of 8 bits has been transferred after the first 16 bits. Otherwise a **TER** bit is asserted. In this way the interface provides daisy chain capability with 16 bits as well as with 8 bits SPI devices.

10.1. SPI for a Single Slave Device

NCS - Chip Select: Whenever the pin is in “low” state, Data transfer can take place, when the pin is in “low” state. Any signals at the SCLK and SDI pins are ignored when NCS is in "high" state and SDO is forced into a high impedance state.

NCS “high” to “low” Transition:

- The requested information is transferred into the shift register.
- SDO changes from high impedance state to "high" or “low” state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SDI. This allows to detect a faulty transmission even in daisy chain configuration.
- If the device is in Sleep mode, SDO pin remains in high impedance state and no SPI transmission occurs.

NCS “low” to "high" Transition:

- Command decoding is only done, when after the falling edge of NCS exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected after the first 16 SCLK pulses. In case of faulty transmission, the transmission error bit (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock: This input pin clocks the internal shift register. The serial input (SDI) transfers data into the shift register on the falling edge of SCLK while the serial output (SDO) shifts date out on the rising edge of the serial clock. It is essential that the SCLK pin is in “low” state whenever chip select NCS makes any transition, otherwise the command may be not accepted.

SDI - Serial Input: Serial input data bits are shift-in at this pin, MSB first. SDI information is read on the falling edge of SCLK.

SDO Serial Output: Data is shifted out serially at this pin, MSB first. SDO is in high impedance state until the NCS pin goes to “low” state. New data appears at the SDO pin following the rising edge of SCLK.

10.2. Parallel and daisy chain capability

SPI communication between microcontroller (SPI master) and multiple these devices (slave) can be operated in parallel or in daisy chain.

Parallel operation: several slave devices are connected to one SPI channel, which share communication lines SDI, SDO and SCLK, but every slave connects dedicated own NCS.

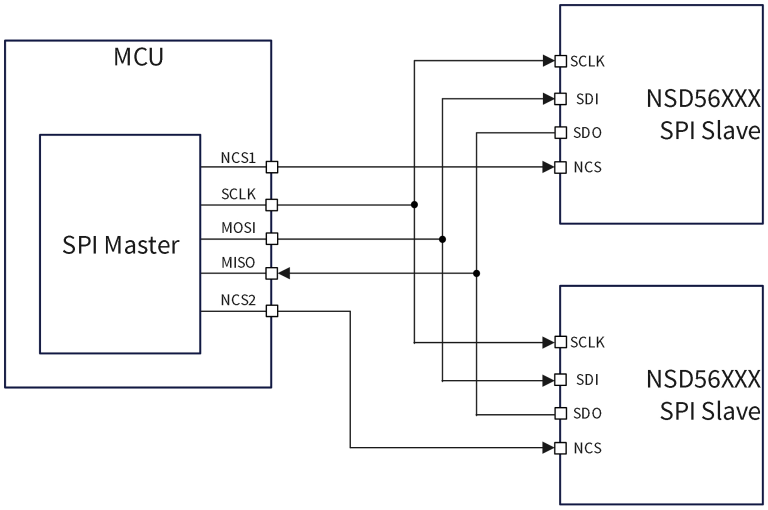


Figure 10.1 Parallel Configuration

Daisy chain operation: multi devices are connected with shared one NCS and SCLK, while each device SDI and SDO are daisy-chain connected. An example of 3 devices in daisy chain as below **Figure 10.2**:

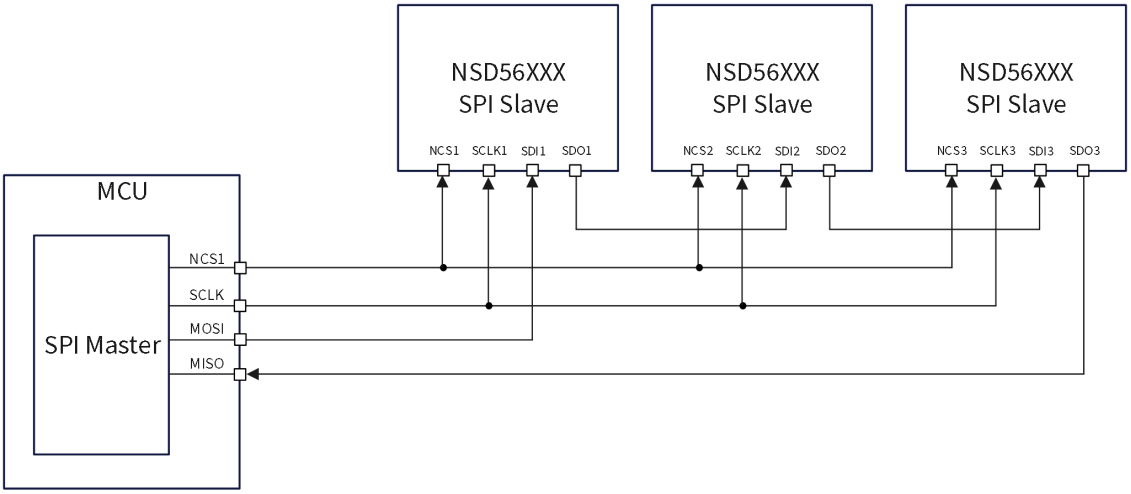


Figure 10.2 Daisy Chain Configuration

The NCS line must turn “high” to make the device acknowledge the transferred data in single chip configuration. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, several multiples of 8 bits have to be shifted through the devices. After that, the NCS line must turn “high”.

10.3. Timing Diagrams

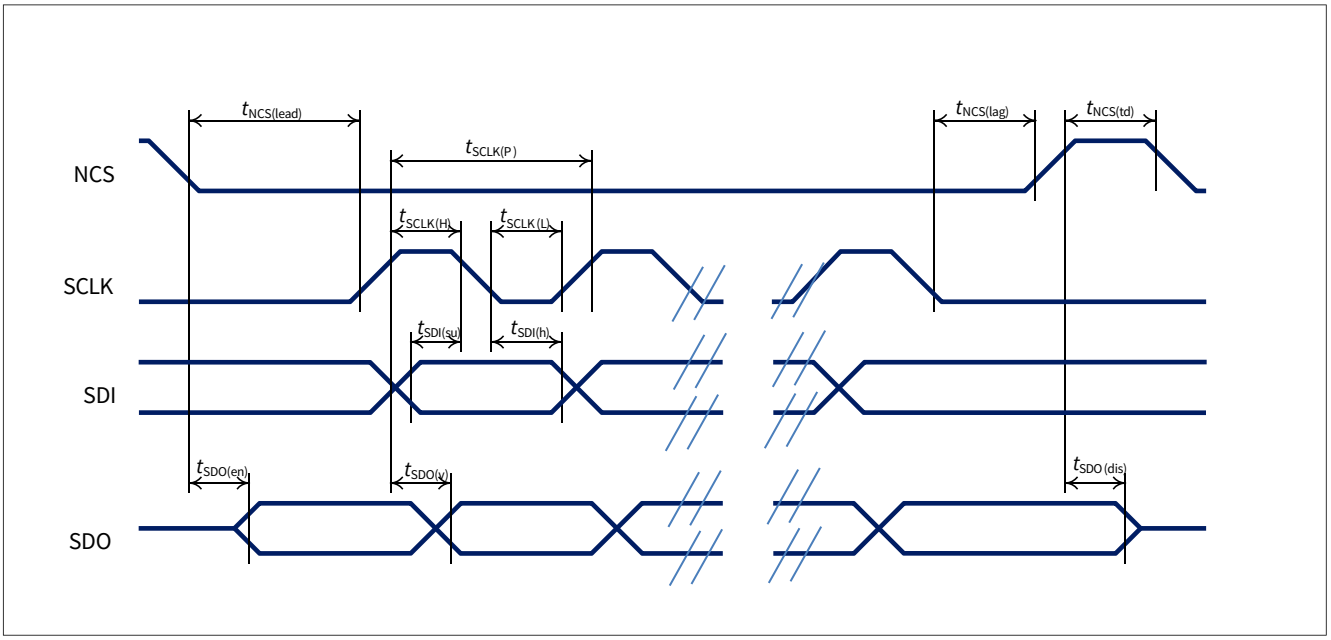


Figure 10.3 Timing Diagram SPI Access

10.4. Electrical Characteristics

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified). Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Characteristics (NCS, SCLK, SDI) - "low" level of pin						
$V_{NCS(L)}$	NCS		0		0.8	V
$V_{SCLK(L)}$	SCLK		0		0.8	V
$V_{SDI(L)}$	SDI		0		0.8	V
Input Characteristics (NCS, SCLK, SDI) - "high" level of pin						
$V_{NCS(H)}$	NCS		2		V_{DD}	V
$V_{SCLK(H)}$	SCLK		2		V_{DD}	V
$V_{SDI(H)}$	SDI		2		V_{DD}	V
Output Characteristics (SDO)						
$V_{SDO(L)}$	L level output voltage	I_{SDO} = -1.5 mA	0		0.4	V
$V_{SDO(H)}$	H level output voltage	I_{SDO} = 1.5 mA	V_{DD} - 0.4		V_{DD}	V
Timings						
$t_{NCS(lead)}$	Enable lead time (falling NCS to rising SCLK)	1) $V_{DD} \geq 3$ V	200			ns
$t_{NCS(lag)}$	Enable lag time (falling SCLK to rising NCS)	1) $V_{DD} \geq 3$ V	200			ns
$t_{NCS(td)}$	Transfer delay time (rising NCS to falling NCS)	1) $V_{DD} \geq 3$ V	250			ns
$t_{SDO(en)}$	Output enable time (falling NCS to SDO valid)	1) $V_{DD} \geq 3$ V C_L = 20 pF at SDO pin			200	ns
$t_{SDO(dis)}$	Output disable time (rising NCS to SDO tristate)	1) $V_{DD} \geq 3$ V C_L = 20 pF at SDO pin			200	ns
f_{SCLK}	Serial clock frequency	1) $V_{DD} \geq 3$ V			5	MHz
$t_{SCLK(P)}$	Serial clock period	1) $V_{DD} \geq 3$ V	200			ns
$t_{SCLK(H)}$	Serial clock "high" time	1) $V_{DD} \geq 3$ V	75			ns
$t_{SCLK(L)}$	Serial clock "low" time	1) $V_{DD} \geq 3$ V	75			ns
$t_{SDI(su)}$	Data setup time (required time SDI to falling SCLK)	1) $V_{DD} \geq 3$ V	20			ns
$t_{SDI(h)}$	Data hold time (falling SCLK to SDI)	1) $V_{DD} \geq 3$ V	20			ns
$t_{SDO(v)}$	Output data valid time with capacitive load	1) $V_{DD} \geq 3$ V C_L = 20 pF at SDO pin			100	ns

1) Not subject to production test, specified by design

10.5. SPI Protocol

The relationship between SDI and SDO content during SPI communication is shown in **Figure 10.4**.

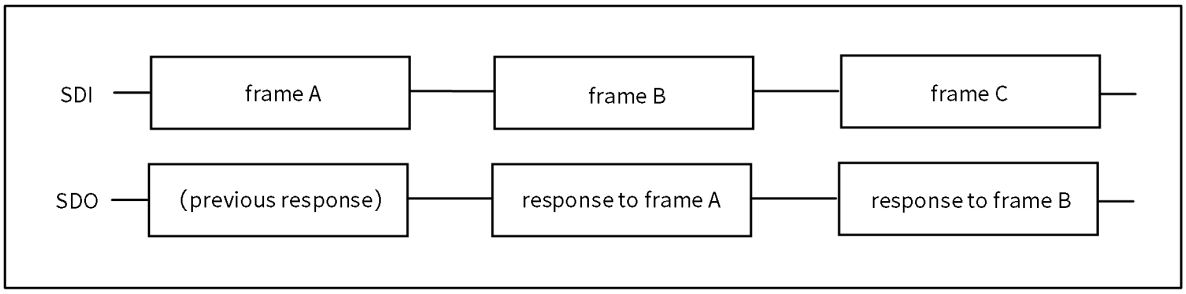


Figure 10.4 Relationship between SDI and SDO during SPI communication

The SPI protocol provides the answer to a command frame only with the next transmission triggered by the MCU.

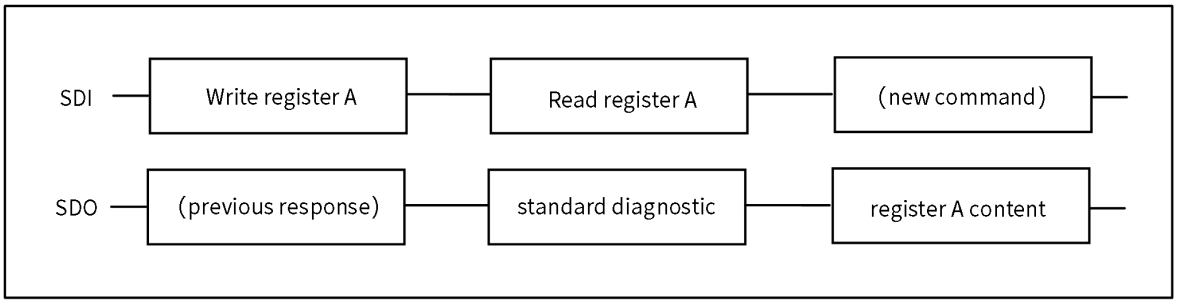


Figure 10.5 Register content sent back to µC

There are 3 special situations where the frame sent back to the µC is not related directly to the previous received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8 with a minimum of 16 bits), shown in **Figure 10.6**
- when NSD56008 logic supply comes out of Power-On reset condition or after a Software Reset, as shown in **Figure 10.7**
- in case of command syntax errors
  - "write" command starting with "11" instead of "10"
  - "read" command starting with "00" instead of "01"
  - "read" or "write" commands on registers which are "reserved" or "not used"

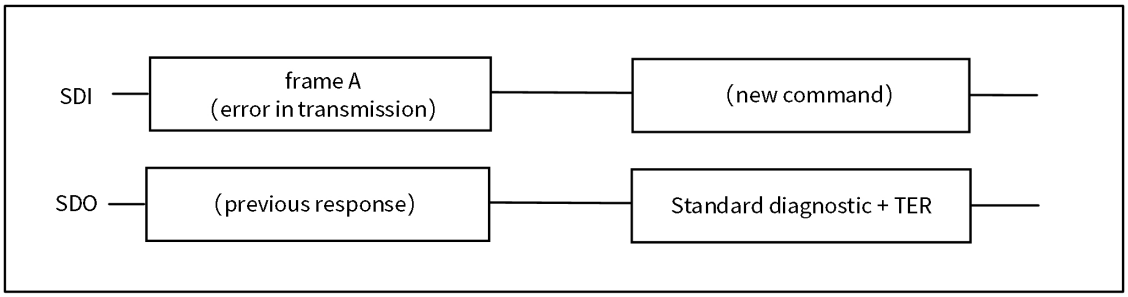


Figure 10.6 NSD56008 response after an error in transmission

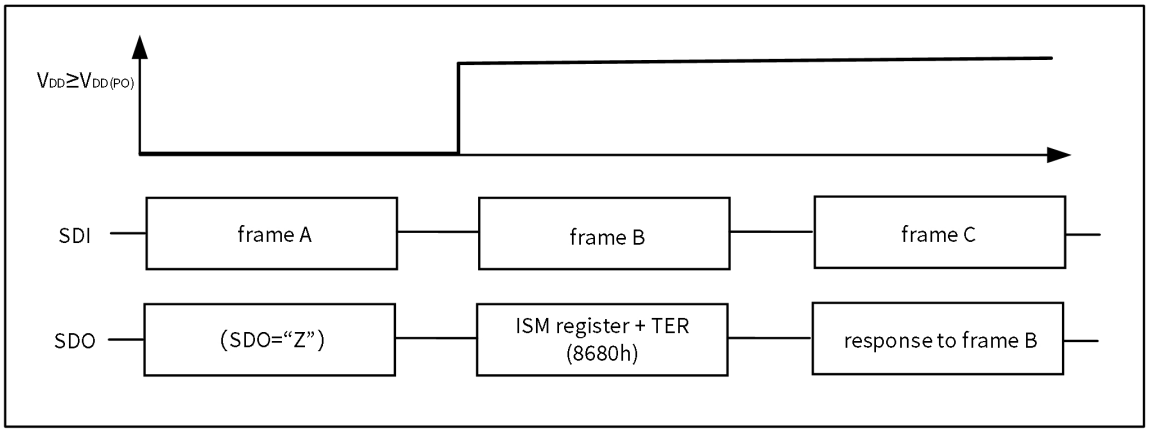


Figure 10.7 NSD56008 response after coming out of Power-On reset at VDD

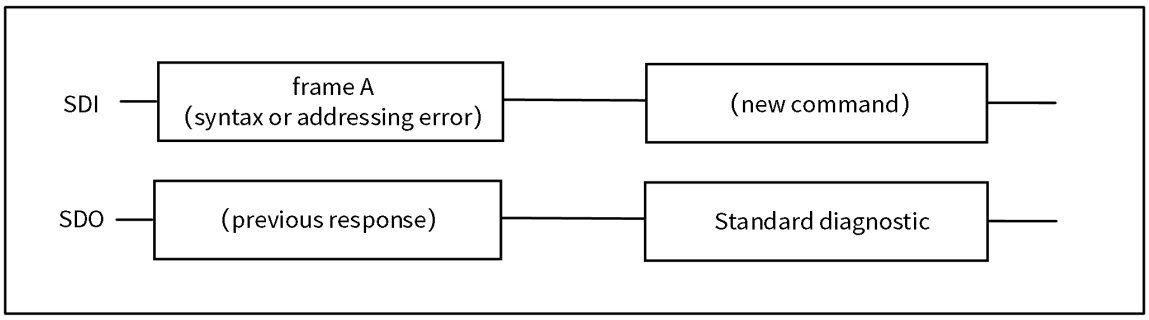


Figure 10.8 NSD56008 response after a command syntax error

A summary of all possible SPI commands is presented in **Table 10.1**, including the answer that NSD56008 sends back at the next transmission.

Table 10.1 SPI Command summary[1)]

Requested Operation	Frame sent to device (SDI pin)	Frame received from device (SDO pin) with the next command
Read Standard Diagnosis	0xxxxxxxxxxxxx01$_B$ ("xxxxxxxxxxxx$_B$" = don´t care)	0ddddddddddddddd$_B$ (Standard Diagnosis)
Write 8-bit register	10aaaabbcccccccc$_B$ where: "aaaa$_B$" = register address ADDR0 "bb$_B$" = register address ADDR1 "cccccccc$_B$" = new register content	0ddddddddddddddd$_B$ (Standard Diagnosis)
Read 8-bit registers	01aaaabbxxxxxx10$_B$ where: "aaaa$_B$" = register address ADDR0 "bb$_B$" = register address ADDR1 "xxxxxx$_B$" = don´t care	10aaaabbcccccccc$_B$ where: "aaaa$_B$" = register address ADDR0 "bb$_B$" = register address ADDR1 "cccccccc$_B$" = register content

1) " a" = address bits for ADDR0 field, "b" = address bit for ADDR1 field, "c" = register content, "d" = diagnostic bit

10.6. SPI Registers Overview

10.6.1. Standard Diagnosis

Table 10.2 Standard Diagnosis register[1)]

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field Name	0	VSUV	LOPVDD	MODE		TER	0	OLOFF	ERR							
Default	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

1) Default value is 7800_H

Table 10.3 Standard Diagnosis register description

Bit	Field Name	Type	Description
15	Reserved	r	0: reserved (default value)
14	VSUV	r	V_S Undervoltage Monitor 0: No undervoltage condition on V_S detected 1: (default) There was at least one V_S Undervoltage condition since last Standard Diagnosis readout
13	LOPVDD	r	VDD Lower Operating Range Monitor 0: V_{DD} is above $V_{DD(LOP)}$ 1: (default) There was at least one "V_{DD} = $V_{DD(LOP)}$" condition since last Standard Diagnosis readout
12:11	MODE	r	Operative Mode Monitor 00: (reserved) 01: Limp Home Mode 10: Active Mode 11: (default) Idle Mode
10	TER	r	Transmission Error 0: Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1: (default) Previous transmission failed The first frame after a reset is **TER** set to "high" and the **ISM** register. The second frame is the Standard Diagnosis with **TER** set to "low" (if there was no fail in the previous transmission).
9	Reserved	r	0: reserved (default value)
8	OLOFF	r	Open Load in OFF Diagnosis 0: (default) All channels in OFF state (which have **DIAG_IOL.OUTn** bit set to "1") have VDS > VDS(OL) 1: At least one channel in OFF state (with **DIAG_IOL.OUTn** bit set to "1") has VDS < VDS(OL) Channels in ON state are not considered
7	ERR7	r	Over Load / Over Temperature Diagnosis of channel 7 0: (default) No failure detected 1: Over Temperature or Over Load
6	ERR6	r	Over Load / Over Temperature Diagnosis of channel 6 0: (default) No failure detected 1: Over Temperature or Over Load
5	ERR5	r	Over Load / Over Temperature Diagnosis of channel 5

			0: (default) No failure detected 1: Over Temperature or Over Load
4	ERR4	r	Over Load / Over Temperature Diagnosis of channel 4 0: (default) No failure detected 1: Over Temperature or Over Load
3	ERR3	r	Over Load / Over Temperature Diagnosis of channel 3 0: (default) No failure detected 1: Over Temperature or Over Load
2	ERR2	r	Over Load / Over Temperature Diagnosis of channel 2 0: (default) No failure detected 1: Over Temperature or Over Load
1	ERR1	r	Over Load / Over Temperature Diagnosis of channel 1 0: (default) No failure detected 1: Over Temperature or Over Load
0	ERR0	r	Over Load / Over Temperature Diagnosis of channel 0 0: (default) No failure detected 1: Over Temperature or Over Load

10.6.2. Register structure

The register banks the digital part have following structure:

Table 10.4 Register structure - all registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field Name	r = 0 w = 1	r = 1 w = 0	ADDR						DATA							
			ADDR0				ADDR1									

Table 10.5 Power output control register (REG_ADDR = 0x00) -OUT

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	OUT.OUT7	OUT.OUT6	OUT.OUT5	OUT.OUT4	OUT.OUT3	OUT.OUT2	OUT.OUT1	OUT.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.6 Power output control register description

Bit	Field Name	Type	Description
7	OUT.OUT7	r/w	0: (default) Channel 7 output is OFF 1: Channel 7 output is ON
6	OUT.OUT6	r/w	0: (default) Channel 6 output is OFF 1: Channel 6 output is ON
5	OUT.OUT5	r/w	0: (default) Channel 5 output is OFF 1: Channel 5 output is ON
4	OUT.OUT4	r/w	0: (default) Channel 4 output is OFF 1: Channel 4 output is ON
3	OUT.OUT3	r/w	0: (default) Channel 3 output is OFF

			1: Channel 3 output is ON
2	OUT.OUT2	r/w	0: (default) Channel 2 output is OFF 1: Channel 2 output is ON
1	OUT.OUT1	r/w	0: (default) Channel 1 output is OFF 1: Channel 1 output is ON
0	OUT.OUT0	r/w	0: (default) Channel 0 output is OFF 1: Channel 0 output is ON

Table 10.7 Input Mapping (Input Pin 0) register (REG_ADDR = 0x04) -MAPIN0

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	MAPIN0.OUT7	MAPIN0.OUT6	MAPIN0.OUT5	MAPIN0.OUT4	MAPIN0.OUT3	MAPIN0.OUT2	MAPIN0.OUT1	MAPIN0.OUT0
Default	0	0	0	0	0	1	0	0

Table 10.8 Input Mapping (Input Pin 0) register description

Bit	Field Name	Type	Description
7	MAPIN0.OUT7	r/w	0: (default) Channel 7 output is not connected to the IN0 1: Channel 7 output is connected to the IN0
6	MAPIN0.OUT6	r/w	0: (default) Channel 6 output is not connected to the IN0 1: Channel 6 output is connected to the IN0
5	MAPIN0.OUT5	r/w	0: (default) Channel 5 output is not connected to the IN0 1: Channel 5 output is connected to the IN0
4	MAPIN0.OUT4	r/w	0: (default) Channel 4 output is not connected to the IN0 1: Channel 4 output is connected to the IN0
3	MAPIN0.OUT3	r/w	0: (default) Channel 3 output is not connected to the IN0 1: Channel 3 output is connected to the IN0
2	MAPIN0.OUT2	r/w	0: Channel 2 output is not connected to the IN0 1: (default) Channel 2 output is connected to the IN0
1	MAPIN0.OUT1	r/w	0: (default) Channel 1 output is not connected to the IN0 1: Channel 1 output is connected to the IN0
0	MAPIN0.OUT0	r/w	0: (default) Channel 0 output is not connected to the IN0 1: Channel 0 output is connected to the IN0

Table 10.9 Input Mapping (Input Pin 1) register (REG_ADDR = 0x05) -MAPIN1

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	MAPIN1.OUT7	MAPIN1.OUT6	MAPIN1.OUT5	MAPIN1.OUT4	MAPIN1.OUT3	MAPIN1.OUT2	MAPIN1.OUT1	MAPIN1.OUT0
Default	0	0	0	0	1	0	0	0

Table 10.10 Input Mapping (Input Pin 1) register description

Bit	Field Name	Type	Description
7	MAPIN1.OUT7	r/w	0: (default) Channel 7 output is not connected to the IN1 1: Channel 7 output is connected to the IN1
6	MAPIN1.OUT6	r/w	0: (default) Channel 6 output is not connected to the IN1 1: Channel 6 output is connected to the IN1
5	MAPIN1.OUT5	r/w	0: (default) Channel 5 output is not connected to the IN1 1: Channel 5 output is connected to the IN1
4	MAPIN1.OUT4	r/w	0: (default) Channel 4 output is not connected to the IN1 1: Channel 4 output is connected to the IN1
3	MAPIN1.OUT3	r/w	0: Channel 3 output is not connected to the IN1 1: (default) Channel 3 output is connected to the IN1
2	MAPIN1.OUT2	r/w	0: (default) Channel 2 output is not connected to the IN1 1: Channel 2 output is connected to the IN1
1	MAPIN1.OUT1	r/w	0: (default) Channel 1 output is not connected to the IN1 1: Channel 1 output is connected to the IN1
0	MAPIN1.OUT0	r/w	0: (default) Channel 0 output is not connected to the IN1 1: Channel 0 output is connected to the IN1

Table 10.11 Input Status Monitor register (REG_ADDR = 0x06) -ISM

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TER	reserved	reserved	reserved	reserved	reserved	IN1	IN0
Default	1	0	0	0	0	0	0	0

Table 10.12 Input Status Monitor register description

Bit	Field Name	Type	Description
7	TER	r	0: Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1: (default) Previous transmission failed
6	reserved	r	0: reserved (default value)
5	reserved	r	0: reserved (default value)
4	reserved	r	0: reserved (default value)
3	reserved	r	0: reserved (default value)
2	reserved	r	0: reserved (default value)
1	IN1	r	0: (default) The input pin is set to “low” 1: The input pin is set to “high”
0	IN0	r	0: (default) The input pin is set to “low” 1: The input pin is set to “high”

Table 10.13 Open Load diagnostic current control register (REG_ADDR = 0x08) -DIAG_IOL

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	IOL.OUT7	IOL.OUT6	IOL.OUT5	IOL.OUT4	IOL.OUT3	IOL.OUT2	IOL.OUT1	IOL.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.14 Open Load diagnostic current control register description

Bit	Field Name	Type	Description
7	IOL.OUT7	r/w	0: (default) Channel7 diagnosis current not enabled 1: Channel7 diagnosis current enabled
6	IOL.OUT6	r/w	0: (default) Channel6 diagnosis current not enabled 1: Channel6 diagnosis current enabled
5	IOL.OUT5	r/w	0: (default) Channel5 diagnosis current not enabled 1: Channel5 diagnosis current enabled
4	IOL.OUT4	r/w	0: (default) Channel4 diagnosis current not enabled 1: Channel4 diagnosis current enabled
3	IOL.OUT3	r/w	0: (default) Channel3 diagnosis current not enabled 1: Channel3 diagnosis current enabled
2	IOL.OUT2	r/w	0: (default) Channel2 diagnosis current not enabled 1: Channel2 diagnosis current enabled
1	IOL.OUT1	r/w	0: (default) Channel1 diagnosis current not enabled 1: Channel1 diagnosis current enabled
0	IOL.OUT0	r/w	0: (default) Channel0 diagnosis current not enabled 1: Channel0 diagnosis current enabled

Table 10.15 Output Status Monitor register (REG_ADDR = 0x09) -DIAG_OSM

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DIAG_OSM. OUT7	DIAG_OSM. OUT6	DIAG_OSM. OUT5	DIAG_OSM. OUT4	DIAG_OSM. OUT3	DIAG_OSM. OUT2	DIAG_OSM. OUT1	DIAG_OSM. OUT0
Default	0	0	0	0	0	0	0	0

Table 10.16 Output Status Monitor register description

Bit	Field Name	Type	Description
7	DIAG_OSM.OUT7	r	0: (default) Channel 7 $V_{DS} > V_{DS(OL)}$ 1: Channel 7 $V_{DS} < V_{DS(OL)}$
6	DIAG_OSM.OUT6	r	0: (default) Channel 6 $V_{DS} > V_{DS(OL)}$ 1: Channel 6 $V_{DS} < V_{DS(OL)}$
5	DIAG_OSM.OUT5	r	0: (default) Channel 5 $V_{DS} > V_{DS(OL)}$ 1: Channel 5 $V_{DS} < V_{DS(OL)}$
4	DIAG_OSM.OUT4	r	0: (default) Channel 4 $V_{DS} > V_{DS(OL)}$ 1: Channel 4 $V_{DS} < V_{DS(OL)}$
3	DIAG_OSM.OUT3	r	0: (default) Channel 3 $V_{DS} > V_{DS(OL)}$ 1: Channel 3 $V_{DS} < V_{DS(OL)}$
2	DIAG_OSM.OUT2	r	0: (default) Channel 2 $V_{DS} > V_{DS(OL)}$ 1: Channel 2 $V_{DS} < V_{DS(OL)}$
1	DIAG_OSM.OUT1	r	0: (default) Channel 1 $V_{DS} > V_{DS(OL)}$ 1: Channel 1 $V_{DS} < V_{DS(OL)}$
0	DIAG_OSM.OUT0	r	0: (default) Channel 0 $V_{DS} > V_{DS(OL)}$ 1: Channel 0 $V_{DS} < V_{DS(OL)}$

Table 10.17 Hardware Configuration Register (REG_ADDR = 0x0C) -HWCR

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	ACT	RST	reserved	reserved	PAR3	PAR2	PAR1	PAR0
Default	0	0	0	0	0	0	0	0

Table 10.18 Hardware Configuration Register description

Bit	Field Name	Type	Description
7	ACT	r/w	0: (default) Normal operation or device leaves Active Mode 1: Device enters Active Mode
6	RST	r/w	0: (default) Normal operation 1: Execute Reset command (self-clearing)
5	reserved	r/w	0: reserved (default value)
4	reserved	r/w	0: reserved (default value)
3	PAR3	r/w	0: (default) Channel 7 and channel 5 Normal operation 1: Channel 7 and channel 5 have Over Load and Over Temperature synchronized
2	PAR2	r/w	0: (default) Channel 6 and channel 4 Normal operation 1: Channel 6 and channel 4 have Over Load and Over Temperature synchronized
1	PAR1	r/w	0: (default) Channel 3 and channel 1 Normal operation 1: Channel 3 and channel 1 have Over Load and Over Temperature synchronized
0	PAR0	r/w	0: (default) Channel 2 and channel 0 Normal operation

			1: Channel 2 and channel 0 have Over Load and Over Temperature synchronized

Table 10.19 Clear Output Error Latch Register (REG_ADDR = 0x0D) -COEL

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	COEL.OUT7	COEL.OUT6	COEL.OUT5	COEL.OUT4	COEL.OUT3	COEL.OUT2	COEL.OUT1	COEL.OUT0
Default	0	0	0	0	0	0	0	0

Table 10.20 Clear Output Error Latch Register description

Bit	Field Name	Type	Description
7	COEL.OUT7	r/w	0: (default) Channel 7 Normal operation 1: Clear the error latch for the channel 7
6	COEL.OUT6	r/w	0: (default) Channel 6 Normal operation 1: Clear the error latch for the channel 6
5	COEL.OUT5	r/w	0: (default) Channel 5 Normal operation 1: Clear the error latch for the channel 5
4	COEL.OUT4	r/w	0: (default) Channel 4 Normal operation 1: Clear the error latch for the channel 4
3	COEL.OUT3	r/w	0: (default) Channel 3 Normal operation 1: Clear the error latch for the channel 3
2	COEL.OUT2	r/w	0: (default) Channel 2 Normal operation 1: Clear the error latch for the channel 2
1	COEL.OUT1	r/w	0: (default) Channel 1 Normal operation 1: Clear the error latch for the channel 1
0	COEL.OUT0	r/w	0: (default) Channel 0 Normal operation 1: Clear the error latch for the channel 0

10.6.3. SPI command quick list

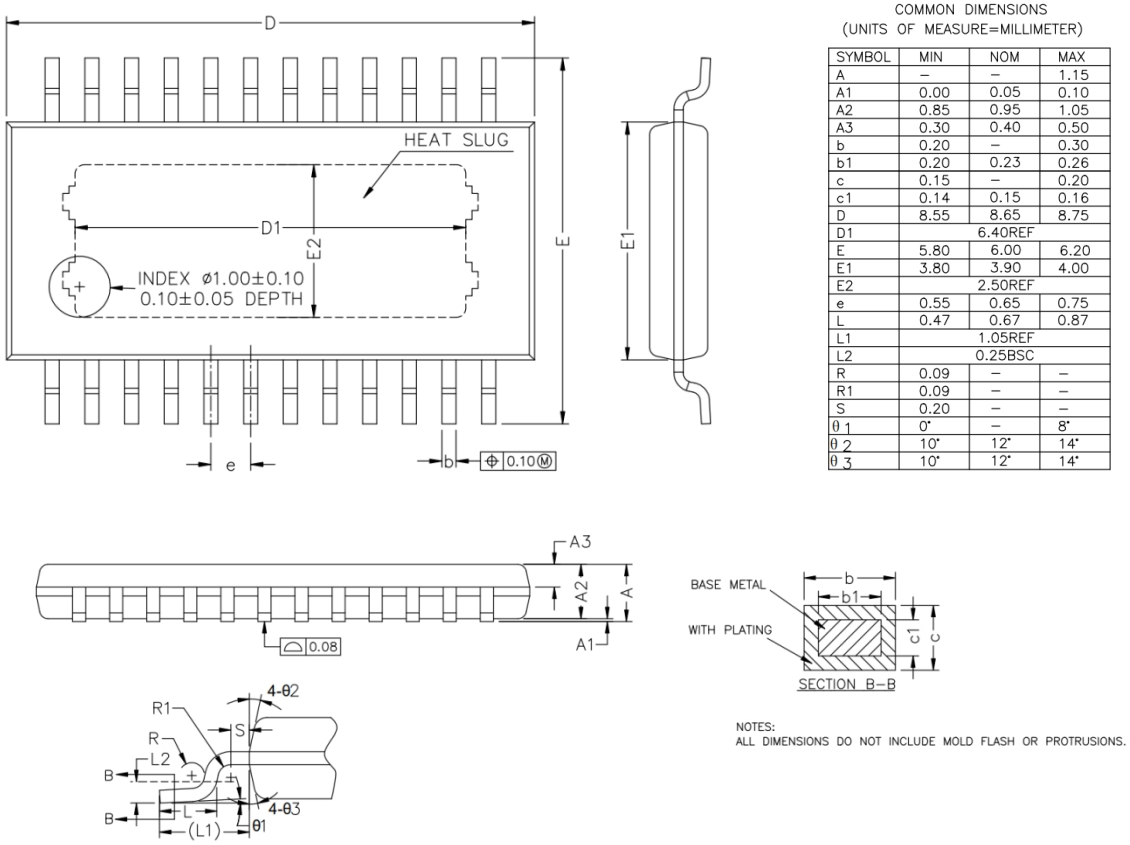
A summary of the most used SPI commands (read and write operations on all registers) is shown in **Table 10.21.**

Table 10.21 SPI command quick list

Register	"read" command	"write" command	content written
OUT	4002_H	$80XX_H$	XX_H = xxxxxxxx$_B$
MAPIN0	4402_H	$84XX_H$	XX_H = xxxxxxxx$_B$
MAPIN1	4502_H	$85XX_H$	XX_H = xxxxxxxx$_B$
ISM	4602_H	n.a. (read-only)	–
DIAG_IOL	4802_H	$88XX_H$	XX_H = xxxxxxxx$_B$
DIAG_OSM	4902_H	n.a. (read-only)	–
HWCR	$4C02_H$	$8CXX_H$	XX_H = xxxxxxxx$_B$
COEL	$4D02_H$	$8DXX_H$	XX_H = xxxxxxxx$_B$

11. Package information

11.1. HTSOP24 Package information

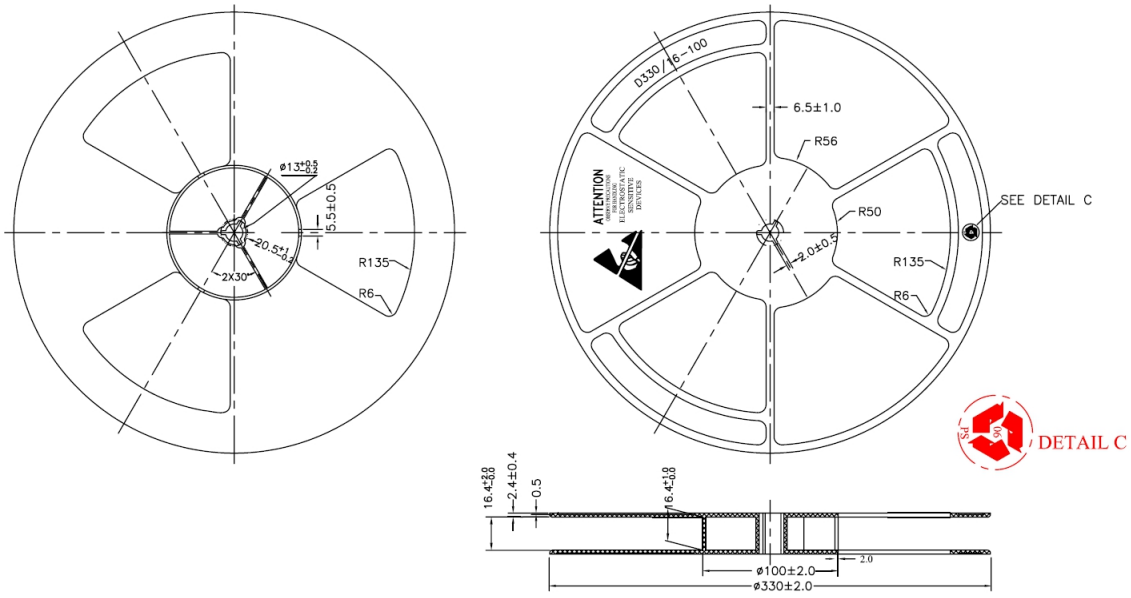


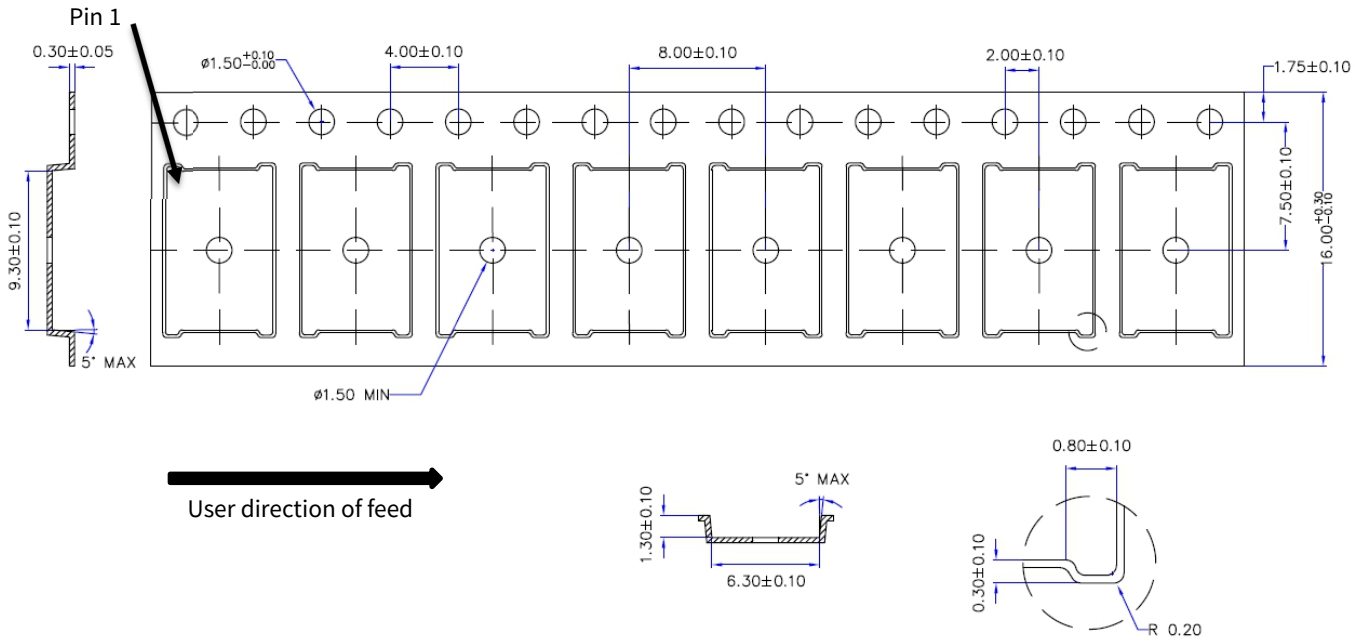
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.15
A1	0.00	0.05	0.10
A2	0.85	0.95	1.05
A3	0.30	0.40	0.50
b	0.20	–	0.30
b1	0.20	0.23	0.26
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	8.55	8.65	8.75
D1		6.40REF	
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2		2.50REF	
e	0.55	0.65	0.75
L	0.47	0.67	0.87
L1		1.05REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

11.2. HTSOP24 Packaging information




Pin 1
0.30±0.05
ø1.50+0.10 -0.00
4.00±0.10
8.00±0.10
2.00±0.10
1.75±0.10
9.30±0.10
5° MAX
7.50±0.10
16.00+0.30 -0.10
ø1.50 MIN
User direction of feed
5° MAX
1.30±0.10
6.30±0.10
0.80±0.10
0.30±0.10
R 0.20

12. Order Information

Part Number	Package Type	MSL	SPQ
NSD56008-Q1HTSBR	HTSOP24	3	4000
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.			

13. Revision History

Revision	Description	Date
1.0	Initial version	2024/5/17
1.1	1) Modified thermal resistance parameters 2) Update the note of application information 3) Add the Clamping Energy Calculation Method 4) Modified the recommended value for R_{SPI}	2024/9/4

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