

Product Overview

NSD12416A-Q1 is a 160mΩ 2 channel low-side switch with 48V clamp voltage for automotive applications. It's designed for driving resistive or inductive loads with one side connected to the battery. Internal 48V clamp circuit protects device from surge energy when fast demagnetization at turn-off.

With internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is built to limit dissipated power to decelerate power accumulation. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnose function is built to indicate any faults when thermal shutdown through an open-drain status output pin. This device operates in ambient temperatures from -40°C to 125°C.

Applications

- Automotive Relays
- Valves
- Solenoid drivers
- Lighting

Device Information

Part Number	Package	Body Size
NSD12416A-Q1SPR	SO-8	4.9mm x 3.9mm

Key Features

- AEC-Q100 (Grade 1) qualified for automotive application
- Drain current limitation: 2.5A
- 48V overvoltage clamp
- Thermal shutdown protection
- Thermal swing protection
- Fault diagnostic block
 - Thermal shutdown diagnosis
- Very low standby current
- Very low electromagnetic susceptibility
- ESD protection
- RoHS & REACH Compliance

Typical Application

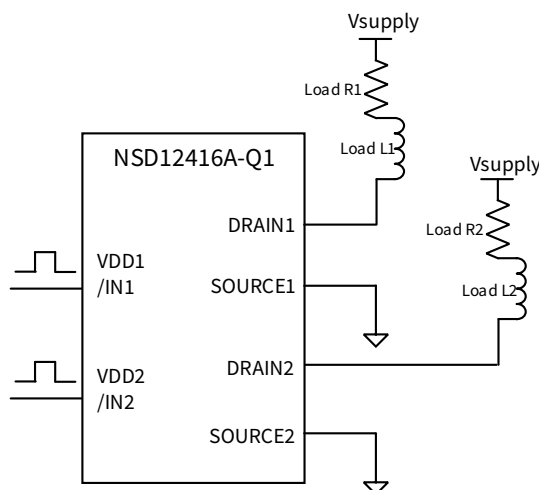


Figure 0.1 NSD12416A-Q1 Typical Application

INDEX

1. PIN CONFIGURATION AND FUNCTIONS 3

2. BLOCK DIAGRAM 3

3. ABSOLUTE MAXIMUM RATINGS 4

4. ESD RATINGS 4

5. THERMAL INFORMATION..... 4

6. SPECIFICATIONS 4

 6.1. ELECTRICAL CHARACTERISTICS 4

 6.2. SWITCHING CHARACTERISTICS 6

7. PROTECTIONS 6

 7.1. CURRENT LIMITATION 6

 7.2. THERMAL SHUTDOWN AND THERMAL SWING..... 6

8. MCU I/O PROTECTION 7

9. PACKAGE INFORMATION 8

 9.1. SO-8 PACKAGE INFORMATION..... 8

 9.2. SO-8 PACKAGING INFORMATION 8

10. ORDERING INFORMATION 9

11. REVISION HISTORY 9

1. Pin Configuration and Functions

SOURCE1	1	●	8	DRAIN1
VDD1/IN1	2		7	DRAIN1
SOURCE2	3		6	DRAIN2
VDD2/IN2	4		5	DRAIN2

Figure 1.1 NSD12416A-Q1SPR Pinout

Table 1.1 NSD12416A-Q1SPR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1,3	SOURCE1,2	PowerMOS source and ground reference for the control section
2,4	VDD1,2/IN1,2	Voltage controlled input pin with hysteresis, CMOS compatible. They control output switch state
8,7,6,5	DRAIN1,2	PowerMOS drain

2. Block diagram

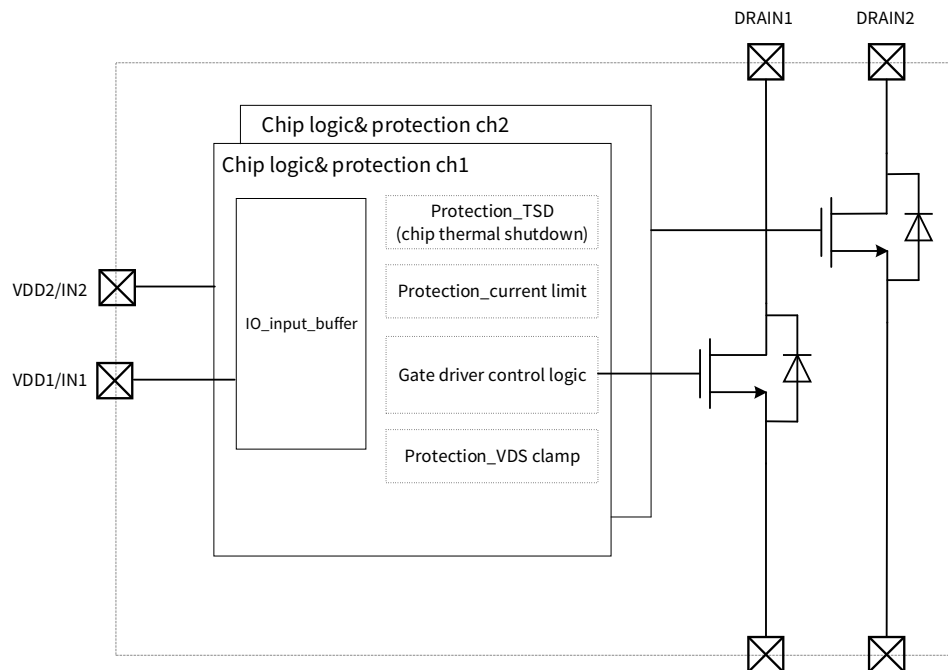


Figure 2.1 NSD12416A-Q1SPR Block diagram

3. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Drain-to-Source Voltage	V_{DS}			Internally clamped	V
DC Drain Current	I_D			Thermal limited	A
INPUT Pin Current	I_{IN}	-1		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C
Single pulse avalanche energy (L = 12mH; $T_J = 150\text{ °C}$; $R_L = 0\Omega$; $I_{OUT} = I_{lim}$)	E_{AS}			40	mJ

4. ESD ratings

Parameters	Symbol	Value	Unit
V(ESD) Electrostatic discharge	Human-body model, per AEC-Q100-002-RevD , $V_{ESD-HBM}$	±2000	V
	Charged-device model, per AEC-Q100-011-RevB , $V_{ESD-CDM}$	±750	V

5. Thermal Information

Parameters	Symbol	SO-8	Unit
Junction-to-ambient Thermal Resistance	θ_{JA}	75.4	°C/W
Junction-to-top characterization parameter	ψ_{JT}	4	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC (top)}$	23.8	°C/W

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layers board.

6. Specifications

6.1. Electrical Characteristics

($V_{DD} = V_{IN} = 4.5\text{ V}$ to 5.5 V , $T_J = -40\text{ °C}$ to 150 °C . Unless otherwise noted.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power MOSFET						
ON-state resistance	R_{ON}		160		m Ω	$I_D = 1\text{ A}$; $T_J = 25^\circ\text{C}$; $V_{DD} = V_{IN} = 5\text{ V}$
				320	m Ω	$I_D = 1\text{ A}$; $T_J = 150^\circ\text{C}$; $V_{DD} = V_{IN} = 5\text{ V}$
Drain-source clamp voltage	V_{CLAMP}	46	48	56	V	$V_{IN} = 0\text{ V}$, $I_D = 1\text{ A}$
Drain-source clamp threshold voltage	V_{CLTH}	40			V	$V_{IN} = 0\text{ V}$, $I_D = 2\text{ mA}$
OFF-state output current	I_{DSS}	0		3	μA	$V_{IN} = 0\text{ V}$; $V_{DS} = 13\text{ V}$; $T_J = 25^\circ\text{C}$
		0		5	μA	$V_{IN} = 0\text{ V}$; $V_{DS} = 13\text{ V}$; $T_J = 125^\circ\text{C}$
Body diode forward voltage	V_{BD}		0.8		V	$I_D = 1\text{ A}$; $V_{IN} = 0\text{ V}$
Input section						
Supply current from input pin	I_{ISS}		30	65	μA	ON-state; $V_{DD}=V_{IN} = 5\text{ V}$; $V_{DS} = 0\text{ V}$
Input clamp voltage	V_{ICL}	5.5		8	V	$I_{ICL} = 1\text{ mA}$
			-0.7			$I_{ICL} = -1\text{ mA}$
Input threshold voltage	V_{INTH}	1		3.5	V	$V_{DS} = V_{IN}$; $I_D = 1\text{ mA}$
Switching characteristics						
Turn-on delay time	$t_{d(ON)}$		9		μs	$R_L = 13\text{ }\Omega$, $V_{CC} = 13\text{ V}$
Turn-off delay time	$t_{d(OFF)}$		9		μs	$R_L = 13\text{ }\Omega$, $V_{CC} = 13\text{ V}$
Rise time	t_r		9		μs	$R_L = 13\text{ }\Omega$, $V_{CC} = 13\text{ V}$
Fall time	t_f		5		μs	$R_L = 13\text{ }\Omega$, $V_{CC} = 13\text{ V}$
Switching energy losses at turn-on	W_{ON}		26		μJ	$R_L = 13\text{ }\Omega$, $V_{CC} = 13\text{ V}$
Switching energy losses at turn-off	W_{OFF}		23		μJ	$R_L = 13\text{ }\Omega$, $V_{CC} = 13\text{ V}$
Protection and diagnostics						
DC short-circuit current	I_{lim}	1.6	2.5	3	A	$V_{DS} = 13\text{ V}$, $V_{DD} = V_{IN} = 5\text{ V}$
Shutdown temperature	T_{TSD}	150	175	200	$^\circ\text{C}$	
Reset temperature	T_R	$T_{RS} + 1$	$T_{RS} + 5$		$^\circ\text{C}$	
Thermal reset of STATUS	T_{RS}	135			$^\circ\text{C}$	
Thermal hysteresis ($T_{TSD} - T_R$)	T_{HYST}		7		$^\circ\text{C}$	
Dynamic temperature	ΔT_J		40		K	$T_J = -40^\circ\text{C}$, $V_{CC} = 13\text{ V}$
Dynamic temperature hysteresis	$\Delta T_J(\text{HYS})$		15		K	

6.2. Switching characteristics

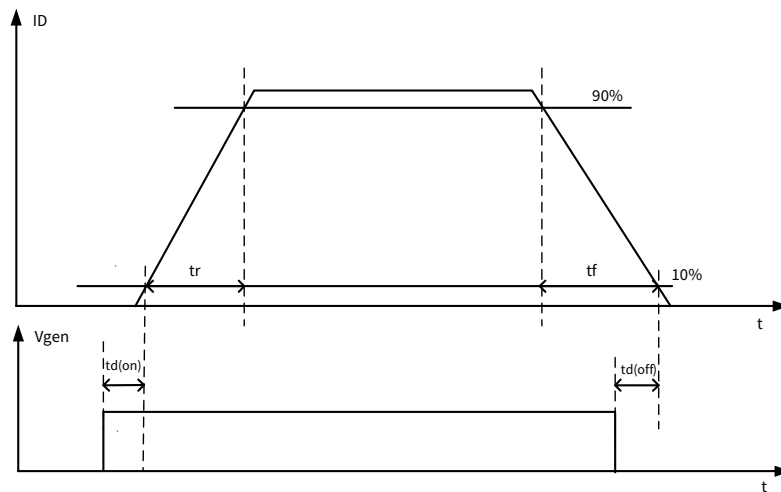


Figure 6.2 NSD12416A-Q1 Switching Characteristics

7. Protections

7.1. Current Limitation

NSD12416A-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to battery.

7.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and another one on the controller is the coldest. The absolute temperature protection is to shut down the MOSFET when the hottest junction temperature exceeds the T_{TSD} , and the dynamic temperature protection is also to shut down the MOSFET when the temperature difference between the hottest and the coldest exceeds ΔT_J .

8. MCU I/O protection

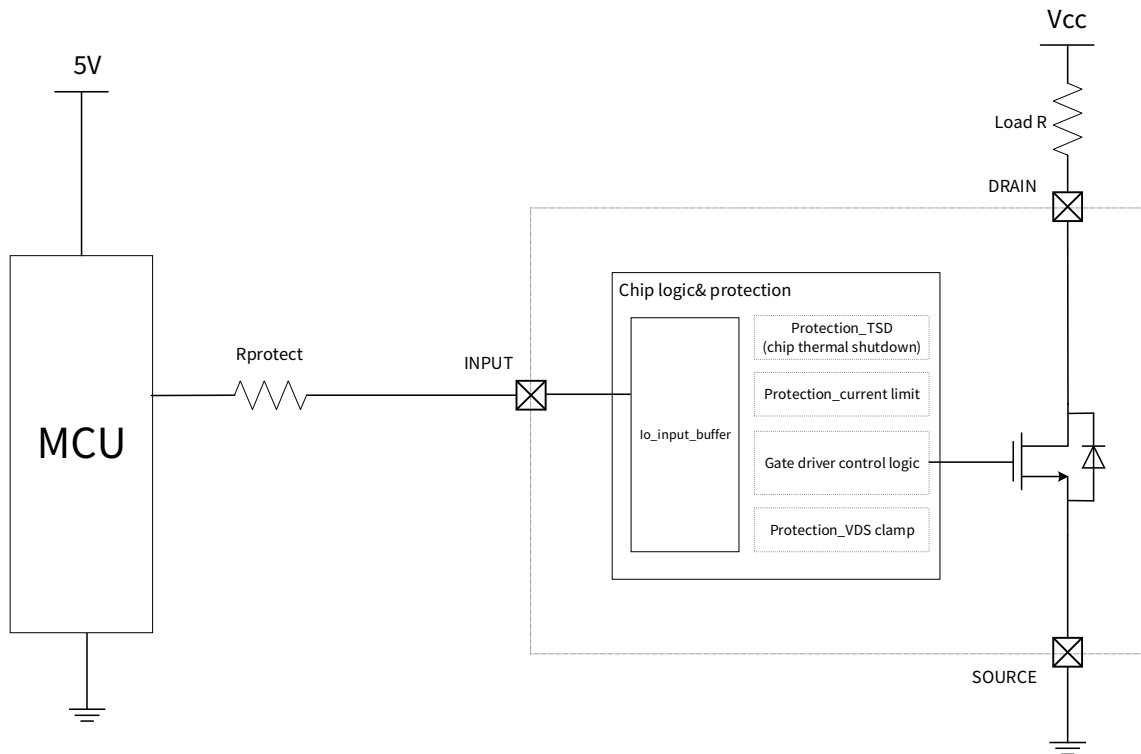


Figure 8.1 NSD12416A-Q1SPR application schematic

NSD12416A has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I/Os during transient and reverse battery conditions.

The value of resistors for protection can be calculated by the formula as shown below:

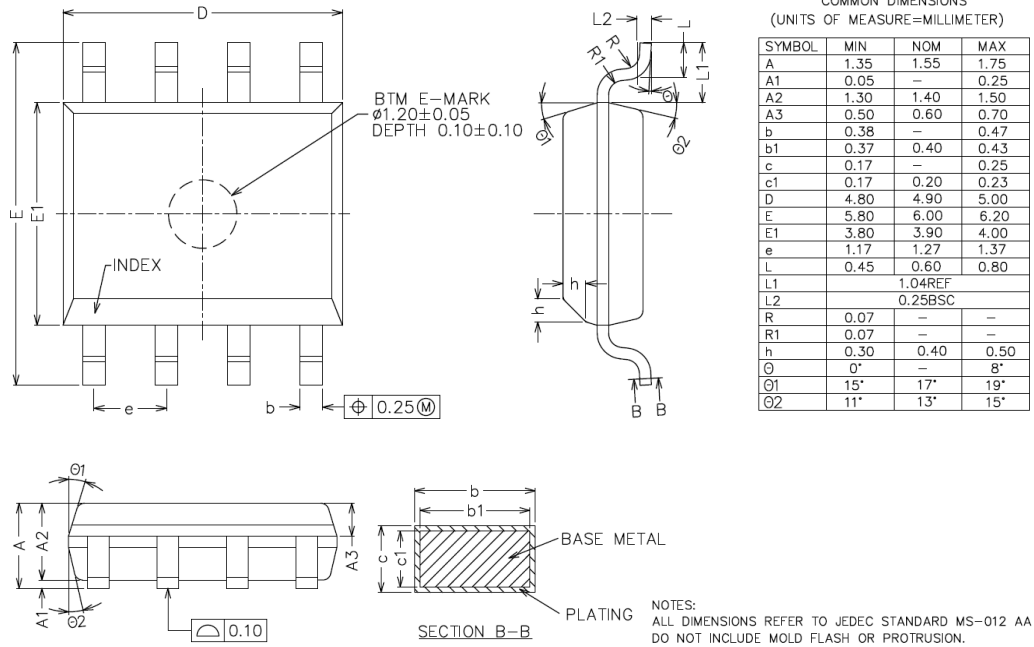
$$\frac{0.7}{I_{latchup}} \leq R_{prot} \leq \frac{V_{MCU_OUT} - V_{IH}}{I_{IHmax}}$$

Where $I_{latchup}$ is the MCU I/O latch up current, V_{MCU_OUT} is the output voltage of MCU I/O, V_{IH} is the High-level input voltage of NSD12416A, I_{IH} is the High-level input current.

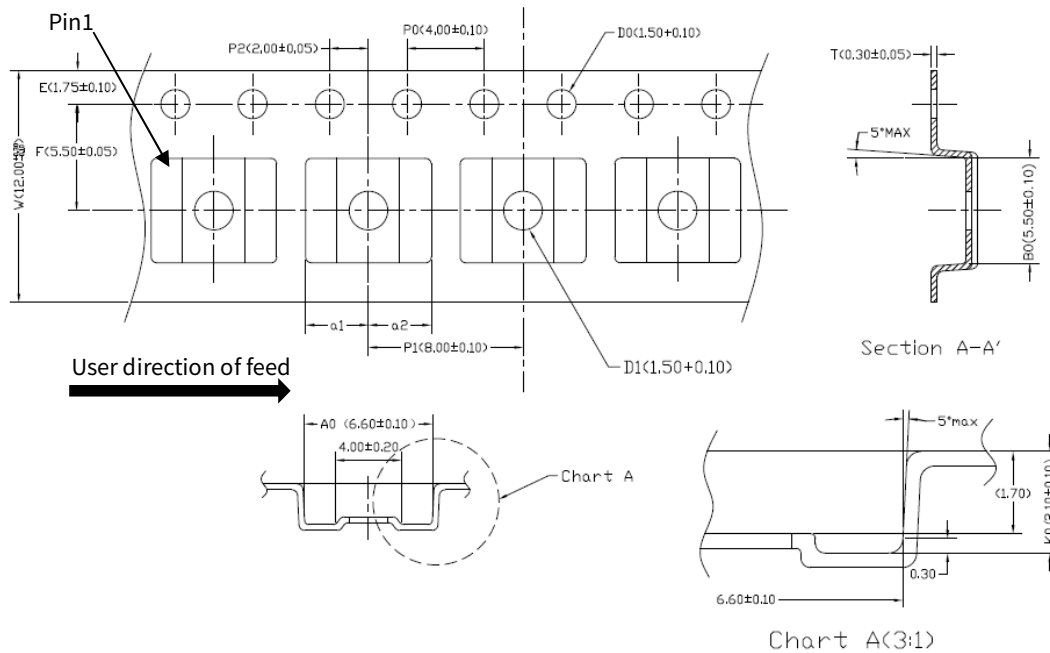
Let: $I_{latchup} \geq 20\text{mA}$; $V_{MCU_OUT} \geq 4.5\text{V}$, so $35\Omega \leq R_{prot} \leq 15\text{k}\Omega$, the recommended value is $1\text{k}\Omega$.

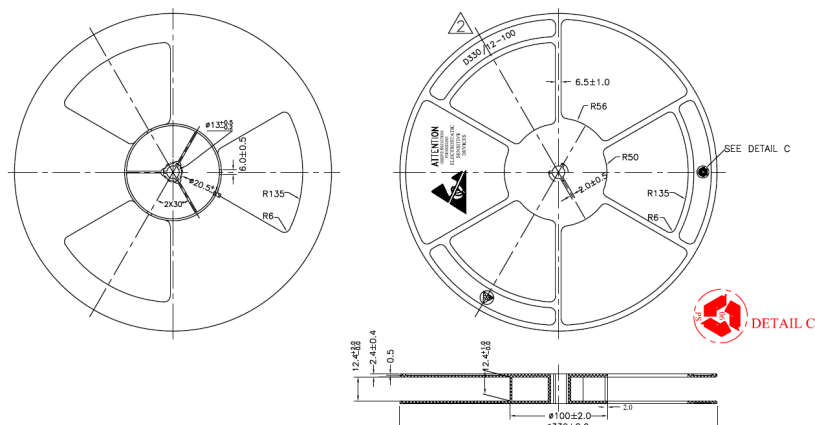
9. Package Information

9.1. SO-8 package information



9.2. SO-8 packaging information





10. Ordering Information

Part Number	Package	MSL	SPQ
NSD12416A-Q1SPR	SO-8	3	2500
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.			

11. Revision History

Revision	Description	Date
1.0	Initial version	2024/2/1
1.1	Update key description	2024/3/26
1.2	Update format	2024/4/7

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’ products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd