NOVOSENSE

NSOPA08x
36-V,6MHz, General-Purpose Operational Amplifiers
Datasheet (EN) 1.2

Product Overview

The NSOPA08x provide industry-leading performance over TL08x devices.

These devices provide outstanding value for cost-sensitive applications, with features including low offset (0.5mV, typical), high slew rate (30V/μs), and common-mode input to the positive supply. High ESD (2kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the NSOPA08x devices to be used in the most rugged and demanding applications.

Device Information

Part Number	*Package*	*Body Size*
NSOPA082-DSPR	SOP8	4.90 mm × 3.90 mm
NSOPA082-DMSR	MSOP8	3.00 mm × 3.00 mm
NSOPA084-DSPKR	SOP14	8.65mm × 3.91mm
NSOPA084-DTSKR	TSSOP14	4.40mm × 5.00mm

Key Features

- High slew rate: 30 V/μs typ
- Unity-gain bandwidth: 6 MHz
- Low offset voltage: 0.5 mV typ
- Low offset voltage drift: 1 μV/°C typ
- High common-mode rejection (CMRR): 109 dB
- Wide common-mode and differential voltage ranges
- Common-mode input voltage range includes V+
- Low input bias and offset currents
- Low noise: e_n = 15 nV/$\sqrt{Hz}$ (typ) at 10 kHz
- Output short-circuit protection
- Low total harmonic distortion: -105 dB typ
- Pulse friendly/comparator input
- Amplifier can be used in open-loop or as comparator
- Wide supply voltage: ±2.25 V to ±18 V, 4.5 V to 36 V
- RoHS and REACH Compliance

Typical Application

- General-purpose amplification
- Power control and monitoring
- Active filters
- Industrial/process control
- Data acquisition

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1. Pin Configuration and Function

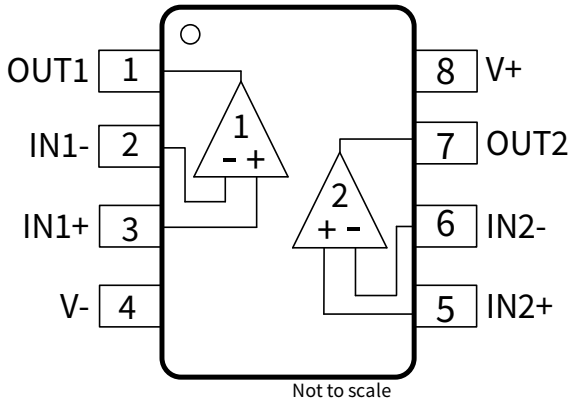


Figure 1-1 NSOPA082 8-Pin SOP and MSOP Package Top View

Table 1-1 NSOPA082 Pin Configuration and Description

Symbol	*No.*	*Function*
IN1-	2	Channel 1 Inverting Input
IN1+	3	Channel 1 Noninverting Input
OUT1	1	Channel 1 Output
IN2-	6	Channel 2 Inverting Input
IN2+	5	Channel 2 Noninverting Input
OUT2	7	Channel 2 Output
V+	8	Positive Power Supply
V-	4	Negative Power Supply

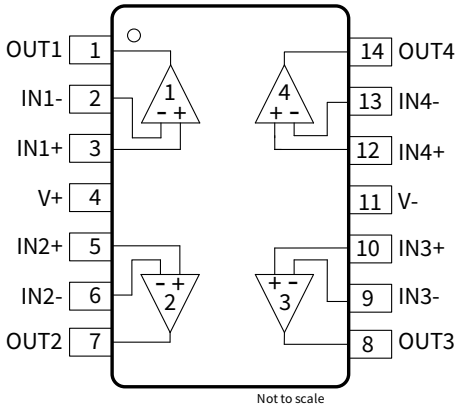


Figure 1-2 NSOPA08x 14-Pin SOP and TSSOP Package Top View

Table 1-2 Pin Functions

Symbol	*Pin No*	*Function*
IN1–	2	Channel 1 Inverting input
IN1+	3	Channel 1 Noninverting input
OUT1	1	Channel 1 Output
IN2–	6	Channel 2 Inverting input
IN2+	5	Channel 2 Noninverting input
OUT2	7	Channel 2 Output
IN3–	9	Channel 3 Inverting input
IN3+	10	Channel 3 Noninverting input
OUT3	8	Channel 3 Output
IN4–	13	Channel 4 Inverting input
IN4+	12	Channel 4 Noninverting input
OUT4	14	Channel 4 Output
V+	4	Positive Power supply
V-	11	Negative Power supply

2. Absolute Maximum Ratings[1]

Parameters	Symbol	Min	Max	Unit
Supply voltage $V_S = (V_+) - (V_-)$	V_S	-0.3	40	V
Differential, IN+ to IN− inputs			$(V_+) + 0.5$	V
Common-Mode input voltage		$(V_-) -0.5$	$(V_+) + 0.5$	V
Current, Signal input pins		-10	10	mA
Output		$(V_-) -0.5$	$(V_+) + 0.5$	V
Junction temperature	T_J		150	°C
Storage temperature	T_{stg}	−55	150	°C

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ● All pins	±2.0	kV
	Charged device model (CDM), per JESD22-C101 ● All pins	±2.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Supply voltage	V_S	4.5	36	V
Input voltage		$(V_-) + 2$	(V_+)	V
Operating free-air temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	SOP8	TSSOP14	SOP14	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	207.9	130	96.25	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(TOP)}$	92.8	59.1	50	°C/W
Junction-to-board thermal resistance	θ_{JB}	129.7	82.8	61	°C/W

[1] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability

6. Electrical Characteristics

For $V_S = (V_+) - (V_-) = 36$ V (±18 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and VOUT = $V_S/2$, unless otherwise noted

Parameters	Symbol	Condition		Min	Typ	Max	Unit
INPUT							
Offset voltage	V_{OS}				±0.5	±2.5	mV
		$T_A = -40°C$ to $125°C$[1]				±3	
Offset voltage Drift	dV_{OS}/d_T	$T_A = -40°C$ to $125°C$[1]			1		µV/°C
Common-mode input range	V_{CM}			(V-) + 2		(V+)	V
Common mode rejection ratio	CMRR	$V_S = 36V$, $(V_-) + 5V < V_{CM} < (V_+)$			120		dB
		$V_S = 36V$, $(V_-) + 2V < V_{CM} < (V_+)$		94	109		
		$T_A = -40°C$ to $125°C$[1]		90			
Channel Separation		f = 0Hz			120		dB
Input bias current[2]	I_B	V_S = 4.5V to 36 V, $V_{CM} = V_S/2$			15		pA
Input offset current[2]	I_{OS}	V_S = 4.5V to 36 V, $V_{CM} = V_S/2$			5		pA
input Impedance	Z_{ID}	Differential			15 || 4		GΩ || pF
	Z_{ICM}	Common-mode			1 || 5		TΩ || pF
OPEN-LOOP GAIN							
Open-loop voltage gain	A_{OL}	$(V_-) +0.3V < V_{OUT} < (V_+) -0.3V$, $V_S = 4.5$ V		103	113		dB
		$(V_-) +0.3V < V_{OUT} < (V_+) -0.3V$, $V_S = 4.5$ V, $T_A = -40°C$ to $125°C$[1]			106		
		$(V_-) +0.3V < V_{OUT} < (V_+) -0.3V$, $V_S = 36$ V		119	124		
		$(V_-) +0.3V < V_{OUT} < (V_+) -0.3V$, $V_S = 36$ V, $T_A = -40°C$ to $125°C$[1]			98		
OUTPUT							
Output swing from Positive rail headroom, 10kΩ		V_S =4.5V	V_{ID} = 500 mV		17	20	mV
		V_S =36V			130	140	
Output swing from Negative rail headroom, 10kΩ		V_S =4.5V	V_{ID} = 500 mV		12	15	
		V_S =36V			90	100	
Output swing from Positive rail headroom, 2kΩ		V_S =4.5V	V_{ID} = 500 mV		80	85	
		V_S =36V			660	700	
Output swing from Negative rail headroom, 2kΩ		V_S =4.5V	V_{ID} = 500 mV		55	60	
		V_S =36V			450	500	
Short-Circuit Output Current	I_{SC}	Sink			28		mA
		Source			32		
Output Impedance	Z_O	f = 1 MHz, I_O = 0 A			146		Ω

[1] Data is specified based on characterization results.

Electrical Characteristics (continued)

For V_S = (V_+) – (V_-) = 36 V (±18 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and VOUT = V_S/2, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Unit
FREQUENCY RESPONSE							
Gain-bandwidth product	GBP	V_S = 36 V, C_L = 20 pF			6		MHz
Phase margin	PM	V_S = 36 V, C_L = 20 pF			55		Degree
Settling time	T_S	To 0.1%, 10 V Step, C_L = 10 pF			0.8		µs
		To 0.1%, 2 V Step, C_L = 10 pF			0.4		
		To 0.01%, 10 V Step, C_L = 10 pF			0.9		
		To 0.01%, 2 V Step, C_L = 10 pF			0.5		
Slew rate	SR	Positive	10-V step, G= +1		40		V/µs
		Negative			30		
Total harmonic distortion + noise	THD+N	V_{rms} = 1 V, G = +1, f = 1 kHz, R_L= 2kΩ			-105		dB
Overload recovery time		V_{IN} × Gain > V_S			200		ns
EMI rejection ratio	EMIRR	f = 1 GHz			66		dB
NOISE (INPUT REFERRED)							
Input voltage noise density	e_n	f = 1 kHz			41		nV/$\sqrt{Hz}$
		f = 10 kHz			15		
Input Voltage noise	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz			12		µVpp
POWER SUPPLY							
Operating voltage range	V_S			4.5		36	V
Power supply rejection ratio	PSRR	V_S = 10V to 36 V, V_{CM} = V_S/2			120		dB
		V_S = 4.5V to 36 V, V_{CM} = V_S/2		94	109		
		T_A = –40°C to 125°C[1]		90			
Quiescent current per amplifier	I_Q	NSOPA082	Vs=4.5V		1.2	1.46	mA
			T_A = –40°C to 125°C[1]			1.8	
			Vs=36V		1.26	1.56	
			T_A = –40°C to 125°C[1]			1.7	
		NSOPA084	Vs=4.5V		0.6	0.73	
			T_A = –40°C to 125°C[1]			0.8	
			Vs=36V		0.63	0.78	
			T_A = –40°C to 125°C[1]			0.85	

[1] Data is specified based on characterization results.

7. Typical Performance Characteristics

at T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

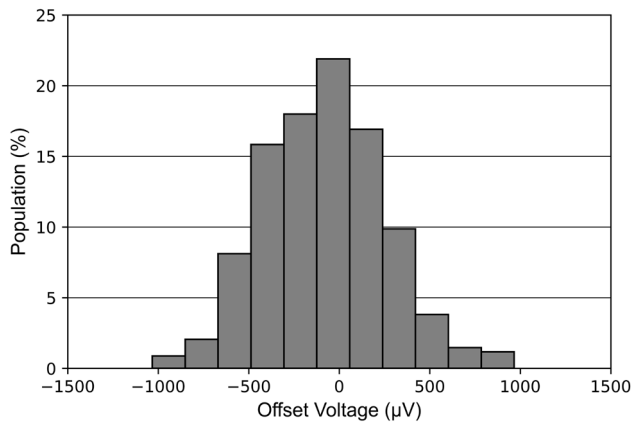


Figure 7-1 Offset Voltage Production Distribution

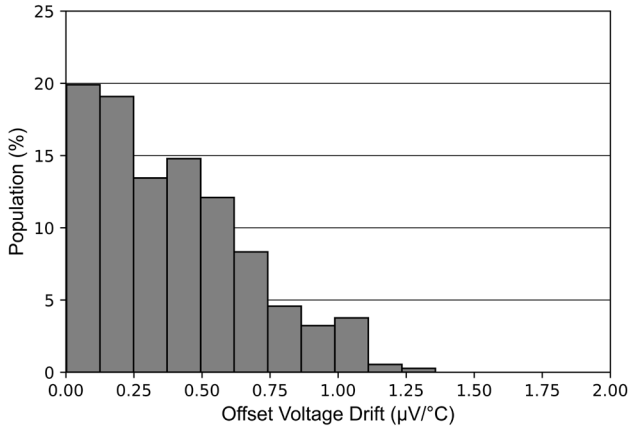


Figure 7-2 Offset Voltage Drift Distribution

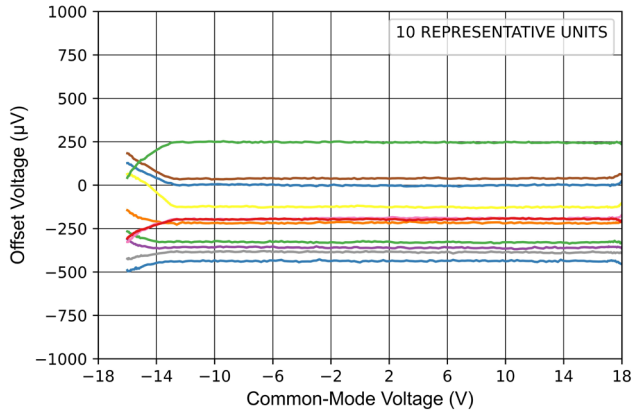


Figure 7-3 Offset Voltage vs Common-Mode Voltage

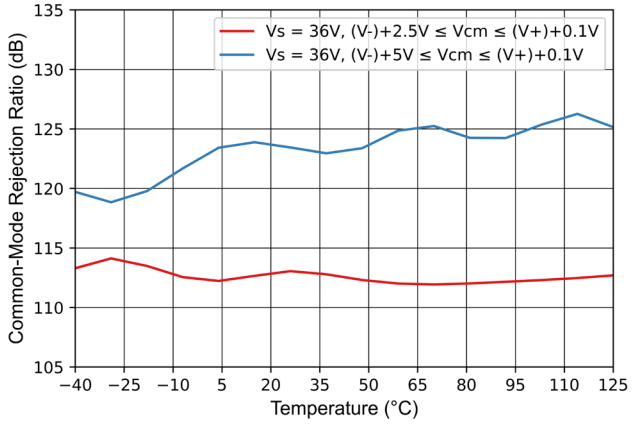


Figure 7-4 CMRR vs Temperature

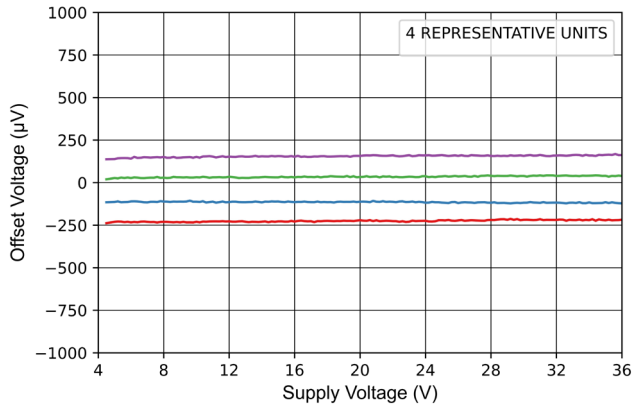


Figure 7-5 Offset Voltage vs Power Supply (VCM=V+)

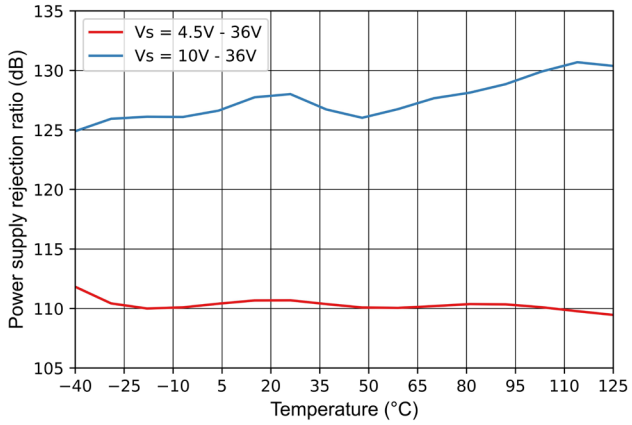


Figure 7-6 PSRR vs Temperature

Typical Performance Characteristics (continued)

at T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

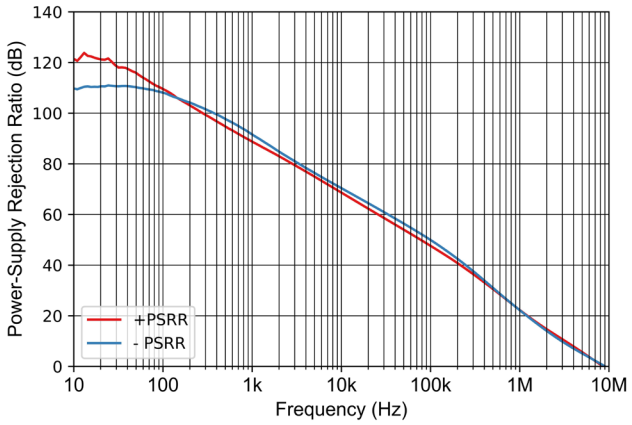


Figure 7-7 Power-Supply Rejection Ratio vs Frequency

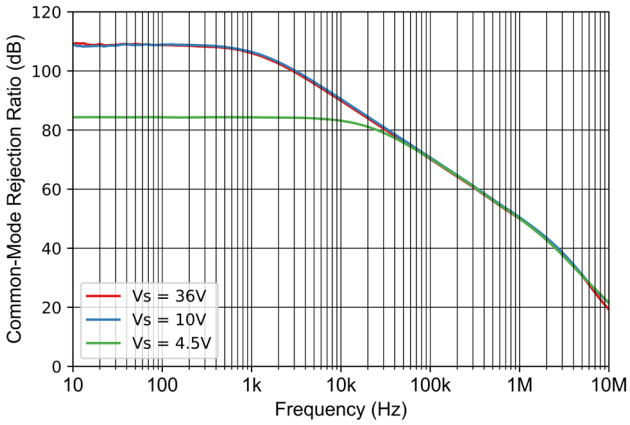


Figure 7-8 Common-Mode Rejection Ratio vs Frequency

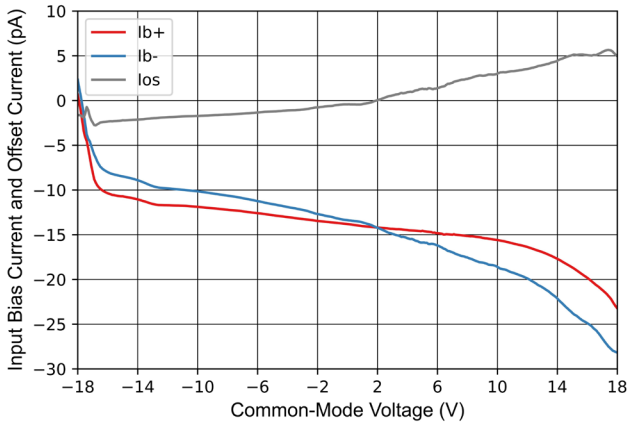


Figure 7-9 Input Bias Current vs Common-Mode Voltage

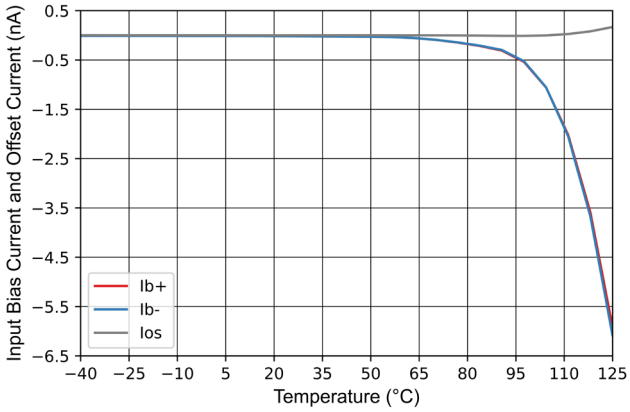


Figure 7-10 Input Bias Current vs Temperature

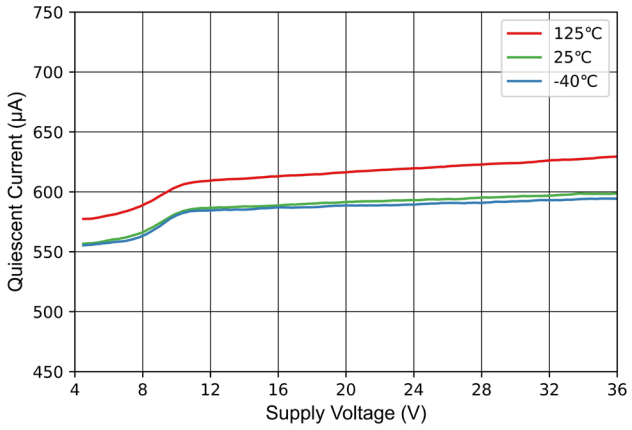


Figure 7-11 Quiescent Current vs Supply Voltage

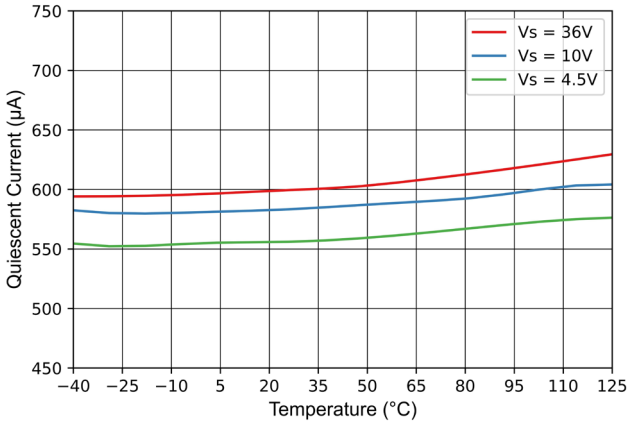


Figure 7-12 Quiescent Current vs Temperature

Typical Performance Characteristics (continued)

at T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

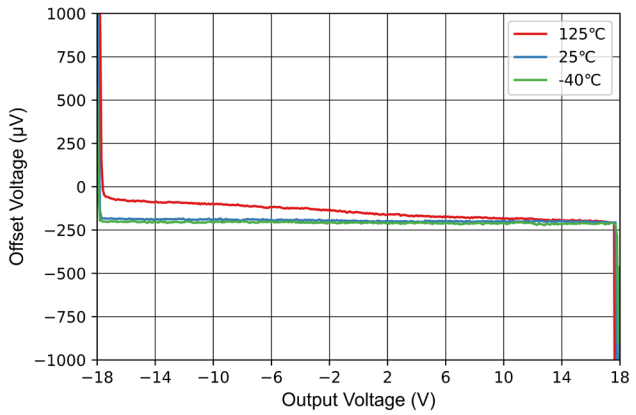


Figure 7-13 Offset Voltage vs Output Voltage

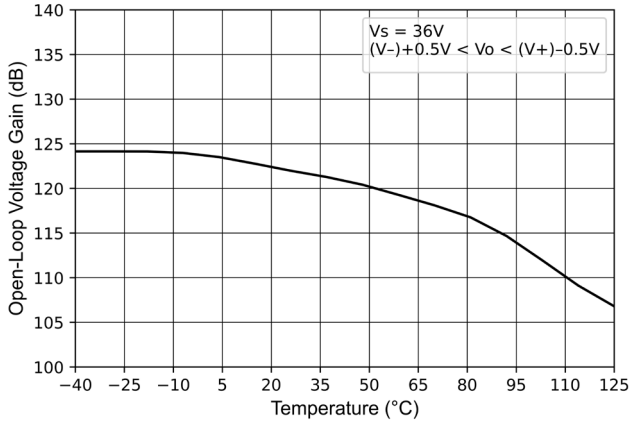


Figure 7-14 Open-Loop Voltage Gain vs Temperature

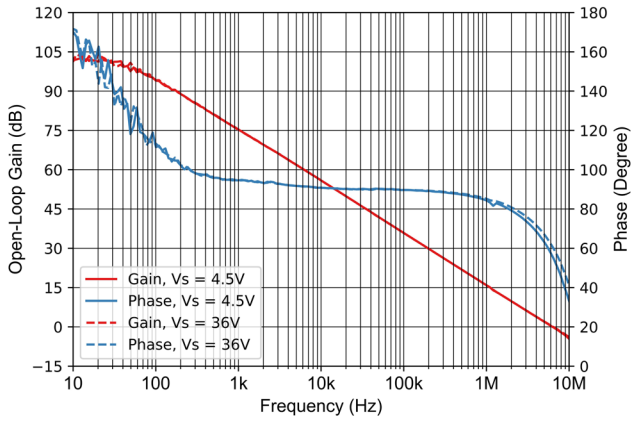


Figure 7-15 Open Loop Gain vs Frequency

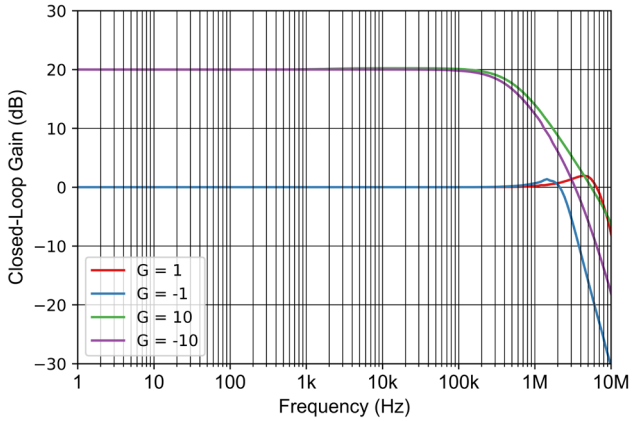


Figure 7-16 Closed Loop Gain and Phase vs Frequency

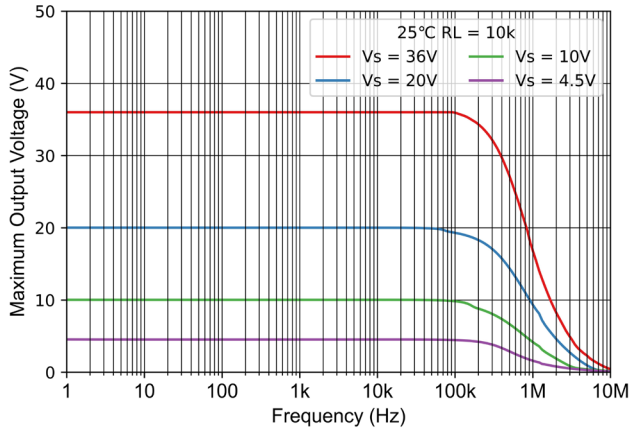


Figure 7-17 Maximum Peak Output Voltage vs. Frequency

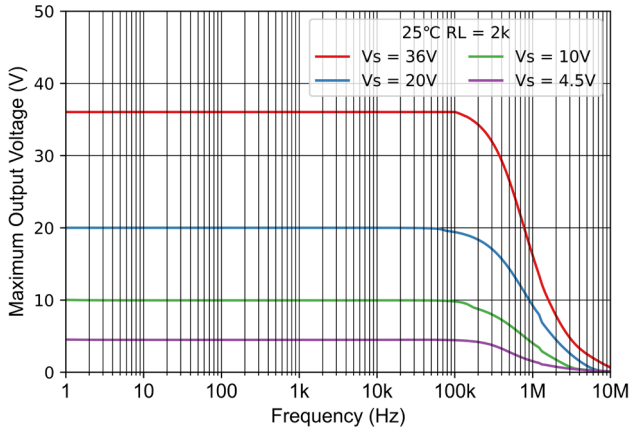


Figure 7-18 Maximum Peak Output Voltage vs. Frequency

Typical Performance Characteristics (continued)

at T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

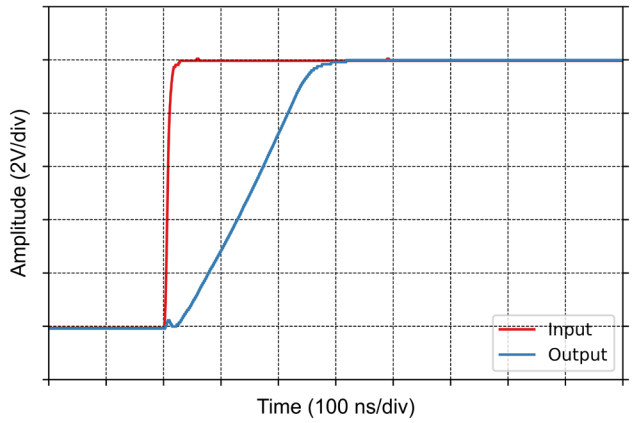


Figure 7-19 Large-Signal Step Response (Rising)

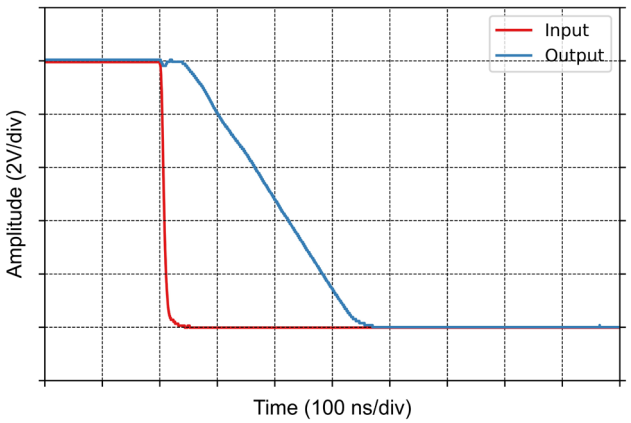


Figure 7-20 Large-Signal Step Response (Falling)

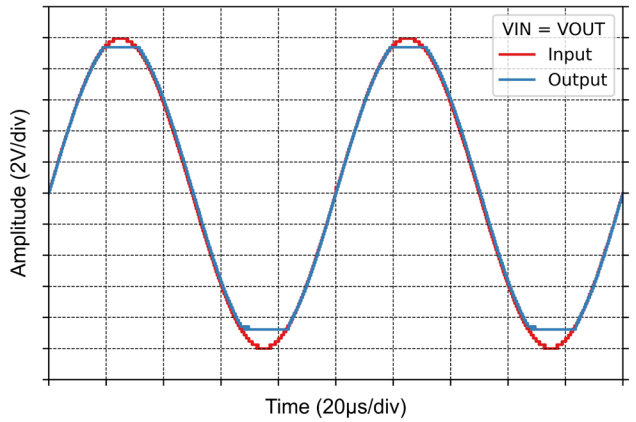
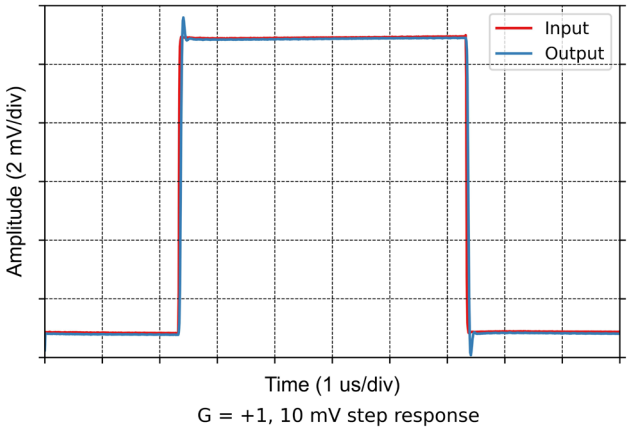


Figure 7-21 No Phase Reversal



G = +1, 10 mV step response

Figure 7-22 Small-Signal Step Response

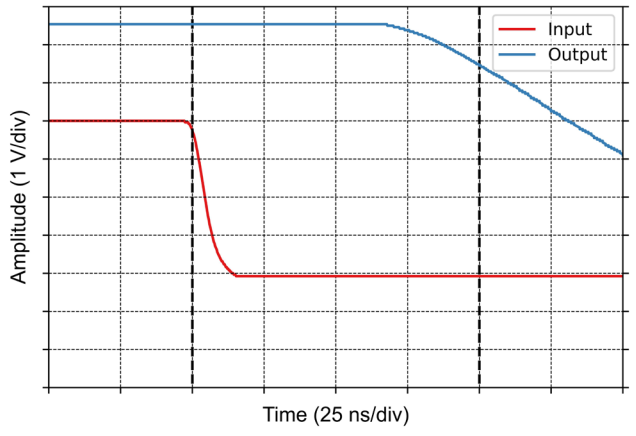


Figure 7-23 Positive Overload Recovery (G = 10)

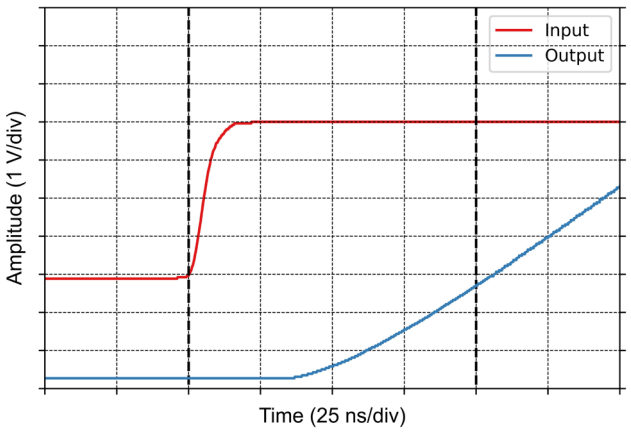


Figure 7-24 Negative Overload Recovery (G = 10)

Typical Performance Characteristics (continued)

at T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

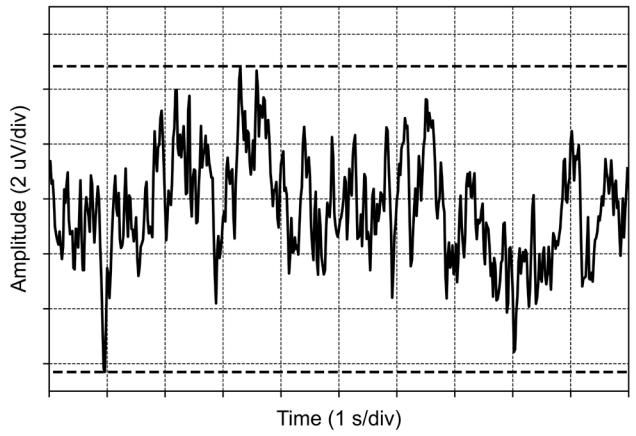


Figure 7-25 0.1-Hz to 10-Hz Noise

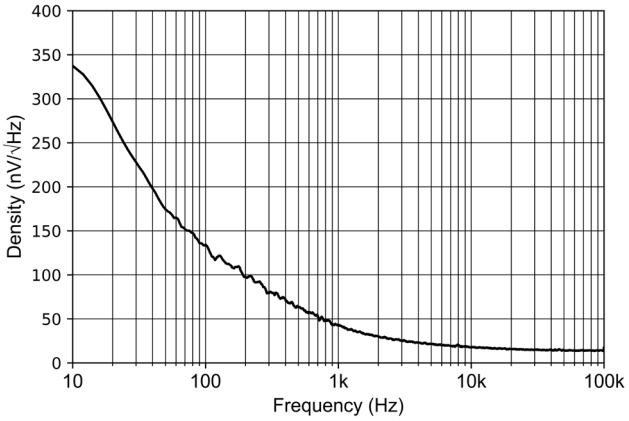


Figure 7-26 Input Voltage Noise Spectral Density

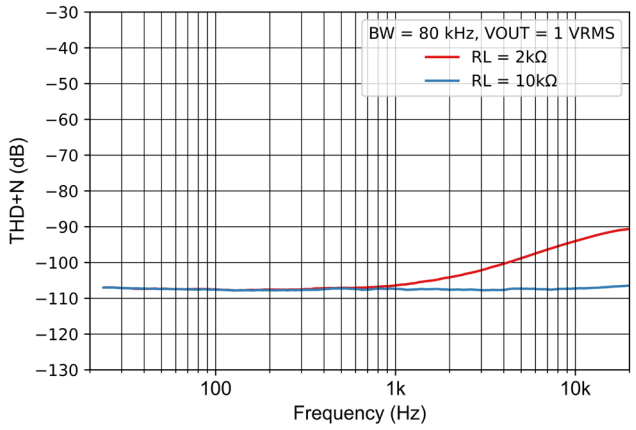


Figure 7-27 THD+N Ratio vs Frequency

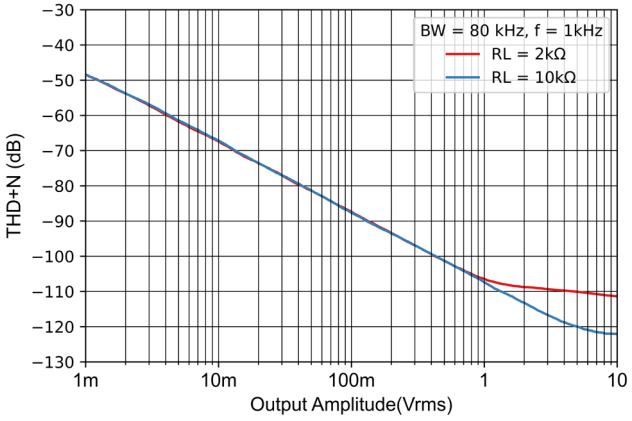


Figure 7-28 THD+N vs Output Amplitude

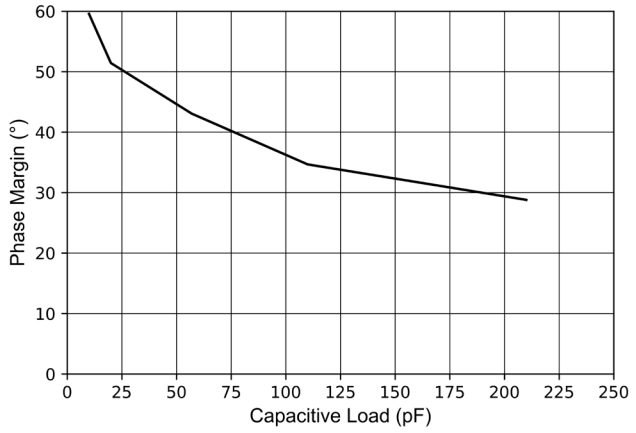


Figure 7-29 Phase Margin vs Capacitive Load

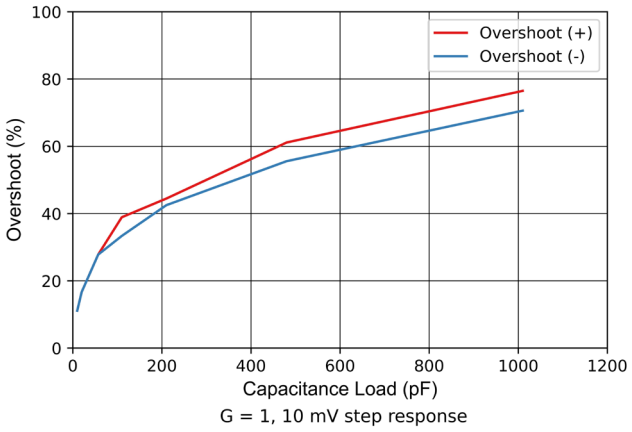


Figure 7-30 Small-Signal Overshoot vs Capacitive Load

Typical Performance Characteristics (continued)

at T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

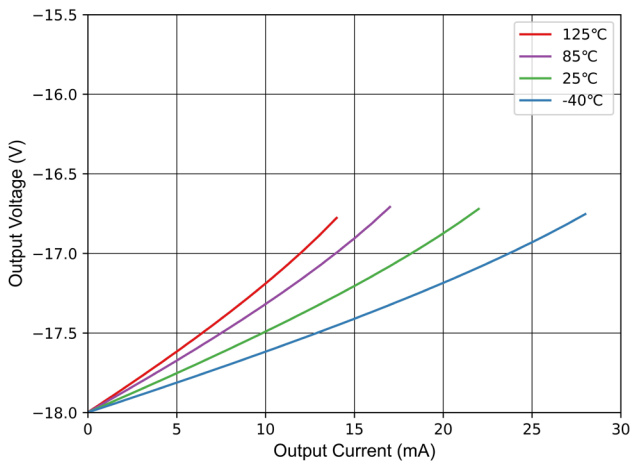


Figure 7-31 Output Voltage Swing vs Output Sinking Current

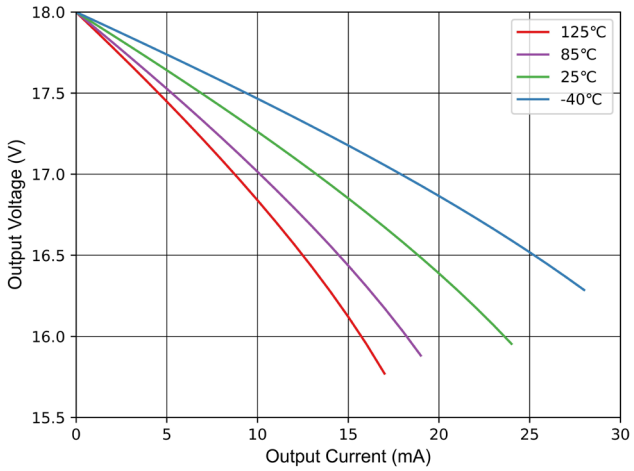


Figure 7-32 Output Voltage Swing vs Output Sourcing Current

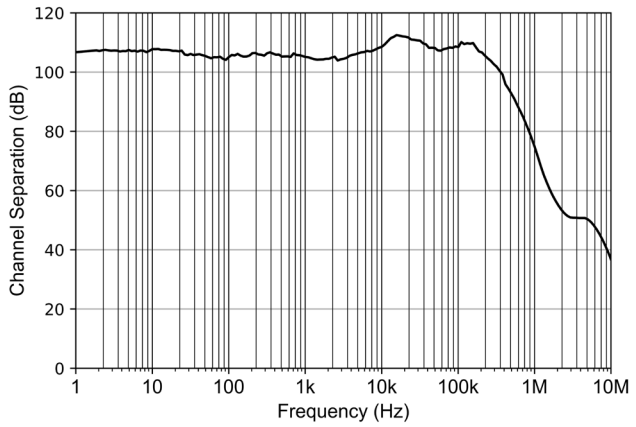


Figure 7-33 Channel Separation vs Frequency

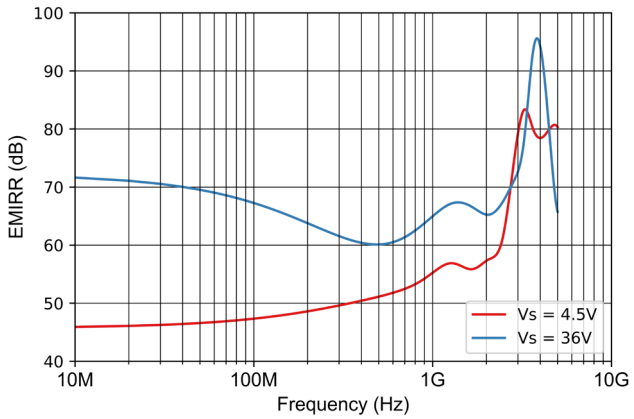


Figure 7-34 EMIRR vs Frequency

8. Detailed Description

8.1. Overview

The NSOPA08x series are high-voltage general-purpose amplifiers that can operate up to 36V. These devices offer excellent parameters and are particularly suitable for high slew rate and cost-sensitive applications that will require high voltage signals, such as motor drives and inverter systems.

8.2. Function Block

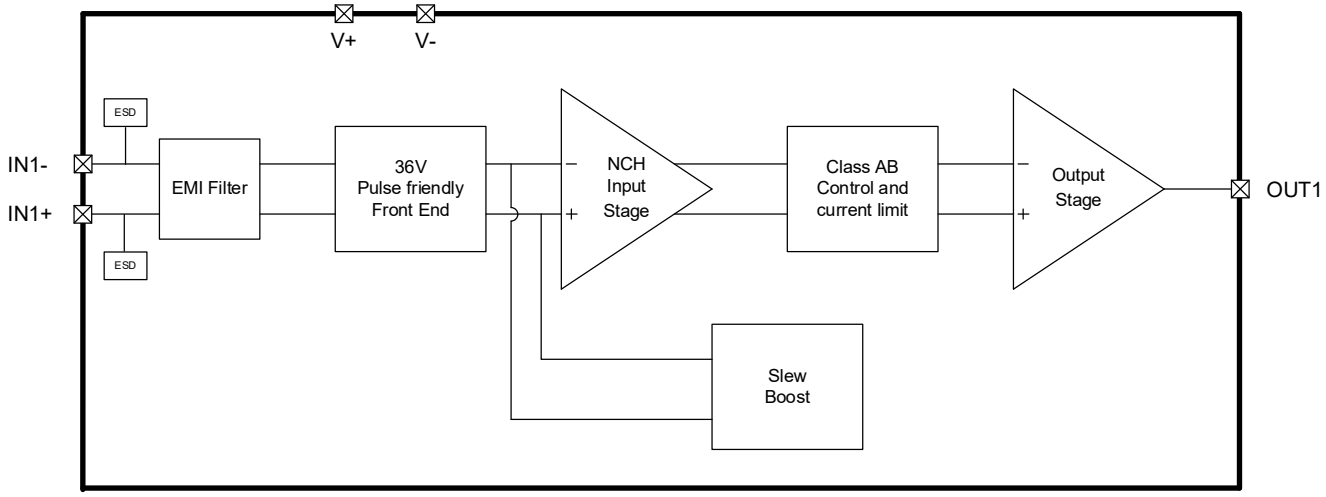


Figure 8-1 NSOPA08x Function Block (One channel is shown)

8.3. EMIRR

The NSOPA08x series use integrated electromagnetic interference (EMI) filtering to reduce the impact of EMI on devices such as wireless communications and dense circuit boards that mix analog signal chains and digital components. EMI immunity can be improved through circuit design technology; the advantage of NSOPA08x lies in these design improvements, making EMIRR=65dB@1GHz. Figure 7-34 shows the EMIRR IN+ values for the NSOPA08x at articular frequencies commonly encountered in real-world applications.

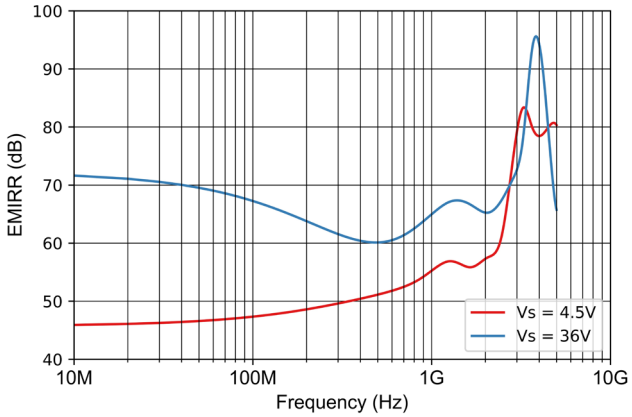


Figure 8-2 NSOPA08x EMIRR vs Frequency

8.4. Slew Boost

NSOPA08x has internal SR boost block. The boost circuit can provide positive and negative current flow to boost both positive and negative slew rates.

8.5. Pulse Friendly

Pulse Friendly means amplifier can operate with differential inputs up to supply rail. Therefore, Amplifier can be used in open-loop or as comparator. But take attention that input common-mode voltage should be not violated.

8.6. Electrical Overstress

Always, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. *Figure 8-3* shows an illustration of the ESD circuits contained in the NSOPA08x (indicated by the dotted area area). The ESD protection circuitry involves several current-steering diodes connected from the input, output pins, and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

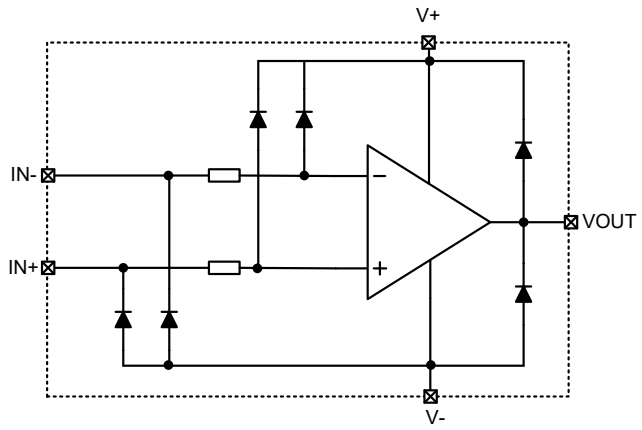


Figure 8-3 Internal ESD Equipment Model

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin.

Electrostatic Discharge (ESD) is defined the transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD is regarded as a high voltage(kV), short duration event(1-100ns). Besides, it is fast edges and lower power event.

But unlike ESD problems, EOS is another common device problem. Electrical Over Stress (EOS) is defined the exposure of an item to current or voltage beyond its maximum ratings.

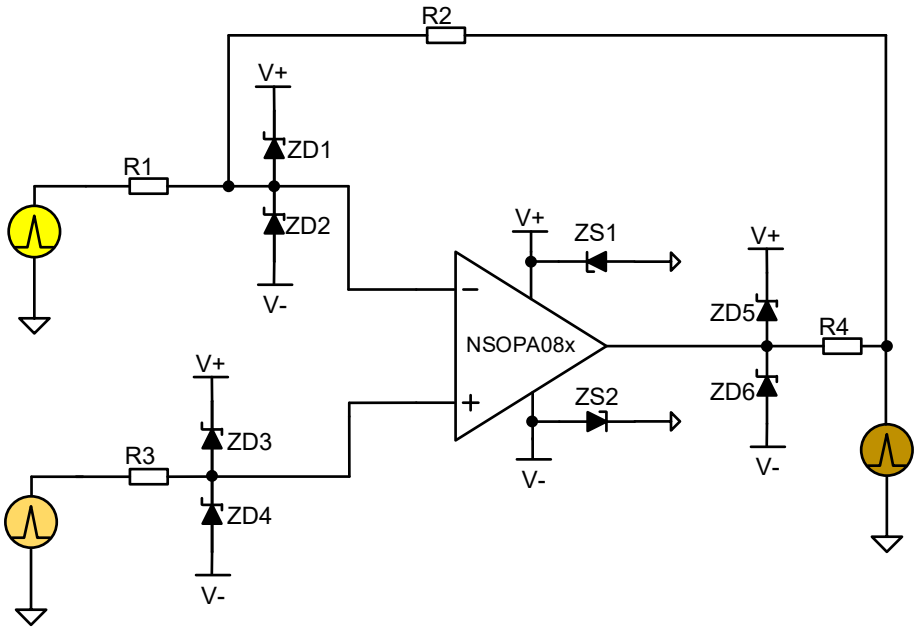


Figure 8-4 External component to enhance EOS performance

Figure 8-4 shows how to use external components to enhance the circuitry robustness.

1. SDx are small signal Schottky diodes. Using power Schottky for power operational amplifier. Diodes limits EOS Voltage to [(V+) +0.3V] or [(V-)-0.3V].
2. ZS1 and ZS2 are Zener diodes or unipolar semiconductor Transient Voltage Suppressors (TVS). They prevent device supply over-voltage, provide reverse polarity protection, and provide a current path for Iq if one supply floats.
3. R1, R2 limit current through SD1, SD2.
4. R3 limits current through SD3, SD4.
5. R4 limits current through SD5, SD6.R4 is inside the feedback loop adding little error at output voltage.
6. **Check Absolute Maximum Ratings before using NSOPA08x and never violate the Absolute Maximum Ratings.**

9. Application Information

9.1. Active Filter

NSOPA08x can be configured into different types of filters for processing complex signals. Here is a brief explanation of Sallen-key filter type.

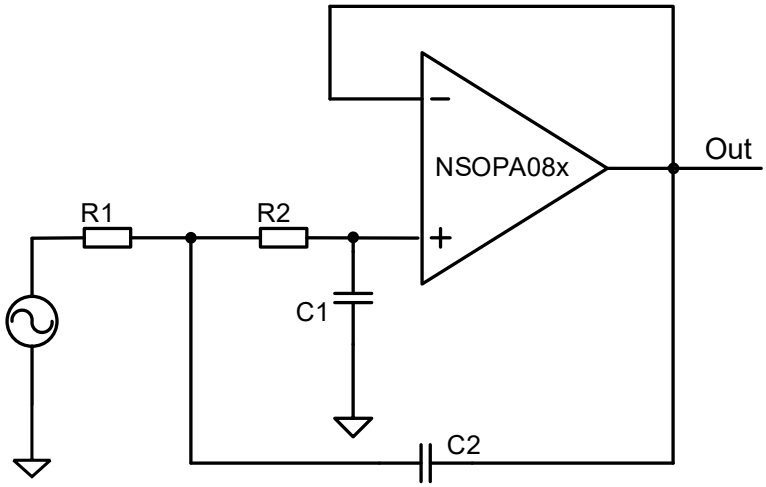


Figure 9-1 Second-Order Sallen-Key Filter

The transfer function of this circuit can be derived as $f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$.

The 1kHz low pass filter is taken as a design example. By setting R1=9.1kΩ, R2=13 kΩ, C1=10nF and C2=20.5nF, we can get the amplitude-frequency and phase-frequency curves as follows.

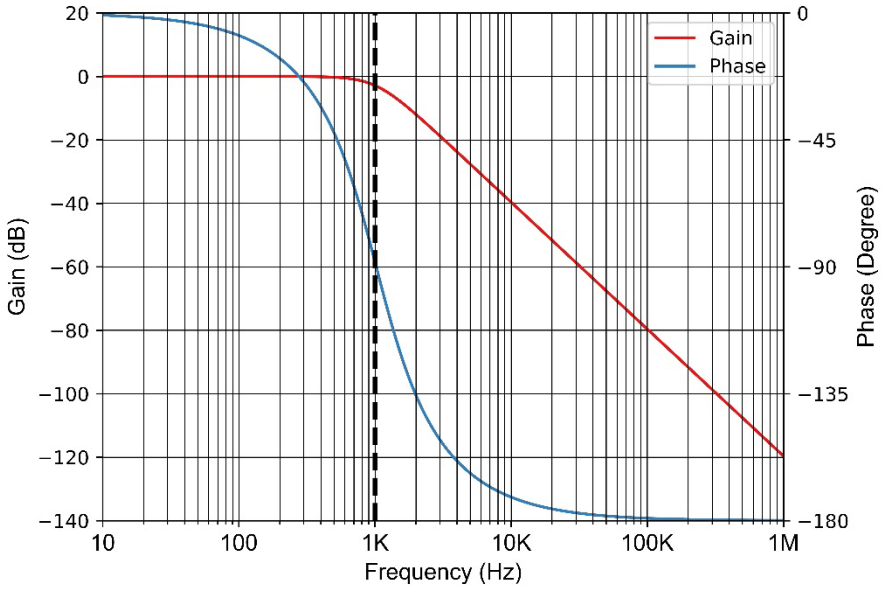


Figure 9-2 Amplitude-Frequency and Phase-Frequency Curves

9.1. High-Side Current Sensing

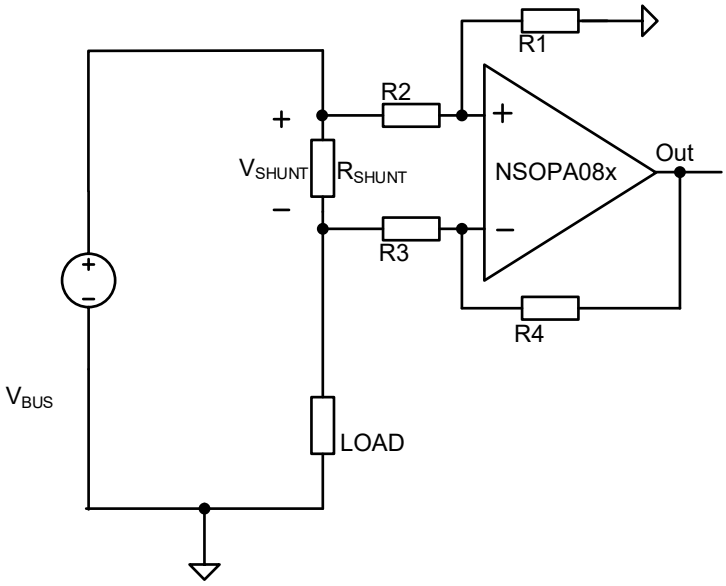


Figure 9-3 High-Side Current Sensing

NSOPA08x can be used in the high-side current sensing application.

When designing high-side current sensing circuits, the common-mode voltage of the op amp must be considered. The common-mode voltage is set by the bus voltage and the resistor divider formed by resistors R1 and R2 (shown in Figure 1) and is calculated using Equation 1 below.

$$\mathrm{Vcm} = \frac{\mathrm{R1}}{\mathrm{R1} + \mathrm{R2}} \times \mathrm{VBUS} \quad (1)$$

Typically, R1=R4, R2=R3. To ensure accuracy, it is important that R1 and R4 and R2 to R3 match closely. Any mismatch may result in gain and CMRR errors. It is recommended to minimize these errors by using matched resistors with an accuracy of 0.1% for external circuitry.

In low-power application, the consumption of resistor shall be taken into consideration.

$$\mathrm{GAIN} = \frac{\mathrm{R4}}{\mathrm{R3}} \quad (2)$$

The input offset voltage must also be considered when determining the accuracy of the solution. Input offset voltage is inherent to the op amp and changes the expected output voltage, as shown in Equation 3.

This error can be significant if the offset voltage is close to the same value as the voltage across the shunt resistor (Vshunt). It is recommended to use op amps with lower inherent offset voltages to minimize system errors.

$$\mathrm{VOUT} = \mathrm{GAIN} \times \mathrm{V_{SHUNT}} + (\mathrm{GAIN} + 1) \times \mathrm{V_{OS}} \quad (3)$$

10. Layout Guidelines

10.1. Guidelines

Poor op amp PCB layout will deteriorate the chip parameters, or even worse, cause it to work abnormally. For better performance, some tips should be considered.

• Noise can propagate into the analog circuitry through the board's power connections and to the power pins of the op amp itself. Bypass capacitors are used to reduce coupled noise by providing a low impedance path to ground.

– Connect a low ESR 0.1μF ceramic bypass capacitor between each supply pin and ground as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single-supply applications.

• To reduce parasitic coupling, keep input traces as far away from power supply or output traces as possible. If these traces cannot be kept separate, route them at a 90-degree angle

It is much better to run overly sensitive traces than to run traces parallel to noisy traces.

• External components should be located as close to the device as possible, as shown in Figure 11-2. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.

• Keep input traces as short as possible. Remember, the input traces are the most sensitive parts of the circuit.

• For best performance, cleaning is recommended after PCB board assembly.

10.2. Example

A single channel is shown as follow. The rest channels should be handled with identical way but not shown in the figure.

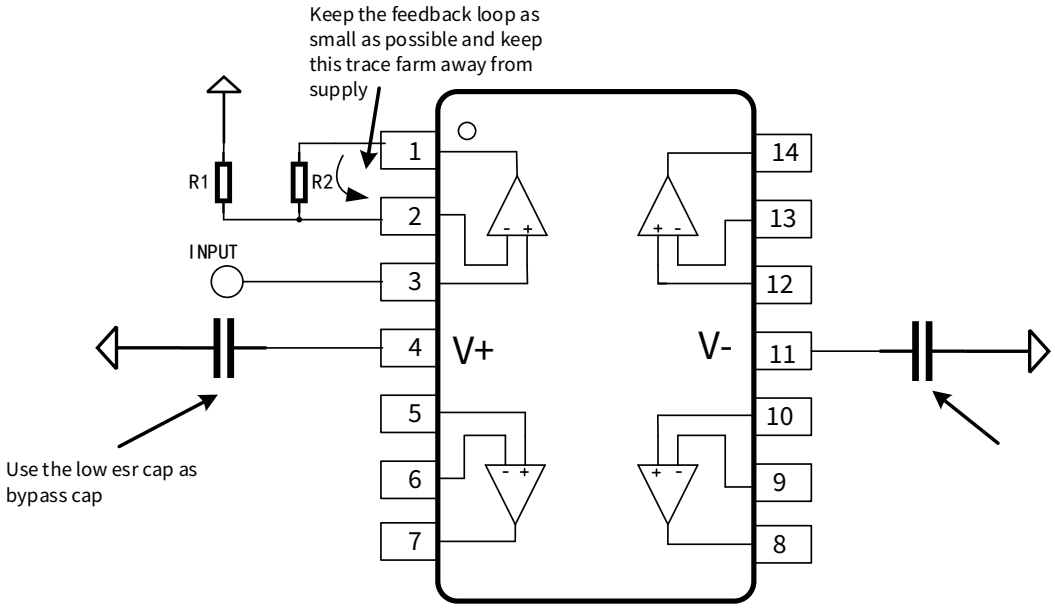
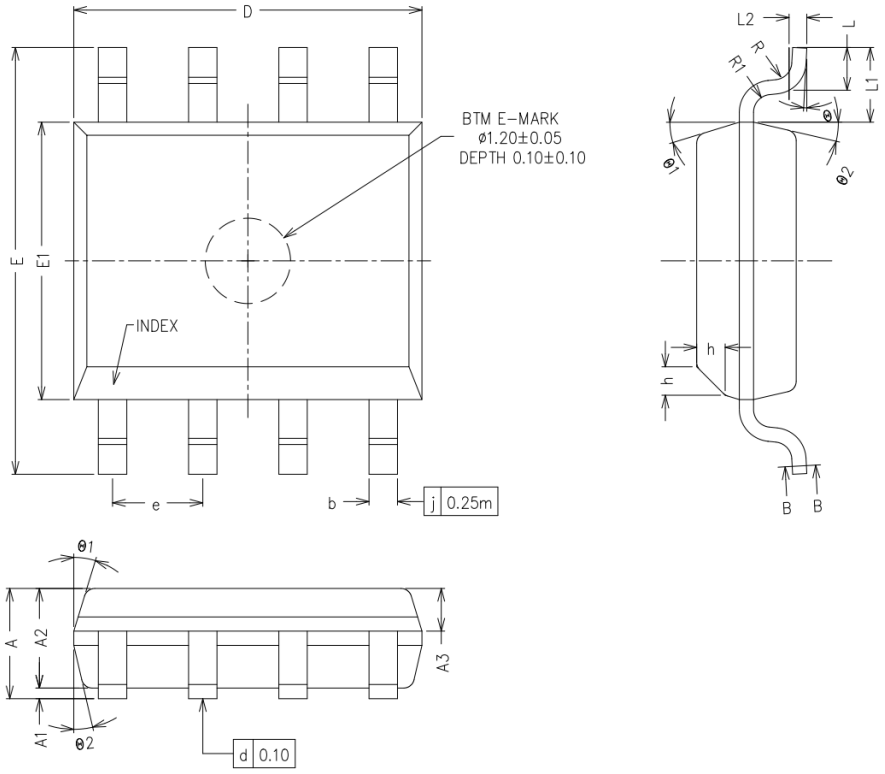


Figure 10-1 Layout Example

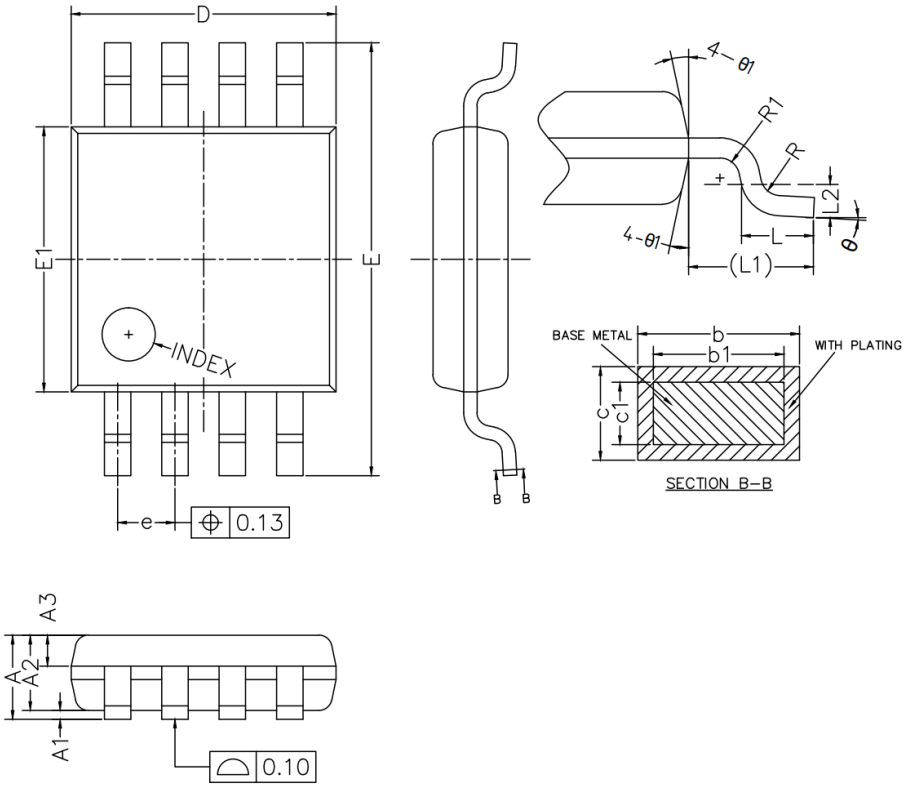
11. Package Information

11.1. SOP8



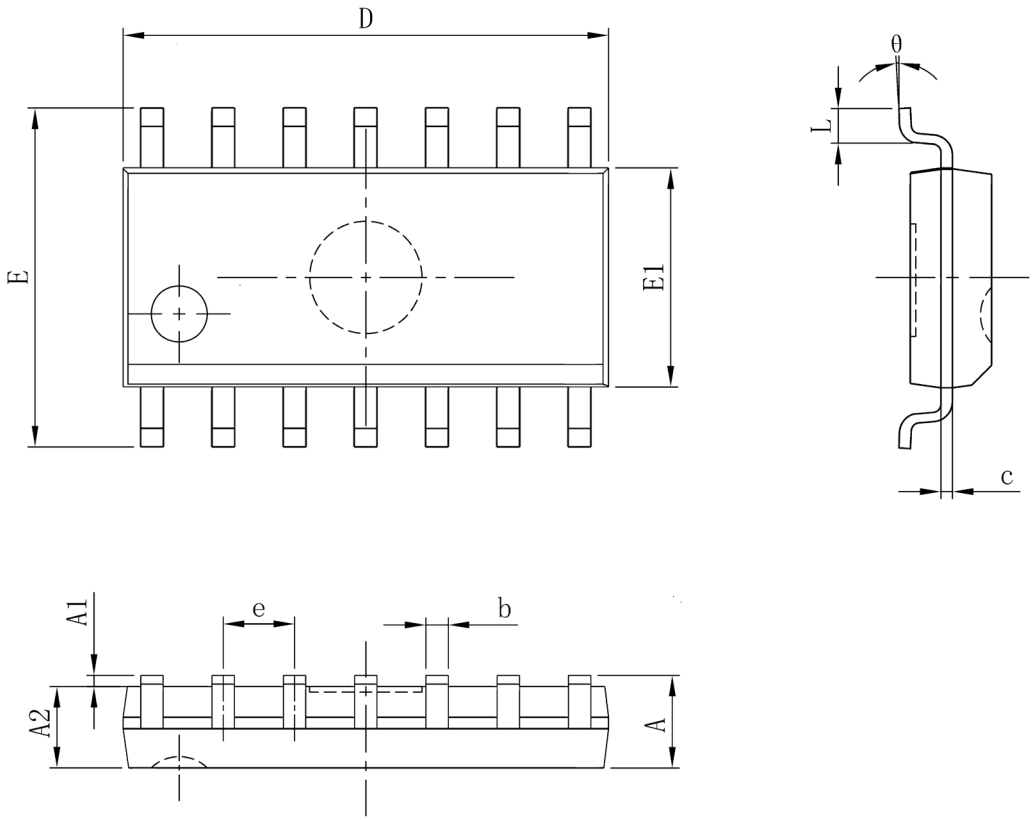
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.75	— —	0.069
A1	0.05	0.25	0.002	0.01
A2	1.30	1.50	0.051	0.059
A3	0.50	0.70	0.020	0.028
b	0.38	0.47	0.015	0.019
b1	0.37	0.40	0.015	0.016
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.15	0.157
e	1.17	1.37	0.046	0.054
L	0.45	0.80	0.018	0.031
L1	1.04REF		0.041REF	
L2	0.25BSC		0.010BSC	
R	0.07	— —	0.003	— —
R1	0.07	— —	0.003	— —
h	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°
θ1	15°	19°	15°	19°
θ2	11°	15°	11°	15°

11.2. MSOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.10	— —	0.043
A1	0.05	0.15	0.002	0.006
A2	0.75	0.95	0.030	0.037
A3	0.30	0.40	0.012	0.016
b	0.25	0.38	0.010	0.015
b1	0.24	0.33	0.009	0.013
c	0.15	0.20	0.006	0.008
c1	0.14	0.16	0.006	0.0062
D	2.90	3.10	0.114	0.122
E	4.75	5.05	0.187	0.199
E1	2.90	3.10	0.114	0.122
e	0.55	0.75	0.022	0.030
L	0.40	0.70	0.016	0.028
L1	0.95REF		0.037(BSC)	
L2	0.25BSC		0.010	
R	0.07	— —	0°	8°
R1	0.07	— —	0.003	— —
θ	0°	8°	0°	8°
θ1	9°	15°	9°	15°

11.3. SOP14

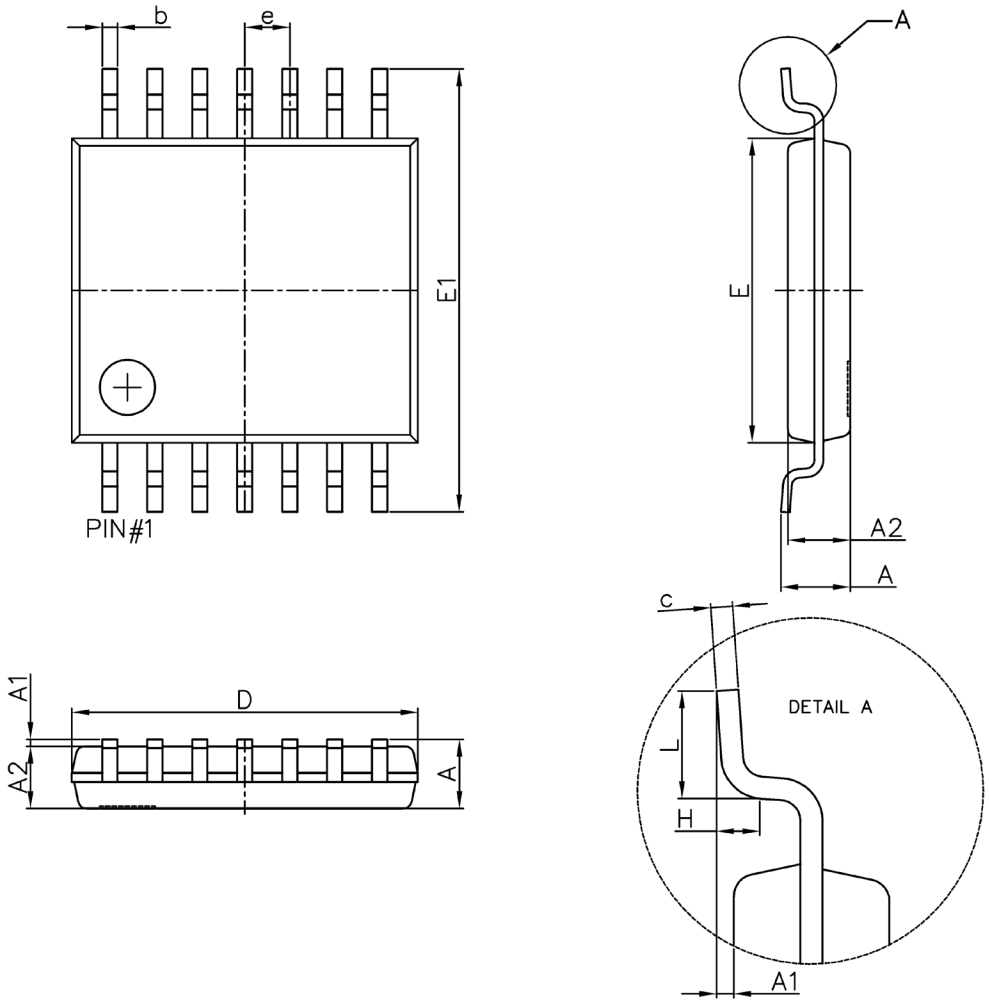


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	— —	1.75	— —	0.069
A1	0.1	0.25	0.004	0.01
A2	1.25	— —	0.049	— —
b	0.31	0.51	0.012	0.02
c	0.1	0.25	0.004	0.01
D	8.45	8.85	0.333	0.348
E	5.8	6.2	0.228	0.244
E1	3.8	4	0.15	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.4	0.08	0.016	0.031
θ	0°	8°	0°	8°

Note:

1. Unit: mm.

11.4. TSSOP14

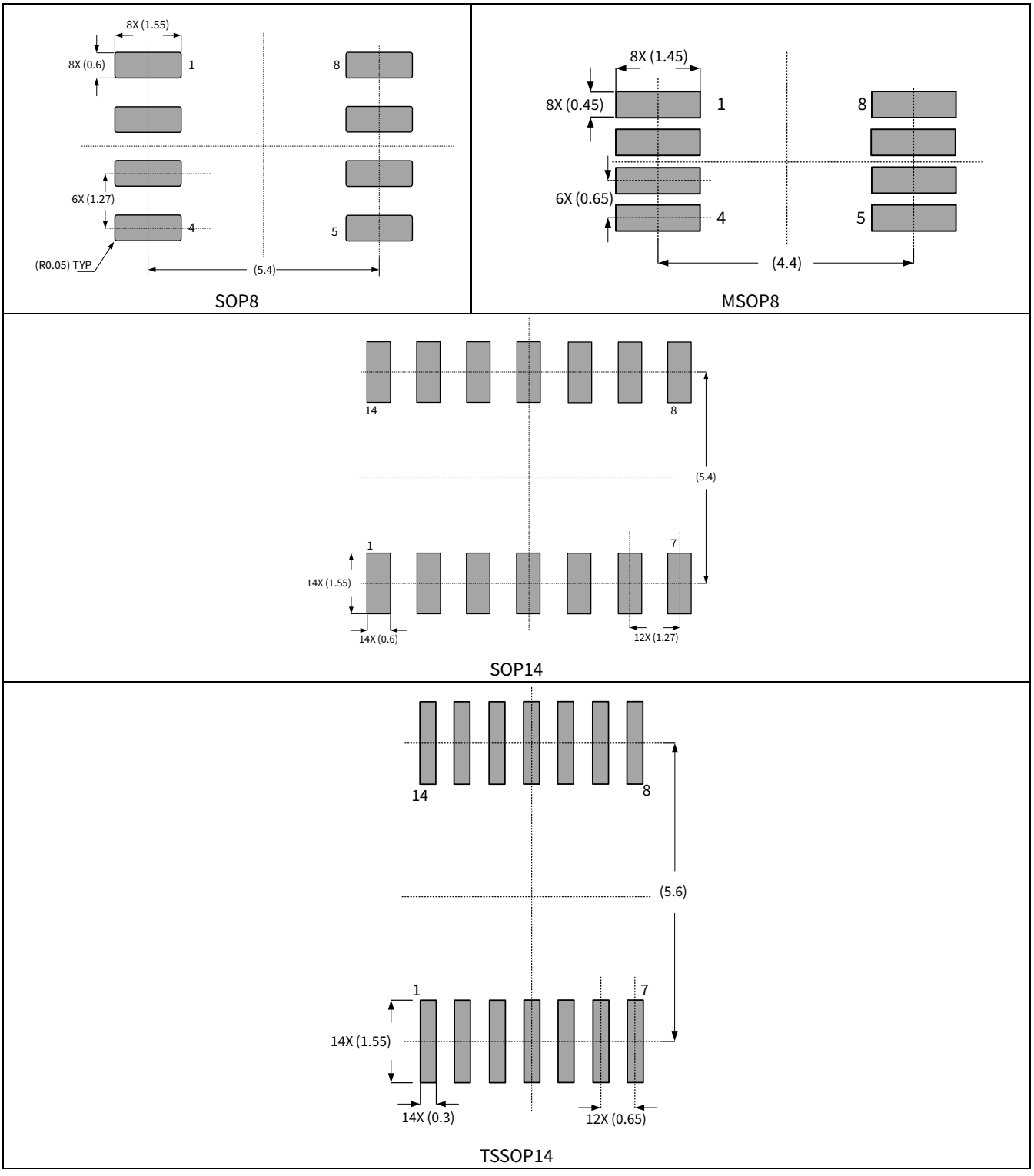


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
D	4.9	5.1	0.193	0.201
E	4.3	4.5	0.169	0.177
b	0.19	0.3	0.007	0.012
c	0.09	0.2	0.004	0.008
E1	6.20	6.60	0.244	0.260
A	—	1.2	—	0.047
A2	0.8	1.05	0.031	0.041
A1	0.05	0.15	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.45	0.75	0.018	0.030
H	0.25(TYP)		0.01(TYP)	
θ	0°	8°	0°	8°

Note:

1. Unit: mm.

11.5. Example of Solder Pads Dimensions



Note:

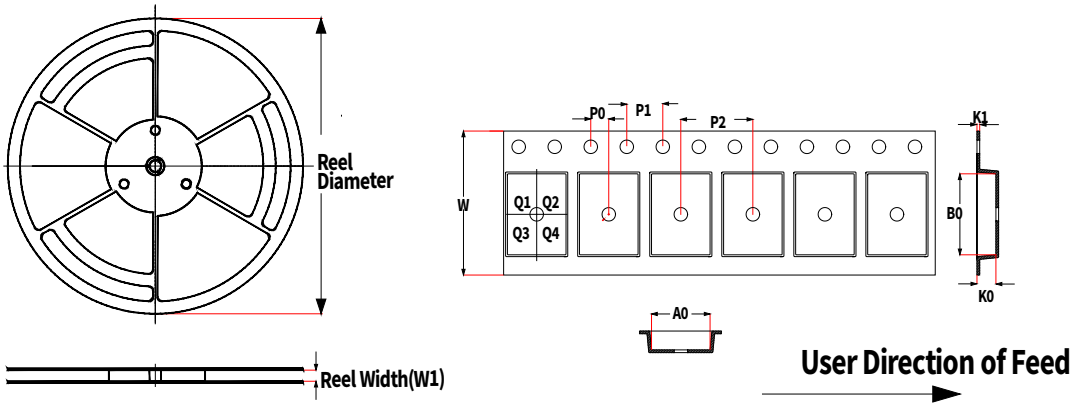
1. Unit: mm.

12. Order Information

Part Number	*Package*	*MSL Level*	*Op Temp (°C)*	*SPQ*
NSOPA082-DSPR	SOP8	1	-40~+125	4000
NSOPA082-DMPR	MSOP8	1	-40~+125	4000
NSOPA084-DTSKR	TSSOP14	1	-40~+125	3000
NSOPA084-DSPKR	SOP14	1	-40~+125	3000
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.				

If NSOPA082-DMPR versions are required, please contact Novosense for special support.

13. Tape and Reel Information



Device	Reel Diameter	Reel Width(W1)	W	A0	B0	P0	P1	P2	K0	K1	PIN1 Quadrant
NSOPA082-DSPR	330	12.4	12	6.55	5.3	2	4	8	2	0.25	Q1
NSOPA084-DTSKR	330	12.4	12	6.8	5.4	2	4	8	1.2	0.3	Q1
NSOPA084-DSPKR	330	16.4	16	6.5	9	2	4	8	2.1	0.3	Q1

Note:

1. All dimensions are nominal.
2. The picture is only for reference. Please make the object as the standard.
3. Unit: mm.

14. Revision History

Revision	Description	Date
V1.0	Initial version	2024/03
V1.1	Add example of solder pads dimensions Add reflow note in order information table	2024/08
V1.2	Add NSOPA082 parts	2024/10

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