NCA1057-Q1
High-speed CAN Transceiver
Datasheet (EN) 1.0

Product Overview

The NCA1057-Q1 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The NCA1057-Q1 implements the CAN physical layer as defined in ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The NCA1057-Q1 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Ideal passive behavior to the CAN bus when the supply voltage is off
- I/O voltage range supports 1.8V, 3.3V and 5V MCU
- Power supply voltage
- V_{IO}: 1.7V to 5.5V
- V_{CC}: 4.5V to 5.5V
- Bus fault protection of -58V to +58V
- Bus common-mode voltage of -30V to +30V
- Transmit data (TXD) dominant time out function
- Over temperature protection
- Data rate: up to 5Mbps
- Low loop delay: <250ns
- Operation temperature: -40°C to +125°C
- AEC-Q100 qualified for automotive, Grade 1
- RoHS & REACH compliant

Applications

- CAN bus standards such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783 and CANaerospace
- Highly loaded CAN networks down to 10 kbps networks
- Automotive gateway
- Body control modules
- Advanced Driver Assistance Systems (ADAS)
- Infotainment system

Device Information

Part Number	*Package*	*Body Size*
NCA1057-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1057-Q1DNR	DFN8	3.00mm × 3.00mm
NCA1057N-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1057N-Q1DNR	DFN8	3.00mm × 3.00mm

Functional Block Diagrams

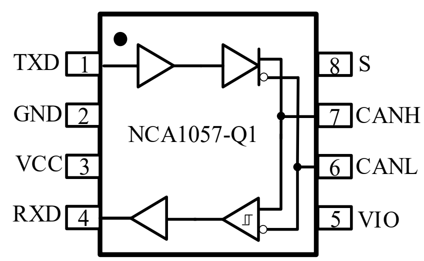

Figure 1. NCA1057-Q1 Block Diagram

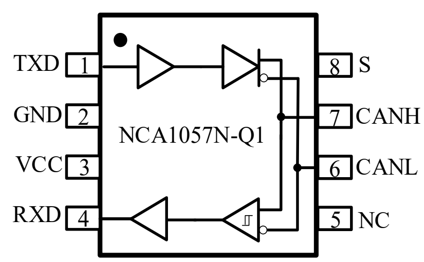

Figure 2. NCA1057N-Q1 Block Diagram

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1. Pin Configuration and Functions

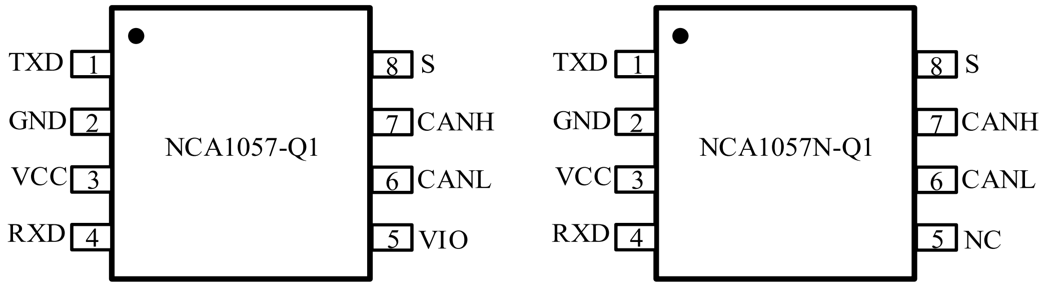

Figure 1-1 NCA1057-Q1, NCA1057N-Q1 Package

Table 1-1 NCA1057-Q1 Pin Configuration and Description

NCA1057-Q1 PIN NO.	*NCA1057N-Q1 PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	2	GND	Ground
3	3	VCC	Power Supply
4	4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	\	VIO	Logic I/O supply voltage
\	5	NC	No connection
6	6	CANL	Low-level CAN bus line
7	7	CANH	High-level CAN bus line
8	8	S	S (silent mode) select pin (active high)

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2. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [1] [2].

Parameters	Symbol	Min	Max	Unit
Power Supply Voltage	VCC, VIO	-0.3	7	V
Logic I/O Voltage	TXD, RXD, S	-0.3	7	V
Maximum bus Pin Voltage	V_{CANH}, V_{CANL}	-58	58	V
Voltage between pin CANH and pin CANL	V_{CANH} - V_{CANL}	-58	58	V
Junction temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating condition for extended periods may affect device reliability.

[2] All voltage values, except for "Voltage between pin CANH and pin CANL", are with respect to GND terminal.

3. EMC Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge	Human Body Model (HBM), per AEC-Q100-002 ● CANH and CANL, to GND ● Other pins, to GND	 ±8 ±8	 kV kV
	Charged Device Model (CDM), per AEC-Q100-011 ● All pins	 ±2	 kV
	Machine Model (MM), per JESD22-A115C ● All pins	 ±400	 V
Electrical disturbances	Electrical transient conduction, per ISO 7637-2, on CANH and CANL ● Pulse 1 ● Pulse 2a ● Pulse 3a ● Pulse 3b	 -100 75 -150 100	 V V V V

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4. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Power Supply Voltage	VCC	4.5	5	5.5	V
I/O Level-Shifting Voltage	VIO	1.7	3.3	5.5	V
Operating Temperature	T_{opr}	-40	-	125	°C

5. Thermal Information

Parameters	*Symbol*	*SOP8*	*DFN8*	*Unit*
IC Junction-to-Air Thermal Resistance	$R_{\theta JA}$	120	52.8	°C /W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	57.8	58.9	°C /W
Junction-to-board thermal resistance	$R_{\theta JB}$	64.2	25.2	°C /W

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6. Specifications

6.1. Electrical Characteristics

V_{CC}=4.5V to 5.5V, V_{IO}=1.7 to 5.5V [1], Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{CC}=5V, V_{IO}=3.3V, R_L=60Ω, Ta = 25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	Supply voltage		4.5	-	5.5	V
I_{CC}	Supply current	Normal mode, recessive, V_{TXD}=V_{IO} [2], V_S=0V	-	5	7	mA
		Normal mode, dominant, V_{TXD} =0V	-	45	60	mA
		Normal mode, dominant, V_{TXD} =0, short circuit on bus lines, -3V < (V_{CANH} = V_{CANL}) < 18V	-	-	110	mA
		Silent mode, V_{TXD} =V_{IO} [2]	-	-	2.5	mA
$V_{uvd(VCC)}$	Undervoltage detection voltage on pin VCC	Rising	4	4.26	4.5	V
		Falling	4	4.17	4.5	V
I/O level adapter supply; pin V_{IO}; only for NCA1057-Q1						
V_{IO}	Supply voltage on pin VIO		1.7	-	5.5	V
I_{IO}	Supply current on pin VIO	Normal mode, recessive, V_{TXD}=V_{IO}	-	12	30	µA
		Normal mode, dominant, V_{TXD}=0V	-	120	320	µA
		Silent mode; V_{TXD}=V_{IO}	-	10	16	µA
$V_{uvd(VIO)}$	Undervoltage detection voltage on pin VIO	Rising	1.4	1.56	1.7	V
		Falling	1.4	1.50	1.7	V
Silent mode control input; pin S						
V_{IH}	High level input voltage	NCA1057-Q1	0.7*V_{IO}	-	V_{IO}+0.3	V
		NCA1057N-Q1	2.0	-	V_{CC}+0.3	V
V_{IL}	Low level input voltage	NCA1057-Q1	-0.3	-	0.3*V_{IO}	V
		NCA1057N-Q1	-0.3	-	0.8	V
I_{IH}	High level input current	V_S=V_{IO}	-1	-	15	µA
I_{IL}	Low level input current	V_S=0V	-1	-	1	µA
CAN transmit data input; pin TXD						
V_{IH}	High level input voltage	NCA1057-Q1	0.7*V_{IO}	-	V_{IO}+0.3	V
		NCA1057N-Q1	2.0	-	V_{CC}+0.3	V

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V_{IL}	Low level input voltage	NCA1057-Q1	-0.3	-	0.3*V_{IO}	V
		NCA1057N-Q1	-0.3	-	0.8	V
R_{pu}	Pull-up resistance		40	55	80	kΩ
C_i	Input capacitance	[3]	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	High level output current	$V_{RXD} = V_{IO}$ - 0.4V [2]	-10	-3	-1	mA
I_{OL}	Low level output current	V_{RXD} = 0.4V; bus dominant	1	3.5	10	mA
Bus lines; pins CANH and CANL; Driver						
$V_{OH(D)}$	CANH output voltage (Dominant)	V_{TXD} =0V, R_L =50Ω to 65Ω[4]	2.75	3.6	4.5	V
$V_{OL(D)}$	CANL output voltage (Dominant)	V_{TXD} =0V, R_L =50Ω to 65Ω[4]	0.5	1.4	2.25	V
$V_{OH(R)}$	CANH output voltage (Recessive)	Normal/ silent mode, no load[4]	2.0	0.5*V_{CC}	3.0	V
$V_{OL(R)}$	CANL output voltage (Recessive)	Normal/ silent mode, no load[4]	2.0	0.5*V_{CC}	3.0	V
$V_{OD(D)}$	Differential output voltage (Dominant)	Normal mode				
		R_L = 50Ω to 65Ω[4]	1.5	-	3.0	V
		R_L = 45Ω to 70Ω[4]	1.4	-	3.3	V
		R_L = 2240Ω[4]	1.5	-	5.0	V
$V_{OD(R)}$	Differential output voltage (Recessive)	Normal mode, no load[4]	-50	-	50	mV
V_{TXsym}	Transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$, [3] f_{TXD} = 1MHz, R_L=60Ω, C_{SPLIT} = 4.7nF, V_{CC} = 4.75V to 5.25V[4] [5]	0.9*V_{CC}	-	1.1*V_{CC}	V
$I_{OSH(R)}$	CANH short-circuit output current, recessive	Normal mode, $V_{CANH} = V_{CANL}$ = -27V to 32V	-2	-	2	mA
$I_{OSL(R)}$	CANL short-circuit output current, recessive	Normal mode, $V_{CANH} = V_{CANL}$ = -27V to 32V	-2	-	2	mA
$I_{OSH(D)}$	CANH short-circuit output current, dominant	Normal mode, V_{CANH} = -15V to 40V, CANL open[4]	-100	-	100	mA
$I_{OSL(D)}$	CANL short-circuit output current, dominant	Normal mode, V_{CANL} = -15V to 40V, CANH open[4]	-100	-	100	mA
Bus lines; pins CANH and CANL; Receiver						

$V_{ID(R)}$	Differential input threshold voltage, recessive	Normal/ silent mode[4] $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	0.5	-	0.9	V
$V_{ID(D)}$	Differential input threshold voltage, dominant	Normal/ silent mode[4] $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	0.5	-	0.9	V
V_{hys}	Differential input hysteresis voltage	Normal/ silent mode $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	-	50	100	mV
$V_{RX(R)}$	Receiver recessive voltage	Normal/ silent mode $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	-4	-	0.5	V
$V_{RX(D)}$	Receiver dominant voltage	Normal/ silent mode $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	0.9	-	9	V
$I_{LKG(OFF)}$	Power-off (unpowered) bus input leakage current	$V_{CANH} = V_{CANL} = 5V$, $V_{CC} = V_{IO} = 0V$[4]	-10	-	10	µA
R_I	Input resistance	$-2V \le V_{CANH} \le 7V$, $-2V \le V_{CANL} \le 7V$ [3] [4]	25	40	50	kΩ
$R_{I(match)}$	Input resistance matching	$V_{CANH} = 5V$, $V_{CANL} = 5V$, $R_{I(match)}=2*(R_{CANH}-R_{CANL}) / (R_{CANH}+R_{CANL})$ [3]	-1	-	1	%
R_{ID}	Differential input resistance	$-2V \le V_{CANH} \le 7V$, $-2V \le V_{CANL} \le 7V$, $R_{ID}=R_{CANH}+R_{CANL}$ [3] [4]	50	80	100	kΩ
C_I	Input capacitance to ground	CANH or CANL[3]	-	-	30	pF
C_{ID}	Differential input	[3]	-	-	15	pF
Temperature detection						
T_{SD}	Thermal shutdown threshold	[3]	-	193	-	°C
$T_{SD(hys)}$	Thermal shutdown hysteresis	[3]	-	11	-	°C

[1] Only NCA1057-Q1 has a VIO pin. For NCA1057N-Q1, the VIO input is internally connected to VCC.

[2] $V_{IO}=V_{CC}$ for the version without VIO pin.

[3] Not tested in production; guaranteed by design.

[4] Required in ISO 11898-2-2024.

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[5] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 6-3.

6.2. Switching Electrical Characteristics

V_{CC} =4.5V~5.5V, V_{IO}=1.7~5.5V[1], Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, R_L=60Ω, Ta = 25°C.

Symbol	Parameters	Comments	Min	Typ	Max	Unit
Driver						
$t_{d(TXD\text{-}bus,\ dom)}$	Delay time from TXD to bus dominant	Normal mode[3]	-	40	-	ns
$t_{d(TXD\text{-}bus,\ rec)}$	Delay time from TXD to bus recessive	Normal mode[3]	-	65	-	ns
$t_{bit(bus)}$	Transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns	155	-	210	ns
Receiver						
$t_{d(bus\text{-}RXD,\ dom)}$	Delay time from bus to RXD dominant	[3]	-	110	-	ns
$t_{d(bus\text{-}RXD,\ rec)}$	Delay time from bus to RXD recessive	[3]	-	100	-	ns
$t_{d(TXD\text{-}RXD,\ dom)}$	Delay time from TXD to RXD dominant	Normal mode[3]	-	150	255	ns
$t_{d(TXD\text{-}RXD,\ rec)}$	Delay time from TXD to RXD recessive	Normal mode[3]	-	165	255	ns
$t_{bit(RXD)}$	Bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns	120	-	220	ns
CAN FD timing characteristics						
Δt_{rec}	Receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$ [3]				
		$t_{bit(TXD)}$ = 500 ns	-65	-	40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-	15	ns
Dominant time-out time; pin TXD						
$t_{to(dom)TXD}$	TXD dominant time-out time	Normal mode[3]	0.8	2.8	5	ms

[1] Only NCA1057-Q1 has a VIO pin. For NCA1057N-Q1, the VIO input is internally connected to VCC.

[2] Not tested in production; guaranteed by design.

[3] Required in ISO 11898-2-2024.

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6.3. Parameter Measurement Information

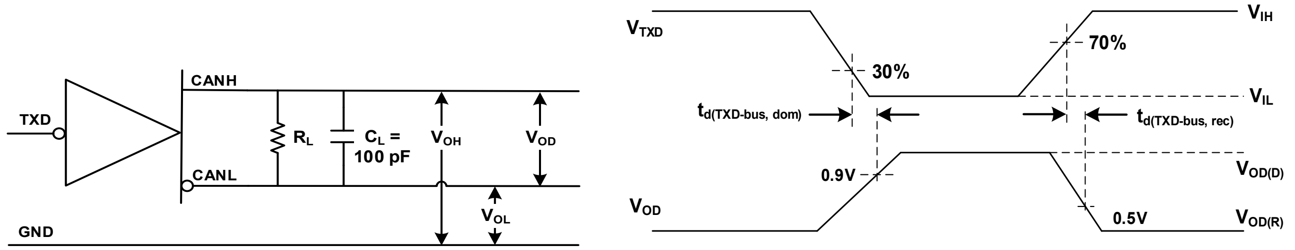

Figure 6-1 Driver Test Circuit and Voltage Waveforms[1]

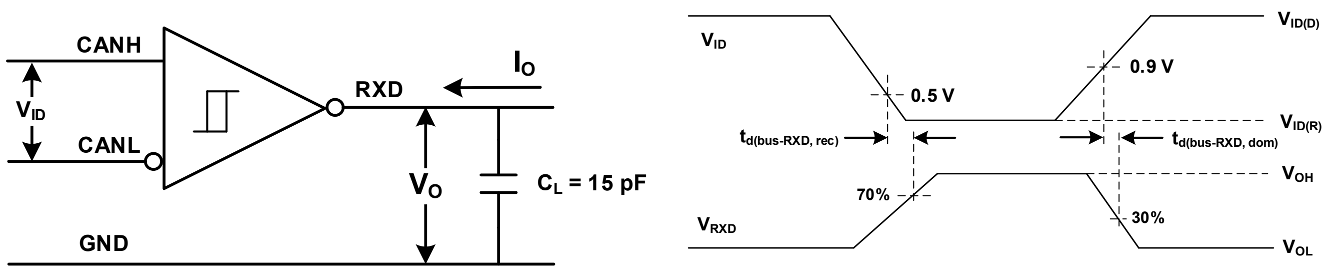

Figure 6-2 Receiver Test Circuit and Voltage Waveforms

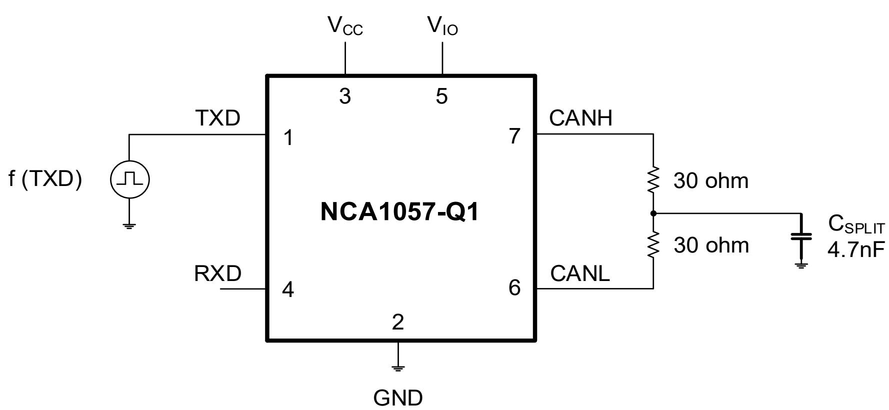

Figure 6-3 Transceiver Driver Symmetry Test Circuit

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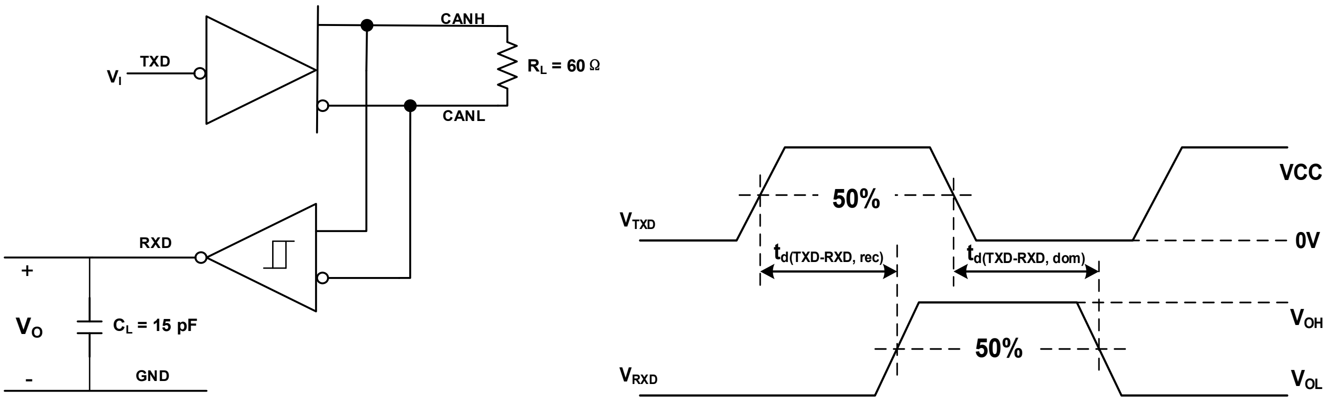

Figure 6-4 Loop Time Test Circuit and Voltage Waveforms

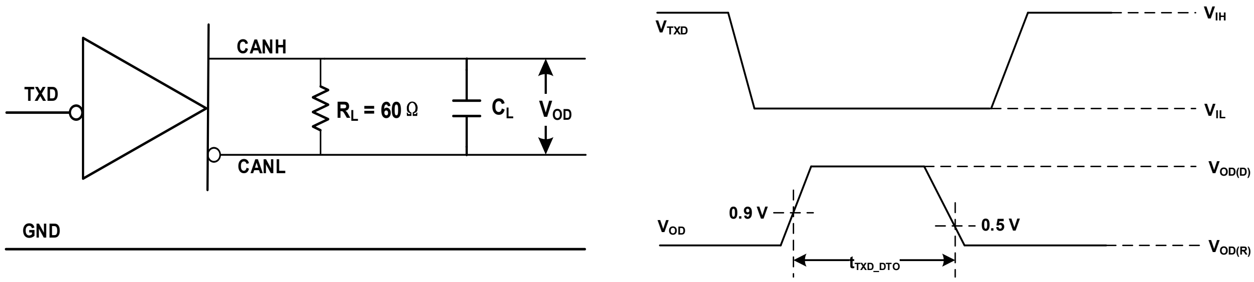

Figure 6-5 TXD Dominant Time-out Test Circuit and Voltage Waveforms

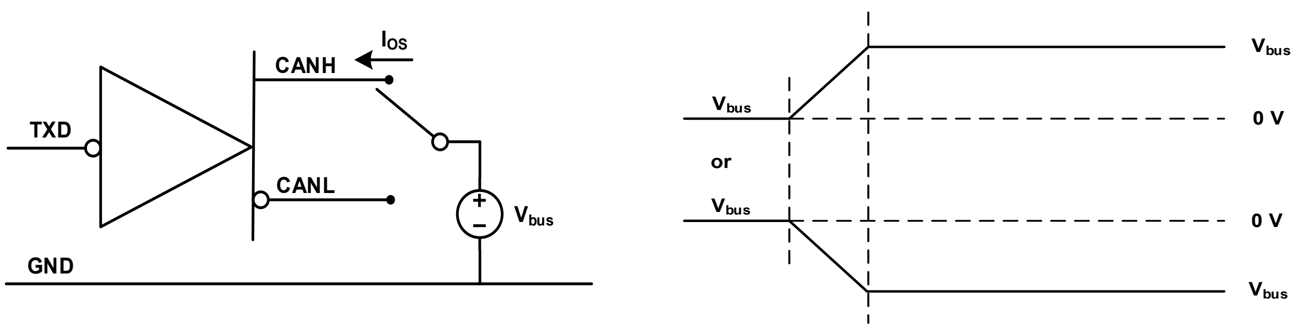

Figure 6-6 Driver Short-Circuit Current Test Circuit and Waveforms

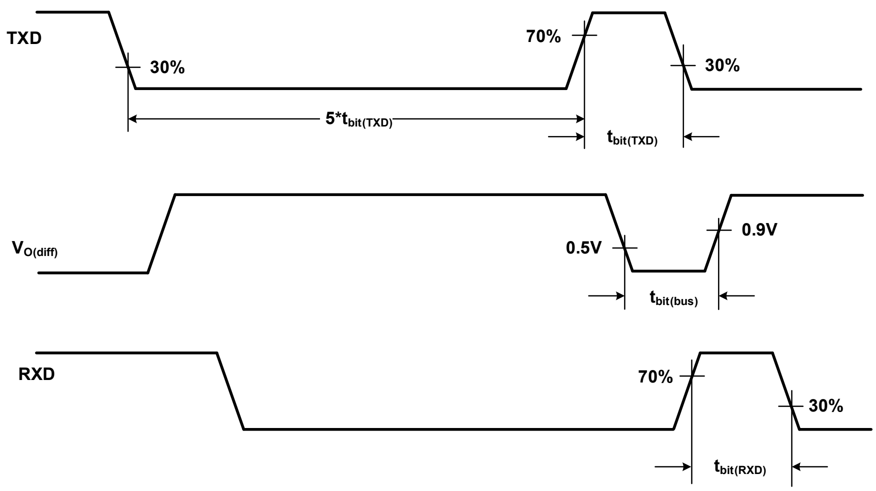

Figure 6-7 $t_{bit(RXD)}$ Test Circuit and Waveforms[1]

[1] For NCA1057N-Q1, TXD high level is set as 2.0V instead; TXD low level, 0.8V instead.

7. Function Description

7.1. Overview

The NCA1057-Q1 is a CAN transceiver which fully compatible with the ISO11898-2 standard. The data rate of the NCA1057-Q1 is up to 5Mbps, and it can support up to 110 CAN nodes. Meanwhile, the maximum transmission rate of the CAN bus is limited by the bus load, the quantity of nodes, the cable length, and other factors. The NCA1057-Q1 has a ±30V input common-mode range, enabling reliable communication between bus nodes with large ground potential deviations.

Comprehensive protection features are designed to enhance the device and network robustness in harsh operating conditions. The transmit data dominant time-out function prevents the bus from lock-up by the faults on micro-controller. Moreover, the NCA1057-Q1 provides thermal protection and short-circuit protection.

7.2. Functional Block Diagram

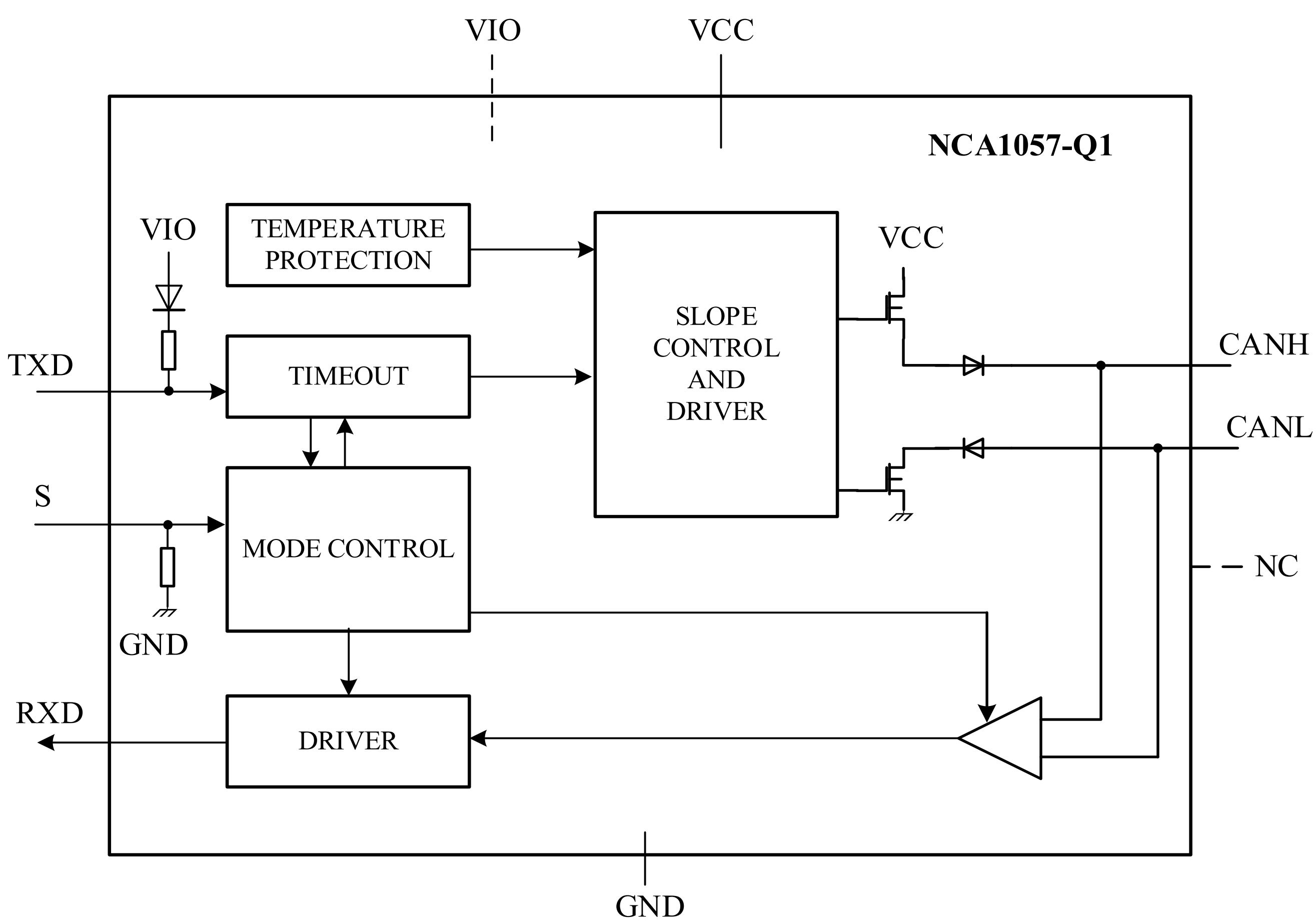

Figure 7-1 Block diagram of NCA1057-Q1

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7.3. VIO Supply Pin

Two versions of the NCA1057-Q1 are available, only differing in the function of a single pin. Pin 5 is either a VIO supply pin or a NC pin.

Pin VIO should be connected to the microcontroller supply voltage (see Figure 8-1). This will adjust the signal levels of pins TXD, RXD and S to the I/O levels of the microcontroller.

For versions of the NCA1057N-Q1 without a VIO pin, the VIO input is internally connected to VCC. This sets the signal levels of pins TXD, RXD and S to levels compatible with 5 V microcontrollers.

7.4. Device Operating Modes

The device has two main operating modes: Normal mode and Silent mode. Operating mode is selected via the S input pin. Table 7-1 shows a description of the operating modes under normal supply conditions.

Table 7-1 Operating Modes

Mode	S pin	TXD pin	CAN driver	RXD pin
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Silent	HIGH	X	recessive	LOW when bus dominant
				HIGH when bus recessive

7.4.1. Normal Mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 7-1). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible Electromagnetic Emission (EME).

After entering normal mode, it is recommended to firstly pull up TXD pin to a high level for at least 200ns before communications, for fear of unwanted TXD timeout caused by unstable TXD level during the power-on phase.

7.4.2. Silent Mode

A HIGH level on pin S selects Silent mode. In Silent mode, the transmitter is disabled, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

7.5. Fail-safe features

7.5.1. TXD Dominant Time-Out Function (TXD DTO)

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value $t_{to(dom)TXD}$, the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

7.5.2. Internal Biasing of TXD and S Input Pins

Pin TXD has an internal pull-up to VIO to ensure a safe, defined state, in case the pin is left floating. Pin S, an internal pull-down to GND. Pull-up current in TXD and pull-down current in S flow in these pins in all states.

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7.5.3. Undervoltage Detection on Pins VCC and VIO

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the VCC or VIO supply terminals.

When VCC or VIO drop below their respective undervoltage detection levels, $V_{uvd(VCC)}$ and $V_{uvd(VIO)}$, the transceiver will switch off and disengage from the bus (zero load) until VCC and VIO have recovered.

Table 7-2 Undervoltage Lockout 5V Only Devices (NCA1057N-Q1)

VCC	Device State	Bus Output	RXD
$>UV_{VCC}$	Normal	Per TXD	Mirrors Bus[1]
$<UV_{VCC}$	Off	High Impedance	High Impedance

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 7-3 Undervoltage Lockout I/O Level Shifting Devices (NCA1057-Q1)

VCC	VIO	Device State	Bus Output	RXD
$>UV_{VCC}$	$>UV_{VIO}$	Normal	Per TXD	Mirrors Bus[1]
$<UV_{VCC}$	$>UV_{VIO}$	Off	High Impedance	High Impedance
$>UV_{VCC}$	$<UV_{VIO}$	Off	High Impedance	High Impedance
$<UV_{VCC}$	$<UV_{VIO}$	Off	High Impedance	High Impedance

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

7.5.4. Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

7.5.5. Over-Temperature Protection (OTP)

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{SD}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{SD} and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

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8. Application Note

8.1. Typical Application

The NCA1057-Q1 requires a 0.1 µF bypass capacitors between VCC and GND. The capacitor should be placed as close as possible to the package. The Figure 8-1 and Figure 8-2 are the typical applications of NCA1057-Q1.

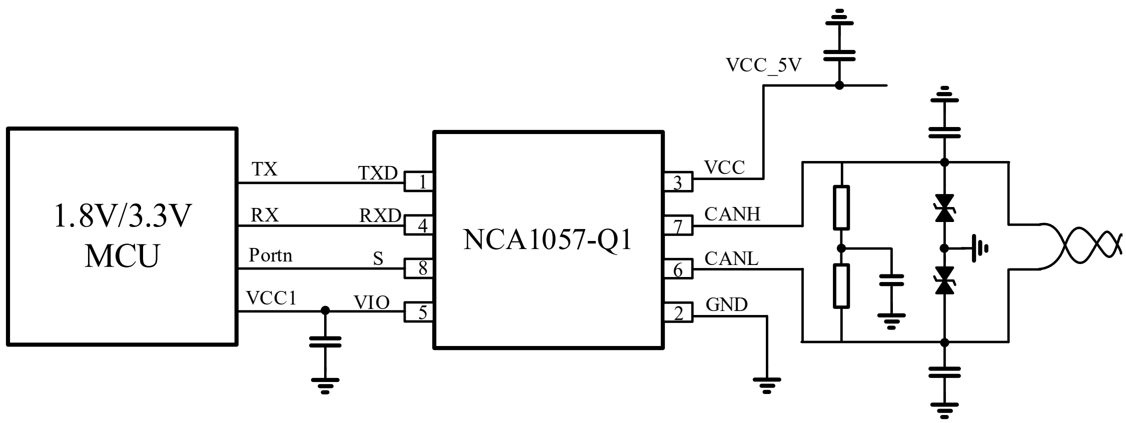

Figure 8-1 Typical CAN Bus Application Using 1.8V/3.3V CAN Controller

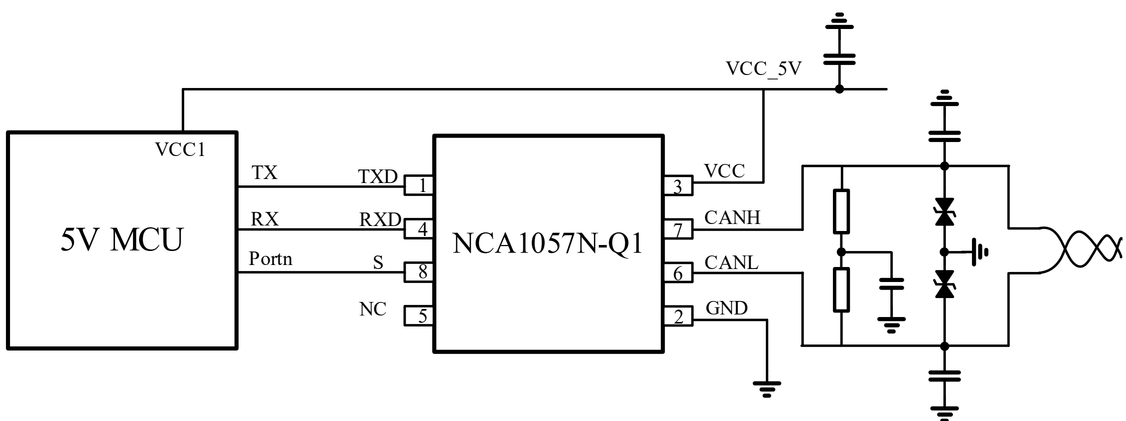

Figure 8-2 Typical CAN Bus Application Using 5V CAN Controller

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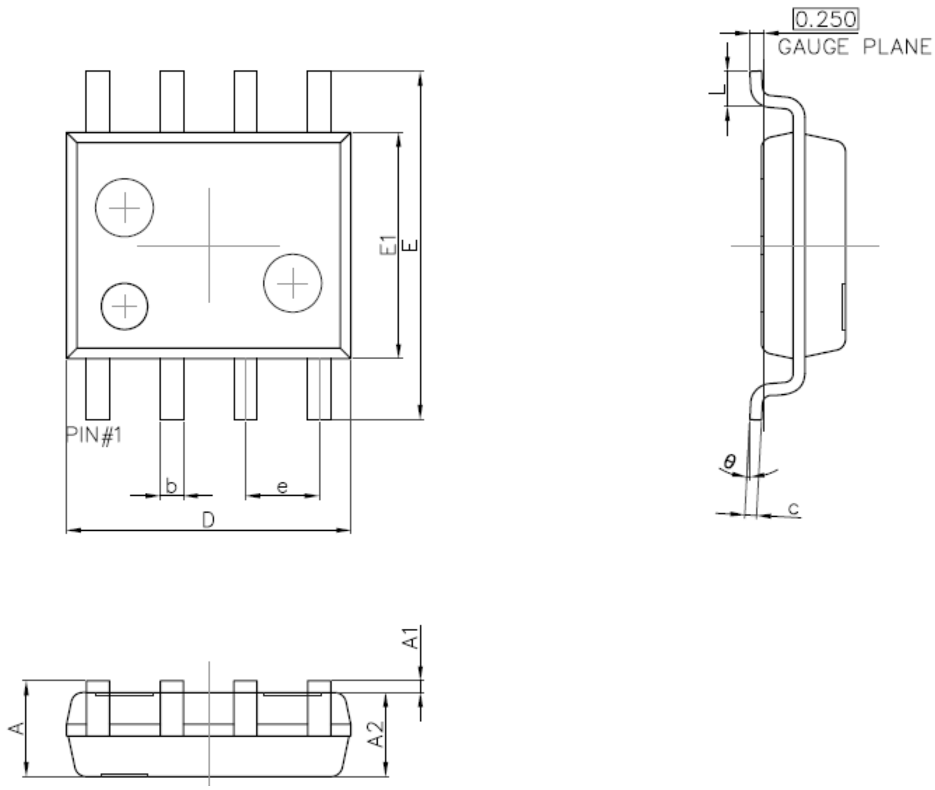
9. Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Figure 9-1 SOP8 Package Shape and Dimension

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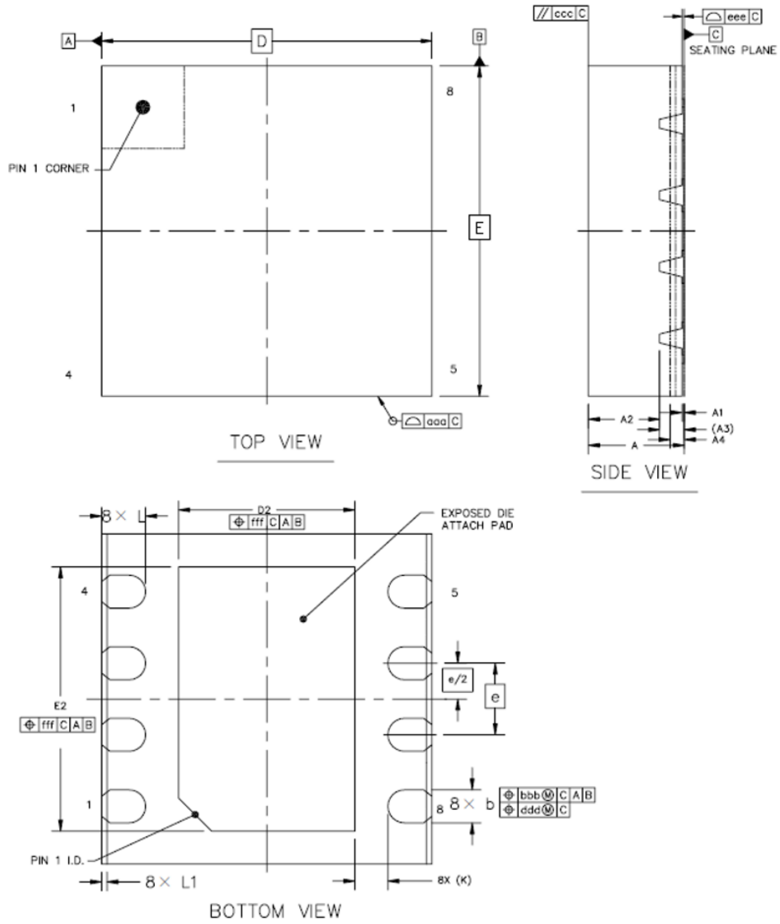

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0	0.02	0.0500
MOLD THICKNESS		A2	---	0.6	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD WIDTH		b	0.25	0.30	0.35
LEAD PITCH		e		0.65 BSC	
EP SIZE	X	D2	1.5	1.6	1.7
	Y	E2	2.3	2.4	2.5
LEAD LENGTH		L	0.35	0.4	0.45
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1000	
MOLD FLATNESS		ccc		0.1000	
COPLANARITY		eee		0.0800	
LEAD OFFSET		bbb		0.1000	
		ddd		0.0500	
EXPOSED PAD OFFSET		fff		0.1000	

Figure 9-2 DFN8 Package Shape and Dimension

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10. Ordering Information

Part Number	*Operation Temperature*	*MSL*	*Package Type*	*SPQ*
NCA1057-Q1SPR	-40 to 125°C	3	SOP8	2500
NCA1057-Q1DNR	-40 to 125°C	2	DFN8	6000
NCA1057N-Q1SPR	-40 to 125°C	3	SOP8	2500
NCA1057N-Q1DNR	-40 to 125°C	2	DFN8	6000

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*
NCA1057-Q1	Click here	Click here	Click here

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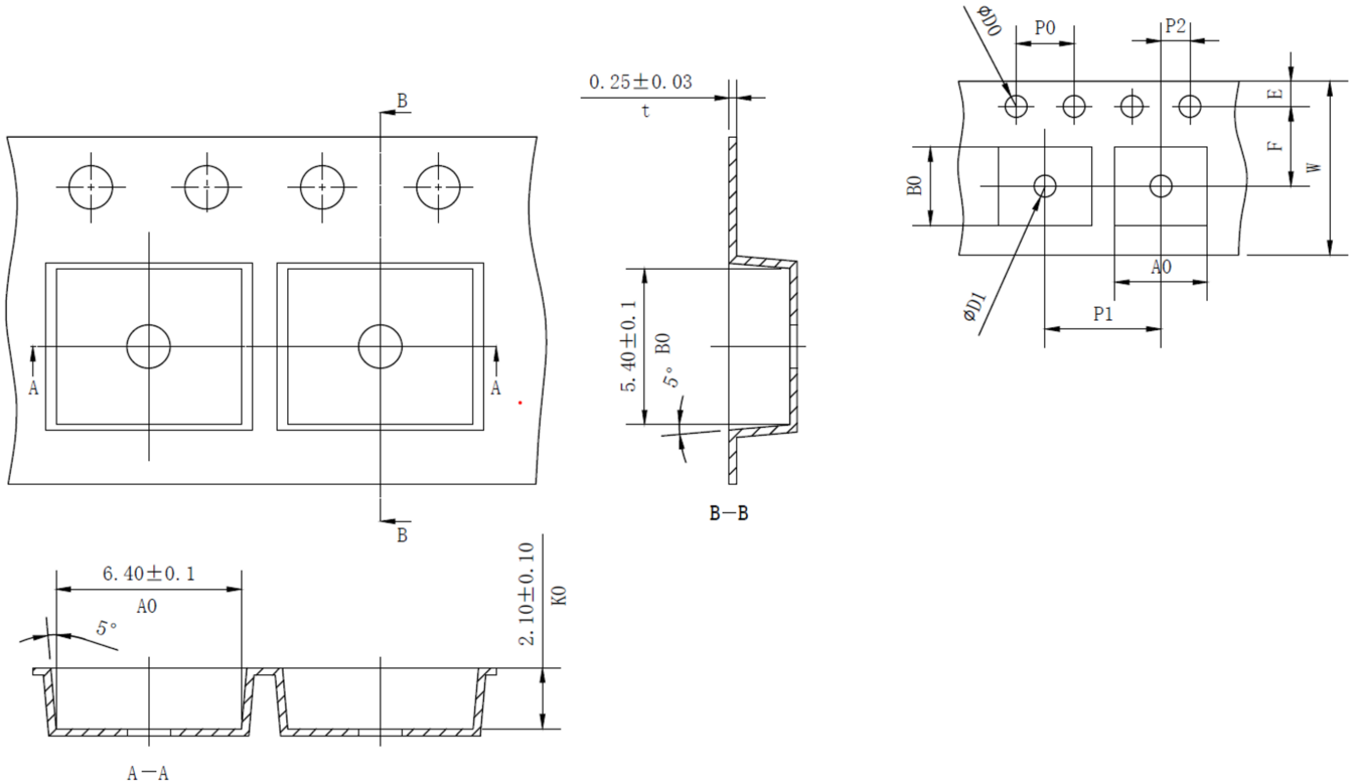
12. Tape and Reel Information



W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	t
12. 00+ +0. 30/−0. 10	1. 75 ±0. 10	5. 50 ±0. 05	1. 50 +0. 10/−0	1. 50 +0. 25/−0	4. 00 ±0. 10	2. 00 ±0. 05	40. 00 ±0. 20	8. 00 ±0. 10	6. 40 ±0. 10		5. 40 ±0. 10		2. 10 ±0. 10		0. 25 ±0. 03

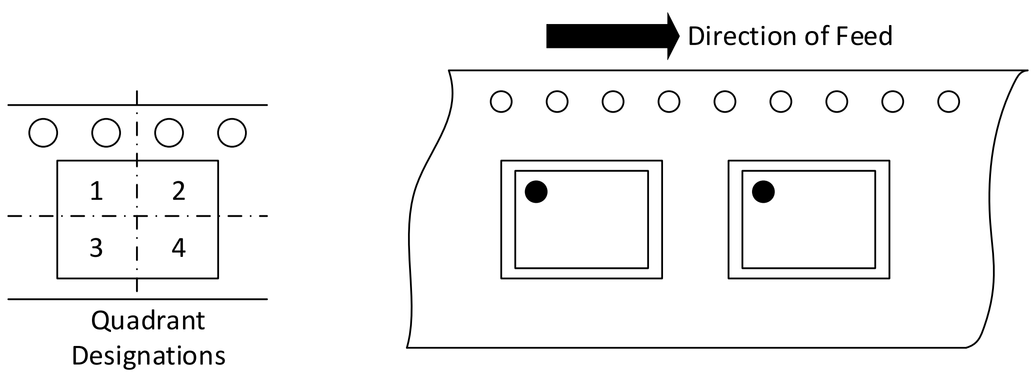
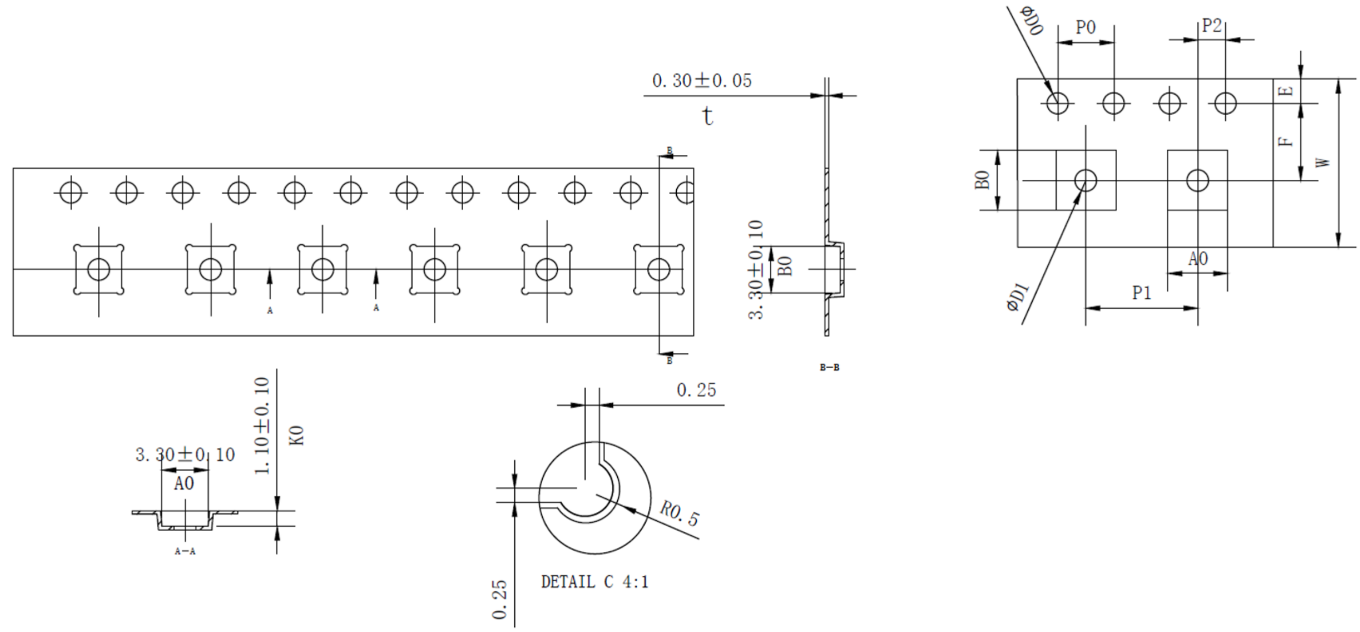


Figure 12-1 Tape Information of SOP8



W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	t
12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	1.55 ±0.05	1.55 ±0.05	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	8.00 ±0.10	3.30 ±0.10		3.30 ±0.10		1.10 ±0.10		0.30 ±0.05

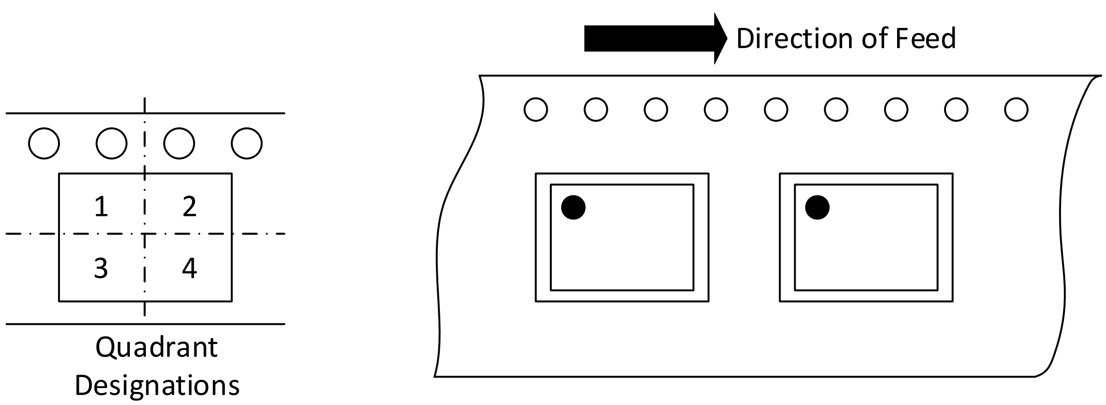
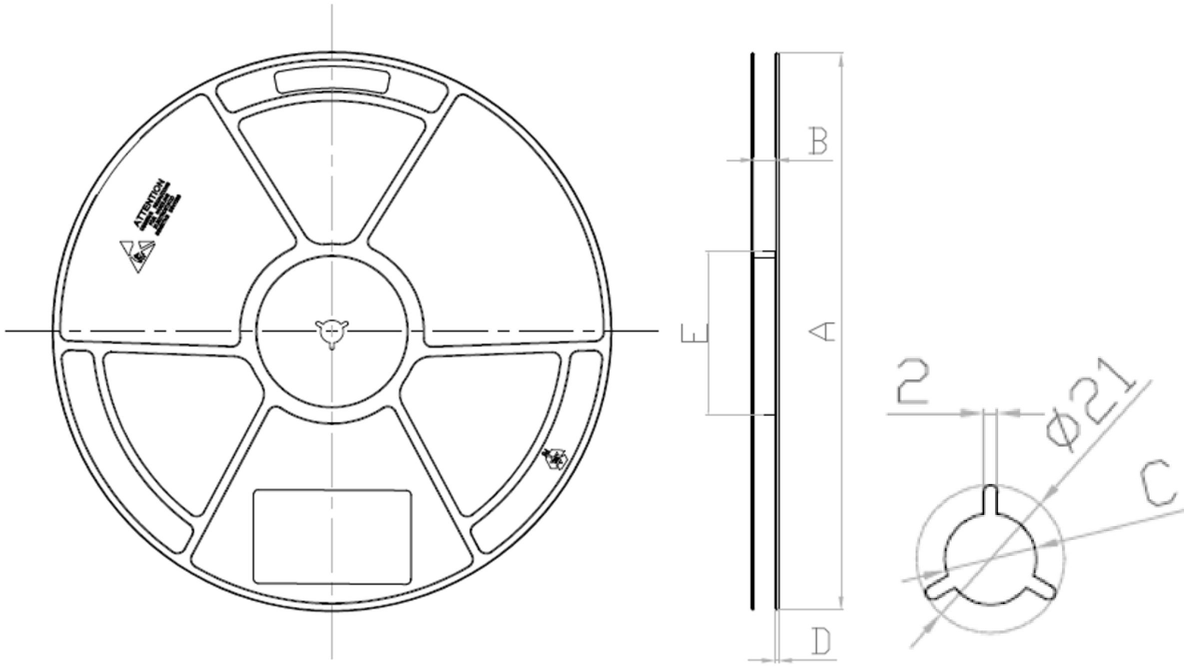


Figure 12-2 Tape Information of DFN8



规格	A	B	C	D	E
12W	330±2.0	12.5±1.00	13.5±1.00	1.9±1.00	100±1.00
16W	330±2.0	16.5±1.00	13.5±1.00	1.9±1.00	100±1.00
24W	330±2.0	24.5±1.00	13.5±1.00	1.9±1.00	100±1.00
32W	330±2.0	32.5±1.00	13.5±1.00	1.9±1.00	100±1.00
44W	330±2.0	44.5±1.00	13.5±1.00	1.9±1.00	100±1.00

Figure 12-3 Reel Information of SOP8 and DFN8

13. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/9/30

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