

Product Overview

The NCA1051C is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The NCA1051C implements the CAN physical layer as defined in ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The NCA1051C provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Ideal passive behavior to the CAN bus when the supply voltage is off
- I/O voltage range supports 1.8V, 3.3V and 5V MCU
- Power supply voltage
- V_{IO} : 1.7V to 5.5V
- V_{CC} : 4.5V to 5.5V
- Bus fault protection of -70V to +70V
- Bus common-mode voltage of -30V to +30V
- Transmit data (TXD) dominant time out function
- Over temperature protection
- Improve the bus signal by ringing reduction
- Data rate: up to 5Mbps
- Low loop delay: <250ns
- Operation temperature: -40°C to +125°C
- RoHS & REACH compliant

Applications

- CAN bus standards such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783 and CANaerospace
- Highly loaded CAN networks down to 10 kbps networks
- Industrial automation, control, sensors, and drive systems
- Building, security, and climate control automation

Device Information

Part Number	Package	Body Size
NCA1051C-DSPR	SOP8	4.90mm × 3.90mm
NCA1051CN-DSPR	SOP8	4.90mm × 3.90mm

Functional Block Diagrams

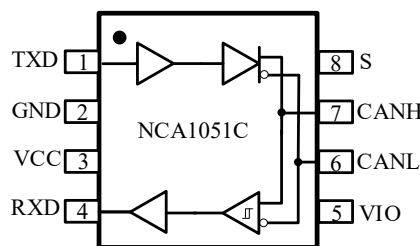


Figure 1. NCA1051C Block Diagram

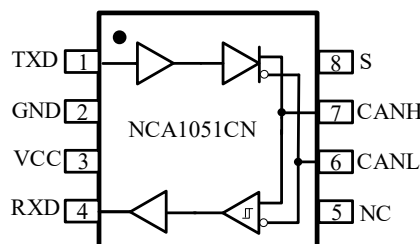


Figure 2. NCA1051CN Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS	3
2. ABSOLUTE MAXIMUM RATINGS	4
3. EMC RATINGS	4
4. RECOMMENDED OPERATING CONDITIONS	5
5. THERMAL INFORMATION	5
6. SPECIFICATIONS	6
6.1. ELECTRICAL CHARACTERISTICS	6
6.2. SWITCHING ELECTRICAL CHARACTERISTICS	9
6.3. PARAMETER MEASUREMENT INFORMATION	10
7. FUNCTION DESCRIPTION	13
7.1. OVERVIEW	13
7.2. FUNCTIONAL BLOCK DIAGRAM	13
7.3. SIGNAL RINGING REDUCTION	14
7.4. VIO SUPPLY PIN	14
7.5. DEVICE OPERATING MODES	14
7.5.1. Normal Mode	14
7.5.2. Silent Mode	14
7.6. FAIL-SAFE FEATURES	14
7.6.1. TXD Dominant Time-Out Function (TXD DTO)	14
7.6.2. Internal Biasing of TXD and S Input Pins	15
7.6.3. Undervoltage Detection on Pins VCC and VIO	15
7.6.4. Unpowered Device	15
7.6.5. Over-Temperature Protection (OTP)	15
8. APPLICATION NOTE	16
8.1. TYPICAL APPLICATION	16
9. PACKAGE INFORMATION	17
10. ORDERING INFORMATION	18
11. DOCUMENTATION SUPPORT	18
12. TAPE AND REEL INFORMATION	19
13. REVISION HISTORY	20

1. Pin Configuration and Functions

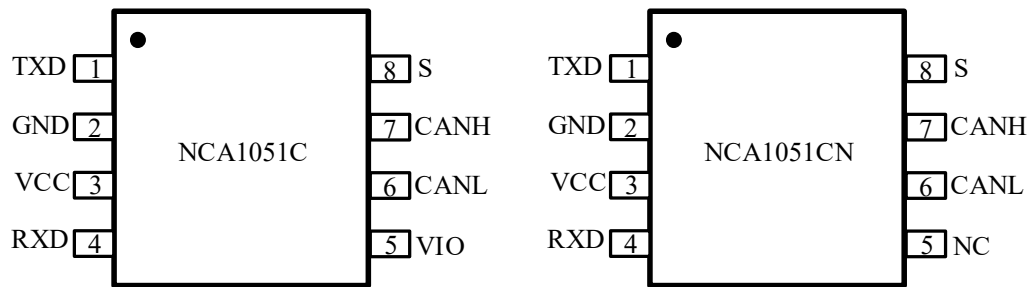


Figure 1-1 NCA1051C, NCA1051CN Package

Table 1-1 NCA1051C Pin Configuration and Description

NCA1051C PIN NO.	NCA1051CN PIN NO.	SYMBOL	FUNCTION
1	1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	2	GND	Ground
3	3	VCC	Power Supply
4	4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	\	VIO	Logic I/O supply voltage
\	5	NC	No connection
6	6	CANL	Low-level CAN bus line
7	7	CANH	High-level CAN bus line
8	8	S	S (silent mode) select pin (active high)

2. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{[1][2]}.

Parameters	Symbol	Min	Max	Unit
Power Supply Voltage	VCC, VIO	-0.3	7	V
Logic I/O Voltage	TXD, RXD, S	-0.3	7	V
Maximum bus Pin Voltage	V _{CANH} , V _{CANL}	-70	70	V
Voltage between pin CANH and pin CANL	V _{CANH} - V _{CANL}	-70	70	V
Junction temperature	T _J	-40	150	°C
Storage Temperature	T _{stg}	-65	150	°C

^[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating condition for extended periods may affect device reliability.

^[2] All voltage values, except for “Voltage between pin CANH and pin CANL”, are with respect to GND terminal.

3. EMC Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge	Human Body Model (HBM), per ANSI/ ESDA/ JEDEC JS-001		
	● CANH and CANL, to GND	±8	kV
	● Other pins, to GND	±8	kV
	Charged Device Model (CDM), per ANSI/ ESDA/ JEDEC JS-002		
Electrical disturbances	● All pins	±2	kV
	Machine Model (MM), per JESD22-A115C		
	● All pins	±400	V
	Electrical transient conduction, per ISO 7637-2, on CANH and CANL		
	● Pulse 1	-100	V
	● Pulse 2a	75	V
	● Pulse 3a	-150	V
	● Pulse 3b	100	V

4. Recommended Operating Conditions

<i>Parameters</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
Power Supply Voltage	VCC	4.5	5	5.5	V
I/O Level-Shifting Voltage	VIO	1.7	3.3	5.5	V
Operating Temperature	T _{opr}	-40	-	125	°C

5. Thermal Information

<i>Parameters</i>	<i>Symbol</i>	<i>SOP8</i>	<i>Unit</i>
IC Junction-to-Air Thermal Resistance	R _{θJA}	120	°C /W
Junction-to-case (top) thermal resistance	R _{θJC(top)}	57.8	°C /W
Junction-to-board thermal resistance	R _{θJB}	64.2	°C /W

6. Specifications

6.1. Electrical Characteristics

$V_{CC}=4.5V$ to $5.5V$, $V_{IO}=1.7$ to $5.5V$ ^[1], $T_a=-40^{\circ}C$ to $125^{\circ}C$. Unless otherwise noted, Typical values are at $V_{CC}=5V$, $V_{IO}=3.3V$, $R_L=60\Omega$, $T_a=25^{\circ}C$.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V _{CC}	Supply voltage		4.5	-	5.5	V
I _{CC}	Supply current	Normal mode, recessive, V _{TXD} =V _{IO} ^[2] , V _S =0V	-	5	7	mA
		Normal mode, dominant, V _{TXD} =0V	-	45	60	mA
		Normal mode, dominant, V _{TXD} =0, short circuit on bus lines, -3V < (V _{CANH} = V _{CANL}) < 18V	-	-	110	mA
		Silent mode, V _{TXD} =V _{IO} ^[2]	-	-	2.5	mA
V _{uvd(VCC)}	Undervoltage detection voltage on pin VCC	Rising	4	4.26	4.5	V
		Falling	4	4.17	4.5	V
I/O level adapter supply; pin V _{IO} ; only for NCA1051C						
V _{IO}	Supply voltage on pin VIO		1.7	-	5.5	V
I _{IO}	Supply current on pin VIO	Normal mode, recessive, V _{TXD} =V _{IO}	-	12	30	μA
		Normal mode, dominant, V _{TXD} =0V	-	120	320	μA
		Silent mode; V _{TXD} =V _{IO}	-	10	16	μA
V _{uvd(VIO)}	Undervoltage detection voltage on pin VIO	Rising	1.4	1.56	1.7	V
		Falling	1.4	1.50	1.7	V
Silent mode control input; pin S						
V _{IH}	High level input voltage	NCA1051C	0.7*V _{IO}	-	V _{IO} +0.3	V
		NCA1051CN	2.0	-	V _{CC} +0.3	V
V _{IL}	Low level input voltage	NCA1051C	-0.3	-	0.3*V _{IO}	V
		NCA1051CN	-0.3	-	0.8	V
I _{IH}	High level input current	V _S =V _{IO}	-1	-	15	μA
I _{IL}	Low level input current	V _S =0V	-1	-	1	μA
CAN transmit data input; pin TXD						
V _{IH}	High level input voltage	NCA1057	0.7*V _{IO}	-	V _{IO} +0.3	V
		NCA1057N	2.0	-	V _{CC} +0.3	V

V_{IL}	Low level input voltage	NCA1057	-0.3	-	$0.3 \cdot V_{IO}$	V
		NCA1057N	-0.3	-	0.8	V
R_{pu}	Pull-up resistance		40	55	80	k Ω
C_i	Input capacitance	[3]	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	High level output current	$V_{RXD} = V_{IO} - 0.4V$ [2]	-10	-3	-1	mA
I_{OL}	Low level output current	$V_{RXD} = 0.4V$; bus dominant	1	3.5	10	mA
Bus lines; pins CANH and CANL; Driver						
$V_{OH(D)}$	CANH output voltage (Dominant)	$V_{TXD} = 0V$, $R_L = 50\Omega$ to 65Ω [4]	2.75	3.6	4.5	V
$V_{OL(D)}$	CANL output voltage (Dominant)	$V_{TXD} = 0V$, $R_L = 50\Omega$ to 65Ω [4]	0.5	1.4	2.25	V
$V_{OH(R)}$	CANH output voltage (Recessive)	Normal/ silent mode, no load [4]	2.0	$0.5 \cdot V_{CC}$	3.0	V
$V_{OL(R)}$	CANL output voltage (Recessive)	Normal/ silent mode, no load [4]	2.0	$0.5 \cdot V_{CC}$	3.0	V
$V_{OD(D)}$	Differential output voltage (Dominant)	Normal mode				
		$R_L = 50\Omega$ to 65Ω [4]	1.5	-	3.0	V
		$R_L = 45\Omega$ to 70Ω [4]	1.4	-	3.3	V
		$R_L = 2240\Omega$ [4]	1.5	-	5.0	V
$V_{OD(R)}$	Differential output voltage (Recessive)	Normal mode, no load [4]	-50	-	50	mV
V_{TXsym}	Transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$, [3] $f_{TXD} = 1MHz$, $R_L = 60\Omega$, $C_{SPLIT} = 4.7nF$, $V_{CC} = 4.75V$ to $5.25V$ [4] [5]	$0.9 \cdot V_{CC}$	-	$1.1 \cdot V_{CC}$	V
$I_{OSH(R)}$	CANH short-circuit output current, recessive	Normal mode, $V_{CANH} = V_{CANL} = -27V$ to $32V$	-2	-	2	mA
$I_{OSL(R)}$	CANL short-circuit output current, recessive	Normal mode, $V_{CANH} = V_{CANL} = -27V$ to $32V$	-2	-	2	mA
$I_{OSH(D)}$	CANH short-circuit output current, dominant	Normal mode, $V_{CANH} = -15V$ to $40V$, CANL open [4]	-100	-	100	mA
$I_{OSL(D)}$	CANL short-circuit output current, dominant	Normal mode, $V_{CANL} = -15V$ to $40V$, CANH open [4]	-100	-	100	mA
Bus lines; pins CANH and CANL; Receiver						

$V_{ID(R)}$	Differential input threshold voltage, recessive	Normal/ silent mode ^[4] $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	0.5	-	0.9	V
$V_{ID(D)}$	Differential input threshold voltage, dominant	Normal/ silent mode ^[4] $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	0.5	-	0.9	V
V_{hys}	Differential input hysteresis voltage	Normal/ silent mode $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	-	50	100	mV
$V_{RX(R)}$	Receiver recessive voltage	Normal/ silent mode $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	-4	-	0.5	V
$V_{RX(D)}$	Receiver dominant voltage	Normal/ silent mode $-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	0.9	-	9	V
$I_{LKG(OFF)}$	Power-off (unpowered) bus input leakage current	$V_{CANH} = V_{CANL} = 5V$, $V_{CC} = V_{IO} = 0V$ ^[4]	-10	-	10	μA
R_I	Input resistance	$-2V \leq V_{CANH} \leq 7V$, $-2V \leq V_{CANL} \leq 7V$ [3] [4]	25	40	50	k Ω
$R_{I(match)}$	Input resistance matching	$V_{CANH} = 5V$, $V_{CANL} = 5V$, $R_{I(match)} = 2 \cdot (R_{CANH} - R_{CANL}) / (R_{CANH} + R_{CANL})$ [3]	-1	-	1	%
R_{ID}	Differential input resistance	$-2V \leq V_{CANH} \leq 7V$, $-2V \leq V_{CANL} \leq 7V$, $R_{ID} = R_{CANH} + R_{CANL}$ [3] [4]	50	80	100	k Ω
C_I	Input capacitance to ground	CANH or CANL ^[3]	-	-	30	pF
C_{ID}	Differential input	[3]	-	-	15	pF
Temperature detection						
T_{SD}	Thermal shutdown threshold	[3]	-	193	-	$^{\circ}C$
$T_{SD(hys)}$	Thermal shutdown hysteresis	[3]	-	11	-	$^{\circ}C$

^[1] Only NCA1051C has a VIO pin. For NCA1051CN, the VIO input is internally connected to VCC.

^[2] $V_{IO} = V_{CC}$ for the version without VIO pin.

^[3] Not tested in production; guaranteed by design.

^[4] Required in ISO 11898-2:2024.

^[5] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 6-3.

6.2. Switching Electrical Characteristics

$V_{CC} = 4.5V \sim 5.5V$, $V_{IO} = 1.7 \sim 5.5V^{[1]}$, $T_a = -40^\circ C$ to $125^\circ C$. Unless otherwise noted, Typical values are at $V_{CC} = 5V$, $V_{IO} = 3.3V$, $R_L = 60\Omega$, $T_a = 25^\circ C$.

Symbol	Parameters	Comments	Min	Typ	Max	Unit
Driver						
t _{d(TXD-bus, dom)}	Delay time from TXD to bus dominant	Normal mode ^[3]	-	40	-	ns
t _{d(TXD-bus, rec)}	Delay time from TXD to bus recessive	Normal mode ^[3]	-	65	-	ns
t _{bit(bus)}	Transmitted recessive bit width	t _{bit(TXD)} = 500 ns	435	495	530	ns
		t _{bit(TXD)} = 200 ns	155	195	210	ns
Receiver						
t _{d(bus-RXD, dom)}	Delay time from bus to RXD dominant	^[3]	-	110	-	ns
t _{d(bus-RXD, rec)}	Delay time from bus to RXD recessive	^[3]	-	100	-	ns
t _{d(TXD-RXD, dom)}	Delay time from TXD to RXD dominant	Normal mode ^[3]	-	150	255	ns
t _{d(TXD-RXD, rec)}	Delay time from TXD to RXD recessive	Normal mode ^[3]	-	165	255	ns
t _{bit(RXD)}	Bit time on pin RXD	t _{bit(TXD)} = 500 ns	400	-	550	ns
		t _{bit(TXD)} = 200 ns	120	-	220	ns
CAN FD timing characteristics						
Δt _{rec}	Receiver timing symmetry	Δt _{rec} = t _{bit(RXD)} - t _{bit(bus)} ^[3]				
		t _{bit(TXD)} = 500 ns	-65	-	40	ns
		t _{bit(TXD)} = 200 ns	-45	-	15	ns
Dominant time-out time; pin TXD						
t _{to(dom)TXD}	TXD dominant time-out time	Normal mode ^[3]	0.8	2.8	5	ms

^[1] Only NCA1051C has a VIO pin. For NCA1051CN, the VIO input is internally connected to VCC.

^[2] Not tested in production; guaranteed by design.

^[3] Required in ISO 11898-2-2024.

6.3. Parameter Measurement Information

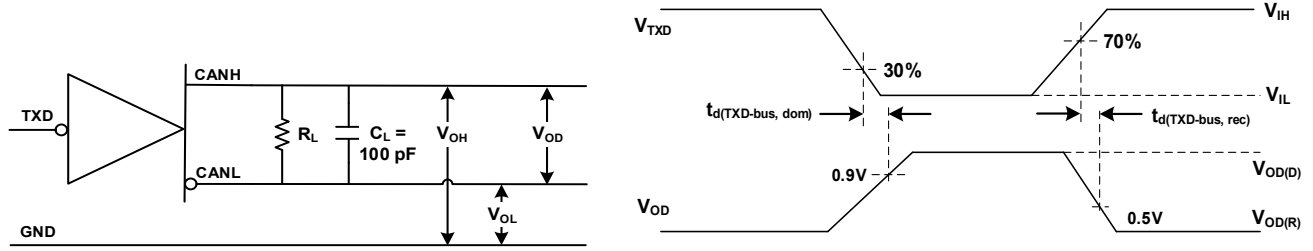


Figure 6-1 Driver Test Circuit and Voltage Waveforms^[1]

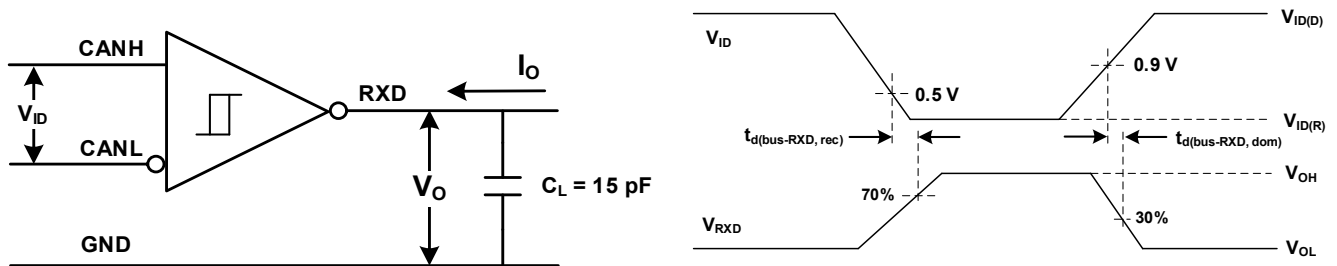


Figure 6-2 Receiver Test Circuit and Voltage Waveforms

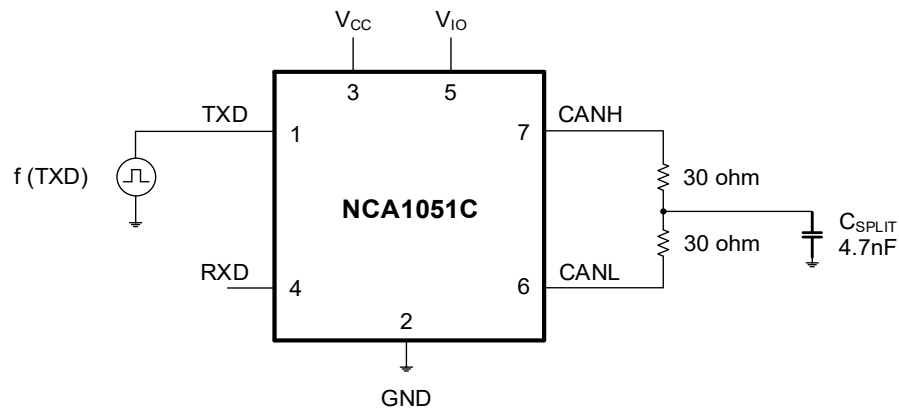


Figure 6-3 Transceiver Driver Symmetry Test Circuit

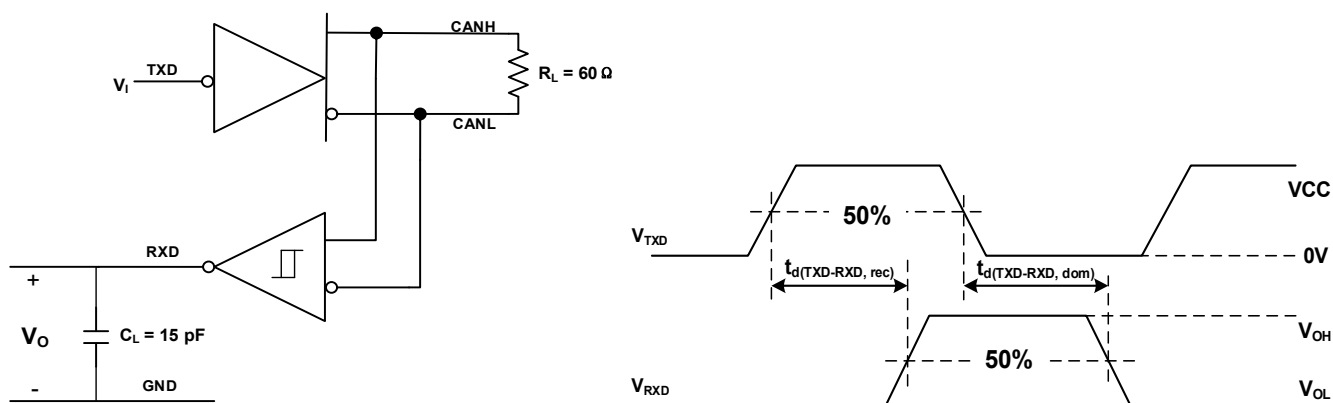


Figure 6-4 Loop Time Test Circuit and Voltage Waveforms

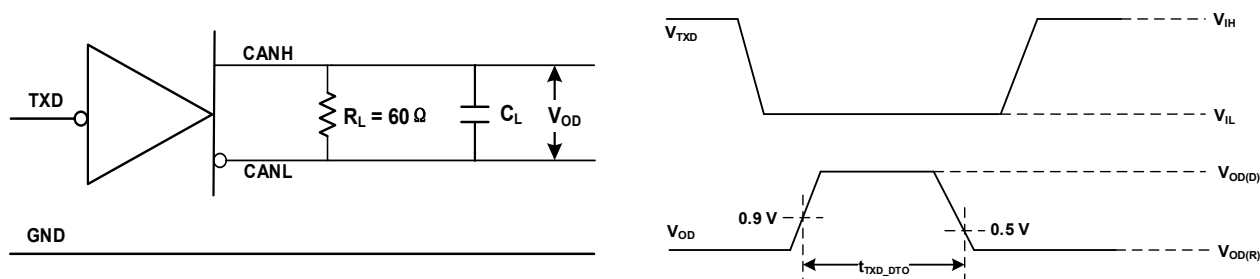


Figure 6-5 TXD Dominant Time-out Test Circuit and Voltage Waveforms

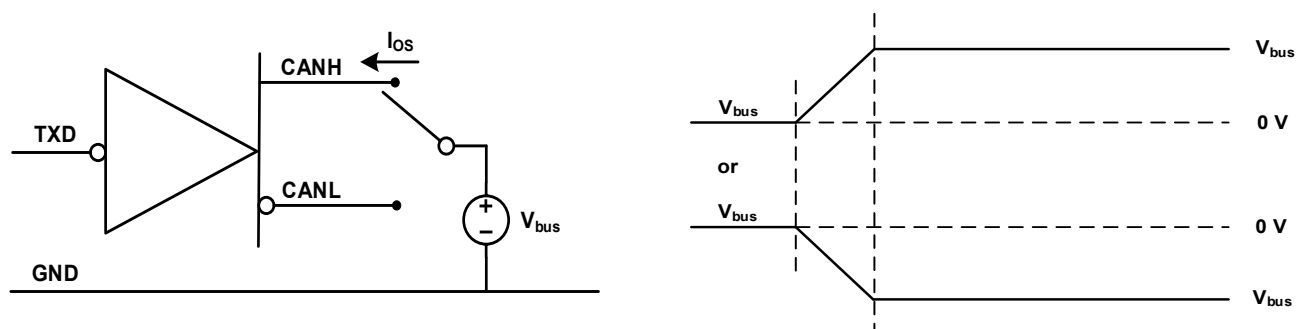


Figure 6-6 Driver Short-Circuit Current Test Circuit and Waveforms

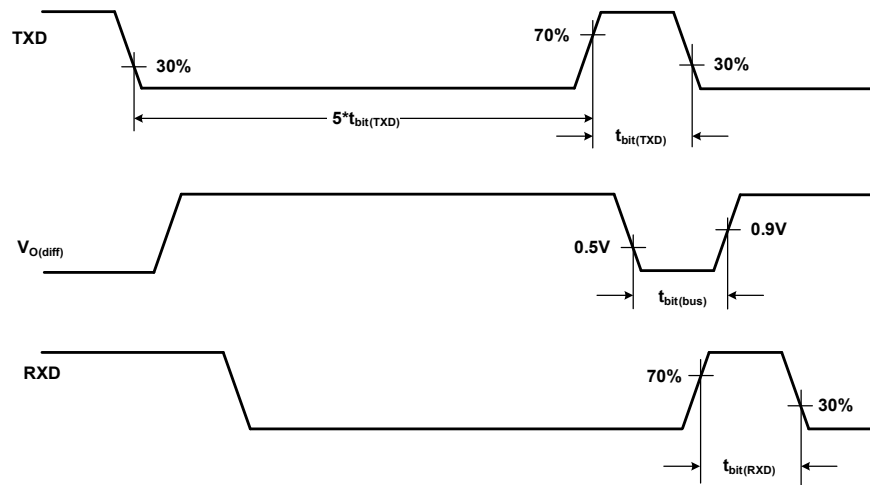


Figure 6-7 $t_{\text{bit(RXD)}}$ Test Circuit and Waveforms^[1]

^[1] For NCA1057N, TXD high level is set as 2.0V instead; TXD low level, 0.8V instead.

7. Function Description

7.1. Overview

The NCA1051C is a CAN transceiver which fully compatible with the ISO11898-2 standard. The data rate of the NCA1051C is up to 5Mbps, and it can support up to 110 CAN nodes. Meanwhile, the maximum transmission rate of the CAN bus is limited by the bus load, the quantity of nodes, the cable length, and other factors. The NCA1051C has a $\pm 30V$ input common-mode range, enabling reliable communication between bus nodes with large ground potential deviations.

Comprehensive protection features are designed to enhance the device and network robustness in harsh operating conditions. The transmit data dominant time-out function prevents the bus from lock-up by the faults on micro-controller. Moreover, the NCA1051C provides thermal protection and short-circuit protection.

7.2. Functional Block Diagram

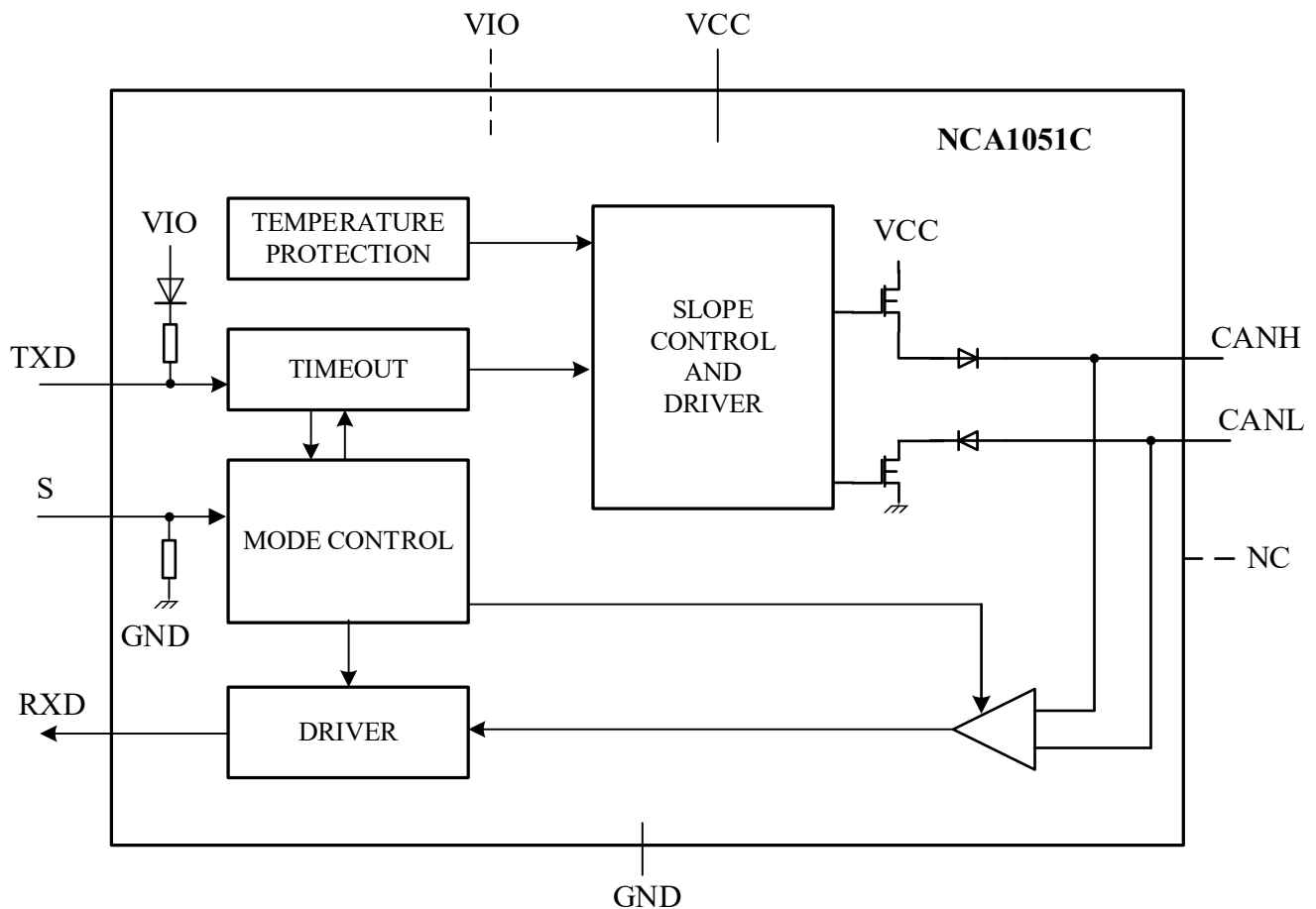


Figure 7-1 Block diagram of NCA1051C

7.3. Signal Ringing Reduction

The signal ringing arises from the reflection caused by the impedance mismatch in complex star topologies of CAN network for the sake of the nodes that act as stubs. On a dominant-to-recessive edge, the driver output impedance goes to about 80 k Ω and signal reflected back experiences impedance mismatch, which causes ringing.

NCA1051C resolves this issue by TX-based signal ringing reduction. Following a dominant-to-recessive edge, transmitter output impedance keeps low (about 100 Ω) at first and therefore matches the network characteristic impedance. After the reflections fade away, driver output impedance goes to high-Z and recessive bit is clean at sampling point.

7.4. VIO Supply Pin

Two versions of the NCA1051C are available, only differing in the function of a single pin. Pin 5 is either a VIO supply pin or a NC pin. Pin VIO should be connected to the microcontroller supply voltage (see Figure 8-1). This will adjust the signal levels of pins TXD, RXD and S to the I/O levels of the microcontroller.

For versions of the NCA1051CN without a VIO pin, the VIO input is internally connected to VCC. This sets the signal levels of pins TXD, RXD and S to levels compatible with 5 V microcontrollers.

7.5. Device Operating Modes

The device has two main operating modes: Normal mode and Silent mode. Operating mode is selected via the S input pin. Table 7-1 shows a description of the operating modes under normal supply conditions.

Table 7-1 Operating Modes

Mode	S pin	TXD pin	CAN driver	RXD pin
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Silent	HIGH	X	recessive	LOW when bus dominant
				HIGH when bus recessive

7.5.1. Normal Mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 7-1). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible Electromagnetic Emission (EME).

After entering normal mode, it is recommended to firstly pull up TXD pin to a high level for at least 200ns before communications, for fear of unwanted TXD timeout caused by unstable TXD level during the power-on phase.

7.5.2. Silent Mode

A HIGH level on pin S selects Silent mode. In Silent mode, the transmitter is disabled, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

7.6. Fail-safe features

7.6.1. TXD Dominant Time-Out Function (TXD DTO)

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value $t_{to(dom)TXD}$, the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

7.6.2. Internal Biasing of TXD and S Input Pins

Pin TXD has an internal pull-up to VIO to ensure a safe, defined state, in case the pin is left floating. Pin S, an internal pull-down to GND. Pull-up current in TXD and pull-down current in S flow in these pins in all states.

7.6.3. Undervoltage Detection on Pins VCC and VIO

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the VCC or VIO supply terminals.

When VCC or VIO drop below their respective undervoltage detection levels, $V_{uvd(VCC)}$ and $V_{uvd(VIO)}$, the transceiver will switch off and disengage from the bus (zero load) until VCC and VIO have recovered.

Table 7-2 Undervoltage Lockout 5V Only Devices (NCA1051CN)

VCC	Device State	Bus Output	RXD
$>UV_{VCC}$	Normal	Per TXD	Mirrors Bus ^[1]
$<UV_{VCC}$	Off	High Impedance	High Impedance

^[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 7-3 Undervoltage Lockout I/O Level Shifting Devices (NCA1051C)

VCC	VIO	Device State	Bus Output	RXD
$>UV_{VCC}$	$>UV_{VIO}$	Normal	Per TXD	Mirrors Bus ^[1]
$<UV_{VCC}$	$>UV_{VIO}$	Off	High Impedance	High Impedance
$>UV_{VCC}$	$<UV_{VIO}$	Off	High Impedance	High Impedance
$<UV_{VCC}$	$<UV_{VIO}$	Off	High Impedance	High Impedance

^[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

7.6.4. Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

7.6.5. Over-Temperature Protection (OTP)

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{SD} , the output drivers will be disabled until the virtual junction temperature becomes lower than T_{SD} and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

8. Application Note

8.1. Typical Application

The NCA1051C requires a 0.1 μF bypass capacitors between VCC and GND. The capacitor should be placed as close as possible to the package. The Figure 8-1 and Figure 8-2 are the typical applications of NCA1051C.

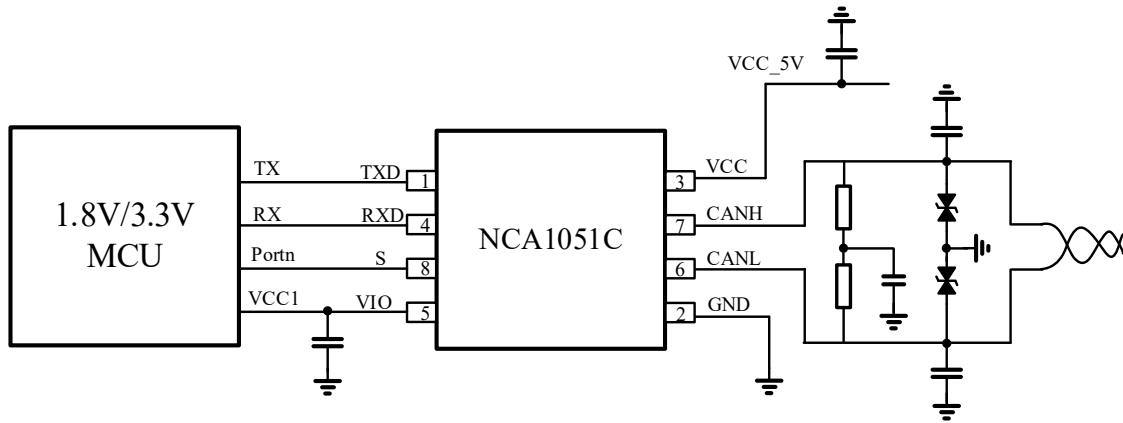


Figure 8-1 Typical CAN Bus Application Using 1.8V/3.3V CAN Controller

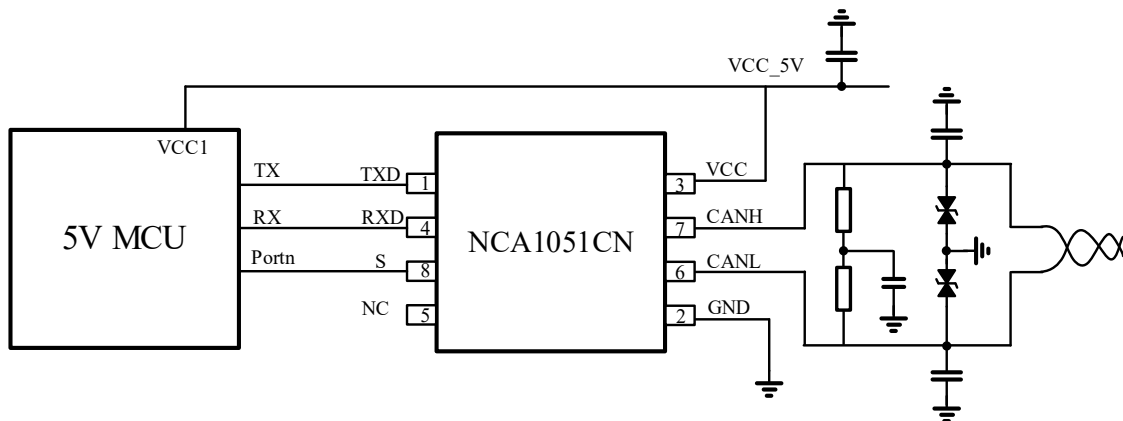
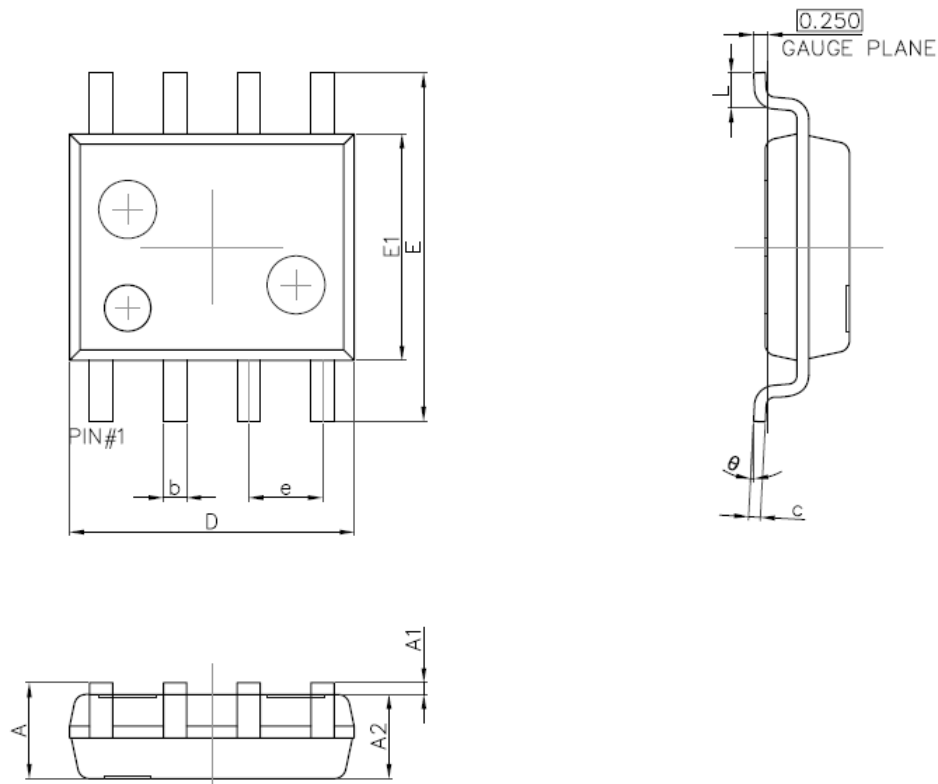


Figure 8-2 Typical CAN Bus Application Using 5V CAN Controller

9. Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Figure 9-1 SOP8 Package Shape and Dimension

10. Ordering Information

<i>Part Number</i>	<i>Operation Temperature</i>	<i>MSL</i>	<i>Package Type</i>	<i>SPQ</i>
NCA1051C-DSPR	-40 to 125°C	3	SOP8	2500
NCA1051CN-DSPR	-40 to 125°C	3	SOP8	2500

11. Documentation Support

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>
NCA1051C	Click here	Click here	Click here

12. Tape and Reel Information

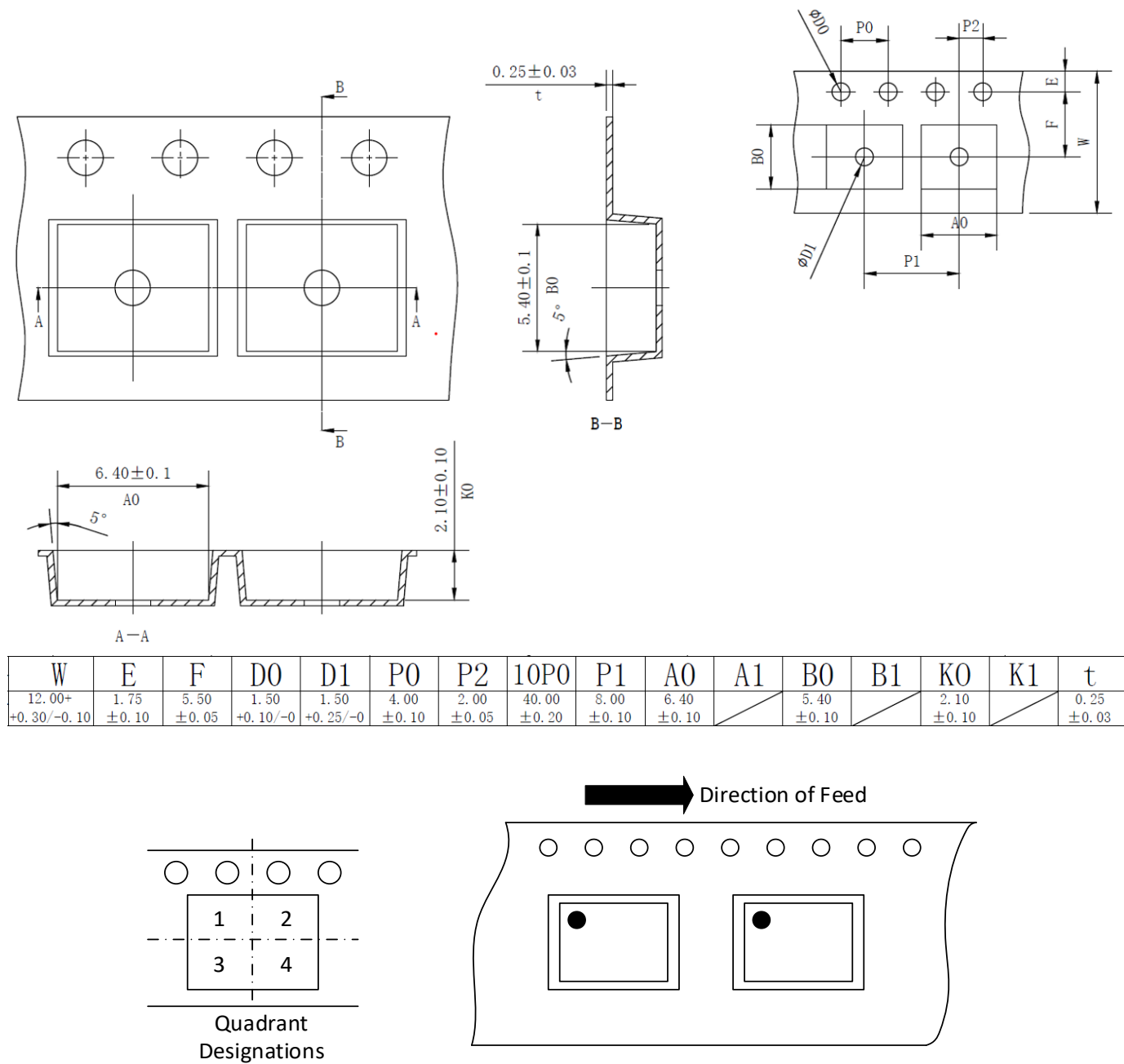
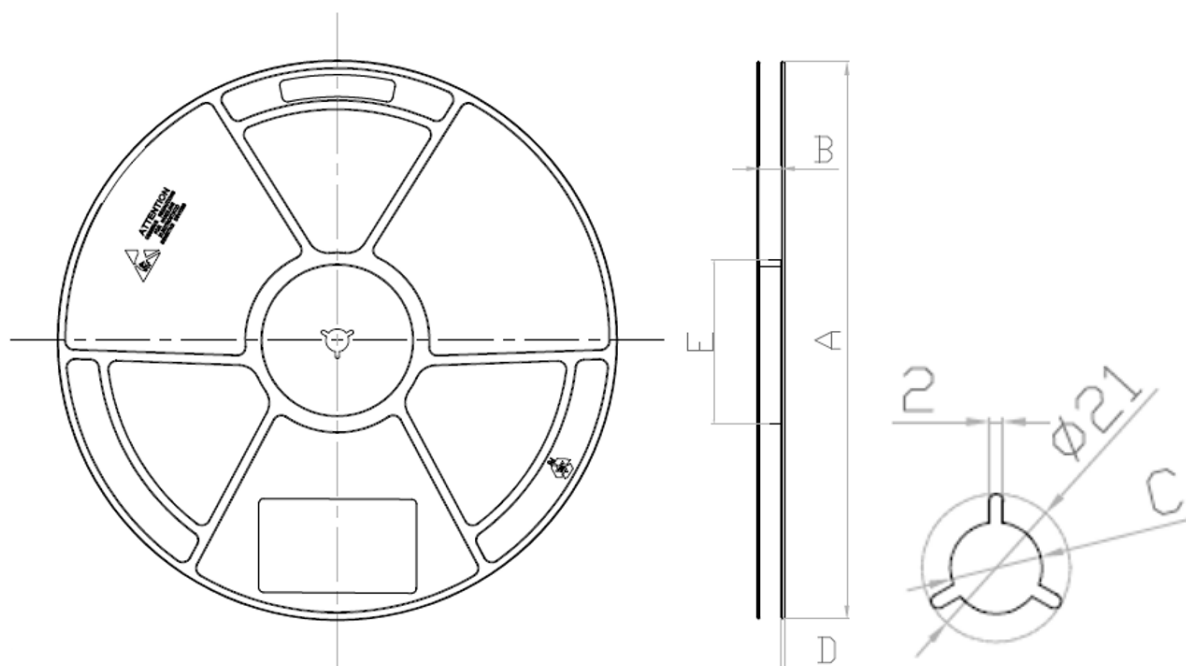


Figure 12-1 Tape Information of SOP8



规格	A	B	C	D	E
12W	330±2.0	12.5±1.00	13.5±1.00	1.9±1.00	100±1.00
16W	330±2.0	16.5±1.00	13.5±1.00	1.9±1.00	100±1.00
24W	330±2.0	24.5±1.00	13.5±1.00	1.9±1.00	100±1.00
32W	330±2.0	32.5±1.00	13.5±1.00	1.9±1.00	100±1.00
44W	330±2.0	44.5±1.00	13.5±1.00	1.9±1.00	100±1.00

Figure 12-2 Reel Information of SOP8

13. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/9/30

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis and is intended only for skilled developers designing with NOVOSENSE’ products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd