NOVOSENSE

NCA1043B
High-speed CAN Transceiver
Datasheet (EN) 1.0

Product Overview

The NCA1043B high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The NCA1043B offers excellent Electro Magnetic Compatibility (EMC) and Electro Static Discharge (ESD) performance, very low power consumption, and passive behavior when the supply voltage is turned off.

These features make the NCA1043B the ideal choice for high-speed CAN networks containing nodes that need to be available all times, even when the internal V_{IO} and V_{CC} supplies are switched off.

Key Features

- Fully compatible with the ISO11898-2 standard and SAE J2284-1 to SAE J2284-5
- I/O voltage range supports 3V and 5V MCU
- Bus fault protection of -58V to +58V
- Transmit data (TXD) dominant time out function
- Bus dominant time out function
- Low-power management controls the power supply throughout the node while supporting local and remote wake-up with wake-up source recognition
- Several protection and diagnostic functions including bus line short-circuit detection and battery connection detection
- CAN FD Date rate: up to 5Mbps
- Low loop delay: <250ns
- Operation temperature: -40℃~125℃
- AEC-Q100 qualified for automotive applications
- RoHS-compliant packages: SOP14, DFN14

Applications

- 12-V or 24-V System applications
- Automotive and transportation
  - Advanced driver assistance system (ADAS)
  - Infotainment
  - Cluster
  - Body electronics & lighting

Device Information

Part Number	*Package*	*Body Size*
NCA1043B-Q1SPKR	SOP14	8.63mm × 3.90mm
NCA1043B-Q1DNKR	DFN14	4.50mm × 3.00mm

Functional Block Diagrams

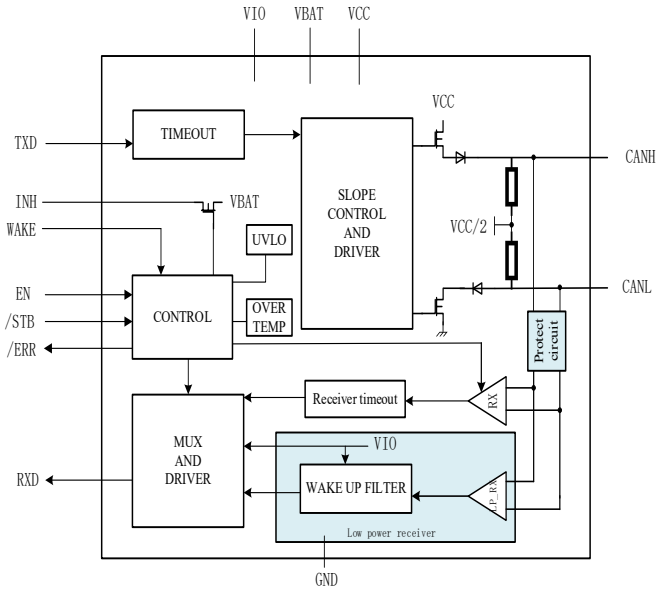

Figure 1 NCA1043B Block Diagram

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1. Pin Configuration and Functions

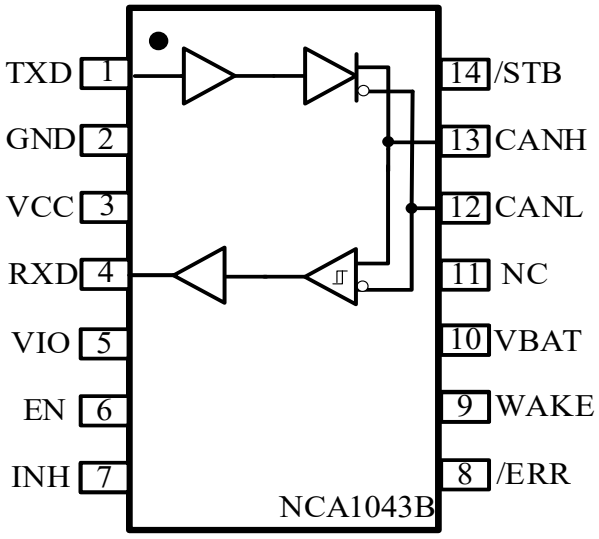


Figure 1.1 NCA1043B Package

Table 1.1 NCA1043B Pin Configuration and Description

NSI8266W PIN NO.	*SYMBOL*	*FUNCTION*
1	TXD	CAN transmit data input (Internal weak pull-up ,LOW for dominant and HIGH for recessive bus states)
2	GND	Ground
3	VCC	Power Supply
4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	VIO	Logic I/O supply voltage
6	EN	enable control input (Internal weak pull-down)
7	INH	inhibit output for switching external voltage regulators
8	/ERR	error and power-on indication output (active LOW)
9	WAKE	local wake-up input (Internal weak pull-up and down)
10	VBAT	battery supply voltage
11	NC	No connection
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	/STB	STB (standby mode) select pin (active LOW, Internal weak pull-down)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	V_{CC}, V_{IO}	-0.3		7	V	
	V_{BAT}	-0.3		58	V	
I/O Voltage	TXD, RXD, STB_N, EN, ERR_N	-0.3		7	V	
	INH and WAKE	-0.3		58	V	
	V_{CANH}, V_{CANL}	-58		58	V	
Voltage Between pin CANH and pin CANL	$V_{(CANH-CANL)}$	-58		58	V	
Current on pin WAKE	I_{WAKE}	-15			mA	
Transient Voltage	V_{trt}	-100			V	On pin CANH and CANL, VBAT, ISO 7637- 3 pulses 1
				75	V	On pin CANH and CANL, VBAT, ISO 7637- 3 pulses 2a
		-150			V	On pin CANH and CANL, VBAT, ISO 7637- 3 pulses 3a
				100	V	On pin CANH and CANL, VBAT, ISO 7637- 3 pulses 3b
Junction Temperature	T_j	-40		150	℃	
Storage Temperature	T_{stg}	-65		150	℃	

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD		
	● CANH,CANL to GND	±8.0	kV
	● Other pins	±4.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB		
	● All pins	±2.0	kV
	System， per IEC 61000 4 2 (150 pF, 330 Ω at pins CANH and	±8.0	kV

	CANL to GND		

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	unit
Power Supply Voltage	V_{BAT}	4.5		40	V
	V_{CC}	4.5		5.5	V
	V_{IO}	2.8		5.5	V
TXD High level input voltage	$V_{IH(TXD)}$	0.7*VIO		VIO+0.3	V
TXD Low level input voltage	$V_{IL(TXD)}$	-0.3		0.3*VIO	V
RXD Output High current	I_{OH}	-12		-1	mA
RXD Output Low current	I_{OL}	2		14	mA
Operating Temperature	T_{opr}	-40		125	℃

5. Thermal Information

Parameters	Symbol	SOP14	DFN14	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	78	33.1	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	33.6	30.5	℃/W
Junction-to-board thermal resistance	θ_{JB}	34.7	10.8	℃/W

6. Specifications

6.1. Static Characteristics

(VCC=4.5V~5.5V, VIO=2.8V~5.5V, VBAT4.5V~40V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V, VBAT=12V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	V_{CC}	4.5		5.5	V	
	$V_{uvd(VCC)}$	3		4.3	V	undervoltage detection voltage on pin VCC
	V_{IO}	2.8		5.5	V	
	$V_{uvd(VIO)}$	0.8		2.5	V	undervoltage detection voltage on pin VIO
	V_{BAT}	4.5		40	V	
	$V_{uvd(VBAT)}$	3		4.3	V	undervoltage detection voltage on pin VBAT
supply current on pin VCC	I_{CC}			65	mA	TXD=0, R_L=60Ω, Normal mode

Parameters	Symbol	Min	Typ	Max	Unit	Comments
				109	mA	Normal mode, TXD=0,short circuit on bus lines: -3V<(V_{CANH}=V_{CANL}) <18V
				9	mA	TXD=V_{IO}, Normal mode or Listen only mode
				3.5	uA	Standby or Sleep mode
supply current on pin VIO	I_{IO}			350	uA	Normal mode, TXD=0, R_L=60Ω
				4	uA	TXD=V_{IO}, Normal or Listen only mode
				4	uA	Standby or Sleep mode
supply current on pin VBAT	I_{BAT}			50	uA	Normal or Listen only mode
			18	40	uA	Standby mode, V_{INH}=V_{WAKE}=V_{BAT}, VCC>4.5V
			18	40	uA	Sleep mode, V_{INH}=V_{CC}=V_{IO}=0, V_{WAKE}=V_{BAT}
Thermal-Shutdown Threshold	T_{TS}		190		℃	
Logic Side						
High level input voltage	V_{IH}	0.7*V_{IO}		V_{IO}+0.3	V	TXD &STB_N, EN pin
Low level input voltage	V_{IL}	-0.3		0.3*V_{IO}	V	TXD &STB_N, EN pin
High level input current	I_{IH}	-5		5	uA	TXD pin, V_{IN}=V_{IO}
High level input current	I_{IH}	1		10	uA	STB_N, EN pin, V_{IN}=V_{IO}
Low level input current	I_{IL}	-260		-30	uA	TXD pin, TXD=0
Low level input current	I_{IL}	-1		1	uA	STB_N, EN pin, V_{IN}=0
Output High current	I_{OH}	-12	-3	-1	mA	RXD=V_{IO}-0.4V
		-50		-4	uA	ERR_N=V_{IO}-0.4, V_{IO}=V_{CC}
Output Low current	I_{OL}	2	5	14	mA	RXD=0.4V
		0.1		2	mA	ERR_N=0.4V
Input Capacitance	C_{IN}		2		pF	TXD pin, Not tested in production, guaranteed by design.
WAKE						
High level Input current	I_{IH}	-10		-1	uA	V_{WAKE}=V_{BAT}-1.9V
Low level Input current	I_{IL}	1		10	uA	V_{WAKE}=V_{BAT}-3.1V
Threshold voltage	V_{th}	V_{BAT}-3		V_{BAT}-2	V	V_{STB_N}=0

Parameters	Symbol	Min	Typ	Max	Unit	Comments
INH						
High level voltage drop	ΔV_H	0		0.8	V	I_{INH}=-0.18mA
Leakage current	I_L	-2		2	uA	Sleep mode
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.75		4.5	V	V_{TXD}=0V, R_{Load} =50 to 65Ω
CANL output voltage (Dominant)	$V_{OL(D)}$	0.5		2.25	V	V_{TXD}=0V, R_{Load} =50 to 65Ω
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	-400		400	mV	$V_{dom(TX)sym}$=V_{CC}-V_{CANH}-V_{CANL}
transmitter voltage symmetry	V_{TXsym}	0.9VCC		1.1VCC	V	V_{TXsym} = V_{CANH} + V_{CANL} f_{TXD} = 250 kHz, 1 MHz and 2.5 MHz Not tested in production, guaranteed by design. See Figure 6.5
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	0..5V_{CC}	3	V	Normal or Listen-only mode, V_{TXD}=V_{IO}, no load
		-0.1		0.1	V	Standby or Sleep mode, no load
Differential output voltage (Dominant)	$V_{OD(D)}$	1.5		3	V	V_{TXD}=0V, R_{Load} =45 to 65Ω
		1.5		3.3	V	V_{TXD}=0V, R_{Load} =45 to 70Ω
		1.5		5		V_{TXD}=0V, R_{Load} =2240Ω
Differential output voltage (Recessive)	$V_{OD(R)}$	-50		50	mV	Normal or listen only mode, VTXD=VIO
		-0.2		0.2	V	Standby or sleep mode
Common-mode output voltage	V_{OC}	2	0..5V_{CC}	3	V	
Peak-to-peak Common-mode output voltage	$V_{OC(PP)}$		250		mV	
Short- circuit output current	I_{OS}	-100		-40	mA	Test CANH, TXD=0, V_{CANH}=-15V to +40 V
		40		100	mA	Test CANL, TXD=0, V_{CANL}=-15 V to +40 V
		-3		3	mA	Normal mode; V_{TXD}=V_{IO} ; V_{CANH} = V_{CANL} =-27 V to +32 V
Receiver						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
differential receiver threshold voltage	$V_{th(RX)dif}$	0.5		0.9	V	-30 V<V_{CANL}<+30 V; -30 V<V_{CANH}<+30 V; normal or listen only mode
		0.4		1.15	V	-30 V<V_{CANL}<+30 V; -30V<V_{CANH}<+30 V; standby or sleep mode
receiver recessive voltage	$V_{rec(RX)}$	-4		0.5	V	-30 V<V_{CANL}<+30 V; -30 V<V_{CANH}<+30 V; normal or listen only mode
		-4		0.4	V	-30V<V_{CANL}<+30 V; -30V<V_{CANH}<+30 V; standby or sleep mode
receiver dominant voltage	$V_{dom(RX)}$	0.9		9	V	-30 V<V_{CAN}L<+30 V; -30 V<VCANH<+30 V; normal or listen only mode
		1.15		9	V	-30 V<VCANL<+30 V; -30V<VCANH<+30 V; standby or sleep mode
Hysteresis voltage	V_{HYS}		50		mV	-30 V<V_{CANL}<+30 V, -30 V<V_{CANH}<+30 V normal or listen only mode
Power-off (unpowered) bus input leakage current	$I_{IOFF(LKG)}$	100		400	uA	V_{CANH} = V_{CANL} = 5 V, V_{CC} = 0V
		-2		8	uA	V_{CANH} = V_{CANL} = 5 V, V_{BAT}= 0V
		-2		8	uA	V_{CC}=V_{IO}=V_{BAT} = 0 V or V_{CC}=V_{IO}=V_{BAT}=shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} =5V
common-mode input capacitance	C_I			20	pF	guaranteed by design
Differential input capacitance	C_{ID}			10	pF	guaranteed by design
Differential input resistance	R_{ID}	18	30	56	kΩ	-2V<V_{CANL}<+7V, -2V<V_{CANH}<+7V;
Input resistance	R_{IN}	9	15	28	kΩ	-2 V<V_{CANL}<+7 V, -2V<V_{CANH}<+7 V;
Input resistance matching	R_{Imatch}	-3		+3	%	0 V<V_{CANL}<+5 V, 0V<V_{CANH}<+5 V;
Common-mode voltage range	V_{CM}	-30		+30	V	

6.2. Dynamic Characteristics

(VCC=4.5V~5.5V, VIO=2.8V~5.5V, VBAT4.5V~40V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V, VBAT=12V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
delay time from TXD Low to RXD Low	$t_{d(TXDL-RXDL)}$	40		240	ns	Driver input to receiver output, Recessive to Dominant, normal mode, see Figure 6.4
delay time from TXD High to RXD High	$t_{d(TXDH-RXDH)}$	40		240	ns	Driver input to receiver output, Dominant to Recessive, normal mode, see Figure 6.4
undervoltage detection time	$t_{det(uv)}$	100		350	ms	guaranteed by design
undervoltage recovery time	$t_{rec(uv)}$	1		5	ms	guaranteed by design
transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)}$ = 500 ns, see Figure 6.4
		155		210	ns	$t_{bit(TXD)}$ = 200 ns, see Figure 6.4
bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)}$ = 500 ns, see Figure 6.4
		120		220	ns	$t_{bit(TXD)}$ = 200 ns, see Figure 6.4
delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$		65		ns	Normal mode. see Figure 6.4
delay time from TXD to bus recessive	$td_{(TXD-busres)}$		70		ns	Normal mode, see Figure 6.4
delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$		80		ns	Normal or listen only mode, see Figure 6.4
delay time from bus recessive to RXD	$t_{d(busres-RXD)}$		90		ns	Normal or listen only mode, see Figure 6.4
Receiver timing symmetry	Δt_{rec}	-65		40	ns	$t_{bit(TXD)}$ = 500 ns
		-45		15	ns	$t_{bit(TXD)}$ = 200 ns
TXD dominant time-out time	t_{TXD_DTO}	0.35		1.5	ms	V_{TXD} = 0 V; Normal mode
Bus dominant time out time	t_{bus_DTO}	0.35		1.5	ms	Listen-only mode
hold time	t_h	20		120	us	from issuing go-to-sleep command to entering Sleep mode
bus dominant wake-up time	$t_{wake(busdom)}$	0.5		3.5	us	Standby or Sleep mode, V_{BAT} = 12 V
bus recessive wake-up time	$t_{wake(busres)}$	0.5		3.5	us	Standby or Sleep mode, V_{BAT} = 12 V
bus wake-up timeout time	$t_{to(wake)bus}$	0.5		2	ms	bus wake-up filter time

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Wakeup time	t_{wake}	5		100	us	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode

6.3. Parameter Measurement Information

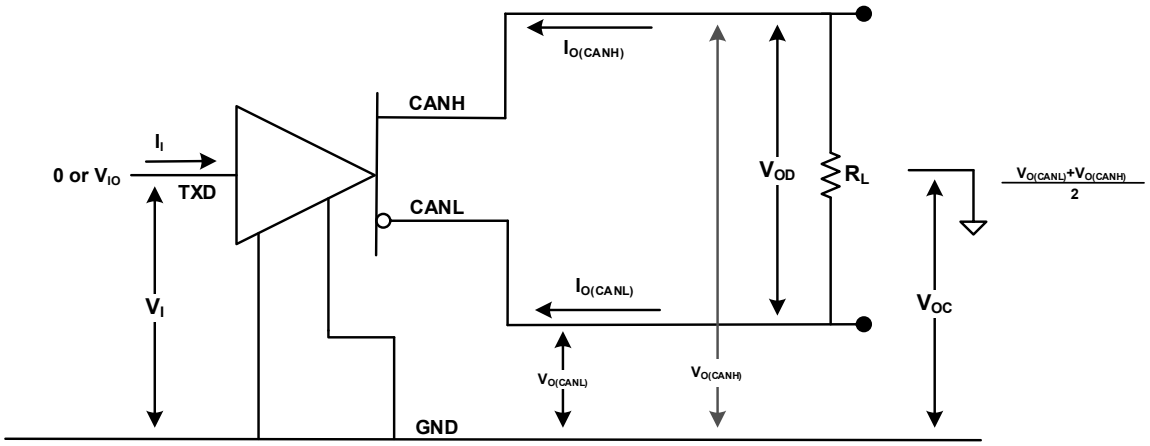


Figure 6.1 Driver Voltage, Current and Test Definitions

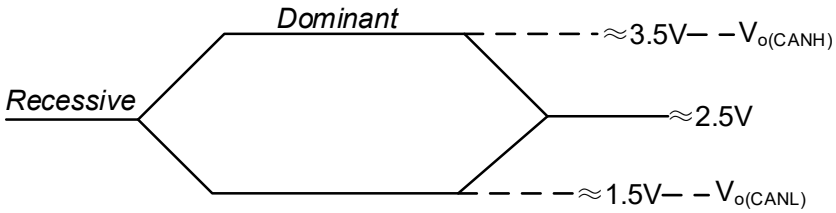


Figure 6.2 Bus Logic State Voltage Definitions

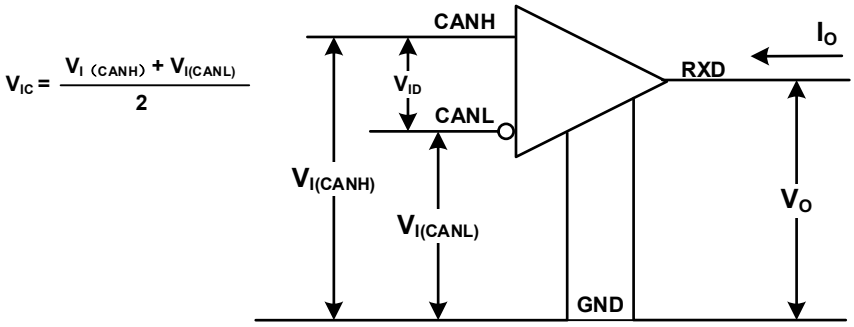


Figure 6.3 Receiver Voltage and Current Definitions

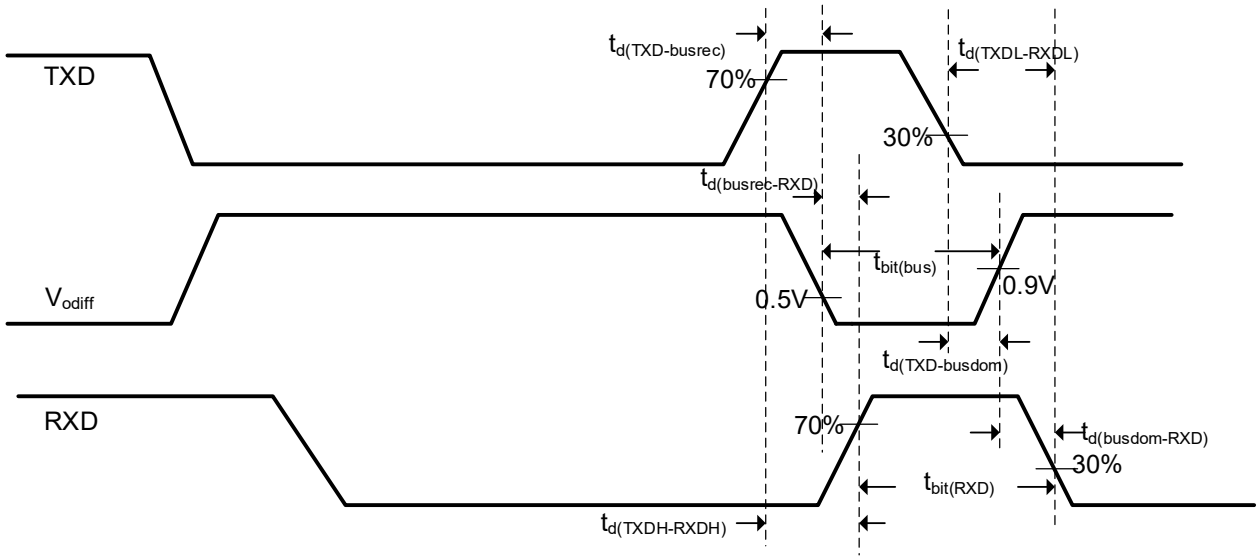


Figure 6.4 CAN timing definitions

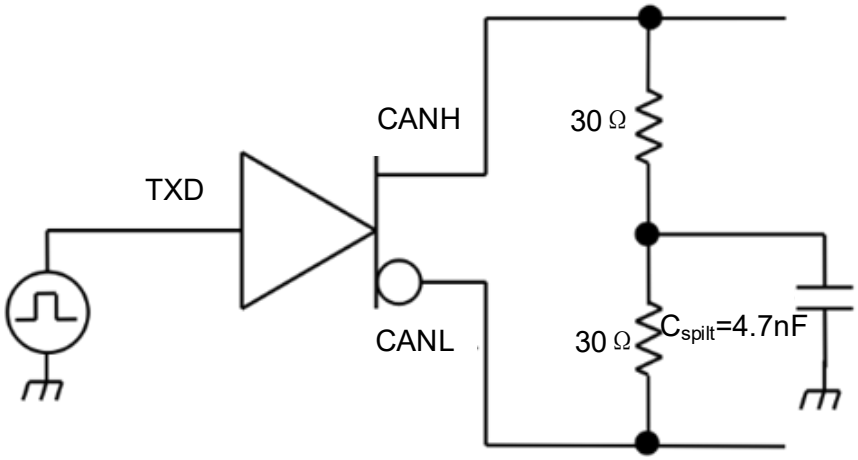


Figure 6.5 Transceiver Driver Symmetry Test Circuit

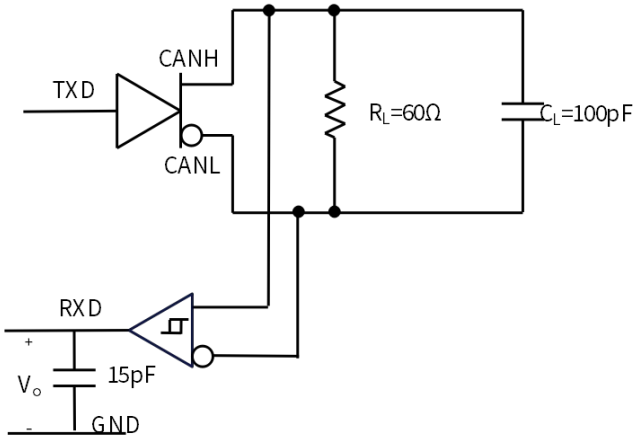


Figure 6.6 Timing test circuit

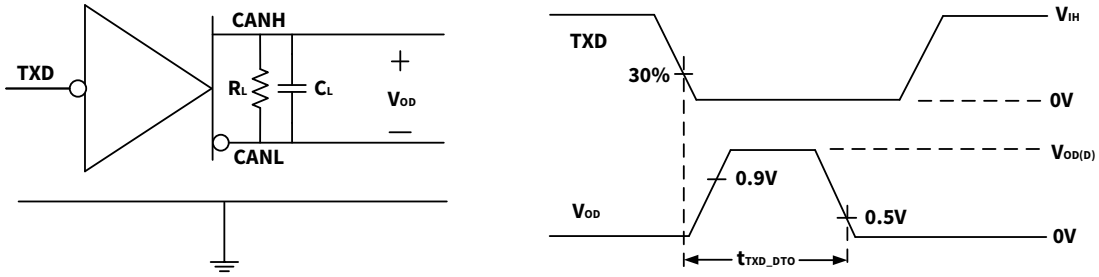


Figure 6.7 TXD Dominant Time Out Test Circuit and Measurement

6.4. Typical Performance Characteristics

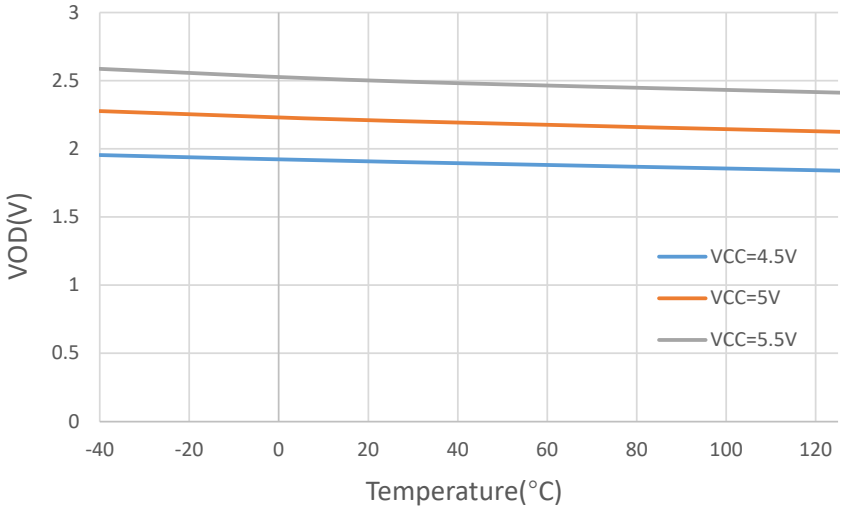


Figure 6.8 $V_{OD(D)}$ vs temperature (R_{Load} = 60Ω)

7. Function Description

The NCA1043B is a stand-alone high-speed CAN transceiver with a number of operating modes, fail-safe features and diagnostic features that offer enhanced system reliability and advanced power management. The transceiver has excellent EMC and ESD capability and quiescent current capability. Slope control and high DC handling capability on the bus pins provide additional application flexibility.

7.1. Operating modes

The NCA1043B supports five operating modes. Control pins STB_N and EN are used to select the operating mode. Switching between modes allows access to a number of diagnostics flags via pin ERR_N. Figure 7.1 and Table 7.1 describes how to switch between modes.

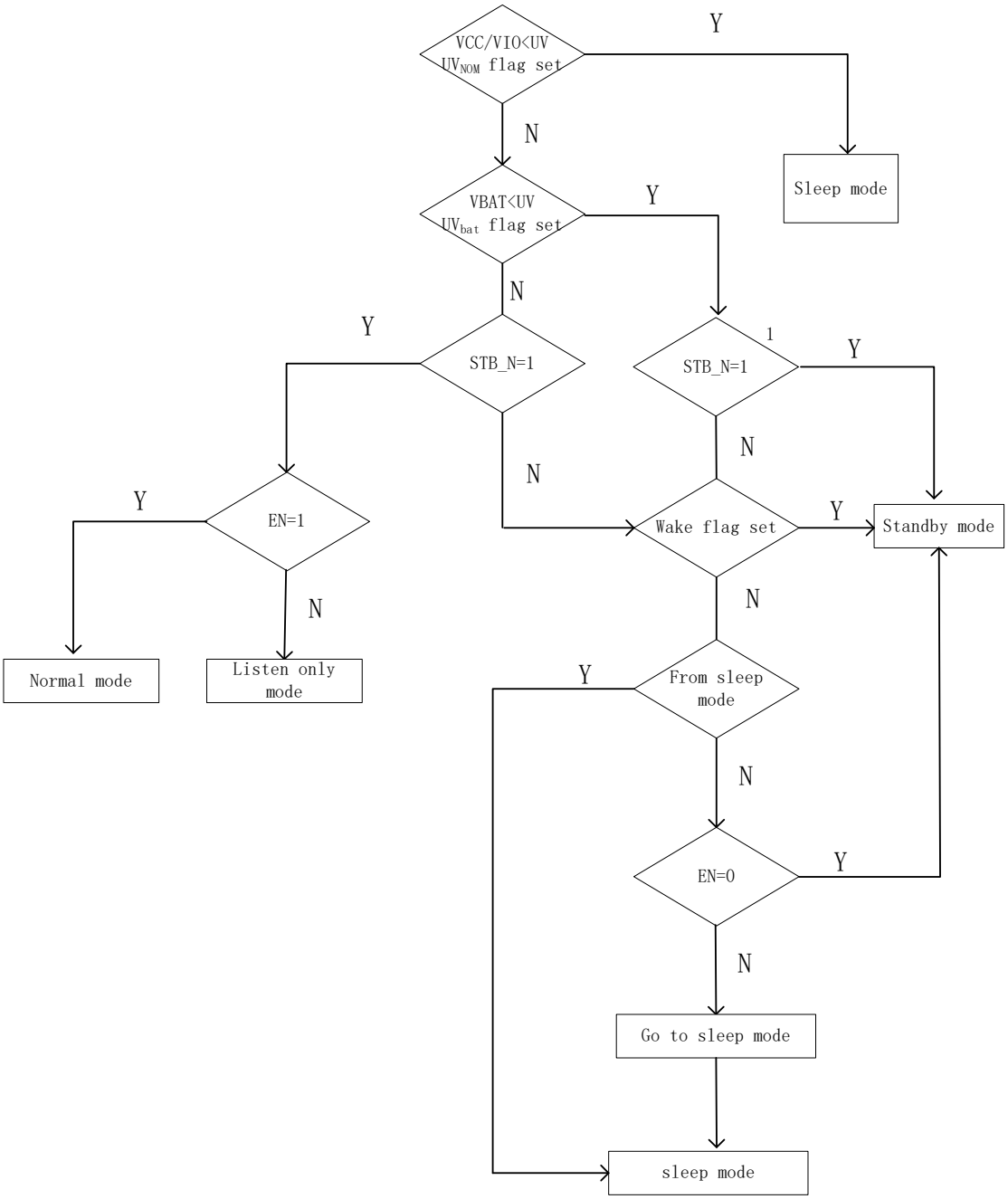


Figure 7.1 Mode transition

Note1: The mode switching is in the precondition of UV_{BAT} is set.

Table 7.1 Operating mode selection

Internal flags			Control pins		Operating mode	INH
UV_{NOM}	UV_{BAT}	Wake	STB_N	EN		
From Normal, Listen-only, Standby and Go-to-Sleep modes						
set	×	×	×	×	Sleep mode	floating
cleared	set	×	High	×	Standby mode	High
cleared	×	set	Low	×	Standby mode	High
cleared	×	cleared	Low	Low	Standby mode	High
cleared	×	cleared	Low	High	Go-to-Sleep mode	High
cleared	cleared	×	High	Low	Listen-only mode	High
cleared	cleared	×	High	High	Normal mode	High
From Sleep mode						
set	×	×	×	×	Sleep mode	floating
cleared	set	×	High	×	Standby mode	High
cleared	×	set	Low	×	Standby mode	High
cleared	×	cleared	Low	×	Sleep mode	floating
cleared	cleared	×	High	Low	Listen-only mode	High
cleared	cleared	×	High	High	Normal mode	High

7.1.1. Normal mode

In Normal mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. The bus pins are biased to $0.5V_{CC}$ (via R_i). Pin INH is active, so voltage regulators controlled by pin INH will be active too.

7.1.2. Listen-only mode

In Listen-only mode, the transceiver's transmitter is disabled, effectively providing a transceiver listen-only feature. The receiver will still convert the analog bus signal on pins CANH and CANL into digital data, available for output on pin RXD. As in Normal mode, the bus pins are biased at $0.5V_{CC}$ and pin INH remains active.

7.1.3. Standby mode

Standby mode is the NCA1043B's first-level power saving mode, offering reduced current consumption. In Standby mode, the transceiver is unable to transmit or receive data and the low-power receiver is activated to monitor bus activity. The bus pins are biased at ground level (via R_i). Pin INH is still active, so voltage regulators controlled by this pin will also be active.

Pins RXD and ERR_N will reflect any active wake-up requests (provided that V_{IO} and V_{BAT} are present).

7.1.4. Go-to-Sleep mode

Go-to-Sleep mode is the controlled route for entering Sleep mode. In Go-to-Sleep mode, the transceiver behaves as in Standby mode, with the addition that a go-to-sleep command is issued to the transceiver. The transceiver will remain in Go-to-Sleep mode for the minimum hold time ($t_{h(min)}$) before entering Sleep mode. The transceiver will not enter Sleep mode if the state of pin STB_N or pin EN is changed or if the Wake flag is set before $t_{h(min)}$ has elapsed.

7.1.5. Sleep mode

Sleep mode is entered via Go-to-Sleep mode, and also when the undervoltage detection time on either V_{CC} or V_{IO} elapses before the relevant voltage level has recovered. In Sleep mode, the transceiver behaves as described for Standby mode, with the exception that pin INH is set floating. Voltage regulators controlled by this pin will be switched off, and the current into pin V_{BAT} will be reduced to a minimum. Pins STB_N, EN and the Wake flag can be used to wake up a node from Sleep mode.

7.2. Internal flags

The NCA1043B makes use of seven internal flags for its fail-safe fallback mode control and system diagnosis support. Five of these flags can be polled by the controller via pin ERR_N. Which flag is available on pin ERR_N at any time depends on the active operating mode and on a number of other conditions. Table 7.2 describes how to access these flags

.

Table 7.2 Accessing internal flags via pin ERR_N

Internal flag	*Flag is available on pin ERR_N [1]*	*Flag is cleared*
UV_{NOM}	No	by setting the Pwon or Wake flags, by a LOW-to-HIGH transition on STB_N or when both V_{IO} and V_{BAT} have recovered.
UV_{BAT}	No	when V_{BAT} has recovered
Pwon	in Listen-only mode (coming from Standby mode, Go-to-Sleep mode, or Sleep mode)	on entering Normal mode
Wake	in Standby mode, Go-to-Sleep mode, and Sleep mode (provided that V_{IO} and V_{BAT} are present)	on entering Normal mode or by setting the UV_{NOM} flag
Wake-up source	in Normal mode (before the fourth dominant-to-recessive edge on pin TXD[2])	on leaving Normal mode
Bus failure	in Normal mode (after the fourth dominant-to-recessive edge on pin TXD[2])	on re-entering Normal mode or by setting the Pwon flag
Local failure	in Listen-only mode (coming from Normal mode)	on entering Normal mode or when RXD is dominant while TXD is recessive (provided that all local failures are resolved) or by setting the Pwon flag

1) Pin ERR_N is an active-LOW output, so a LOW-level indicates a set flag and a HIGH-level indicates a cleared flag. Allow pin ERR_N to stabilize for at least 8 us after changing operating modes.
2) Allow for a TXD dominant time of at least 4 us per dominant-recessive cycle.

7.2.1. UV_{NOM} flag

UV_{NOM} is the V_{CC} and V_{IO} undervoltage detection flag. The flag is set when the voltage on pin V_{CC} drops below the V_{CC} undervoltage detection voltage, $V_{uvd(VCC)}$, for longer than the undervoltage detection time, $t_{det(uv)}$, or when the voltage on pin V_{IO} drops below $V_{uvd(VIO)}$ for longer than $t_{det(uv)}$. When the UV_{NOM} flag is set, the transceiver enters Sleep mode to save power and to ensure the bus is not disturbed. In Sleep mode the voltage regulators connected to pin INH are disabled, avoiding any extra power consumption that might be generated as a result of a short-circuit condition.

Any wake-up request, setting the Pwon flag or a LOW-to-HIGH transition on STB_N will clear UV_{NOM} and the timers, allowing the voltage regulators to be reactivated (at least until UV_{NOM} is set again). UV_{NOM} will also be cleared if both V_{CC} and V_{IO} recover for longer than the undervoltage recovery time, $t_{rec(uv)}$. The transceiver will then switch to the operating mode indicated by the logic levels on pins STB_N and EN (see Figure 7.1 and Table 7.1).

7.2.2. UV_{BAT} flag

UV_{BAT} is the V_{BAT} undervoltage detection flag. This flag is set when the voltage on pin V_{BAT} drops below $V_{uvd(VBAT)}$. When UV_{BAT} is set, the transceiver will try to enter Standby mode to save power and will disengage from the bus (zero load). UV_{BAT} is cleared when the voltage on pin V_{BAT} recovers. The transceiver will then switch to the operating mode indicated by the logic levels on pins STB_N and EN (see Figure 7.1 and Table 7.1).

7.2.3. Pwon flag

Pwon is the V_{BAT} power-on flag. This flag is set when the voltage on pin V_{BAT} recovers after previously dropping below $V_{uvd(VBAT)}$ (usually because the battery was disconnected). Setting the Pwon flag clears the UV_{NOM} flag and timers. The Wake and Wake-up source flags are set to ensure consistent system power-up under all supply conditions. In Listen-only mode the Pwon flag can be polled via pin ERR_N (see Table 7.2). The flag is cleared when the transceiver enters Normal mode.

7.2.4. Wake flag

The Wake flag is set when the transceiver detects a local or remote wake-up request. A local wake-up request is detected when the logic level on pin WAKE changes, and the new level remains stable for at least t_{wake}. The Wake flag can be set in Standby mode, Go-to-Sleep mode or Sleep mode. Setting the Wake flag clears the UV_{NOM} flag and timers. Once set, the Wake flag status is immediately available on pins ERR_N and RXD (provided V_{IO} and V_{BAT} are present). This flag is also set at power-on and cleared when the UV_{NOM} flag is set or the transceiver enters Normal mode.

7.2.5. Remote wake-up (via the CAN bus)

The NCA1043B wakes up from Standby or Sleep mode when a dedicated wake-up pattern (specified in ISO 11898-2: 2024) is detected on the bus. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above-mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 7.2). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The NCA1043B switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} or V_{IO} undervoltage is detected (UV_{NOM} flag set)

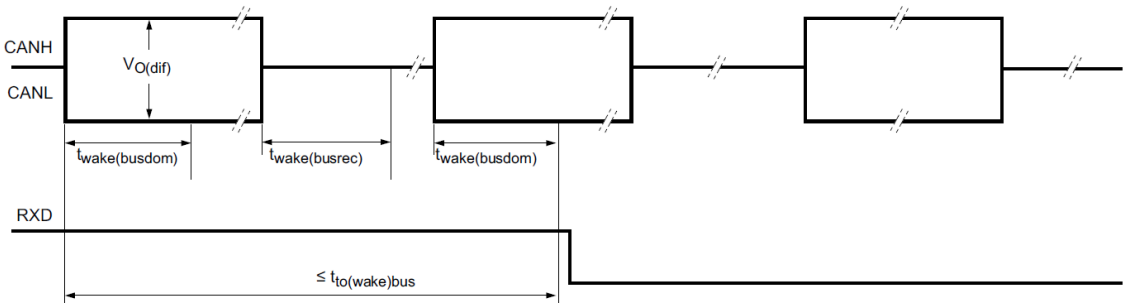


Figure 7.2 Wake-up timing

7.2.6. Wake-up source flag

Wake-up source recognition is provided via the Wake-up source flag, which is set when the Wake flag is set by a local wake-up request via the WAKE pin. The Wake-up source flag can be polled via the ERR_N pin in Normal mode (see Table 7.1). This flag is also set at power-on and cleared when the transceiver leaves Normal mode.

7.2.7. Bus failure flag

The Bus failure flag is set if the transceiver detects a bus line short-circuit condition to V_{BAT}, V_{CC} or GND during four consecutive dominant-recessive cycles on pin TXD, while trying to drive the bus lines dominant. The Bus failure flag can be polled via the ERR_N pin in Normal mode (see Table 7.1). This flag is cleared at power-on or when the transceiver re-enters Normal mode.

7.2.8. Local failure flag

In Normal and Listen-only modes, the transceiver can distinguish four different local failure events, any of which will cause the Local failure flag to be set. The four local failure events are: TXD dominant clamping, TXD-to-RXD short circuit, bus dominant clamping and an overtemperature event. The nature and detection of these local failures is described in Section 7.3. The Local failure flag can be polled via the ERR_N pin in Listen-only mode (see Table 7.1). This flag is cleared at power-on, when entering Normal mode or when RXD is dominant while TXD is recessive, provided that all local failures have been resolved.

7.3. Local Failures

The NCA1043B can detect four different local failure conditions. Any of these failures will set the Local failure flag, and in most cases the transmitter of the transceiver will be disabled.

7.3.1. TXD dominant time-out function

A permanent LOW level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communications. The TXD dominant time-out function prevents such a network lock-up by

disabling the transmitter if pin TXD remains LOW for longer than the TXD dominant time-out time $t_{to(dom)TXD}$. The $t_{to(dom)TXD}$ timer defines the minimum possible bit rate of 40 kbit/s. The transmitter remains disabled until the Local failure flag has been cleared.

7.3.2. TXD-to-RXD short-circuit detection

A short-circuit between pins RXD and TXD would lock the bus in a permanent dominant state once it had been driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. TXD-to-RXD short-circuit detection prevents such a network lock-up by disabling the transmitter. The transmitter remains disabled until the Local failure flag has been cleared.

7.3.3. Bus dominant time-out function

A CAN bus short circuit (to V_{BAT}, V_{CC} or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not start transmission if the bus is dominant, the normal bus failure detection will not detect this failure, but the bus dominant clamping detection will. The Local failure flag is set if the dominant state on the bus persists for longer than $t_{to(dom)bus}$. By checking this flag, the controller can determine if a clamped bus is blocking network communications. There is no need to disable the transmitter. Note that the Local failure flag does not retain a bus dominant clamping failure and is released as soon as the bus returns to recessive state.

7.3.4. Overtemperature detection

If the junction temperature becomes excessive, the transmitter will shut down in time to protect the output drivers from overheating without compromising the maximum operating temperature. The transmitter will remain disabled until the Local failure flag has been cleared.

7.4. VIO supply pin

Pin VIO should be connected to the microcontroller supply voltage. This will cause the signal levels of pins TXD, RXD, STB_N, EN and ERR_N to be adjusted to the I/O levels of the microcontroller, facilitating direct interfacing without the need for glue logic.

7.5. WAKE pin

A local wake-up event is triggered by a LOW-to-HIGH or HIGH-to-LOW transition on the WAKE pin, allowing for maximum flexibility when designing a local wake-up circuit. To minimize current consumption, the internal bias voltage will follow the logic state on the pin after a delay of t_{wake}. A HIGH level on pin WAKE is followed by an internal pull-up to V_{BAT}. A LOW level on pin WAKE is followed by an internal pull-down towards GND. In applications that don't make use of the local wake-up facility, it is recommended that the WAKE pin be connected to V_{BAT} or GND to ensure optimal EMI performance.

8. Application Note

8.1. Typical Application Circuit

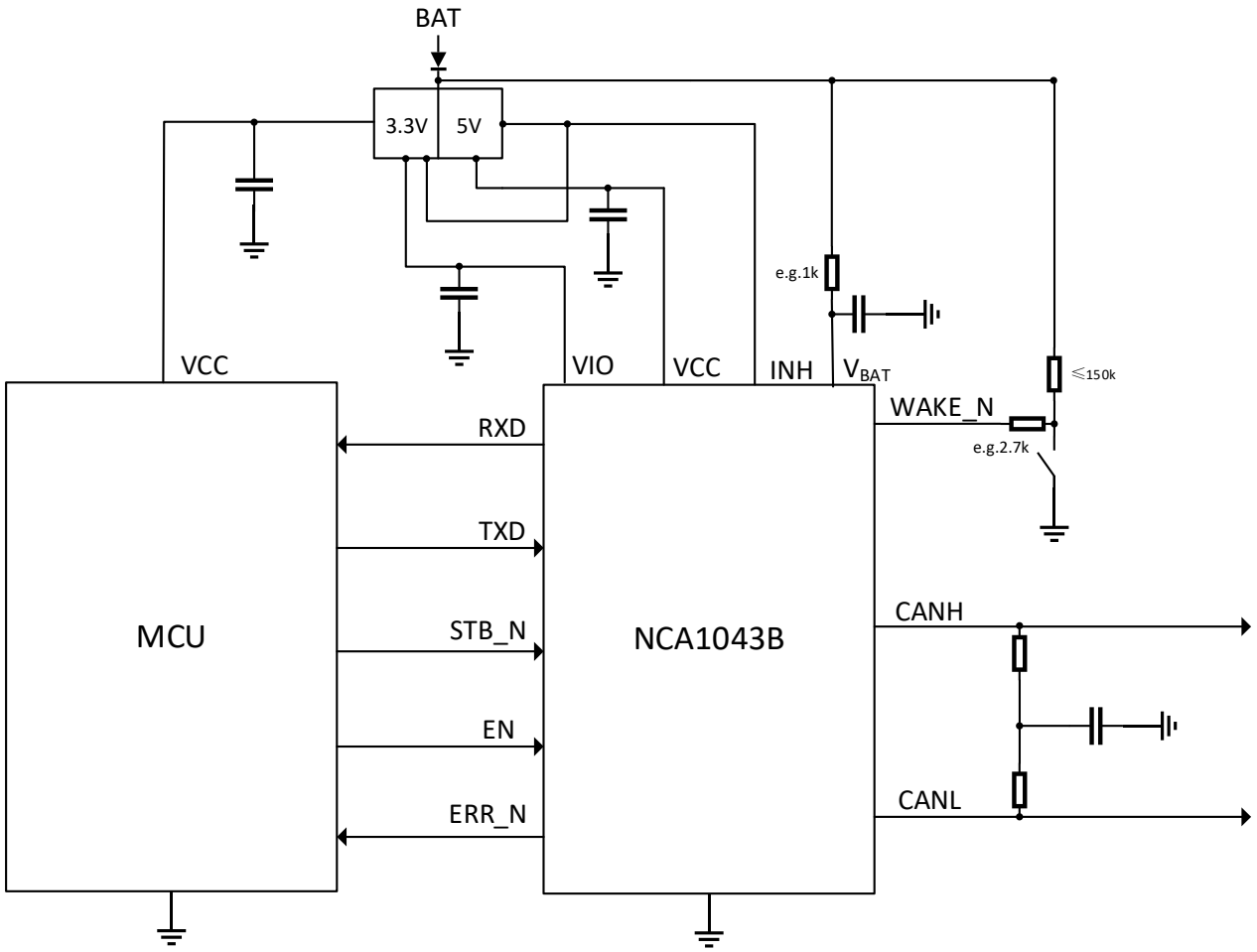
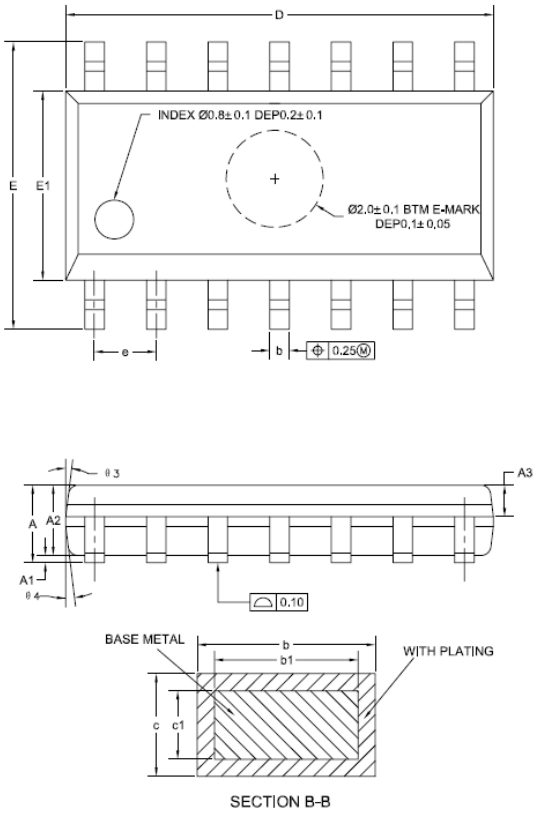


Figure 8.1 Typical Application Circuit

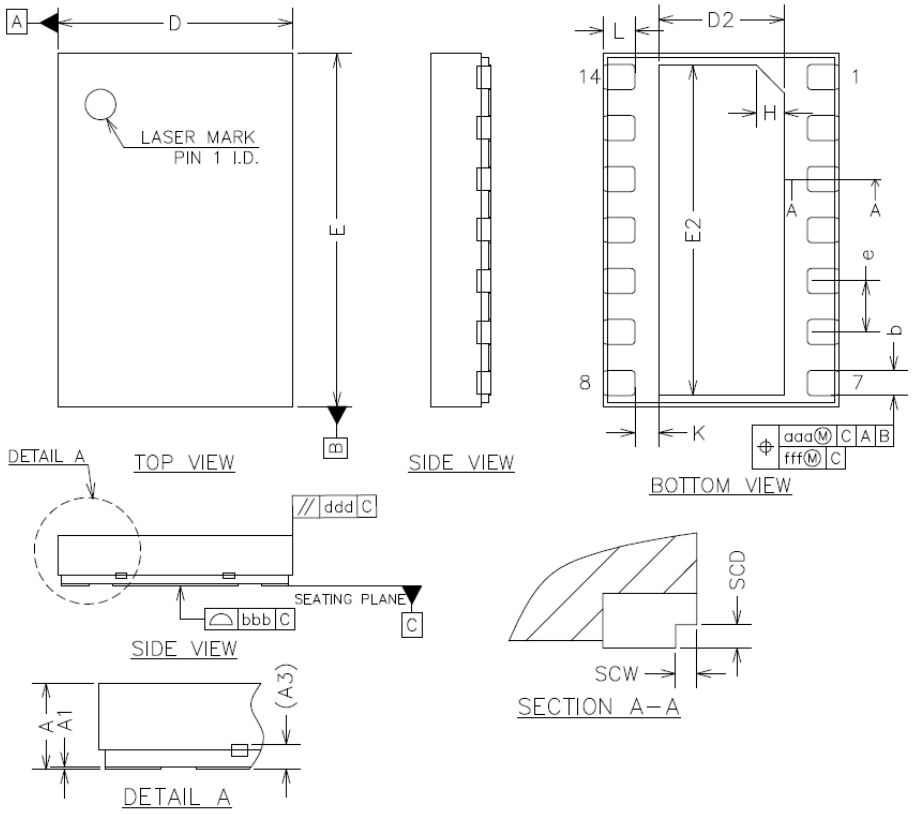
9. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1,35	1.60	1,75
A1	0.10	0,15	0.25
A2	1.25	1,45	1.65
A3	0,55	0.65	0.75
b	0,36	-	0,49
b1	0.35	0,40	0.45
⚠3 c	0.17	-	0.25
⚠3 c1	0.17	0.20	0.23
D	8,53	8.63	8,73
E	5.80	6.00	6.20
E1	3.80	3,90	4.00
e	1.27BSC		
L	0,45	0.60	0.80
L1	1.04REF		
L2	0,25BSC		
R	0.07	-	-
R1	0.07	-	-
h	0,30	0.40	0,50
θ	0°	-	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

Figure 9.1 SOP14 Package Shape and Dimension in millimeters



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.27	0.32	0.37
D	2.90	3.00	3.10
E	4.40	4.50	4.60
D2	1.50	1.60	1.70
E2	4.10	4.20	4.30
e		0.65 BSC	
H		0.35REF	
K	0.20	0.30	0.40
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.05	
ddd		0.10	
fff		0.08	
SCW	0.01	–	0.09
SCD	0.08	–	0.18

Figure 9.2 DFN14 Package Shape and Dimension in millimeters

10. Ordering Information

Part Number	*Max Data Rate (Mbps)*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NCA1043B-Q1SPKR	5	-40 to 125℃	3	SOP14	SOP14	2500
NCA1043B-Q1DNKR	5	-40 to 125℃	2	DFN14	DFN14	6000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
All devices are AEC-Q100 qualified.

11. Tape and Reel Information

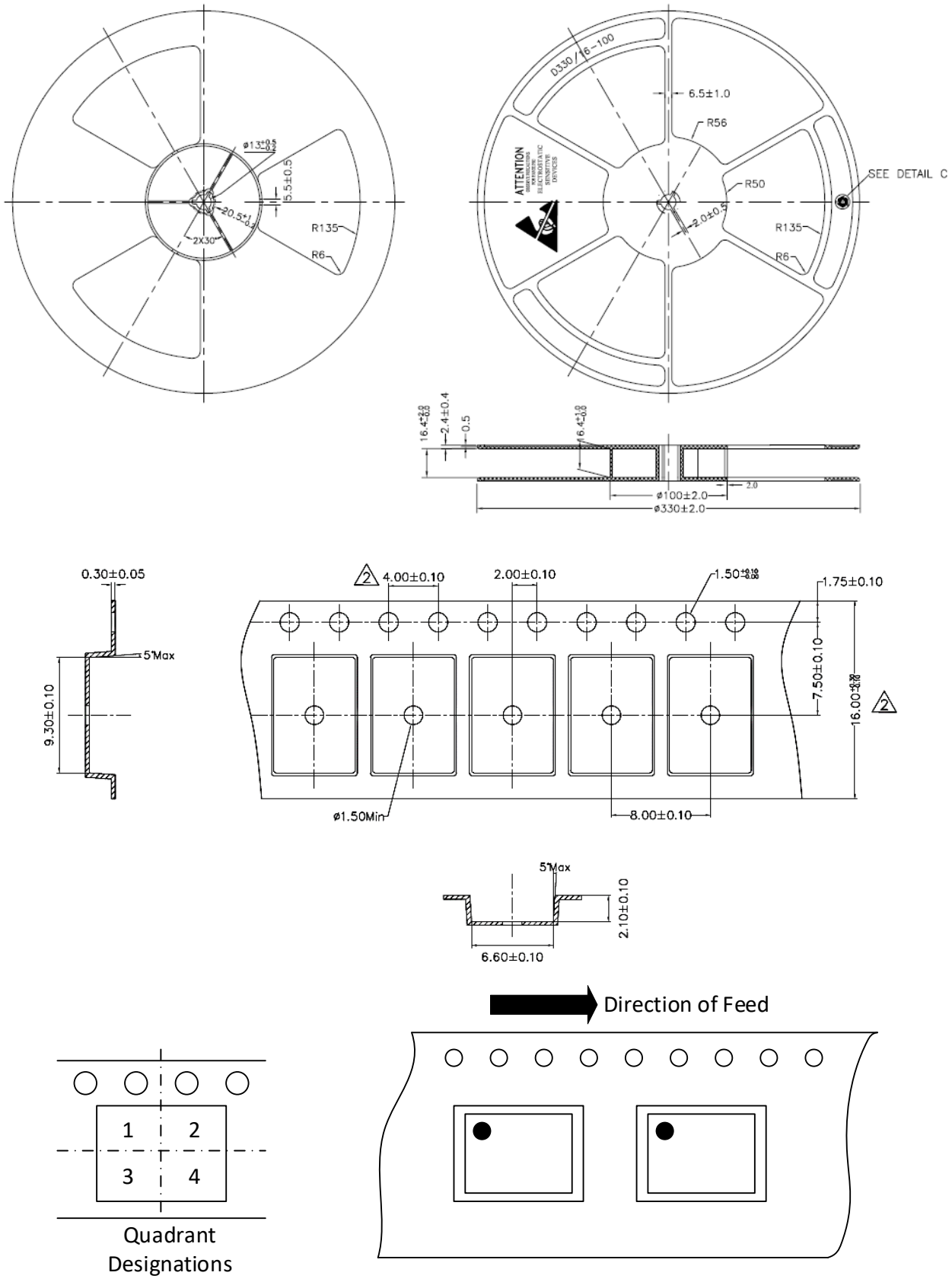
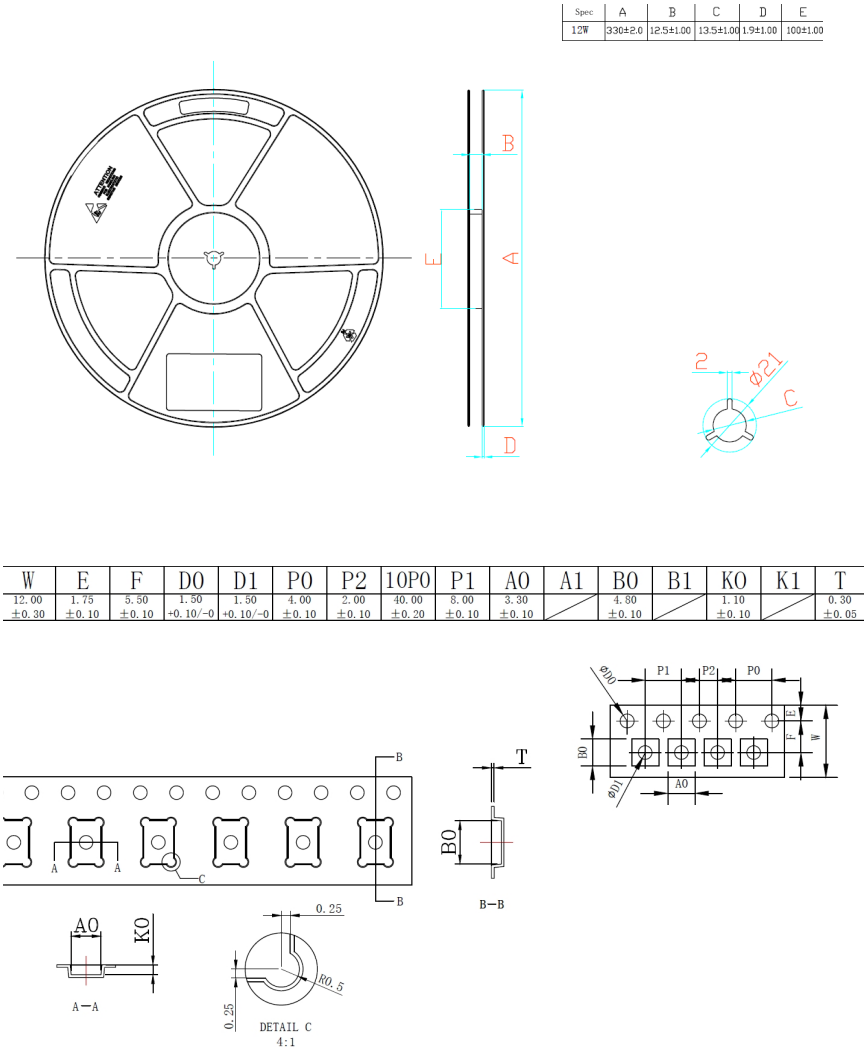


Figure 11.1 Tape and Reel Information of SOP14



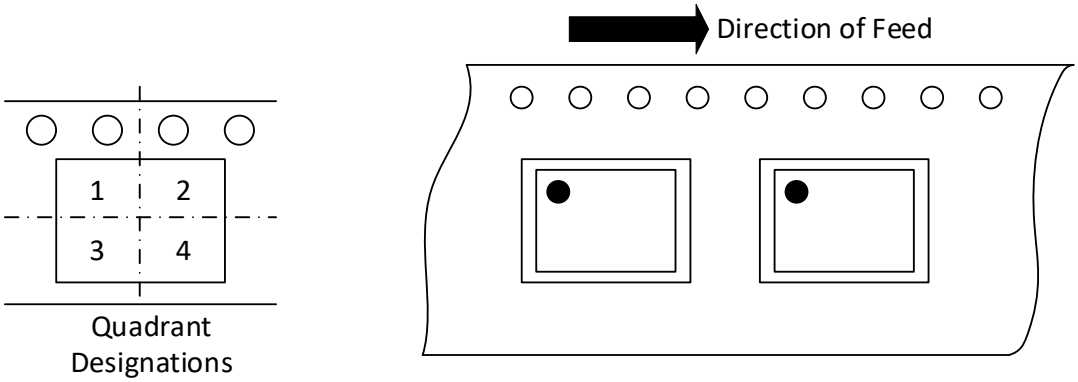


Figure 11.2 Tape and Reel Information of DFN14

12. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/9/11

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